# GMSLE FDD PHY SIMULATION RESULTS AND PHY COMPLEXITY

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# Contributors and Supporters

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# Outline

- Objective
- GMLSE Baseline
- DME Noise Analysis
  - Receiver/Test Setup
  - CW Noise Simulation Results
  - Burst Noise Simulation Results
- Power Over Coax (POC) with GMSLE
  - POC Qualification
  - “Mystery” POC with GMSLE
- Complexity Revisited
  - Detailed Camera Complexity Analysis
- Conclusion

# Objective

- Show performance results for GMSLE DME Upstream receiver in presence of automotive noise
- Present POC testing methodology and reveal 'mystery' POC
- Revisit camera-side complexity analysis
  - Provide detailed analysis on digital and analog blocks for GMSLE and TDD-based camera PHYs
  - Provide more detail on host-side complexity

# GMSLE FDD SerDes Baseline

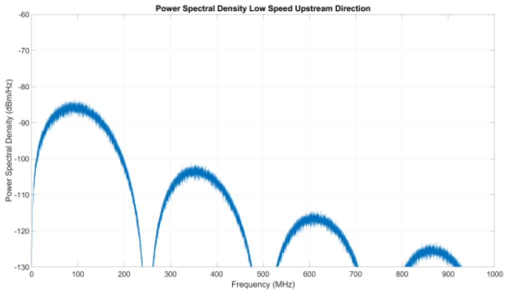
| | |
|---|---|
| Ethernet MAC Interface | XGMII |
| Line Coding | 64B/65B encoding (see detail, next slide) |
| Duplexing | FDD (Echo Subtraction/Partial Echo Cancellation possible) |
| Link Rates and Modulation | Forward Link: 2.5Gbps NRZ, 5Gbps NRZ, 5Gbps PAM4 (option) ,10Gbps PAM4<br>Reverse Link: 100Mbps |
| Scrambler | Downstream: $1+x^{13}+x^{33}$<br>Upstream: $1+x^{20}+x^{33}$ |

| PHY Transmit Parameters | | Rate | Mod | Encoding | FEC RS(n,k) | Baud Rate | TX Power | Burst Noise Protection |
|---|---|---|---|---|---|---|---|---|
| | Downstream high-speed link rate: | 2.5Gbps<br>5Gbps<br>5Gbps<br>10Gbps | **NRZ**<br>**NRZ**<br>**PAM4**<br>**PAM4** | 15x65b+1 bit OAM<br>2x(15x65b+1b OAM)<br>2x(15x65b+1b OAM)<br>4x(15x65b+1b OAM) | RS(144,122) L=1 m=8<br>RS(144,122) L=2 m=8<br>RS(144,122) L=2 m=8<br>RS(144,122) L=4 m=8 | 2.5Gbps: 3GBaud<br>5Gbps: 6GBaud<br>5Gbps: 3GBaud<br>10Gbps: 6GBaud | -0.76dBm<br>-0.76dBm<br>-1.76dBm<br>-1.76dBm | 88 PAM-2 symbols, 29.3ns<br>176 PAM-2 symbols, 29.3ns<br>88 PAM-4 symbols, 29.3ns<br>176 PAM-4 symbols, 29.3ns |
| | Upstream low-speed link rate: | 100Mbps | **DME** | 3x65b+13bit OAM | RS(30,26) L=1 m=8 | 100Mbps: 250MHz | -5dBm | 16 DME Symbols, 64ns |

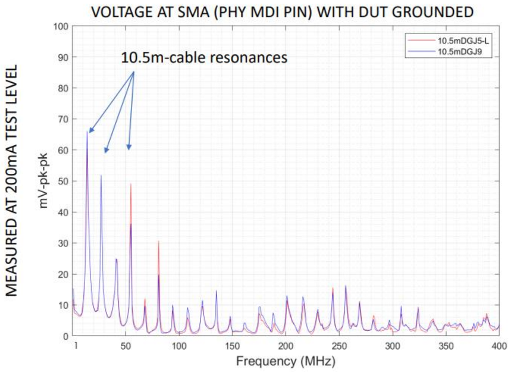
| | |
|---|---|
| Low complexity POC | Yes, single inductor, also compact dual inductor |
| XTAL-less Camera PHY? | Yes, supported |

# Upstream Low Speed Direction Noise Considerations

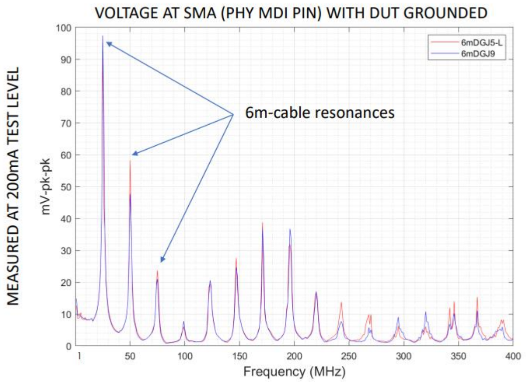
- EMI tolerance is a critical issue for automotive PHYs
- GMSLE Upstream PSD is within ISO 11452-4 Part 4 Bulk Current Injection (BCI) frequency range




- Pischl contribution [1] shows EMC measurements for BCI clamp on coax for DUT grounded and floating conditions with 200mA test level




From [1]

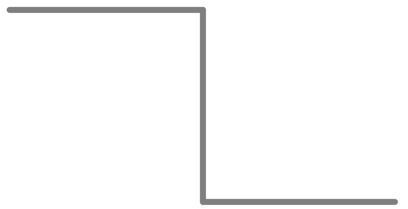



From [1]

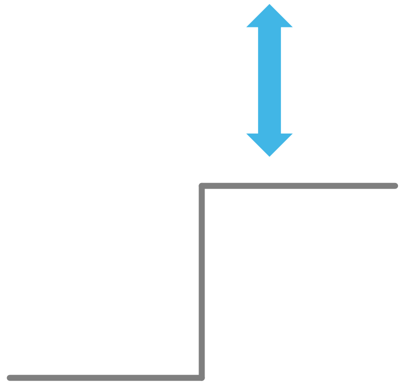
- Evaluate possible low complexity GMSLE DME receiver implementation with respect to 355mA BCI test level measurements (scale Pischl DUT GNDed and float results 1.78x)

# Possible GMSLE DME Matched Filter Receiver

- A matched filter receiver [3] for DME [2] is one possible receiver implementation for the GMSLE upstream (low-speed data rate) direction
- Evaluate a comparator matched filter with CW noise.
  - Very similar to William Lo's contribution [4]

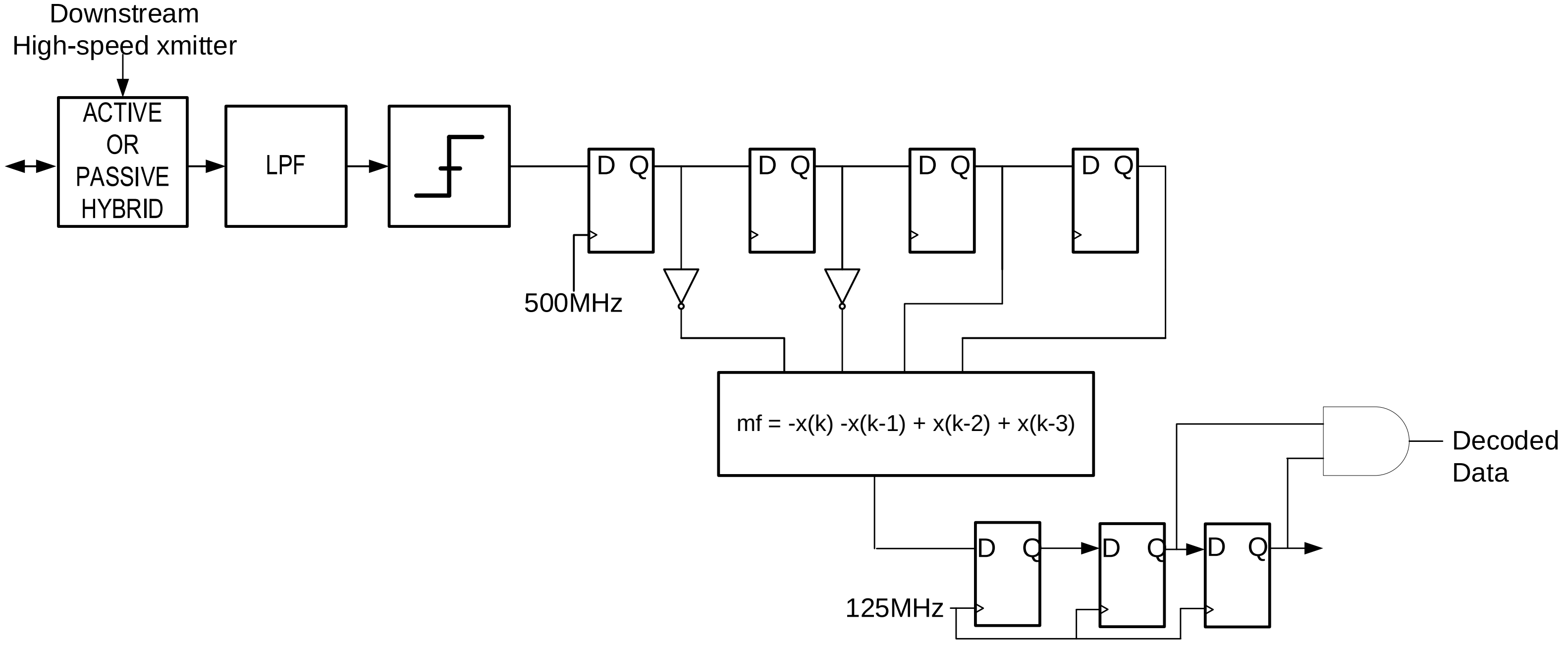


Delay detection by ½ symbol, Match to this symbol



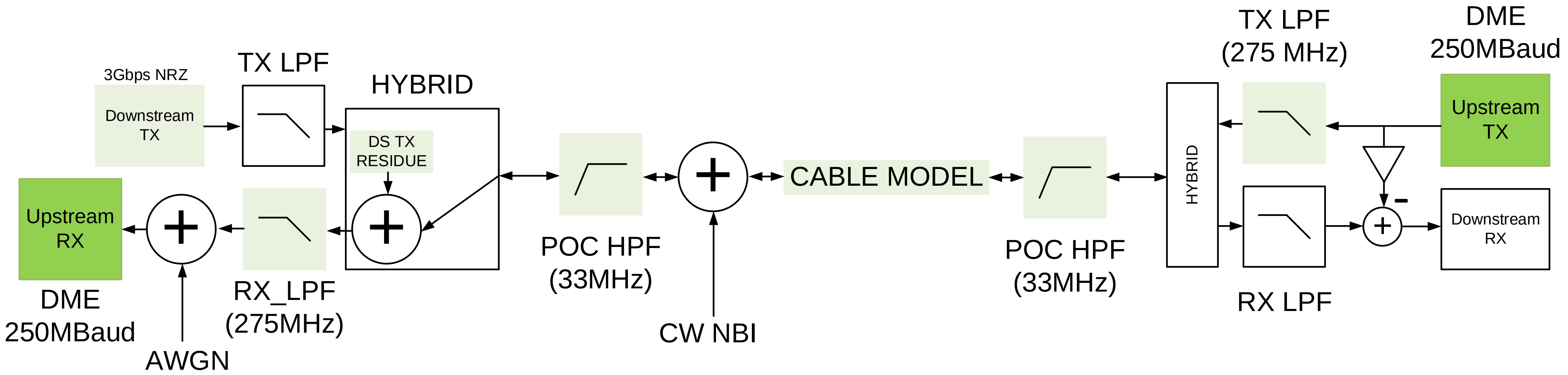
Flip the symbol (correlation, see [3] fig 3.7)

Match to "--++"



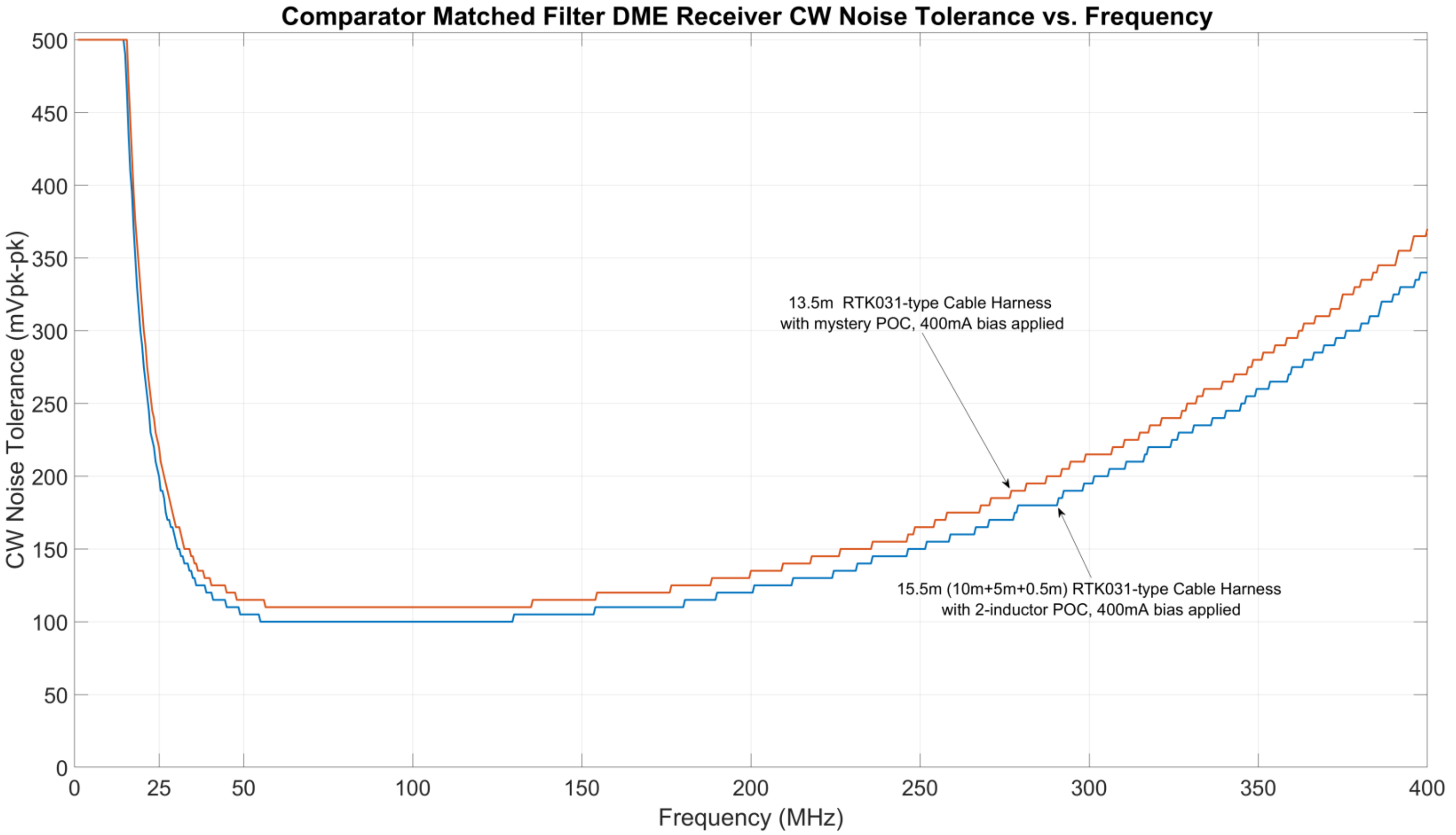

Possible Implementation, similar to [4]

# DME Noise Simulation Setup




- Upstream Low-speed TX
  - Power: -5dBm for FM band EMC compatibility
  - TX Rate: 250Mbaud
  - TX filtering 2$^{nd}$ order Butterworth, fc=275MHz
- Downstream High-speed TX
  - Power: -0.76dBm
  - TX Rate: 3Gbps NRZ
- Packets
  - 100e5 packets per 500kHz step
  - Random packet payload with $1+x^{20}+x^{33}$ scrambler applied
- Channel
  - 15.5m harness:
    - 2 inductor POC biased at 400mA, 33MHz POC HPF Corner (both sides)
    - 0.5m+5m+10m link segment RTK031-type cable
  - 13.5m harness:
    - **Mystery POC**, biased at 400mA, 33MHz POC HPF corner (both sides)
    - 0.5m+13m RTK031-type cable
- AWGN
  - Inject -25dBc just before receiver
- CW interference
  - Inject from 1-400 MHz CW with pi/2 offset in 500kHz steps
  - Start at 250mV peak and reduce until passing
- Hybrid
  - Active hybrid -24dB
- Upstream Low-speed Receiver
  - RX Filtering:
    - 2$^{nd}$ order Butterworth LPF, fc=275MHz
    - Matched filter (see previous page)
- Criteria
  - Dwell CW noise at each frequency
  - Pass criteria: 0 Pre-FEC errors, reduce TX power and rerun until pass at each frequency

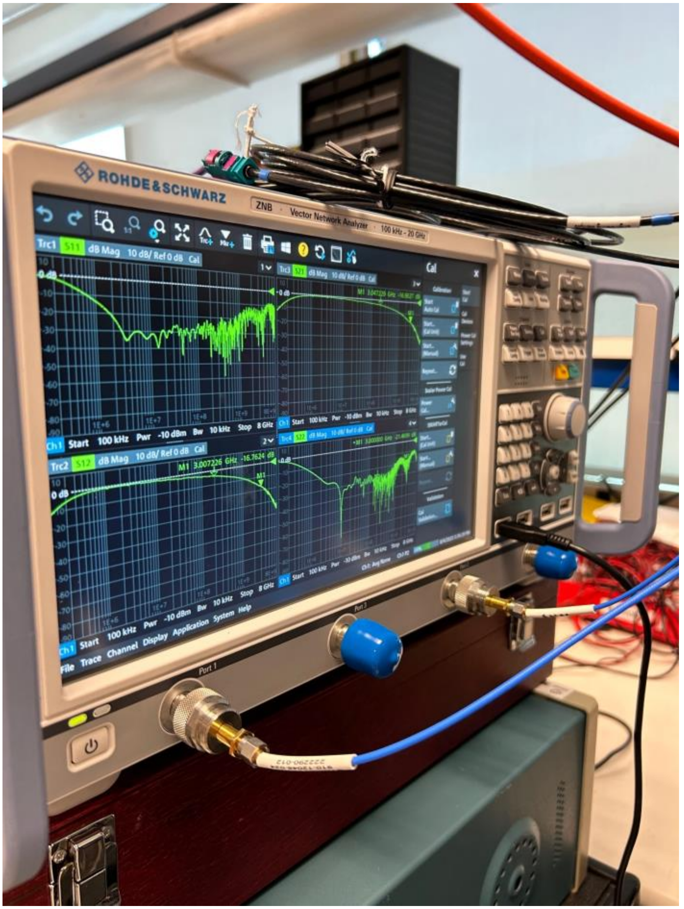
# DME Receiver CW Noise Simulation Results



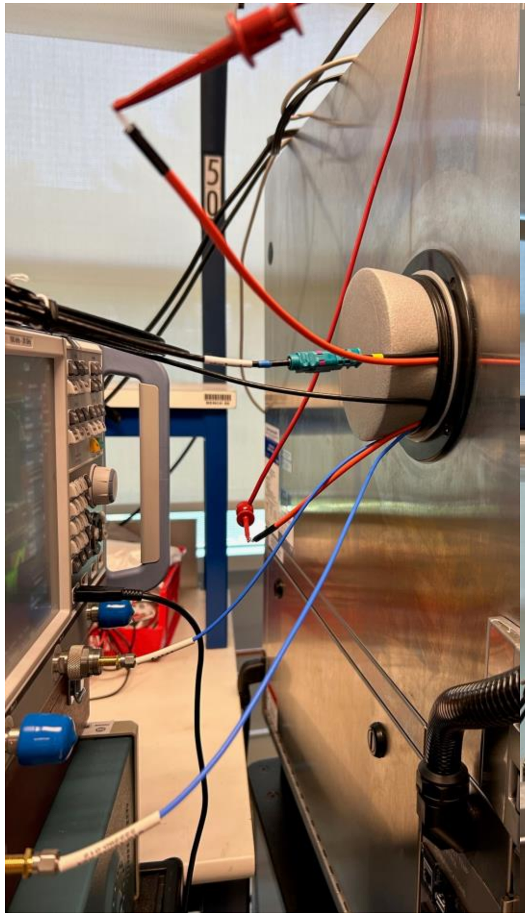

- GMSLE DME MF receiver meets 355mA BCI test level-equivalent noise with margin at -5dBm transmit level
  - A mixed-signal single-bit matched filter receiver meets requirements with low complexity
  - Multi-bit matched filter, higher OSR, give higher performance and may be used but are not required
  - GMSLE Upstream low data rate transmit level of -5dBm keeps spectral energy in FM band low

# POC Qualification Process Test Setup

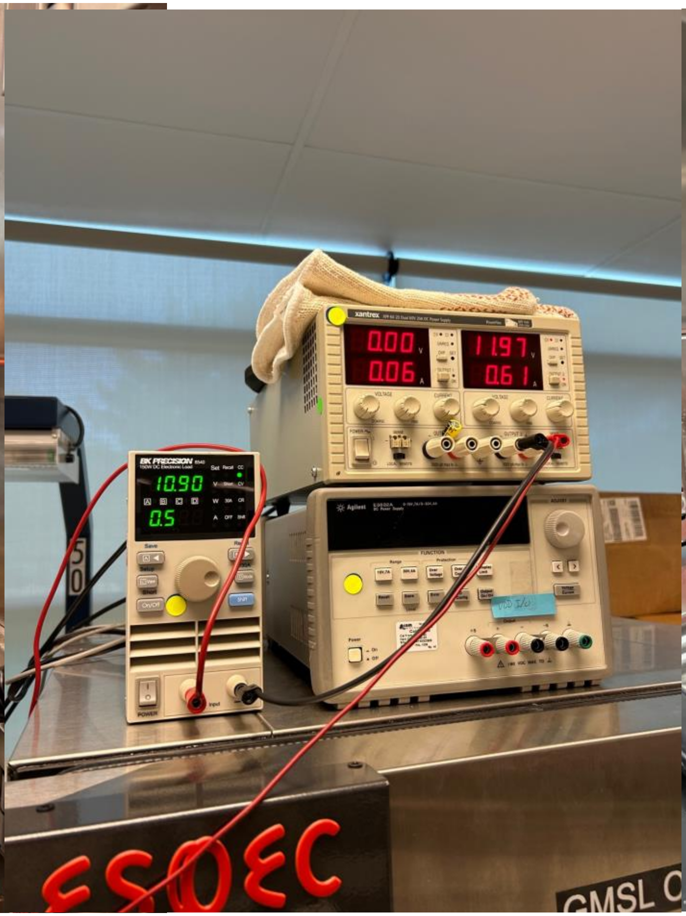





2-port VNA for IL & RL measurement



View from VNA going into Oven




DC power supply and Electronic Load (bias)

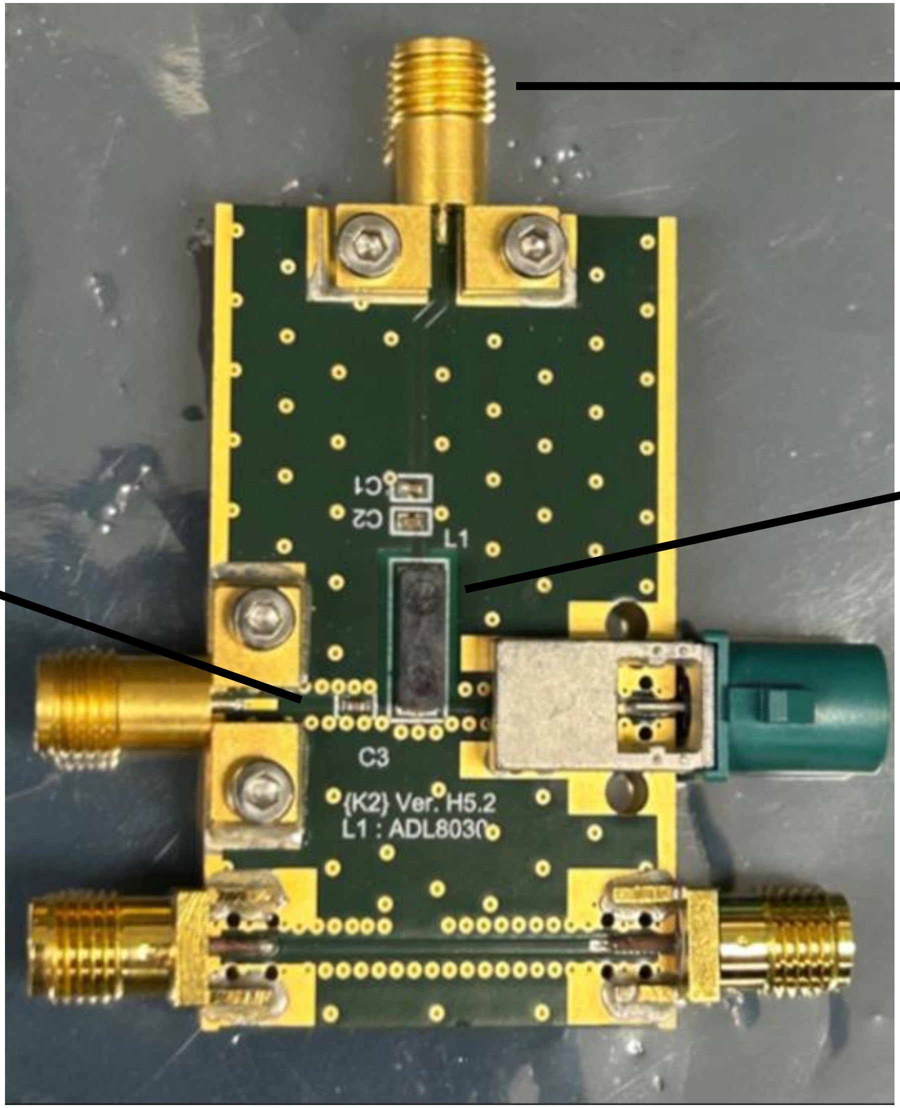
PoC coupon boards inside oven chamber

# POC Coupon Board Example

Connection to 12V source/load

AC coupling Capacitor

PoC Inductor




Connection to VNA for s-param measurement

Automotive coax connector

Reference trace

# Mystery Revealed: Single Inductor POC with GMSLE

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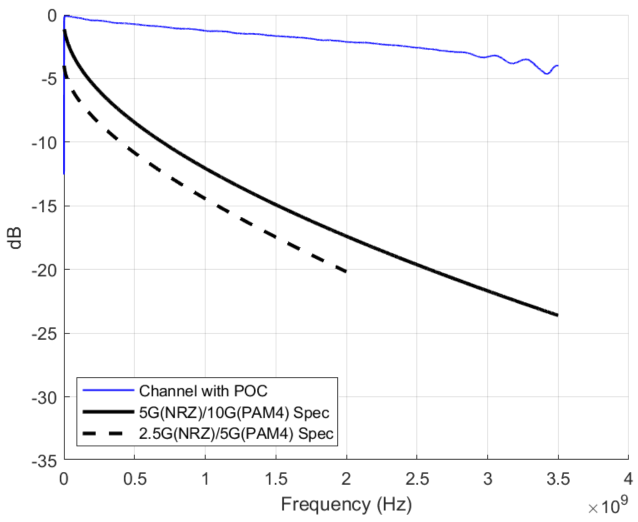
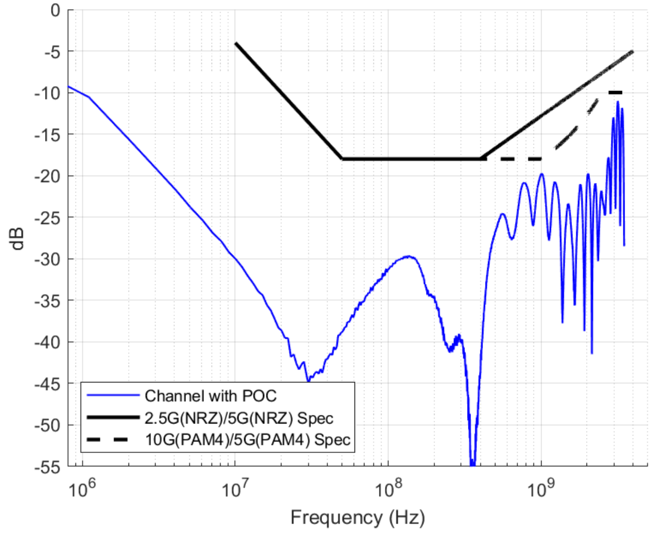
- Single inductor POC solution measured at 600mA load current:
  - Short channel – 0.5m RTK031-type cable + 2xPOC at 105C (RL worst case)
  - Long channel – 13.5m RTK031 with 2xPOC at 105C (IL worst case)

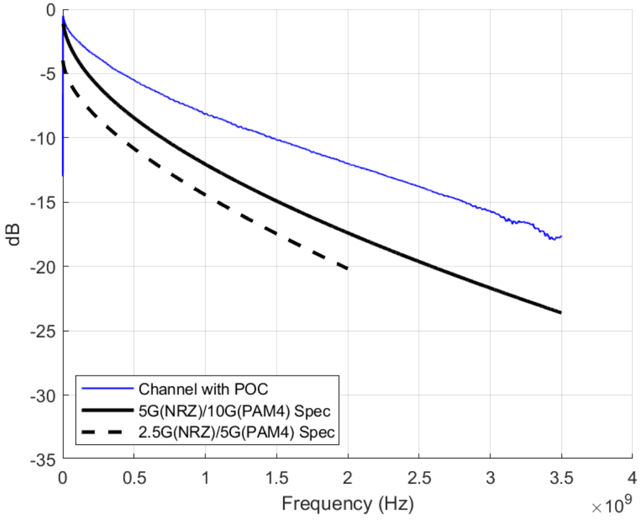
**IL – Short Channel with POC**



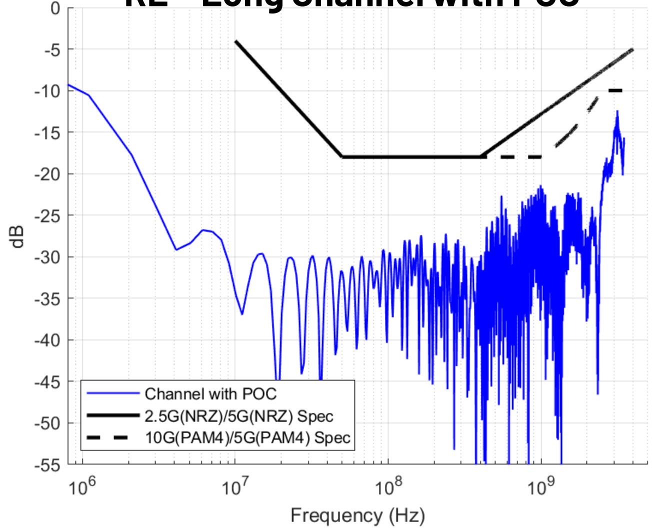

**RL – Short Channel with POC**




**IL – Long Channel with POC**

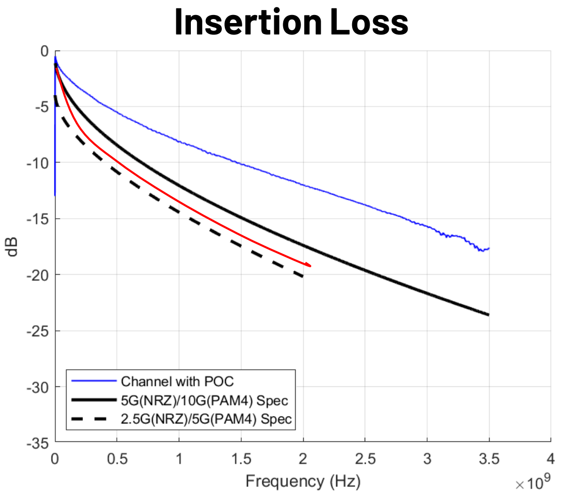


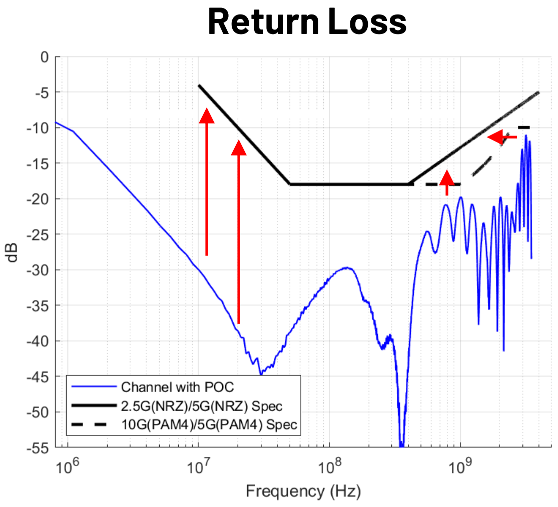

**RL – Long Channel with POC**



# Single Inductor POC Considerations

- Single inductor POC solutions are available today which meet RL and IL specifications for PAM4 limits with margin in worst-case conditions
  - With GMSLE, a more compact single inductor POC solution than GMSL3/2 can be used, due to upstream DME modulation. More low frequency return loss is allowed
  - For low-cost 3MP and 5MP applications, relaxing RL requirements at high frequencies and IL to the proposed limit line can further reduce the size of POC inductor for these applications



# Complexity Revisited: Detailed Camera Analysis

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- For widespread adoption of 802.3dm, reducing camera PHY complexity is paramount
  - GMSLE takes advantage of asymmetrical data rates
    - Reduce receive complexity for the low rate receiver on one side of the link
  - TDD by contrast needs to implement a full speed receiver on both sides of the link
- Build on analysis of Lo [4] and Houck [5]
- Compare GMSLE PHY with TDD PHY
  - Starting point: ASA PHY and GMSL3/2 PHYs in same geometry
  - Make allowances for changes for GMSLE and TDD:
    - No OAM root/leaf node command overhead in TDD vs. ASA
    - Adjust FEC (ASA->TDD-proposed; GMSL->GMSLE-proposed)
- Digital
  - TDD estimated at **26% more** NAND gate equivalent digital area^ primarily in these areas:
    - Least Mean Squared (LMS) or other adaptive alg. vs. none in GMSLE
      - Adaptation for TDD CTLE + DFE* vs. matched filter in GMSLE
    - RS-FEC
      - TDD: (130,122) t=4 vs. GMSLE: (30,26) t=2
      - FEC Decoder complexity + 130 vs 30 symbol buffer storage
    - Additional FIFOs in TDD

^after Post-shrink of 10% and considering 60% utilization for both

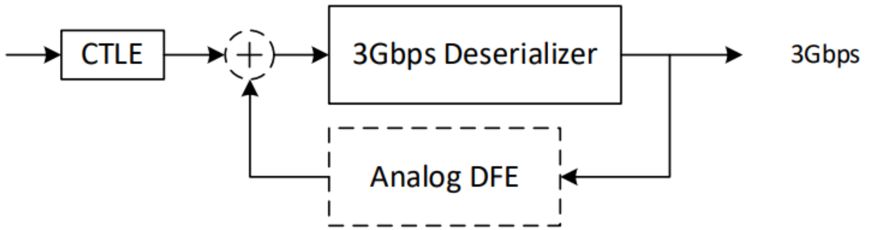
* A DFE is a very good idea at 3GBaud

| | Approx. Extra relative Digital Area |
|---|---|
| Adaptation/LMS | +12.6% |
| RS-FEC difference | +11.9% |
| Additional FIFOs + misc | +1.5% |
| Total: | +26% |

# Detailed Camera Complexity Analysis

- Analog
  - TDD estimated at **250% more** analog area primarily in these areas:
    - TDD: High-speed 3Gbps CTLE+DFE receiver vs. GMSLE hybrid + DME matched filter
    **→TDD: 245% more area**
    - CDR, 4%
    - Power management, 1%

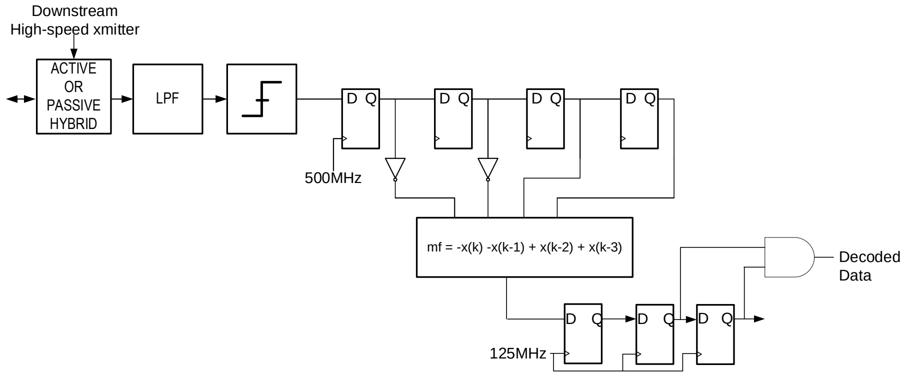
**TDD Upstream Receiver**




From [4]

≠

**GMSLE DME Upstream Receiver**




- Integration
  - 26% increase in digital complexity is significant
    - Camera nodes will stay with 22nm and even 40nm processes for foreseeable future
  - 250% increase in analog complexity is extremely significant and scales less with process
  - TDD increased complexity translates to larger die area and higher cost

# Relative Complexity Analysis, Camera PHY Revisited

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| | GMSLE | ACT | TDD |
|---|---|---|---|
| Camera Downstream highspeed TX Complexity | **Least complex**<br>**Lower PAPR (NRZ)**<br>▪ **2.5Gbps NRZ, 5Gbps NRZ opt.** | Slightly more complex<br>Higher PAPR (2.5 & 5Gbps vs NRZ)<br>▪ PAM4 @ 2.5 & 5Gbps | More complex<br>▪ TDD > 1.5% Digital |
| Camera Upstream lowspeed RX Complexity | **Much Less Complex**<br>▪ **Analog Matched Filter**<br>▪ **No EQ Required** | **Much Less Complex**<br>▪ **Analog Matched Filter**<br>▪ **No EQ Required** | Much more complex<br>▪ TDD<br>▪ Equalization<br>>250% Analog<br>> 24.5% Digital |
| Camera Power Consumption | **Lowest** | **Lowest** | Highest, Higher Peak Power<br>▪ TDD<br>▪ Equalization |
| Camera LS RX FEC | n=30,k=26, m=8, t=2 | n=50, k=46, m=6, t=2 | n=130, k=122, m=8, t=4 |
| Camera LS RX FEC decoder area complexity^ | 1.0x<br>1 symbol/clock impl @125MHz | **0.71x**<br>1 syml/clk @117.1875 MHz | **2.66x** Much more complex |
| Upstream burst protection | **64ns** | 51.2ns less than GMSLE | 10.6ns much less than GMSLE |
| Crystal-less Camera Serializer | **Simple**<br>▪ **Mass production** (GMSL) | Simple | Possible, but more Complex |
| Upstream latency (including FEC) | 8μs | Similar to GMSLE (est) | ~9.6μs (est., based on [2]) |
| Summary | ▪ **Lowest PAPR (NRZ modes)**<br>▪ **Lowest Complexity for 3MP 2.5Gbps and 8Mp 5Gbps cameras**<br>▪ **Highest burst protection** | Slightly higher PAPR<br>Low Complexity | Highest complexity. Raises cost, power for 3MP 2.5Gbps and 8MP 5Gbps cameras. XTAL-less more complex. Lower burst protection margin with > 2x the complexity |



^equivalent area of num 2 input NAND gates + 2-port memory in same geometry ^^(floor((n-k)/2)*m)/Baud

# Relative Complexity Analysis, HS RX, LS TX PHY

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| | GMSLE | ACT | TDD |
|---|---|---|---|
| POC | Small, single inductor, proven | Small, single inductor | **Smallest, single inductor** |
| Downstream HS Receiver Complexity | **Least complex**<br>▪ More Euclidean dist. @2.5 Gbps & 5Gbps PAM2 mode<br>▪ Analog or Digital EQ OK | Most complex<br>▪ Less Euclidean distance @2.5 & 5 Gbps<br>• Long digital FFE + 1-tap MLSE or DFE (or DFFE)<br>200% | More complex<br>▪ TDD |
| Downstream HS FEC | n=144,k=122, m=8, t=11 | n=360,k=326, m=10, t=17 | n=130,k=122, m=8, t=4 |
| Downstream HS RX FEC Correctable burst length ^^ | 29.3ns (L=1,2,4) | **60.4ns** (L=1,2,4 in 2.5/5/10Gbps) | 10.6ns (L=1,2,4) |
| Downstream HS RX FEC Decoder Area Complexity^ | 1.0x | 1.6x | 0.66x |
| Downstream Latency (including FEC) | 2.5Gbps: 2.75μs<br>5Gbps: 1.8μs (L=2)<br>10Gbps: <2μs (L=4) | 2.5Gbps: 4.096μs^^^<br>5 Gbps: 2.764μs (L=2)<br>10Gbps: 2.048μs (L=4) | Claimed 1μs from [2] |
| Downstream Summary | **Lowest complexity**<br>**Analog or digital EQ OK** | Higher complexity<br>Digital ADC and EQ required | High Complexity, TDD<br>Lower burst noise protection |
| Reliability (DFMEA) | **Proven (GMSL)** | Limited volume | **Not proven** |
| Units Shipped | Base architecture (GMSL):<br>**> 1.1 Billion links** | Base architecture (802.3ch):<br>100k (est.) | (ASA)<br>0 |

^equivalent 2 input NAND gates area + two port memory area in same geometry. 750MHz clock in all designs
^^^ from 802.3 clause 149 table 149-20

# Conclusion

- This presentation has shown GMSLE complexity is lower than proposed TDD and ACT solutions
  - GMSLE DME Upstream Low-speed link operates with margin over automotive noise conditions with low complexity
  - Single inductor POC solutions are available for FDD, today
    - Relaxed RL requirements at low frequency for GMSLE enable even more compact 1 inductor POC
- GMSLE complexity is less than TDD at the camera and less than ACT at a host PHY
- GMSLE offers an appropriate level of complexity for the channel and meets Task Force Objectives
- Future contributions, Downstream high-speed receiver noise measurements and cable considerations, will be presented
- Looking to collaborate and build consensus in the Task Force

# References

[1] BCI-Induced Noise Ingres to Coaxial MDI Test Method and Measured Levels, N Pischl, and M Tazebay, https://www.ieee802.org/3/dm/public/1124/Pischl_3dm_01a_1124.pdf

[2] Proposed Preamble: Synchronization and Harness Defect Detectio, J Cordaro, https://www.ieee802.org/3/cg/public/adhoc/cordaro_3cg_06_0418.pdf pp 19-21

[3] B Sklar, and f harris, Digital Communications Fundamentals and Applications, 3rd Edition. New York: Pearson Education, Inc, 2021 pp 117-121

[4] Upstream Receiver, W Lo, https://www.ieee802.org/3/dm/public/0125/Lo_3dm_02a_0125.pdf

[5] Exploring Receiver Tradeoffs: 100Mbps and 3Gbps Implementations, TJ Houck, https://www.ieee802.org/3/dm/public/0125/Houck_3dm_01_0121_5.pdf