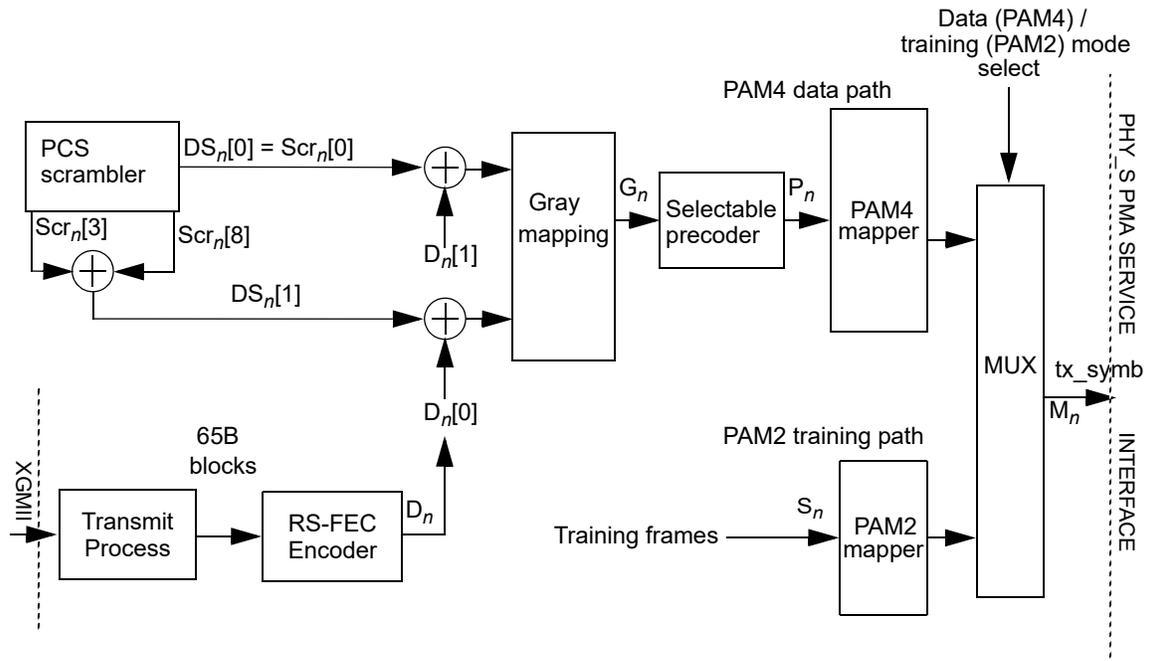
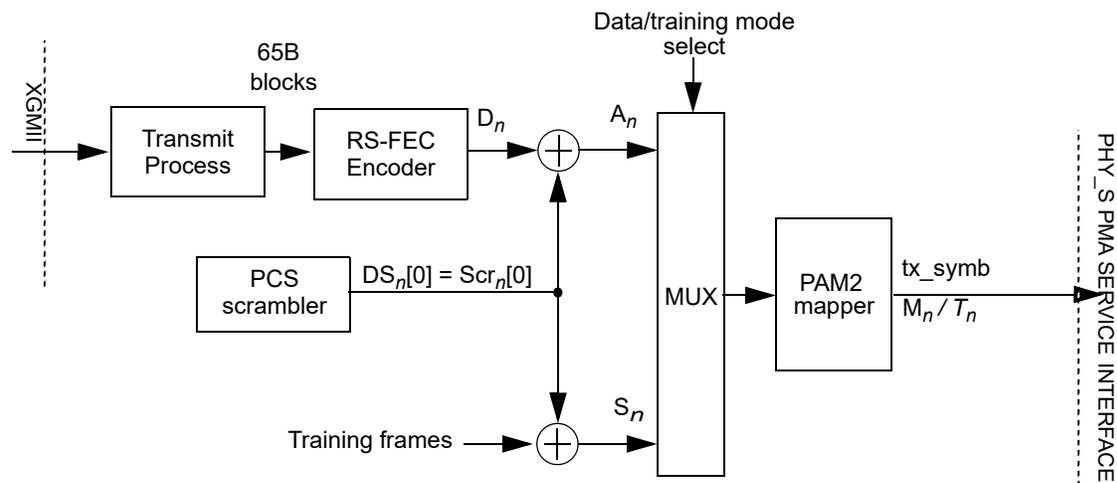


The block diagram of HS\_TX PCS Transmit functions is shown in Figure 201–7a and Figure 201–7b, replacing Figure 149-5. .



NOTE —The  $S_n$  are from the training frame, and the MUX selects the PAM2 path while in PAM2 training states.

Figure 201–7a—10Gbps HS\_TX PCS Transmit function block diagram



NOTE 1 —The  $S_n$  are from the training frame, and the  $A_n$  are for the 2.5G and 5G HS\_PATH.  
 NOTE 2 — The output of the PAM2 mapper is  $M_n$  in data mode and  $T_n$  in training mode.

Figure 201–7b—2.5Gbps and 5 Gbps HS\_TX PCS Transmit function block diagram

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A block diagram of the low speed path PCS Transmit functions is shown in Figure 201–11.

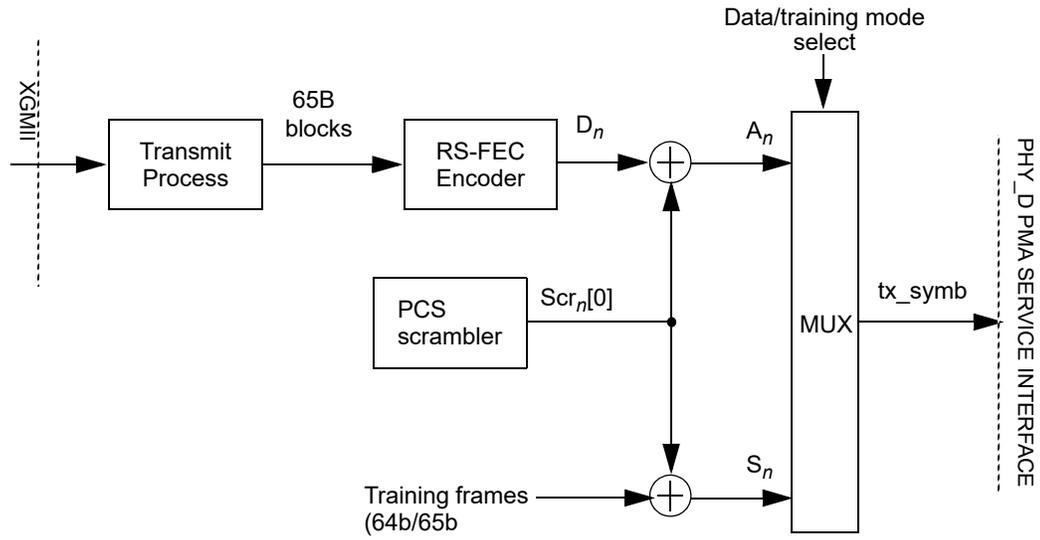


Figure 201–11—PCS Transmit function block diagram for low speed path

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