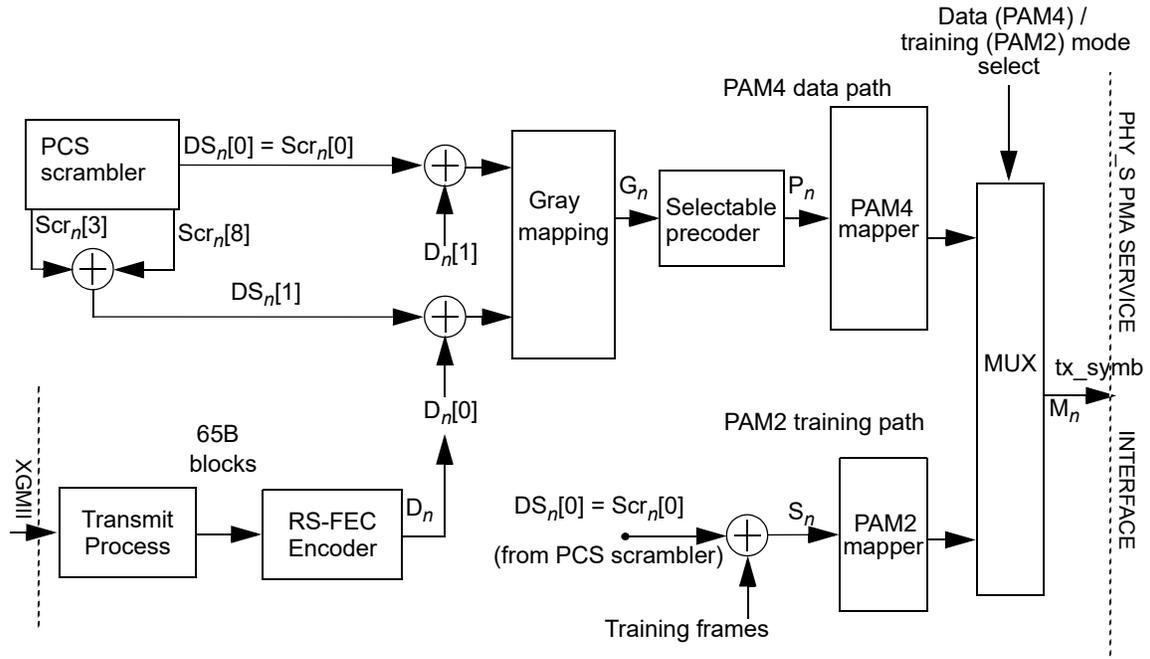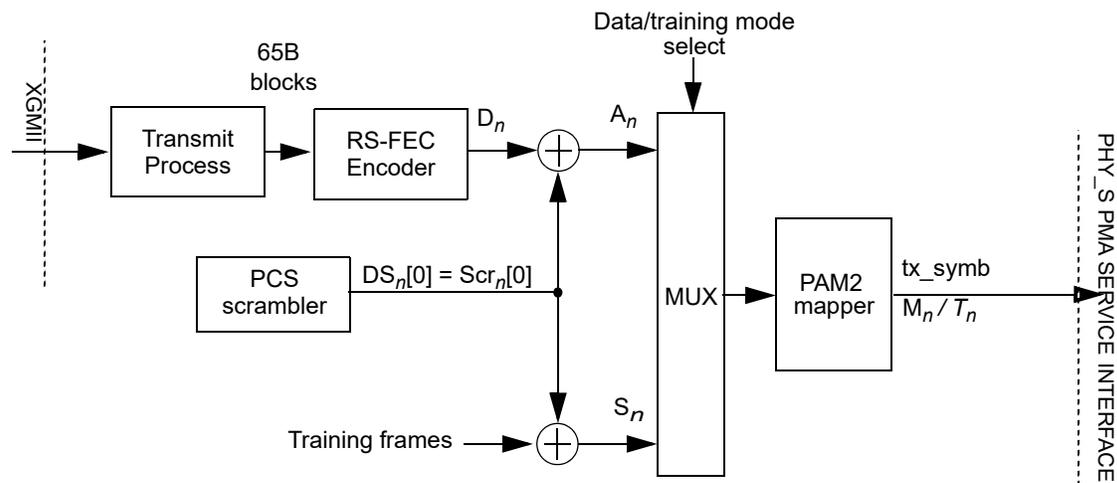The block diagram of HS_TX PCS Transmit functions is shown in Figure 201–7a and Figure 201–7b, replacing Figure 149-5. .

NOTE —The S_n are from the training frame, and the MUX selects the PAM2 path while in PAM2 training states.

Figure 201–7a—10Gbps HS_TX PCS Transmit function block diagram

NOTE 1 —The S_n are from the training frame, and the A_n are for the 2.5G and 5G HS_PATH.
NOTE 2 — The output of the PAM2 mapper is M_n in data mode and T_n in training mode.

Figure 201–7b—2.5Gbps and 5 Gbps HS_TX PCS Transmit function block diagram

A block diagram of the low speed path PCS Transmit functions is shown in Figure 201–11.

NOTE – The RS-FEC encoder for the data mode and training mode paths is the same (See 201.4.5), but are shown in separate chains for clarity.
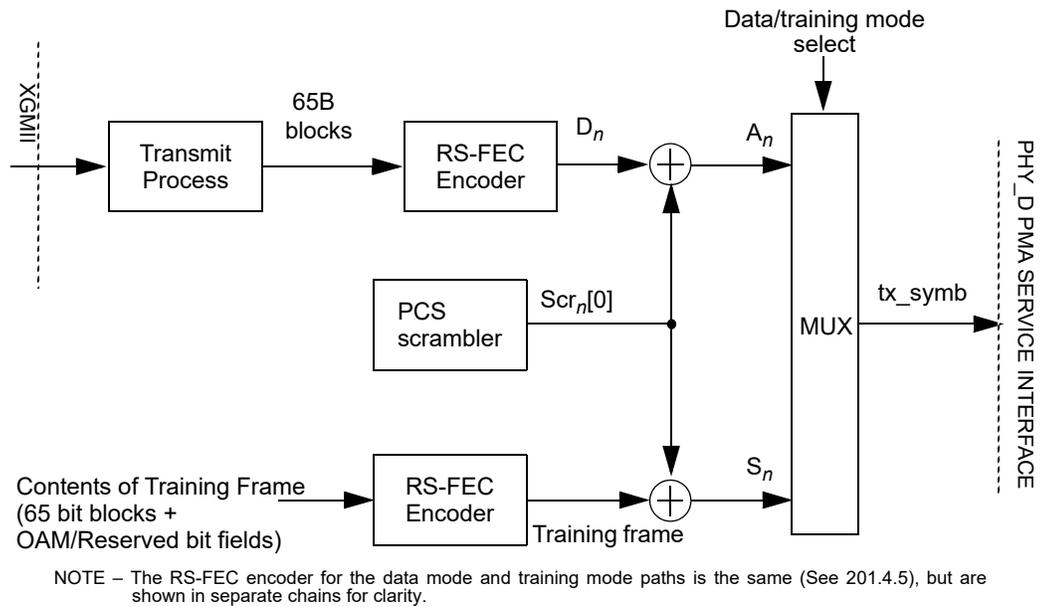
Figure 201–11—PCS Transmit function block diagram for low speed path