Annex 201 Allocation of Delay Limit Budget (Informative)

In 201.14, the Delay Limits are set for the HS_PATH and LS_PATH, not including the delays introduced by the physical medium interconnecting the two PHYs. In asymmetrical operation, the delay limits between the HS_PATH and LS_PATH are quite different.

To increase the chance of interoperability between different implementors it is recommended the transmit and receive portions of the PHY delay limits in 201.14 be allocated as follows:

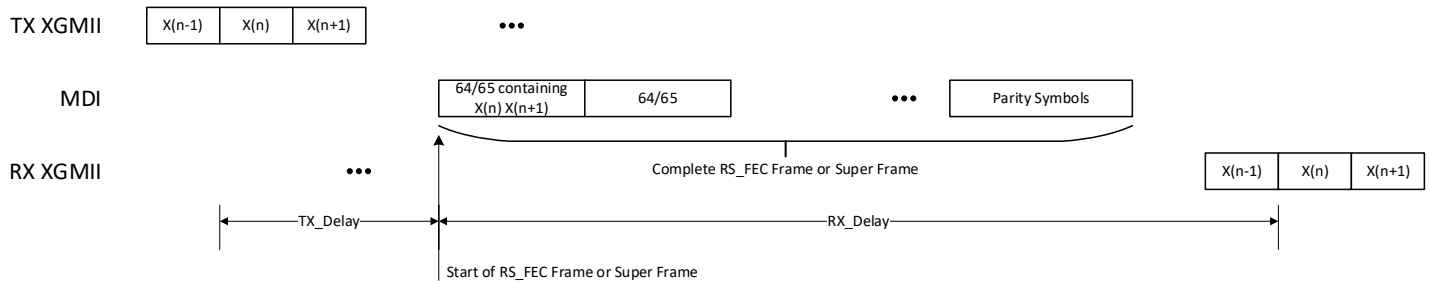
- The HS_TX TX_Delay is allocated 10% of the delay budget.
- The HS_RX RX_Delay is allocated 90% of the delay budget.
- The LS_TX TX_Delay is allocated 25% of the delay budget.
- The LS_RX RX_Delay is allocated 75% of the delay budget.

In figure XXX, XGMII transfers are shown as X(#) where # is sequentially incrementing. Let the first 64/65 block of a RS frame or super frame contain the X(n) and X(n+1) XGMII transfers. To insure a consistent methodology on measuring the delays is used by all implementors, the following points in the data stream are used.

The TX_Delay is measured from the start of the X(n) transfer on the TX XGMII to the start of the first symbol of the frame or super frame at the MDI.

The RX_Delay is measured from the start of the first symbol of the frame or super frame at the MDI to the start of the X(n) transfer on the RX XGMII.

Figure XXX XGMII to MDI to XGMII Timing Diagram



Since the start of the first symbol of the frame or super frame may not be measurable directly on the MDI, it is recommended that the PHY implementors specify TX_Delay and RX_Delay in the product documentation.