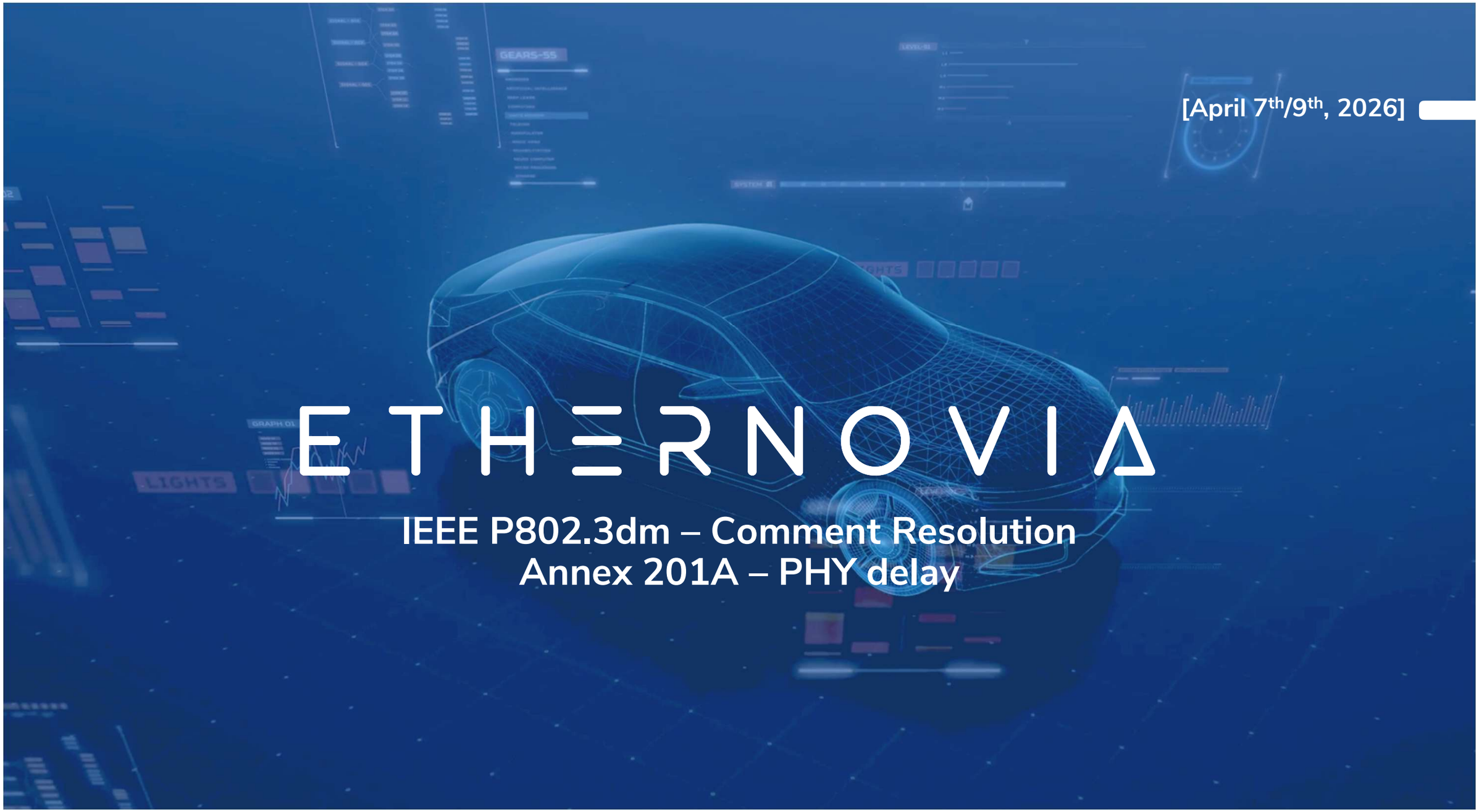
[April 7th/9th, 2026]



IEEE P802.3dm – Comment Resolution
Annex 201A – PHY delay

Denoting Interfaces incl. IEEE Std 802.3 Clause 90

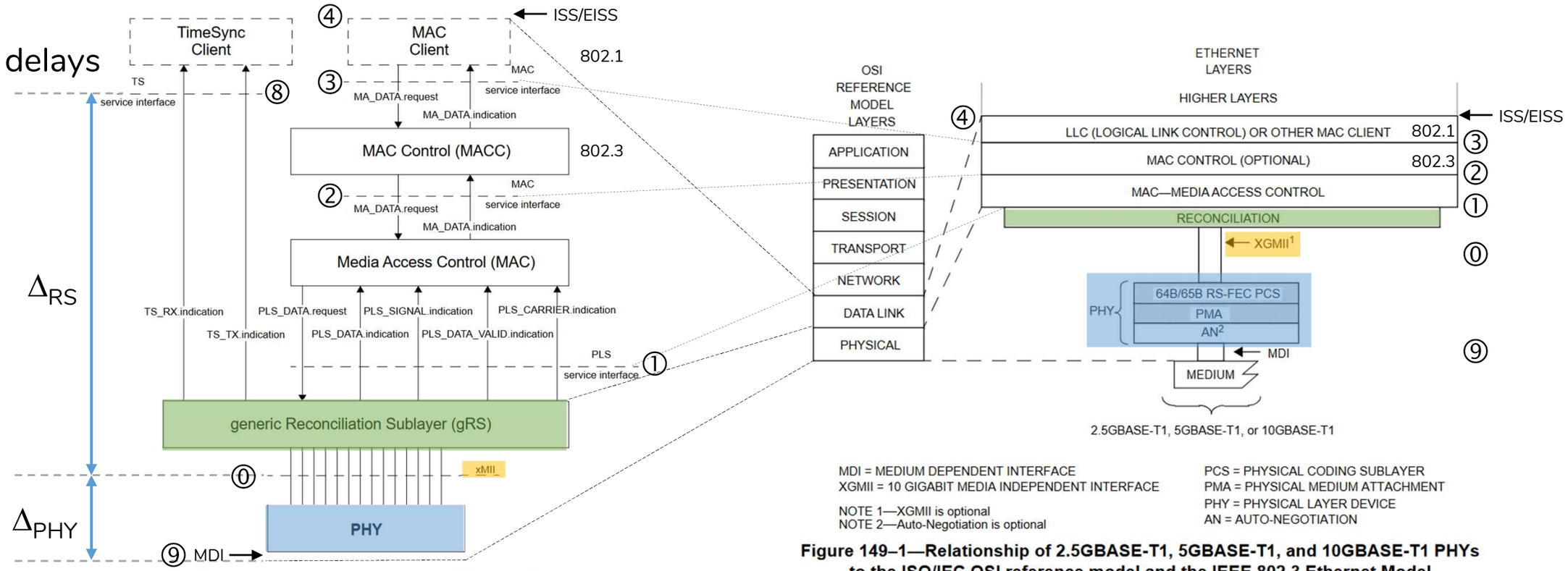


Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

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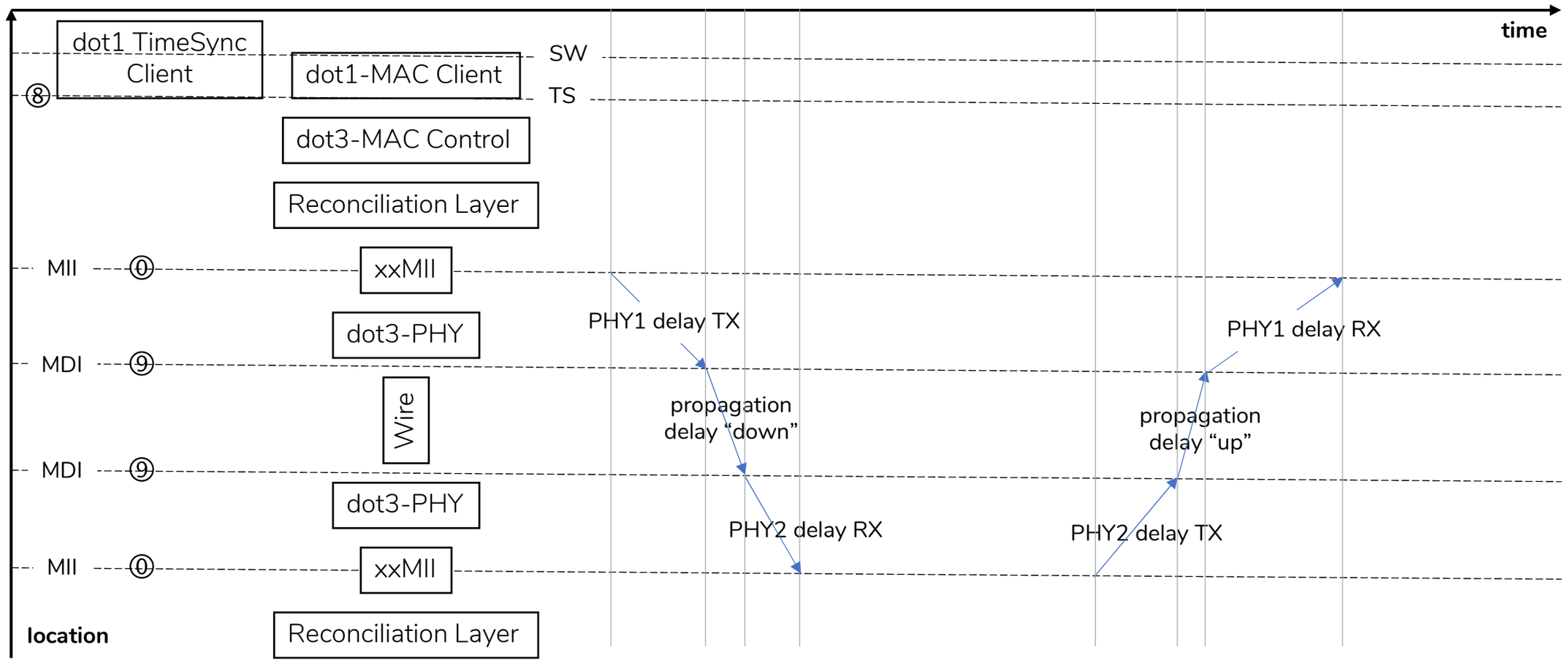
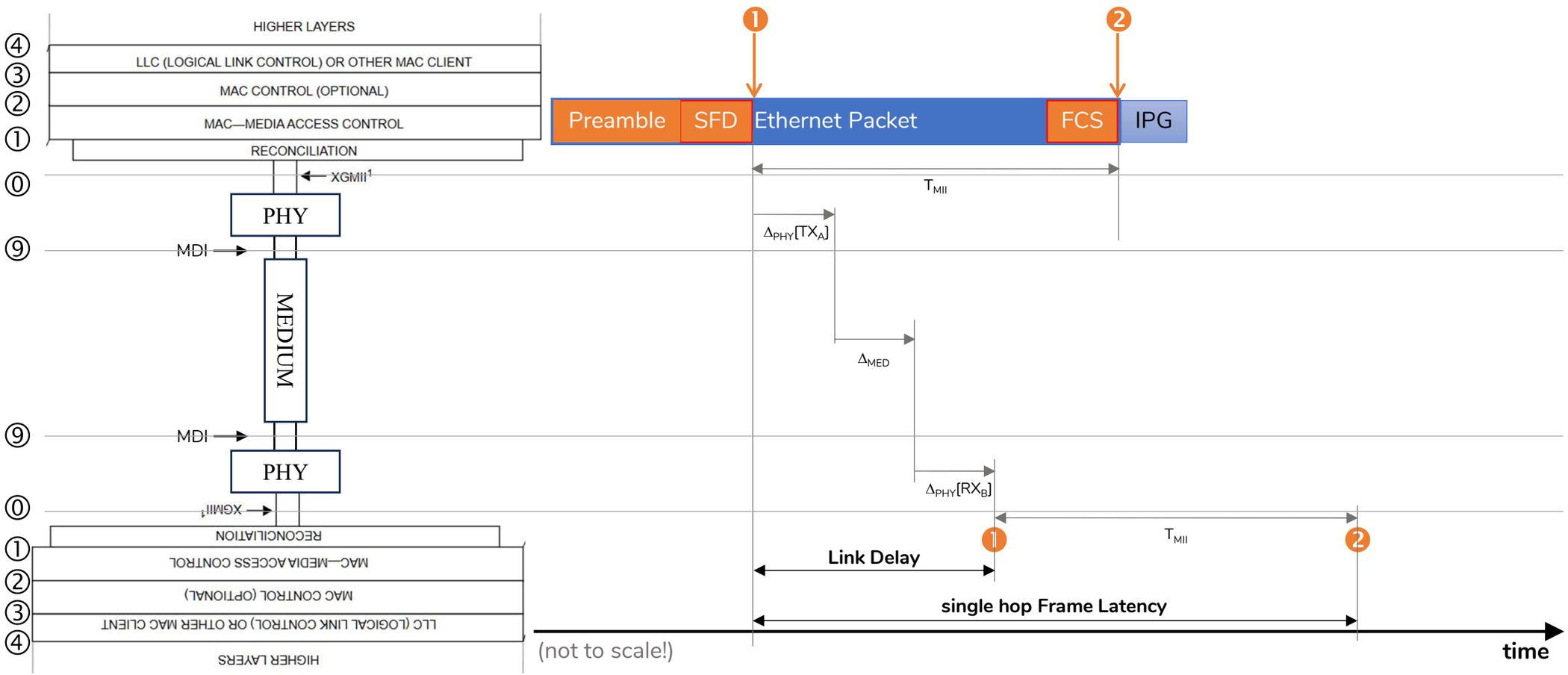
Transmit and Receive Delays



Same Bit Rate[1)] R for MII and MDI
No Interleaving, no FCS



[1)] 802.3:1.4.213 bit rate (BR)

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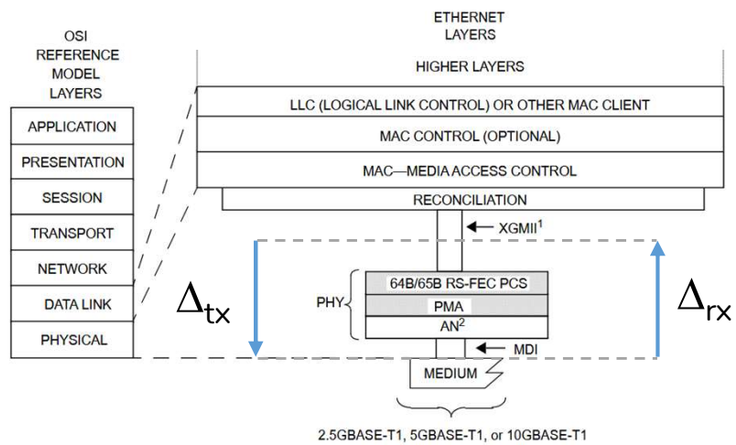
IEEE Std 802.3CH – Section 149.10 Delay Limits

149.10 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 149–20. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.



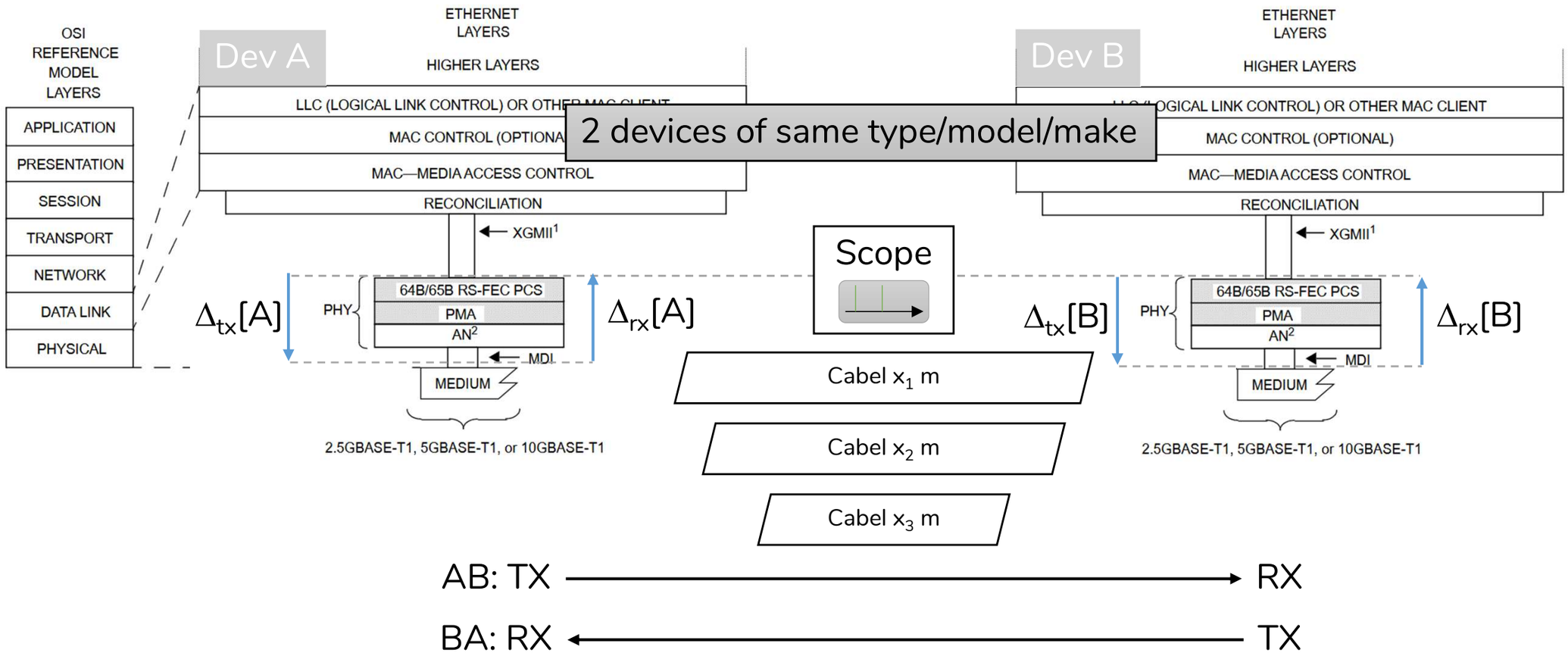
per line-item:

$\Delta_{CH}[M,I] > \Delta_{tx} + \Delta_{rx}$

Table 149–20—Delay Limits

Mode	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5GBASE-T1	1x	10 240	20	4096
5GBASE-T1	1x	10 240	20	2048
5GBASE-T1	2x	13 824	27	2764.8
10GBASE-T1	1x	10 240	20	1024
10GBASE-T1	2x	13 824	27	1382.4
10GBASE-T1	4x	20 480	40	2048

IEEE Std 802.3CH – Section 149.10 Measurement Setup



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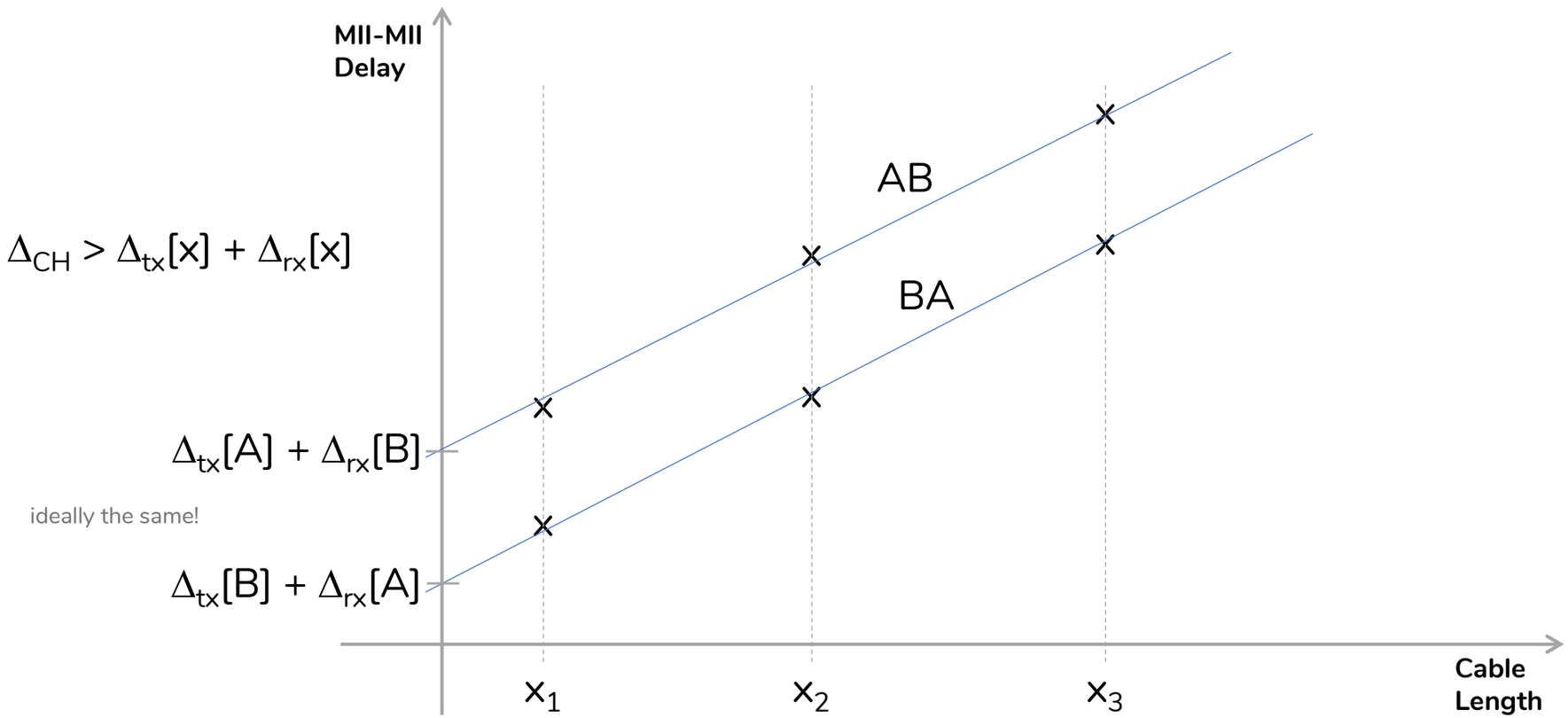
IEEE Std 802.3CH - Section 149.10 Measurement Analysis



(use linear regression on measured data)

NOT to scale – just a concept depiction

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MAC Control PAUSE Operation IEEE Std 802.3CH

$d_{Total} = d_{Pause} + (d_{TA} + d_W + d_{RB}) + d_{React} + d_{MTU} + (d_{TB} + d_W + d_{RA})$

$d_{Total} = (d_{TA} + d_{RA}) + (d_{TB} + d_{RB}) + (d_{Pause} + d_{React} + d_{MTU} + 2d_W)$

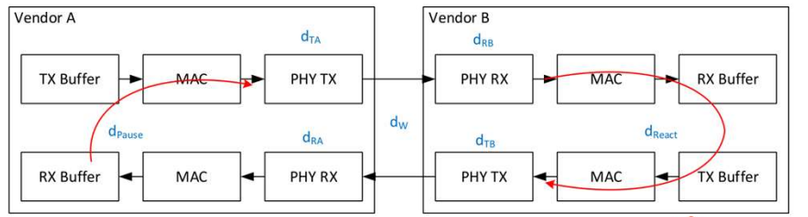
- Regroup transmit and receive of each path to be from same device

$d_{Total} = d_A + d_B + d_O$

Where:

- d_A and d_B are PHY Delay limit specified by IEEE (i.e. Clause 149.10) reported by vendor

- d_{Pause} RX buffer high water mark to pause frame generated on XGMII
- d_{React} Pause frame received on XGMII to TX buffer stopping traffic
- d_{TA}, d_{TB} XGMII to MDI PHY delay for vendor A and B
- d_{RA}, d_{RB} MDI to XGMII PHY delay for vendor A and B
- d_W Wire propagation delay. Assumed to be the same both direction
- d_{MTU} Duration of maximum size packet



https://www.ieee802.org/3/dm/public/0326/Lo_3dm_01_030926.pdf

Because the PAUSE control information passes through each PHY once in TX and once in RX direction, only the sum (as specified in .3CH) of the two is relevant!

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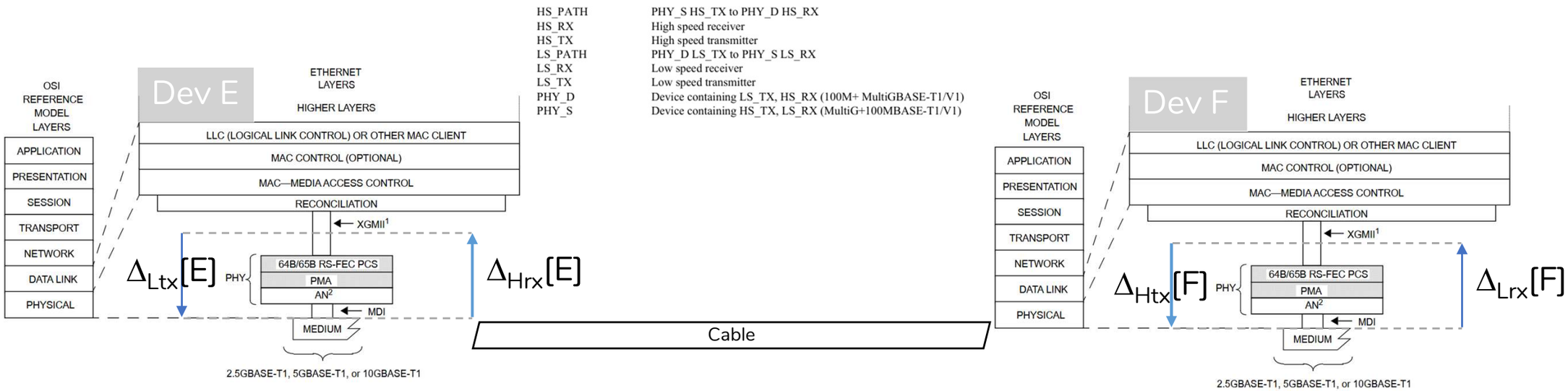
IEEE P802.3dm – Asymmetric Ethernet



PHY_D: LS_TX - HS_RX

from .3dm Table 201-23
not in same PHY

$\Delta_{Hdm} = \Delta_{Htx}[x] + \Delta_{Hrx}[y]$

$\Delta_{Ldm} = \Delta_{Ltx}[y] + \Delta_{Lrx}[x]$

PHY_S: HS_TX – LS_RX

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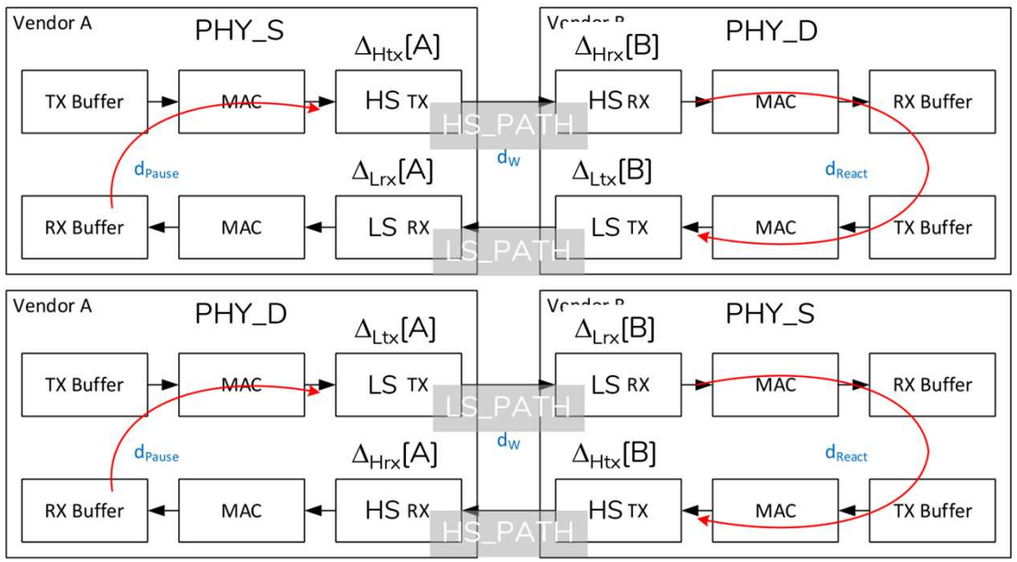
IEEE P802.3dm – Two distinct cases



HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter
PHY_D	Device containing LS_TX, HS_RX (100M+ MultiGBASE-T1/V1)
PHY_S	Device containing HS_TX, LS_RX (MultiG+100MBASE-T1/V1)

The HS_PATH delays for an implementation of the PHY link shall not exceed the limits shown in Table 201–23. The data delay is measured from the input of a given unit of data at the PHY_S XGMII to the presentation of the same unit of data by the PHY_D XGMII.

The LS_PATH delays for an implementation of the PHY link shall not exceed the limits shown in Table 201–23. The data delay is measured from the input of a given unit of data at the PHY_D XGMII to the presentation of the same unit of data by the PHY_S XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

Table 201–23—Delay Limits

PATH	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5G+100MBASE-T1/V1	1x	10 240	20	4096
5G+100MBASE-T1/V1	1x	10 240	20	2048
5G+100MBASE-T1/V1	2x	13 824	27	2764.8
10G+100MBASE-T1/V1	1x	10 240	20	1024
10G+100MBASE-T1/V1	2x	13 824	27	1382.4
10G+100MBASE-T1/V1	4x	20 480	40	2048
100M_MultiGBASE-T1/V1	—	TBD	TBD	TBD

Δ_{Hdm}[MI]

Δ_{Ldm}

HS_PATH: $\Delta_{Hdm} > \Delta_{Htx} + \Delta_{Hrx}$

LS_PATH: $\Delta_{Ldm} > \Delta_{Ltx} + \Delta_{Lrx}$

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gRS – xMII – PHY

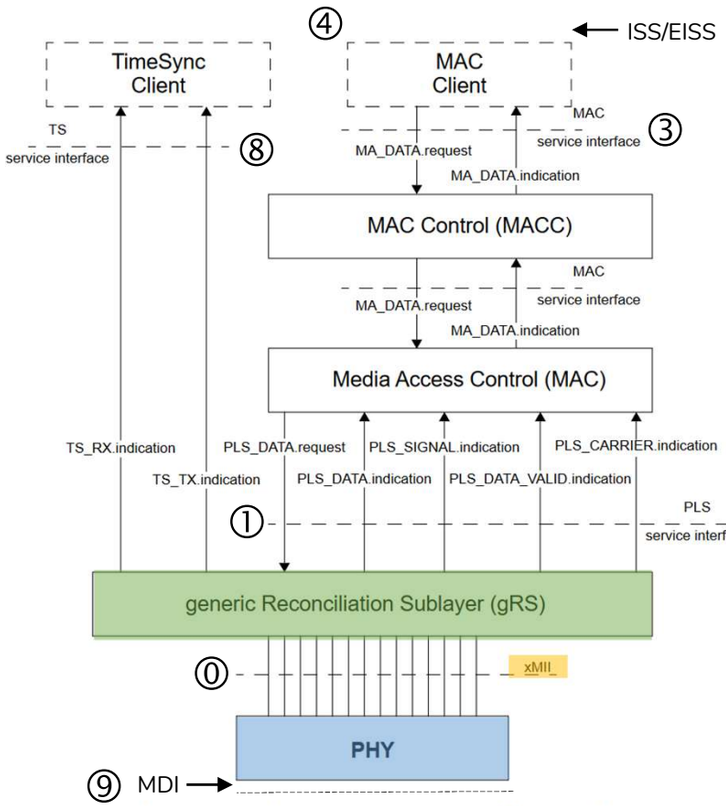
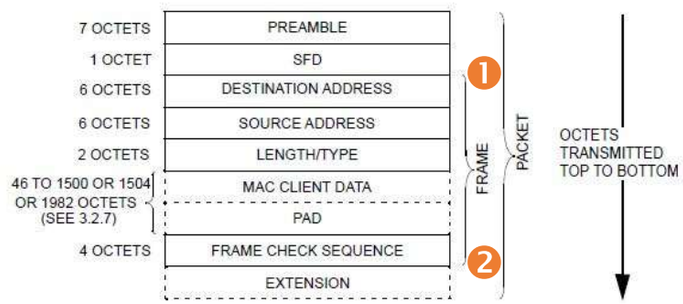
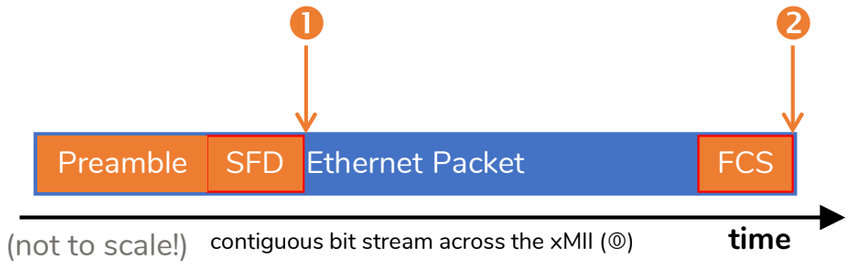


Figure 90–1—Relationship of the TimeSync Client, TSSI and gRS sublayer relative to MAC and MAC Client and associated interfaces

Processing through the MAC model layers is not considered here!



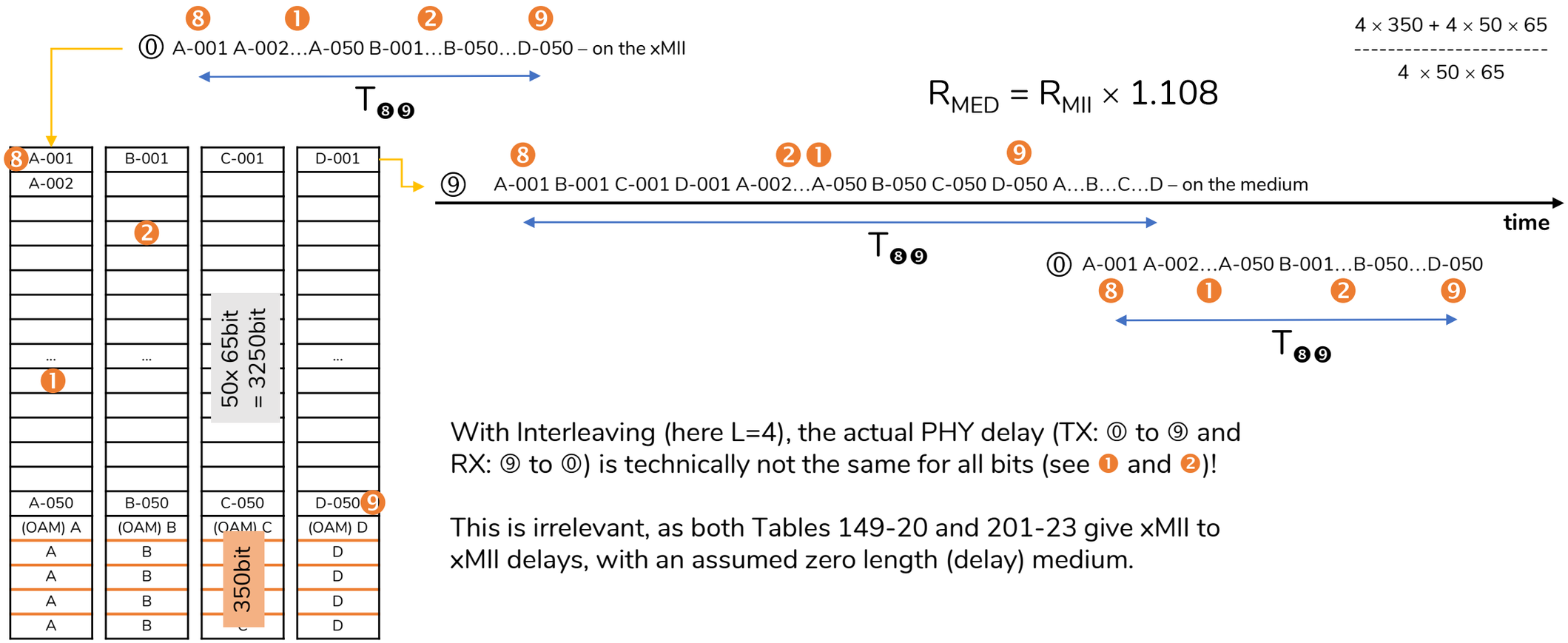
Below the (g)RS (at ⓪) the time between ❶ and ❷ (T_{MII}) is given by <the number of bits contained in the Ethernet Frame> (L) divided by <the nominal bit rate[1)] of the xMII> (R_{MII})



The bit stream across the xMII (at ⓪) is contiguous for TX and RX, independent of Interleaving

[1)] 802.3:1.4.213 bit rate (BR)

IEEE Std 802.3CH - Interleaving



With Interleaving (here L=4), the actual PHY delay (TX: ⓪ to ⑨ and RX: ⑨ to ⓪) is technically not the same for all bits (see ❶ and ❷)!

This is irrelevant, as both Tables 149-20 and 201-23 give xMII to xMII delays, with an assumed zero length (delay) medium.

The RS-FEC output superframe consists of L × 3600 bits

IEEE Std 802.1AS

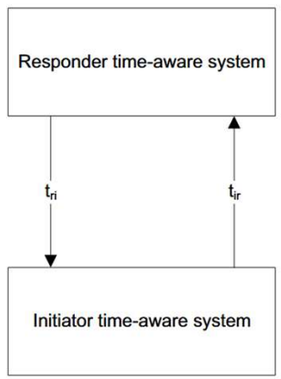


Figure 8-1—Propagation asymmetry

The meanLinkDelay is the mean value of t_{ir} and t_{ri}, i.e., meanLinkDelay = (t_{ir} + t_{ri}) / 2. The delayAsymmetry is defined as:

t_{ir} = meanLinkDelay – delayAsymmetry

t_{ri} = meanLinkDelay + delayAsymmetry

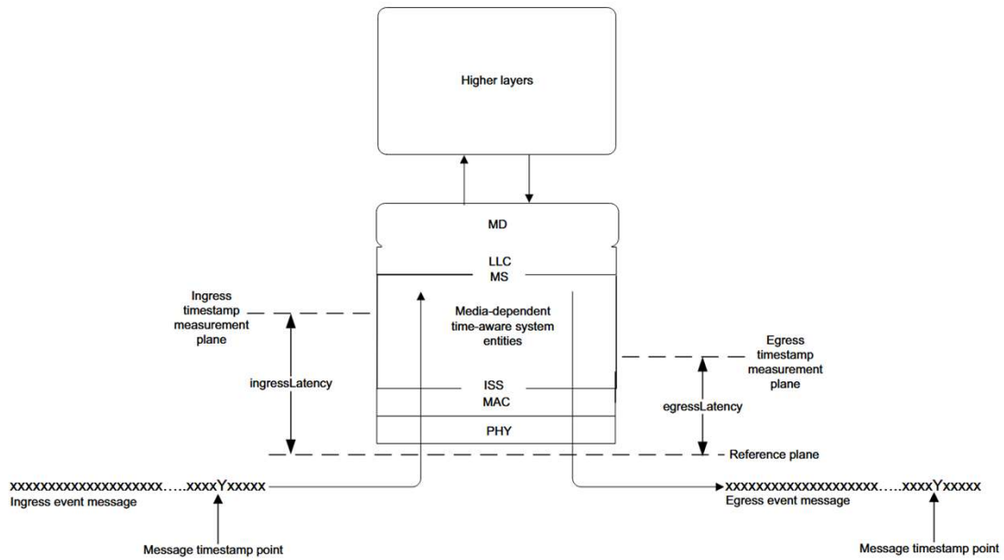


Figure 8-2—Definition of message timestamp point, reference plane, timestamp measurement plane, and latency constants

This does not make “physical” sense for Interleaving!

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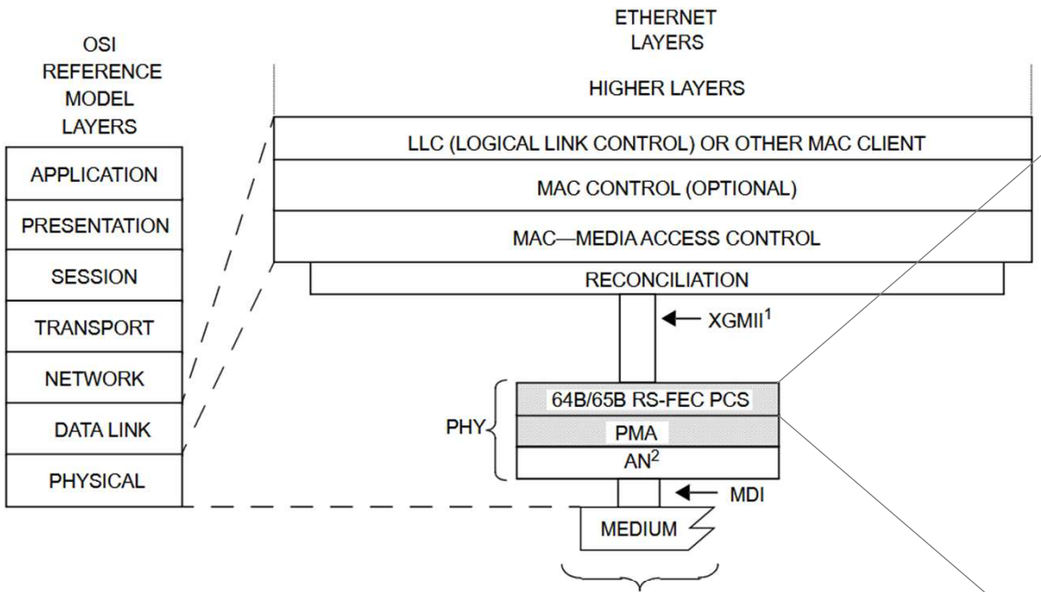
IEEE Std 802.3CH – PCS OAM

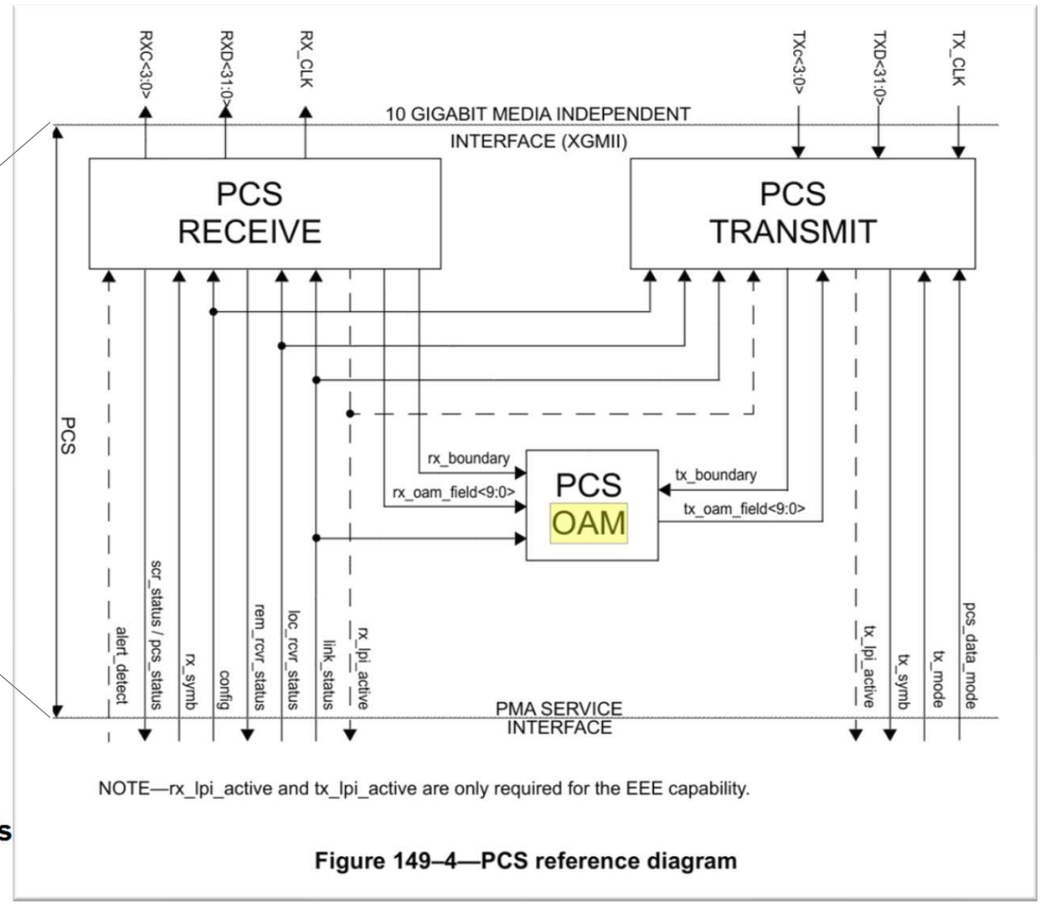


MDI = MEDIUM DEPENDENT INTERFACE
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

NOTE 1—XGMII is optional
NOTE 2—Auto-Negotiation is optional

PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

Figure 149–1—Relationship of 2.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model



NOTE—rx_lpi_active and tx_lpi_active are only required for the EEE capability.

Figure 149–4—PCS reference diagram

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Max Turner
Utrechtseweg 75
NL-3702AA Zeist
The Netherlands
+49 177 863 7804
max.turner@ethernovia.com

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IEEE Std 802.3CH – OAM

149.3.9.1 Definitions

OAM frame: A frame consisting of 14 octets of data, 14 framing bits, 14 reserved bits and two 10-bit Reed-Solomon parity symbols.

OAM symbol: A 10-bit symbol consisting of either one data octet plus a framing bit and a reserved bit, or a 10-bit Reed-Solomon parity symbol. Sixteen OAM symbols make up an OAM frame.

OAM field: A 10-bit field in each PHY frame reserved for the OAM symbol as described in 149.3.2.2.14 or in each refresh cycle as described in 149.3.6.3.

OAM message: A message contains a 4-bit message number plus 8 octets of message data (Message<7:0><7:0>) embedded in an OAM frame. The same OAM message can be repeated on multiple OAM frames.

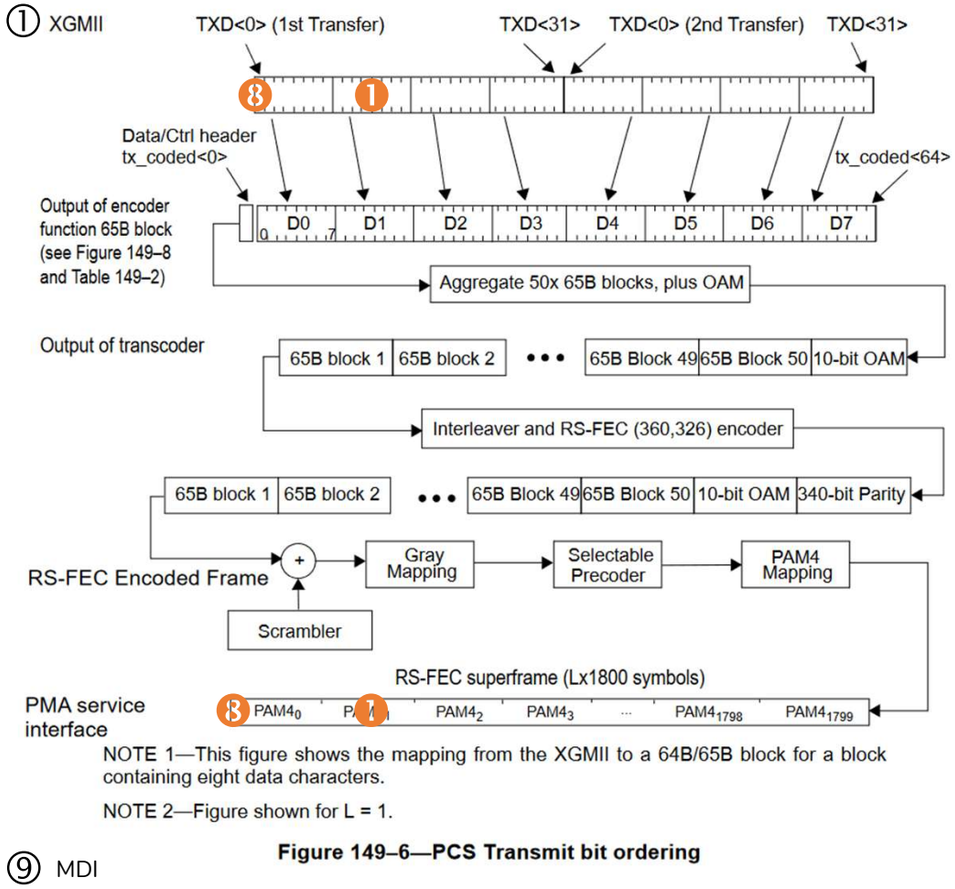
OAM status: The 4 octets of status data (Message<11:8><7:0>) that is embedded in each OAM frame.

$$(14 \times 8) + 14 + 14 + (2 \times 10) = 160$$

When the PCS frame is operating in interleaved mode of 2x or 4x, the first symbol (OAM<0>) shall be inserted in the first RS frame in the superframe so that the full OAM frame can be packed into eight superframes in the 2x interleaved mode, and into four superframes in the 4x interleaved mode.

$$8 \times 2 \times 10 = 160$$
$$= 4 \times 4 \times 10$$

IEEE Std 802.3CH – PHY Delay



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

Figure 149–6—PCS Transmit bit ordering

continuous bit stream, i.e this could be IDLE symbols or Packet bits

The (maximum) time it takes for any bit within the data stream (here - as an example - the end of the SFD) to pass between the MII ① and the MDI ⑨ is referred to as the (maximum) PHY delay

Upper limit values are given in IEEE802.3 Table 149–20

Table 149–20—Delay Limits

Mode	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5GBASE-T1	1x	10 240	20	4096
5GBASE-T1	1x	10 240	20	2048
5GBASE-T1	2x	13 824	27	2764.8
10GBASE-T1	1x	10 240	20	1024
10GBASE-T1	2x	13 824	27	1382.4
10GBASE-T1	4x	20 480	40	2048