202. TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

202.1 Overview

MultiGBASE-A PHYs support multiple rate options~~. They features~~ and baud commonality across high speed and low speed implementations. The PHYs use the same TDD cycle for all data rates (see 202.3.6), as well as use the same base FEC with different shortening parameters for the high speed and low speed directions.

202.1.1 Nomenclature

Editor's Note (to be removed prior to Working Group Ballot):

Need to add some explanation of TDD bursts, LEADER vs. FOLLOWER behavior, and TDD burst structure in US/DS direction as this is implied but not given much context in other parts of the text. For example needs to be defined that bursts are non-overlapping at the receiver, US bursts include one RS-FEC frame, DS bursts include 25 RS-FEC frames, etc. diagram of overall burst structure (refresh header plus data payload).

The MultiGBASE-AT1 and MultiGBASE-AV1 PHYs described in this clause represent two distinct PHY types that share the same PCS and PMA specifications subject to frequency scaling. In order to efficiently describe the two PHYs, the following nomenclature is used.

HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter
PHY_D	LS_TX, HS_RX mode of operation (high speed XGMII destination)
PHY_S	HS_TX, LS_RX mode of operation (high speed XGMII source)

When talking about the asymmetric PHY communicating on a shielded, balanced, pair of conductors, use:

MultiGBASE-AT1

When talking about the asymmetric PHY communicating on a coaxial cable, use:

MultiGBASE-AV1

When talking about all PHYs, regardless of transmit bit rate or cable type, use:

MultiGBASE-A

The six modes of operation and MAC data rate combinations for each of the two PHY types are shown in Table 202–1.

Table 202–1—PHY/PMD type definitions

PHY name	Medium interface	Mode of operation	Transmit MAC data rate	Receive MAC data rate
MultiGBASE-AT1	Differential (balanced)	PHY_D	100 Mb/s	2.5 Gb/s
			100 Mb/s	5 Gb/s
			100 Mb/s	10 Gb/s
		PHY_S	2.5 Gb/s	100 Mb/s
			5 Gb/s	100 Mb/s
			10 Gb/s	100 Mb/s
MultiGBASE-AV1	Single-ended (unbalanced)	PHY_D	100 Mb/s	2.5 Gb/s
			100 Mb/s	5 Gb/s
			100 Mb/s	10 Gb/s
		PHY_S	2.5 Gb/s	100 Mb/s
			5 Gb/s	100 Mb/s
			10 Gb/s	100 Mb/s

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

-T1 represents a single shielded balanced pair of conductors (i.e., differential)
-V1 represents a single coaxial cable (i.e., unbalanced)

Additionally, for parameters that scale with the PHY's supported MAC data rate, the parameter *S* is used for scaling as shown in Table 202–2.

Table 202–2—Scaling parameters

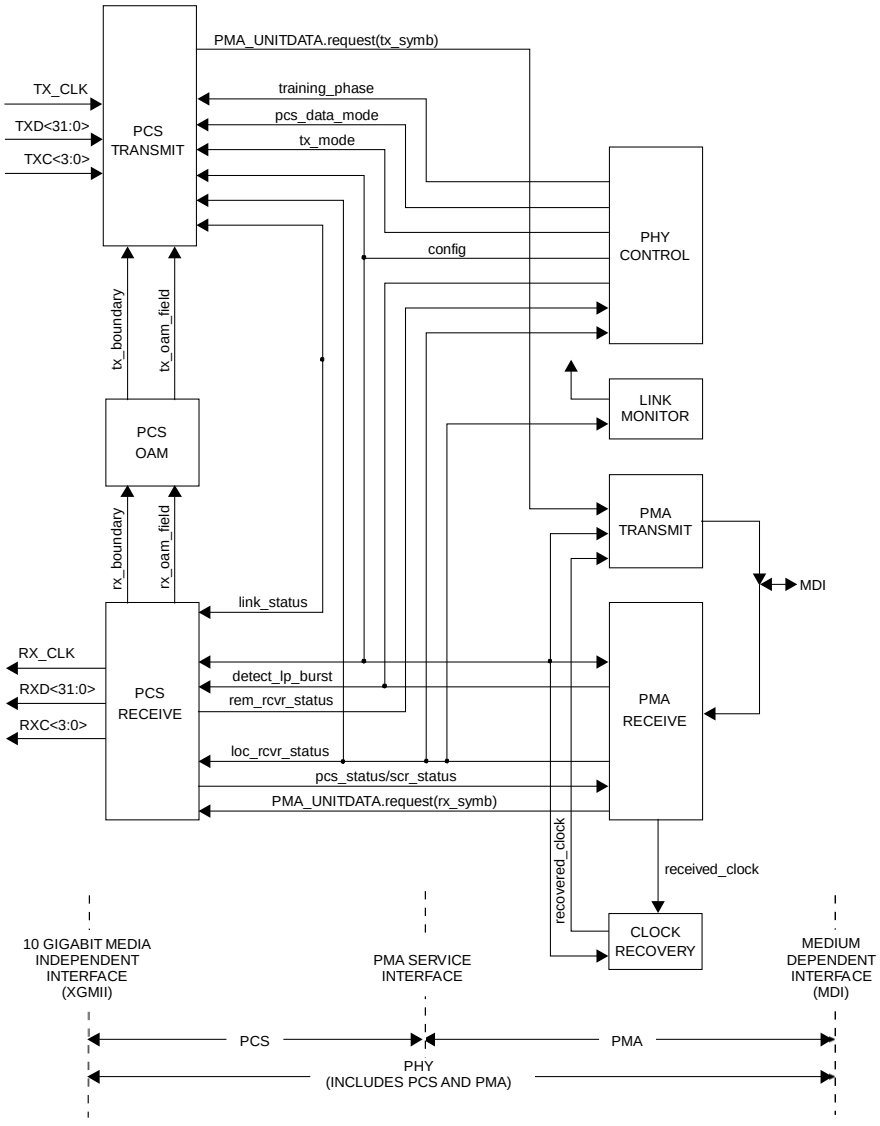
Transmit MAC data rate	***S***
100 Mb/s	0.5
2.5 Gb/s	0.5
5 Gb/s	1
10 Gb/s	1

202.1.2 Relationship of MultiGBASE-A to other standards

Editor's Note (to be removed prior to Working Group Ballot):

May be added by Editor based on project details.

202.1.3 Operation of MultiGBASE-A



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

Figure 202–1—Functional block diagram

202.1.3.1 Physical Coding Sublayer (PCS) in PHY_S mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 1-bit OAM field is appended to form a 976-bit block. A number, L (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 4 for 10 Gb/s), of these 976-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC(128,122,8) and the round-robin interleaving as described in 202.3.2.2.15. The RS-FEC output superframe consists of L × 1040 bits. The duration of the superframe is 1024 / 3 ns.

NOTE—Duration = L × 1024 bits / bits per symbol / baud rate. For 10 Gb/s, Duration = 4 × 1024 / 2 / 6 GBd; for 5 Gb/s, Duration = 2 × 1024 / 1 / 6 GBd; for 2.5 Gb/s, Duration= 1 × 1024 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the HS_TX payload. The PCS Transmit functions are described in 202.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where i = 0 to 14, j = 0 to 64, and $\text{tx\_coded}_i\langle 64:0 \rangle$ is the i^{th} 64B/65B block where $\text{tx\_coded}_0\langle 64:0 \rangle$ is the first block transmitted.

In the training mode (see 202.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 202.3. The interface to the PMA is an abstract message-passing interface specified in 202.4.

202.1.3.2 Physical Coding Sublayer (PCS) in PHY_D mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 17-bit OAM field is appended to form a 992-bit block. Each of these 992-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(130,124,8). The RS-FEC output frame consists of 1040 bits. The duration of the frame is 1040 / 3 ns.

NOTE—Duration = 1040 bits / bits per symbol / baud rate = 1040 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the LS_TX payload. The PCS Transmit functions are described in 202.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where i = 0 to 14, j = 0 to 64, and $\text{tx\_coded}_i\langle 64:0 \rangle$ is the i^{th} 64B/65B block where tx_coded0<64:0> is the first block transmitted.

In the training mode (see 202.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 202.3. The interface to the PMA is an abstract message-passing interface specified in 202.4.

202.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto a single balanced pair of conductors (-T1) or a single coaxial cable (-V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides communications at $6 \times S$ GBd. See Table 202–2 for the definition of *S*.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled and provides the startup functions required for successful operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link and communicates this status to other functional blocks. A failure of the receive link causes the data mode operation to stop and startup functions to restart.

PMA functions and state diagrams are specified in 202.4 and 202.5. The electrical parameters of the PMA (i.e., test modes and electrical specifications for the transmitter and receiver) are specified in 202.5.

202.1.4 LS_PATH signaling

LS_PATH signaling is performed by the LS_TX PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The code-group sequences consist of PAM2 symbols within a burst and Z symbols between bursts. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.

b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the transmit path.

c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.

d) Uncorrelated symbols in the transmitted symbol stream.

e) No correlation between symbol streams traveling in opposite directions.

f) Block framing and other control signals.

g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the normal data mode or the training mode.

In both normal mode and training mode, the LS_TX PCS generates a continuous stream of PAM2 symbols during the payload that are transmitted via the PMA at one of two voltage levels (see Figure 202–26). The Z symbols are transmitted at the same payload rate.

202.1.5 HS_PATH signaling

HS_PATH signaling is performed by the HS_TX PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The code-group sequences consist of PAM2 or PAM4 symbols within a burst and Z symbols between bursts. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.

b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.

c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.

d) Uncorrelated symbols in the transmitted symbol stream.

e) No correlation between symbol streams traveling in opposite directions.

f) Block framing and other control signals.

g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the normal data mode or the training mode.

In normal mode, during the payload the HS_TX PCS generates a continuous stream of either PAM4 symbols that are transmitted via the PMA at one of four voltage levels for 10 Gb/s or PAM2 symbols that are transmitted via the PMA at one of two voltage levels for 2.5 Gb/s and 5 Gb/s. In training mode, the HS_TX PCS is directed to generate only PAM2 symbols for transmission by the PMA (see Figure 202–26). The refresh headers use PAM2 regardless of the MAC data rate. The Z symbols are transmitted at the same payload rate.

202.1.6 Interfaces

All MultiGBASE-A PHY implementations are compatible at the XGMII, if implemented. Implementation of the XGMII is optional. All MultiGBASE-AT1 PHY implementations are compatible at the -T1 MDI. All MultiGBASE-AV1 PHY implementations are compatible at the -V1 MDI. The MDI for a single balanced pair of conductors (-T1) and a single coaxial cable (-V1) are different. Designers are free to implement

circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

202.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

202.2 Service primitives and interfaces

MultiGBASE-A transfers data and control information across the following three service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) PMA service interface
c) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46. The PMA service interface is defined in 202.2.1. The -T1 MDI is defined in 202.9. The -V1 MDI is defined in 202.10.

202.2.1 PMA service interface

MultiGBASE-A uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication(pcs_data_mode)
PMA_DET_LP_BURST.indication(detect_lp_burst)

The use of these primitives is illustrated in Figure 202–2. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 202–2.

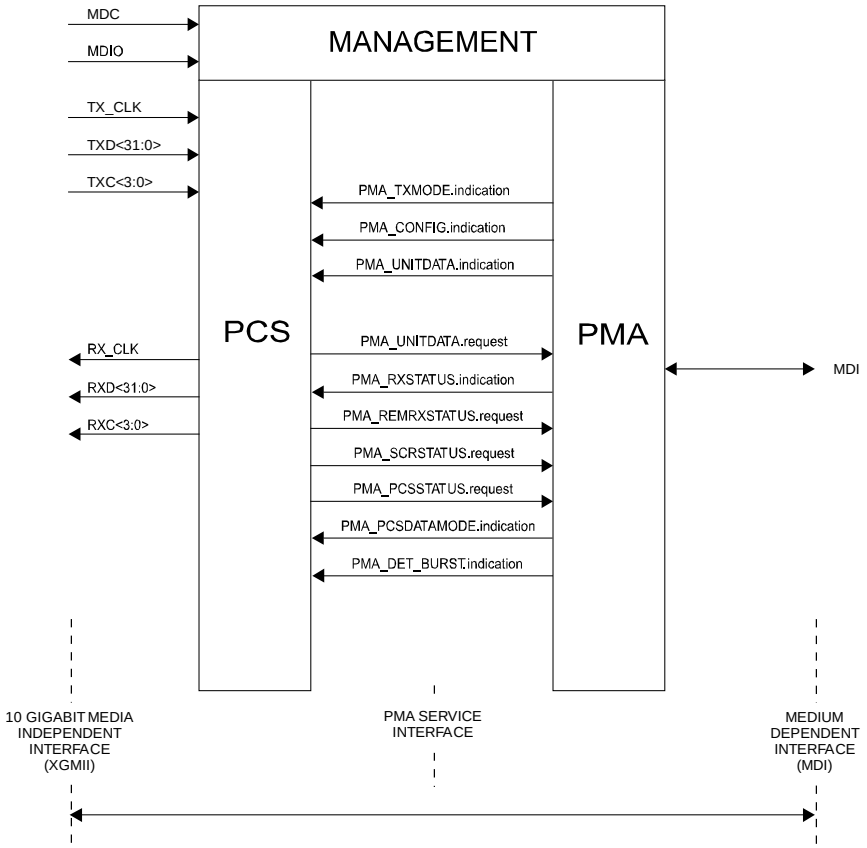


Figure 202–2—MultiGBASE-A service interface

202.2.1.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE-A link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

202.2.1.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.

SEND_TS This value is continuously asserted in case transmission of sequences of symbols representing the TDD symmetric training mode is to take place. LS_TX and HS_TX send at 3 GBd with PAM2 TDD training frames.

SEND_TA This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. LS_TX sends at 3 GBd with PAM2 TDD training frames. HS_TX sends at 3 GBd or 6 GBd with PAM2 TDD training frames.

SEND_Z This value is continuously asserted in case transmission of ~~zero~~ Z symbols is required (e.g., during the TDD QUIET period) for either data or training modes.

202.2.1.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

202.2.1.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 202.3.2.2.

202.2.1.2 PMA_CONFIG.indication

PMA_CONFIG FOLLOWER-LEADER configuration is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

202.2.1.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PHY functions via the parameter config whether the PHY operates as the LEADER or FOLLOWER. The parameter config can take on one of the following two values of the form:

LEADER This value is continuously asserted when the PHY operates as the LEADER.

FOLLOWER This value is continuously asserted when the PHY operates as the FOLLOWER.

202.2.1.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

202.2.1.2.3 Effect of receipt

PCS and PMA perform their functions in the LEADER or FOLLOWER configuration according to the value of the parameter config.

202.2.1.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 202.3.2.2 to represent XGMII data and control streams or other sequences.

202.2.1.3.1 Semantics of the primitive

Editor's Note (to be removed prior to Working Group Ballot):

Need to confirm if tx_symb is really sending "0" or if there is another definition intended similar to Tx disable.

PMA_UNITDATA.request(tx_symb)

The PMA_UNITDATA.request primitive conveys the value of the symbol to be transmitted over the MDI via the tx_symb parameter. The tx_symb may take on one of the following values:

{–1, –1/3, +1/3, +1} in normal operation for 10 Gb/s mode's data payload.

{-1, +1} in training mode and in normal operation for all refresh header, 2.5 Gb/s mode, and 5 Gb/s mode data payloads.

0 when zeros are to be transmitted in the following two cases:

1) when PMA_TXMODE.indication is SEND_Z during PMA training, and

2) after data mode is reached, the transmit function is in the QUIET period.

202.2.1.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

202.2.1.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 202.5.2.

202.2.1.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

202.2.1.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception, the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

202.2.1.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive, as governed by the recovered clock, is 3 GHz for 100 Mb/s and 2.5 Gb/s receive modes and 6 GHz for 5 Gb/s and 10 Gb/s receive modes.

202.2.1.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

202.2.1.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the PCS descrambler has achieved synchronization.

202.2.1.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The PCS descrambler has achieved synchronization.
NOT_OK	The PCS descrambler is not synchronized.

202.2.1.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

202.2.1.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 202.4.2.3 and 202.4.2.4.

202.2.1.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

202.2.1.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in the data mode.
NOT_OK	The PCS is not operating reliably in the data mode.

202.2.1.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

202.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 202.4.2.3 and 202.4.4.1.

202.2.1.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criteria for setting the parameter loc_rcvr_status is left to the implementer. For example, it can be based on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

202.2.1.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK This value is asserted and remains true during reliable operation of the receive link for the local PHY.

NOT_OK This value is asserted whenever operation of the link for the local PHY is unreliable.

202.2.1.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

202.2.1.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 202–2, 202.3.2.3, 202.4.2.4, and 202.5.

202.2.1.8 PMA_REMRXSTATUS.request

Editor's Note (to be removed prior to Working Group Ballot):

Needs review.

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

202.2.1.8.1 Semantics of the primitive

PMA_REMRXSTATUS.requent(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK	The receive link for the remote PHY is operating reliably.
NOT_OK	Reliable operation of the receive link for the remote PHY is not detected.

202.2.1.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request message to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infofield messages received from the remote PHY during training.

202.2.1.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 202–26.

202.2.1.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

202.2.1.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

202.2.1.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

202.2.1.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 202.3.2.2.

202.2.1.10 PMA_DET_LP_BURST.indication(detect_lp_burst)

Editor's Note (to be removed prior to Working Group Ballot):

TBD.

This primitive is generated by PMA Receive to indicate it has detected a burst from link partner. The parameter detect_lp_burst conveys to the PCS Receive function and PHY Control.

202.2.1.10.1 Semantics of the primitive

Editor's Note (to be removed prior to Working Group Ballot):

TBD.

PMA_DET_LP_BURST.indication(detect_lp_burst)

PMA_DET_LP_BURST.indication specifies to PCS Receive and PHY Control via the parameter detect_lp_burst that the TDD burst has been detected. Set to FALSE when the PMA detected the burst has ended (PMA could use timer timeout to terminate this detection signal).

202.2.1.10.2 When generated

PMA Receive generates PMA_DET_LP_BURST.indication messages to indicate a change in detect_lp_burst.

202.2.1.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 202–26.

202.3 Physical Coding Sublayer (PCS) functions

202.3.1 PCS service interface (XGMII)

The PCS service interface allows the PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

202.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

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The PCS reference diagram (see Figure 202–3) shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 202–3.

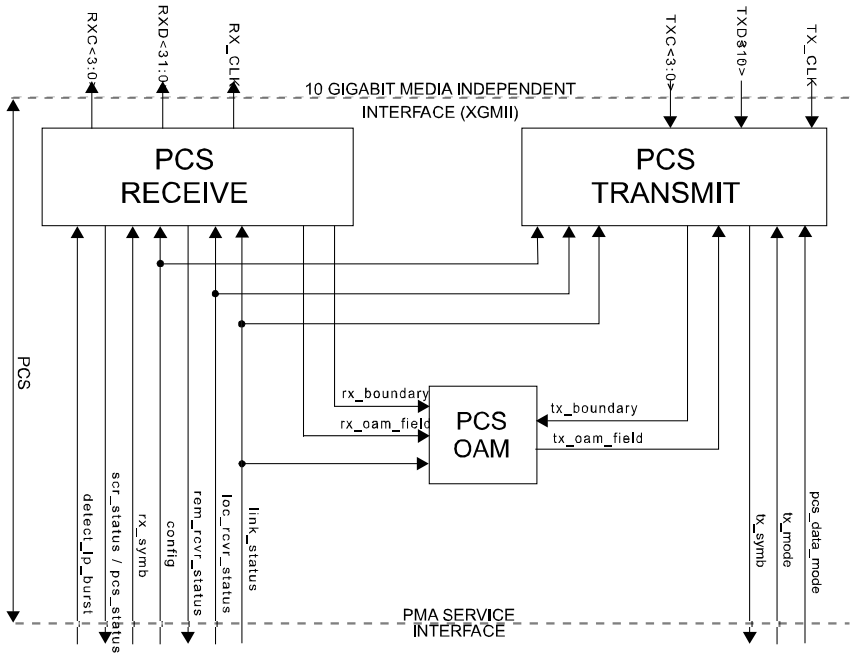


Figure 202–3—PCS reference diagram

202.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of following conditions occur:

a) Power on (see 202.3.7.2.2)
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15 (TBD).

202.3.2.2 PCS Transmit function

PCS Transmit function block diagram is shown in Figure 202–4. The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 202–20 and to the PCS Transmit bit ordering in Figure 202–5 for the LS_TX or Figure 202–6 for the HS_TX.

Dashed rectangles in Figure 202–6 indicate the data path of PAM2 or PAM4 signals. Only one of them shall be chosen for a particular operational speed mode.

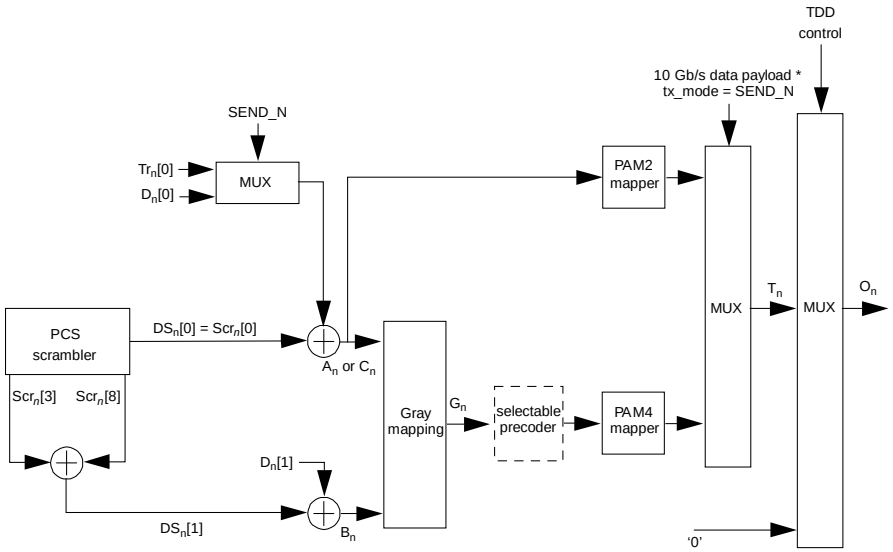


Figure 202–4—PCS Transmit function block diagram

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals.

Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

For LS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the LS_TX PCS Transmit process take 1 group of 15 65B blocks and append a 17-bit OAM field to it, shown in Figure 202–5. This forms the input to the RS_FEC(130,124) which adds 48 parity bits. The resulting 1040 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. Transmit data-units are sent to the LS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For HS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the HS_TX PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC(128,122) superframe which adds L × 64 parity bits, shown in Figure 202–6. 25 such superframes are formed for one data payload. L = 1 for 2.5 Gb/s and L = 2 for 5 Gb/s. For 2.5 Gb/s and 5 Gb/s PAM2 transmission, the resulting L × 1024 × 25 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. L = 4 for 10 Gb/s PAM4 transmission. The resulting L × 1024 × 25 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol. Transmit data-units are sent to the HS_TX PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM2 or PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, *T*, is 1000 / (6 × *S*) ps. See Table 202–2 for the definition of *S*.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_TS or SEND_TA, PCS Transmit shall generate a sequence (O_n) defined in 202.3.5 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {-1, +1}.

During training mode, an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes request for remote transmitter settings (see 202.4.2.4).

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. For LS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 17-bit OAM field to form the RS-FEC input frame. During data encoding, LS_TX PCS Transmit utilizes Reed-Solomon encoders to generate and append 48 parity check bits to form 1040-bit (130,124) RS-FEC frames. For HS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 1-bit OAM field to form the RS-FEC input frame. During data encoding, HS_TX PCS Transmit utilizes L-interleaved (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, or L = 4 for 10 Gb/s) Reed-Solomon encoders to generate and append 48 parity check bits to form 1024-bit (128,122) RS-FEC frames that are interleaved into an L-interleaved RS-FEC superframe.

Editor's Note (to be removed prior to Working Group Ballot):

L interleaving and Superframe structure - TBD (similar to 802.3ch format).

202.3.2.2.1 Use of blocks

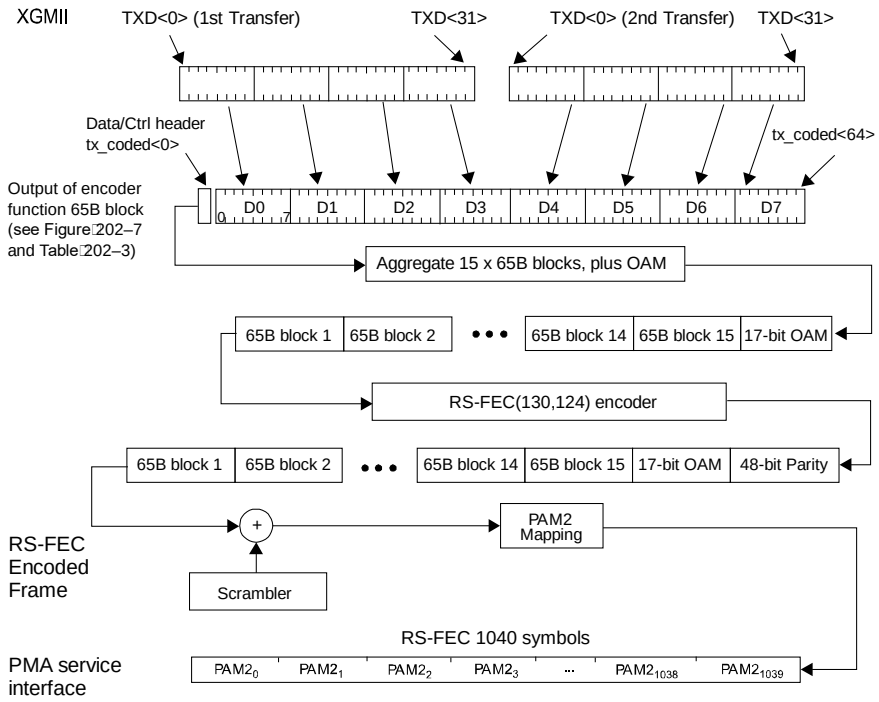
The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2/PAM4 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 202.3.2.2.2.

202.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

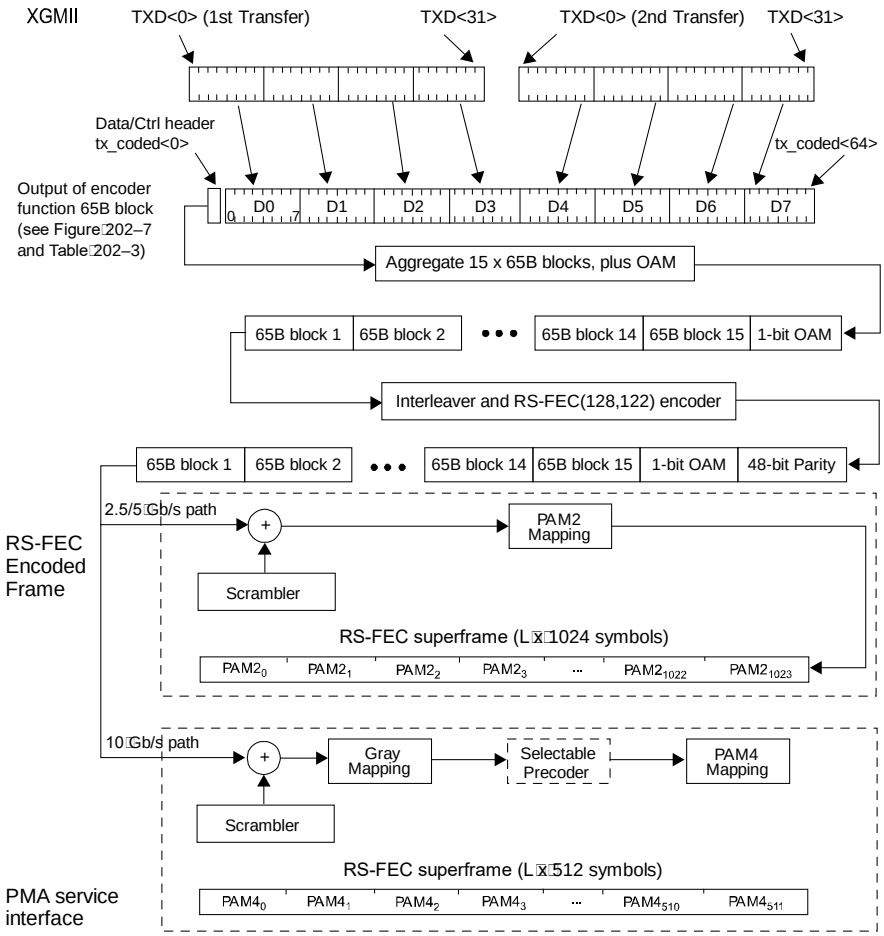
The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 202–5 for LS_TX, Figure 202–6 for HS_TX, Figure 202–10 for LS_RX, and Figure 202–11 for HS_RX. These

figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 202.3.2.2.4 for information on how blocks containing control characters are mapped.



NOTE—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

Figure 202–5—IS_TX RCS Transmit bit ordering



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

NOTE 3—Either the PAM2 or PAM4 path is chosen.

Figure 202–6—MB_TX PCS Transmit bit ordering

202.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D0 to D7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O0 or O4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S0 or S4 for the same reason. The control character for terminate is labeled as T0 to T7.

The two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

202.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks is shown in Figure 202–7. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the

figure) are sent as zero and ignored upon receipt.

Input data	data ctrl header	**Block payload**							
Bit position: / **Data block format:**	0	1							64
D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
C_0 C_1 C_2 C_3/O_4 D_5 D_6 D_7	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
C_0 C_1 C_2 C_3/S_4 D_5 D_6 D_7	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
O_0 D_1 D_2 D_3/S_4 D_5 D_6 D_7	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
O_0 D_1 D_2 D_3/O_4 D_5 D_6 D_7	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
O_0 D_1 D_2 D_3/C_4 C_5 C_6 C_7	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 202–7—64B/65B block formats for MultiGBASE-A

202.3.2.2.5 Control codes

All control characters are supported by both the XGMII and the PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The PCS encodes the start and terminate control characters implicitly by the block type field. The PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to MultiGBASE-A control codes and XGMII control codes are specified in Table 202–3.

Table 202–3—MultiGBASE-A control codes

Control character	Notation	XGMII control code	Control code	O code
idle	/I/	0x07	0x00	—
start	/S/	0xFB	Encoded by block type field	—
terminate	/T/	0xFD	Encoded by block type field	—
error	/E/	0xFE	0x1E	—
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5

Signal ordered set[1]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

202.3.2.2.6 Ordered sets

Editor's Note (to be removed prior to Working Group Ballot):

"remote fault" is not used in the document. Suggest to delete?

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and Local Fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 202–3 for the mappings

202.3.2.2.7 Idle (*/I/*)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

202.3.2.2.8 Start (*/S/*)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

202.3.2.2.9 Terminate (*/T/*)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

[1]Reserved for INCITS T11 Fibre Channel use.

202.3.2.2.10 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

202.3.2.2.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 202.3.7.2.4 for further information.

202.3.2.2.12 Transmit process

The LS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. It takes 1040 PMA_UNITDATA transfers to send an RS-FEC frame of data.

The HS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. L × 30 XGMII data transfers are encoded into an RS-FEC superframe. For 2.5 Gb/s and 5 Gb/s mode, it takes L × 1024 PMA_UNITDATA PAM2 transfers to send an RS-FEC superframe of data. For 10 Gb/s mode, it takes L × 512 PMA_UNITDATA PAM4 transfers to send an RS-FEC superframe of data. Where the XGMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 202–20). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. Tx_coded<0> contains the data/ctrl header and the remainder of bits contain the block payload.

202.3.2.2.13 RS-FEC framing and RS-FEC encoder

For LS_TX transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 17-bit OAM/Reserved field and 48 parity bits is 1040 bits. See Figure 202–5 and 202.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

For HS_TX transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 1-bit OAM/Reserved field and 48 parity bits is 1024 bits. See Figure 202–6 and 202.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

202.3.2.2.14 RS-FEC superframe and round-robin interleaving

The interleaver depth L of the transmitter shall be predefined for each speed. When the defined interleaving depth L = 1, there is no interleaving, and the RS-FEC superframe is the same as the RS-FEC frame.

When the defined interleaving depth L > 1, the round-robin interleaving scheme shown in Figure 202–8 shall be applied.

100 Mb/s mode supports L = 1.

2.5 Gb/s mode supports L = 1.

5 Gb/s mode supports L = 2.

10 Gb/s mode supports L = 4.

The HS_TX PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 976 × L bits, or 122 × L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are as follows:

$m_{122 \times L-1}, m_{122 \times L-2}, \ldots m_1, m_0$

These message symbols are distributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message symbols from the superframe. Otherwise, the RS-FEC encoder operates exactly the same as specified in 202.3.2.2.16.

202.3.2.2.15 RS-FEC recombine

The L encoded RS-FEC frames are combined into an interleaved RS-FEC superframe when the PCS operates as a HS_RX. The output symbols are as follows:

$m_{122 \times L-1}, m_{122 \times L-2}, \ldots, m_1, m_0, p_{1,5}, \ldots, p_{L,5}, \ldots, p_{1,0}, \ldots, p_{L,0}$

where $p_{i,r}$ is the r^{th} parity symbol of the i^{th} encoder.

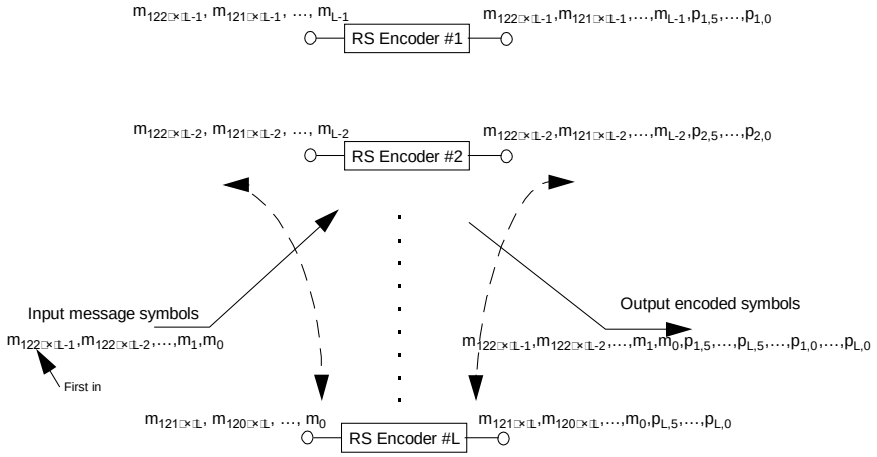


Figure 202–8—Interleaving block diagram with interleaving depth *L*

202.3.2.2.16 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field GF(2^8) where the symbol size is 8 bits. For the LS_PATH, the encoder processes *k* 8-bit RS FEC message symbols to generate (130-*k*) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. For the HS_PATH, the encoder processes *k* 8-bit RS FEC message symbols to generate (128-*k*) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 128 8-bit RS-FEC symbols. *k* = 124 is adopted for the LS_PATH and *k* = 122 is adopted for the HS_PATH. For the purposes of this clause, the respective particular Reed-Solomon code is denoted as RS-FEC(*n*,*k*), where *n* designates the FEC code block with *n* = 130 for the LS_PATH and *n* = 128 for the HS_PATH.

The code is based on the generating polynomial shown in Equation (202–1).

(202–1)

$$g(x) = \prod_{j=0}^{n-k-1} (x - \alpha^j) = g_{n-k}x^{n-k} + g_{129-k}x^{129-k} + \ldots + g_3x^3 + g_2x^2 + g_1x + g_0$$

In Equation (202–1), α is a primitive element of the finite field defined by the primitive polynomial $0x11D = x^8 + x^4 + x^3 + x^2 + 1$.

Equation (202–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0.

(202–2)

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1x^{n-k+1} + m_0x^{n-k}$$

Each message symbol m_i is the bit vector ($m_{i,7}$, $m_{i,6}$, …, $m_{i,1}$, $m_{i,0}$), which is identified with the element of the finite field $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<(8 × *k* - 1):0>.

For LS_TX, $m_{i,j}$ = tx_RSmessage<(123 - *i*) × 8 + *j*>, for *i* = 0 to 123, and *i* = 0 to 7.

tx_RSmessage<991:0> prior to RS-FEC(130,124) encoder is formed as follows:

tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<991:975> = OAM_field<16:0>.

For HS_TX, $m_{i,j}$ = tx_RSmessage<(121 - *i*) × 8 + *i*>, for *i* = 0 to 121, and *i* = 0 to 7.

tx_RSmessage<975:0> prior to RS-FEC(128,122) encoder is formed as follows for L = 1 (see 202.3.2.2.14):

tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<975> = OAM_field<0>.

For L = 2 and L = 4, see both 202.3.2.2.14 and 202.3.2.2.15.

The first symbol input to the encoder is m_{k-1}.

Equation (202–3) defines the parity polynomial $p(x)$ whose coefficients are the message symbols p_{n-k-1} to p_0.

(202–3)

$p(x) = p_{n-k-1}x^{n-k-1} + p_{130-k-2}x^{n-k-2} + \ldots + p_2x^2 + p_1x + p_0$ Each parity symbol p_i is the bit vector ($p_{i,7}$, $p_{i,6}$, …, $p_{i,1}$, $p_{i,0}$), which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 202–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x (e.g., $c_{129} = m_{k-1}$) is transmitted first and the coefficient of the lowest power of x (e.g., $c_0 = p_0$) is transmitted last. The first bit transmitted from each symbol is bit 0.

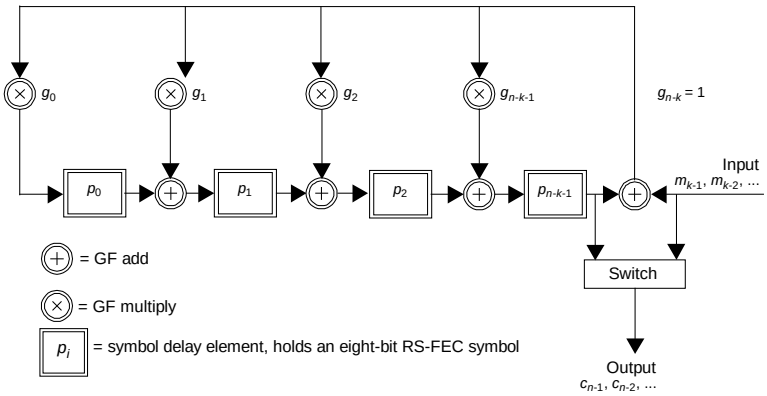


Figure 202–9—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 202–4

Table 202–4—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(130,124)	RS-FEC(128,122)
0	38	38
1	227	227
2	32	32
3	218	218
4	1	1
5	63	63
6	1	1

.

202.3.2.2.17 PCS scrambler

As explained in 202.3.4, a different PCS scramblers are used for the burst refresh header and payload.

PAM2 encoding is used for the refresh header (see 202.3.5) at all symbol rates. Consequently, the scrambled header data stream, C_n, is shown in Equation (202–4).

(202–4)

$$C_n = \begin{cases} DS_n[0] \oplus Tr_n[0] & \text{tx\_mode ! = SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad 0 \le n \le N\_r - 1$$

where

$DS_n[0]$ is produced using the scrambler defined in 202.3.4.1

PAM2 symbols are used for rates less than 10 Gb/s. The scrambled data stream, A_n, for PAM2 is shown in Equation (202–5). Bit $DS_n[0]$ is produced using the scrambler defined in 202.3.4.2. It is applied as an additive scrambler sequence to incoming data bit Dn[0] (LSB) to generate the scrambled data bit, A_n.

(202–5)

$$A_n = \begin{cases} DS_n[0] \oplus Tr_n[0] & \text{tx\_mode ! = SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1$$

For 10 Gb/s interfaces using PAM4 coding, the burst data bits of the interleaved RS-FEC superframe are grouped into pairs. Each pair of bits, $D_n[0]$ and $D_n[1]$, where n is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the PCS scrambler. The first least significant bit (LSB) bit is $DS_n[0]$ equal to $Scr_n[0]$ defined in 202.3.4. The second most significant (MSB) bit is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$.

Bits $DS_n[0]$ and $DS_n[1]$ in Equation (202–6) and Equation (202–7) are produced using the scrambler defined in 202.3.4.2. They are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$.

(202–6)

$$A_n = \begin{cases} DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1$$

(202–7)

$$B_n = \begin{cases} DS_n[1] \oplus D_n[1] & N\_r \le n \le N\_r + N\_p - 1 \end{cases}$$

202.3.2.2.18 Gray mapping for PAM4 encoding

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where A_n is the bit arriving first, and n is an index indicating the symbol number, to Gray-coded symbols $G(n)$ with one of four levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

When receiving at 10 Gb/s in the PAM4 transmission period, the PCS Receive process shall map Gray-coded PAM4 symbols $G(n)$, with one of four levels, to pairs of bits, $\{A_n, B_n\}$, where A_n is considered to be the first bit as follows:

0 maps to {0, 0},
1 maps to {0, 1},
2 maps to {1, 1}, and
3 maps to {1, 0}.

202.3.2.2.19 PAM4 encoding

Editor's Note (to be removed prior to Working Group Ballot):

Deleting clause "202.3.2.2.19 Selectable precoder" during d0pb means that text referencing a precoder and other text needs to be adjusted (e.g., replace "precoder output symbol" with "Gray-coded" symbol. Diagrams should be checked, too.

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this clause.

The PAM4 encoded symbols are denoted $M(n)$, where n is an index indicating the symbol number.

Each consecutive precoder output symbol, $P(n)$, is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output $M(n)$.

Mapping from the precoder output symbol $P(n)$ to a PAM4 encoded symbol $M(n)$ is as follows:

0 maps to -1,
1 maps to -1/3,
2 maps to +1/3, and
3 maps to +1.

202.3.2.2.20 PAM2 mapping

During the PAM2 transmission period, the PCS Transmit process sends out PAM2 symbols according to following mapping:

Input bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$, then $T_n = +1$, if $S_n = 1$, then $T_n = -1$.

202.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 202–21 and the PCS Receive bit ordering in Figure 202–10 for the LS_RX and Figure 202–11 for the HS_RX, including compliance with the associated state variable as specified in 202.3.7.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM2 or PAM4 symbols are demapped and descrambling is performed according to rules.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For LS_RX, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks. For HS_RX, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each ~~burst~~data payload, the 25 superframes can form a 25-bit OAM field for 2.5 Gb/s mode, a 50-bit OAM field for 5 Gb/s mode, and a 100-bit OAM field for 10 Gb/s mode.

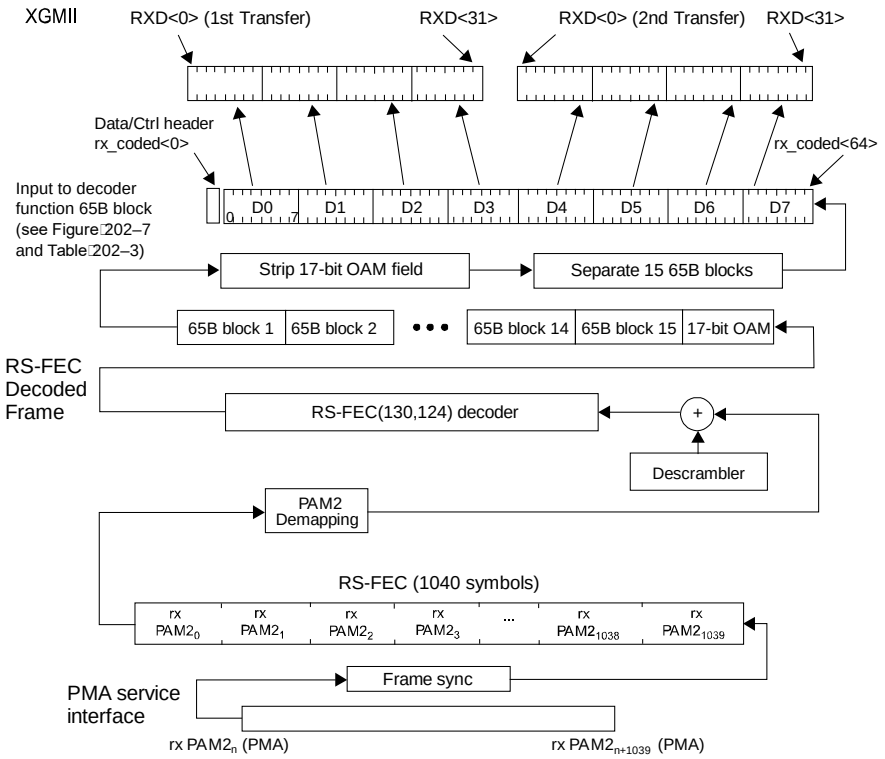
This process generates the 64B/65B block vector rx_coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 202–21). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 (TBD) consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi _rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

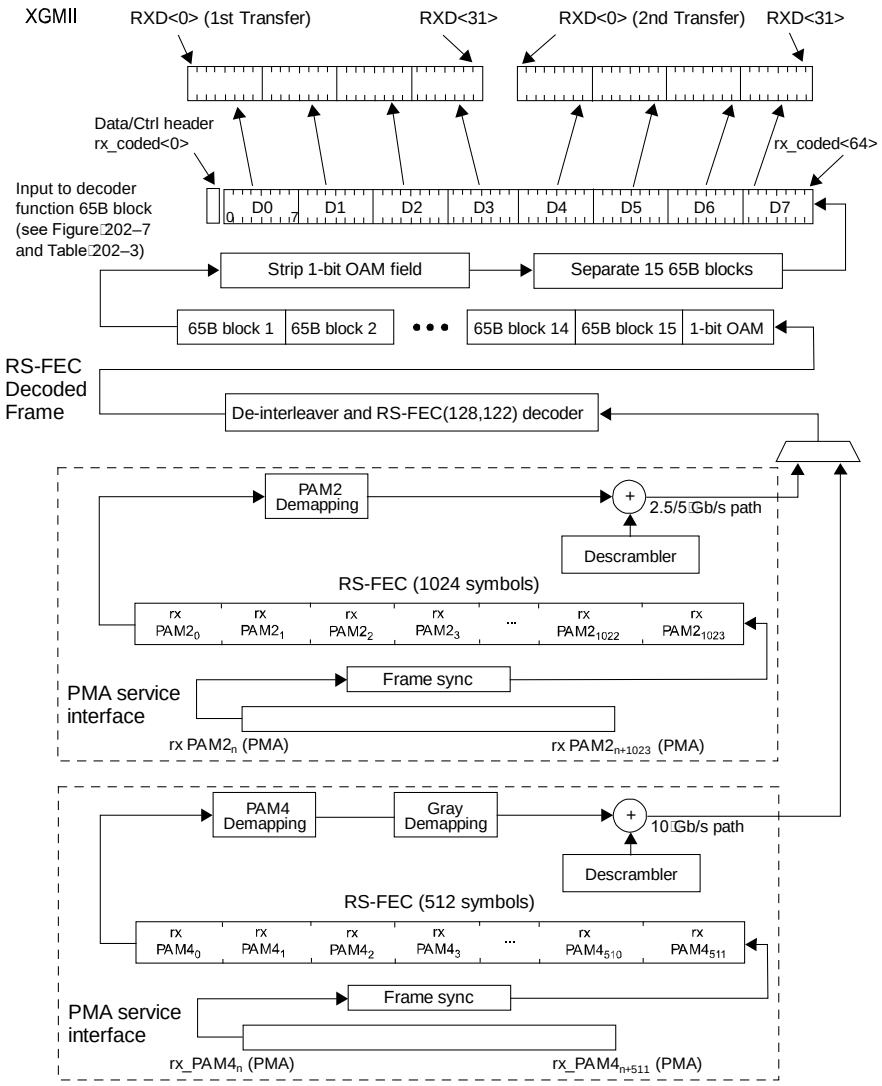
When the receiver is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status).

When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process when PHY Control is in PCS_TEST or PCS_DATA state. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header (see 202.3.5). It also includes training payload which has an Infofield, inserted in the N_inf^{th} bit of the training payload (see 202.3.5.3). When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.



NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

Figure 202–10—IS_RX PCS Receive bit ordering



NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

NOTE 3—Either the PAM2 or PAM4 path is chosen.

Figure 202–11—BS_RX PCS Receive bit ordering

202.3.2.3.1 Frame and block synchronization

When operating in 100 Mb/s, 2.5 Gb/s, or 5 Gb/s data mode, the receiving PCS shall form a PAM2 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM2_0 to rx_PAM2_1023 (see Figure 202–10 for LS_RX or Figure 202–11 for HS_RX). When operating in 10 Gb/s data mode, the receiving PCS shall form a PAM4 stream from PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM4_0 to rx_PAM4_511 (see Figure 202–10).

The receiving PCS obtains block_lock to the PHY frames during training using synchronization sequence and Infofield provided in the training frames.

202.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For descrambling, the LEADER PHY shall employ the receiver descrambler generator polynomial per Equation (202-6) and the FOLLOWER PHY shall employ the receiver descrambler generator polynomial per Equation (202-5).

202.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.

b) Any control character contains a value not in Table 202–3.

c) Any O code contains a value not in Table 202–3.

d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 202.3.2.2.13. If the check fails, the RS-FEC frame is invalid. The R_BLOCK_ TYPE of an invalid block is set to E.

202.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, channel, and remote receiver.

When the transmit PCS is operating in test-pattern mode, ~~it shall transmit TDD bursts as illustrated in Figure 202–5 or Figure 202–6, with~~ the input to the RS-FEC encoder (see Figure 202–5 or Figure 202–6) is set to zero and the initial condition of the PCS scrambler set to any non-zero value. This has the same effect as setting the input to the PCS scrambler to zero.

When the receiver PCS is operating in test-pattern mode, ~~it shall receive TDD bursts~~the received information is processed as illustrated in Figure 202–10 or Figure 202–11. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero. However, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 (TBD) in 202.5.1.

202.3.4 PCS scrambler polynomials

The TDD bursts use different scrambler polynomials for the refresh_hdr and the burst payload. The scrambler used for the refresh_hdr, as well as some test modes, is defined in 202.3.4.1 The payload scrambler used for burst payloads is defined in 202.3.4.2.

202.3.4.1 PRBS11 scrambler polynomial

The refresh header specified in 202.3.5 shall be scrambled from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 202–12. This implements the generator polynomial shown in Equation (202–8), which is the same as Equation (72–1).

(202–8)

$$G(x) = 1 + x^{9} + x^{11}$$

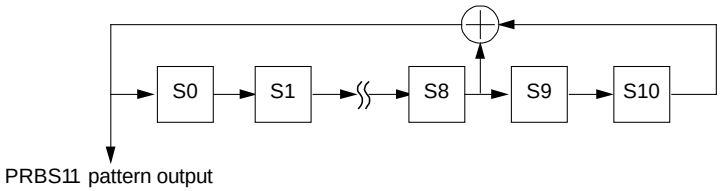


Figure 202–12—PRBS11 pattern generator

202.3.4.2 PRBS33 scrambler polynomials

The PCS Transmit function employs additive scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value LEADER, PCS Transmit shall employ Equation (202–9) as the transmitter scrambler generator polynomial.

(202–9)

$$g_M(x) = 1 + x^{13} + x^{33}$$

If the PMA_CONFIG.indication message assumes the value FOLLOWER, PCS Transmit shall employ Equation (202–10) as the transmitter scrambler generator polynomial.

(202–10)

$$g_S(x) = 1 + x^{20} + x^{33}$$

An implementation of the LEADER PCS and FOLLOWER PCS transmitter scramblers by linear-feedback shift registers is shown in Figure 202–13. The bits stored in the shift register delay line at time *n* are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the scrambler state

are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case, shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the payload of PMA training frames and data mode frames and shall stop during QUIET and refresh headers.

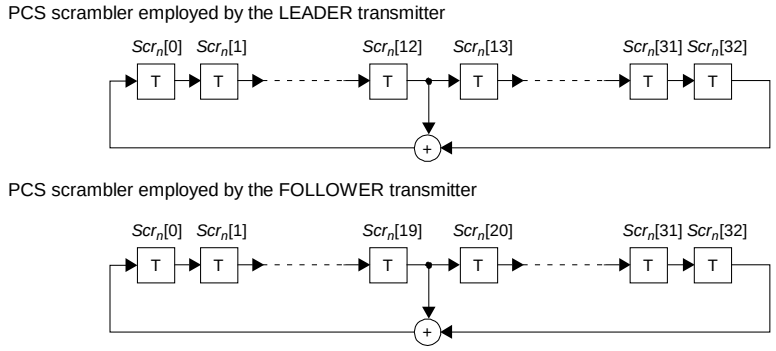


Figure 202–13—Realization of PCS scramblers by linear feedback shift registers

202.3.5 PMA training frame

Each PMA training frame includes a refresh header followed by a training payload.

Refresh header (refresh_hdr) is a sequence of PAM2 symbols with length of N_r symbols. Training payload is a sequence of PAM2 symbols with length of N_p symbols. The refresh header bits are all zeros except for the final 64 bits (see 202.3.5.2.1).

An 11-bit scrambler (see 202.3.5.2.1) is used to scramble the refresh_hdr. This scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

The training payload data sequence bits are all zeros, with the exception that a 96-bit Infofield is started at N_inf^{th} symbol of the training payload. This training data sequence $S\_t_{(n)}$ is defined in Equation (202–13).

The 33-bit scrambler (see 202.3.4) is used to scramble the training payload. Once started at the beginning of the training payload of the first training burst, this scrambler shall continue to run uninterrupted for each symbol during training payloads and shall stop during the QUIET period and refresh headers.

The Infofield is used to exchange messages between link partners during the startup training.

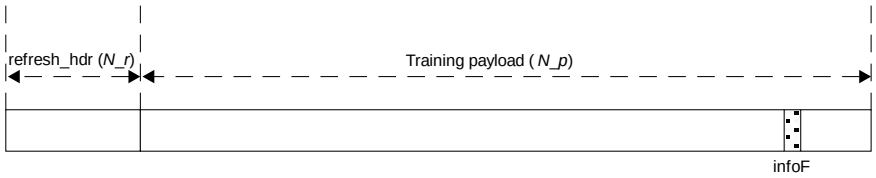


Figure 202–14—PMA Training frame

202.3.5.1 Refresh header and training payload length

The lengths for refresh_hdr and training payload are described in Table 202–5, Table 202–6, and Table 202–7.

Table 202–5—*N_r* and *N_p* value for 100 Mb/s mode transmission

tx_mode	refresh_header *N_r*(symb)	training_payload *N_p*(symb)
SEND_TS	560	12 880
SEND_TA	624	1024
SEND_N	624	1024

Table 202–6—*N_r* and *N_p* value for 2.5 Gb/s mode transmission

tx_mode	refresh_header *N_r*(symb)	training_payload *N_p*(symb)
SEND_TS	560	12 880
SEND_TA	480	26 000
SEND_N	480	26 000

Table 202–7—*N_r* and *N_p* value for 5 Gb/s mode and 10 Gb/s mode transmission

tx_mode	refresh_header *N_r*(symb)	training_payload *N_p*(symb)

SEND_TS	560	12 880
SEND_TA	960	52 000
SEND_N	960	52 000

202.3.5.2 Refresh header and training payload data bits generation

N_b is the number of bits in the training payload. N_inf is the bit position where Infofield starts within the training payload. The first bit of the training frame starts at bit 0, with $0 \le n \le N\_r$ - 1 consisting of the refresh header. Per Equation (202–13), $S\_t_{(n)}$ is all zeros from the end of the refresh header to the beginning of the Infofield, followed by the 96-bit Infofield, then followed by all zeros from the end of the Infofield to the end of the training payload, which is the end of the burst.

$$N\_b = N\_p \quad (202–11)$$

$$N\_inf = N\_b - 256 \quad (202–12)$$

(202–13)

$$S\_t_{(n)} = \begin{cases} refresh\_hdr(n) & 0 \le n \le N\_r - 1 \\ 0 & N\_r \le n \le N\_r + N\_inf - 1 \\ Infofield(n - [N\_r + N\_inf]) & N\_r + N\_inf \le n \le N\_r + N\_inf + 95 \\ 0 & N\_r + N\_inf + 96 \le n \le N\_r + N\_b - 1 \end{cases}$$

(202–14)

$$Tr_n[0] = \begin{cases} S\_t_{(n)} & 0 \le n \le N\_r + N\_b - 1 \end{cases}$$

$Tr_n[0]$ is the same as $S\_t_{(n)}$ and it is scrambled by the PRBS11 scrambler during the refresh header and scrambled by the PRBS33 scrambler during the training payload.

202.3.5.2.1 Refresh header encoding

The refresh_hdr is all zeros until eight bytes before the end of refresh_hdr. The next eight bytes header shall consist of 4 bytes of 0x01, followed by 4 bytes of 0xF0. The refresh_hdr bits are scrambled with the PRBS11 scrambler defined in (see 202.3.4.1). The PRBS11 scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

202.3.5.3 PMA training symbol generation

For training payload, $Tr_n[0]$ shall be scrambled with the $DS_n[0]$ which is equal to $Scr_n[0]$ defined in 202.3.4. The output scrambled bit A_n shall be input to PAM2 mapper. The refresh header is scrambled with the PBRS11 scrambler per 202.3.5.2.1.

Editor's Note (to be removed prior to Working Group Ballot):

Since training is never PAM4, the following can be deleted or moved to a section on the 10G data payload. Perhaps along with Equation (202–15).

The generation of scrambled bits $\{A_n,B_n\}$ can be found at Figure 202–4, with Equation 202.3.2.2.18. The $\{A_n,B_n\}$ shall be input to the Gray mapping for PAM4 encoding specified by 202.3.2.2.18. The output G_n can be input to precoder and then to the PAM4 mapper defined by 202.3.2.2.19.

$$G_n = \text{Gray mapping}(\{A_n, B_n\}) \quad \text{(202–15)}$$

Editor's Note (to be removed prior to Working Group Ballot):

These equations need to be amended and put in the correct section probably next section works. T(n) is not just training symbols, it's the whole burst, so it is PAM2 all the time except when tx_speed = 10G AND tx_mode = SEND_N AND (N_r<=n<=N_p-1).

$$T_{(n)} = \begin{cases} PAM2\_Mapper(A_n) & \sim(\text{tx\_speed} = 10\text{ Gb/s} \times (\text{tx\_mode} = \text{SEND\_N} + \\ & \quad \text{tx\_mode} = \text{SEND\_TA\_EXT})) + (0 \le n \le N\_r - 1) \\ PAM4\_Mapper(G_n) & \text{tx\_speed} = 10\text{ Gb/s} \times (\text{tx\_mode} = \text{SEND\_N} + \\ & \quad \text{tx\_mode} = \text{SEND\_TA\_EXT}) \times (N\_r \le n \le N\_r + N\_p - 1) \end{cases} \quad \text{(202–16)}$$

202.3.5.4 Generation of symbol O_n

Editor's Note (to be removed prior to Working Group Ballot):

From 202.3.2.2, On denotes the training sequence for SEND_TS and SEND_TA. (Note that Tn is used in 802.3ch.). May need linkage to T_n.

The transmit symbol O_n is selected by TDD control logic. For each TDD cycle (specified in 202.3.6), the PCS transmit function ~~transmitter will send out~~ T_n and 0Z symbols, based on symbol time index *n*.

n will be continuous symbol count modulo *N_tdd*. The 33-bit scrambler shall be stopped during refresh headers and QUIET period.

PAM2_Mapper is specified in 202.3.2.2.20.

PAM4_Mapper is specified in 202.3.2.2.19.

Gray mapping is specified in 202.3.2.2.18.

N_tdd is the number of symbols equivalent to a nominal 9.6 µs TDD cycle time.

$$O_n = \begin{cases} T_{(n)} & 0 \le n \le N\_r + N\_p - 1 \\ 0 & N\_r + N\_p \le n \le N\_tdd - 1 \end{cases} \quad \text{(202–17)}$$

202.3.5.5 PMA training mode descrambler polynomials

Editor's Note (to be removed prior to Working Group Ballot):

Needs to be acquired from PAM2, and then just continues on with PAM4.

The PCS shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. The FOLLOWER PCS employs the receiver descrambler generator polynomial per Equation (202–9) and the LEADER PCS employs the receiver descrambler generator polynomial per Equation (202–10).

202.3.6 PCS TDD signaling

The timing diagram in Figure 202–15 shows the TDD cycle signaling and TDD frame structures assuming the LS_TX is configured as the LEADER and the HS_TX is configured as the FOLLOWER. Table 202–8 specifies the LS_TX and HS_TX transmit times in each TDD cycle.

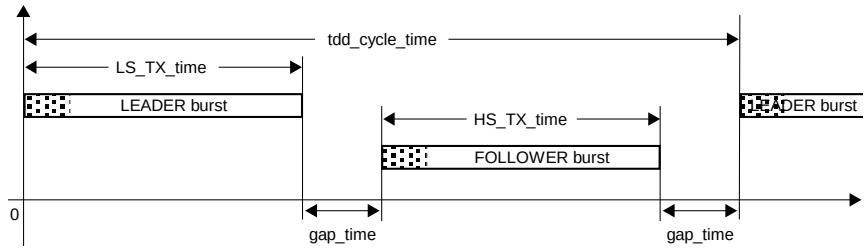


Figure 202–15—FOLLOWER/ LEADER TDD cycle illustration

[Commenter's note: Change "gap time" to "QUIET period" or add that phrase in parentheses below gap time.]

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Table 202–8—LS_TX_time and HS_TX_time

tx_mode	LS_TX_time (ns)	HS_TX_time (ns)
SEND_TS	4480	4480
SEND_TA	560	8826.67
SEND_N		

The symmetric training burst timing and structure are illustrated in Figure 202–16 where TS_ON indicates a symmetric training burst and TS_Quiet indicates the ~~QUIET~~ quiet period between bursts during which Z symbols are transmitted by the PHY.

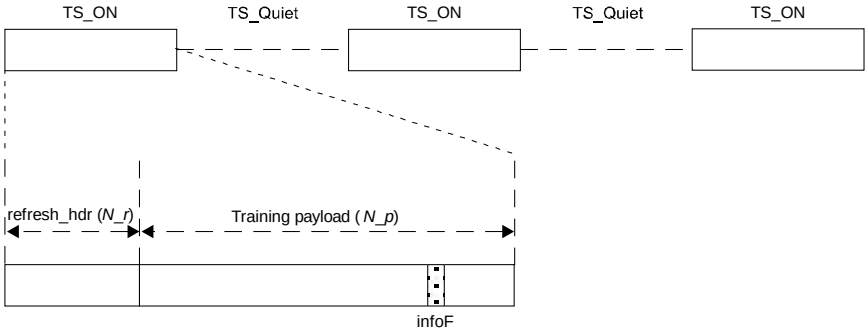

Figure 202–16—Symmetric training timing and frame structure

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Figure 202–17 illustrates the LS_TX timing and frame structure for both the data mode and the asymmetric training modes where TA_ON indicates an asymmetric training burst and TA_Quiet indicates the ~~QUIET~~ quiet period between bursts during which Z symbols are transmitted by the PHYs on both ends of the link. The refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 202.3.5. Note that FEC is not used with the training payload.

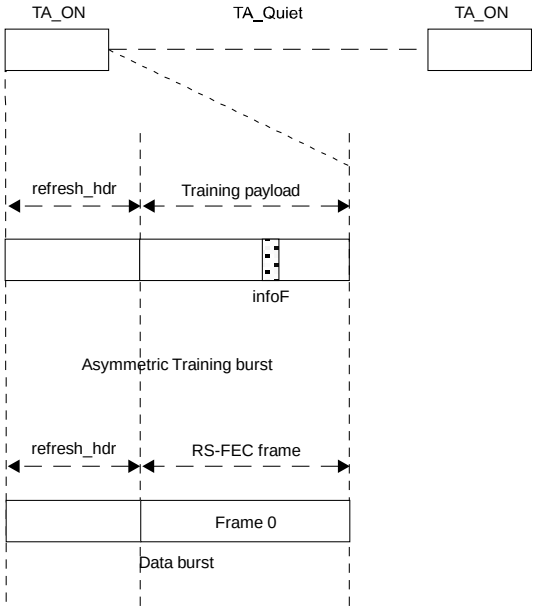


Figure 202–17—Asymmetric training/Data Mode timing and frame structure—LS_TX

Figure 202–17 illustrates the LS_TX timing and frame structure for both the data mode and the asymmetric training modes. The refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 202.3.5. Note that FEC is not used with the training payload.

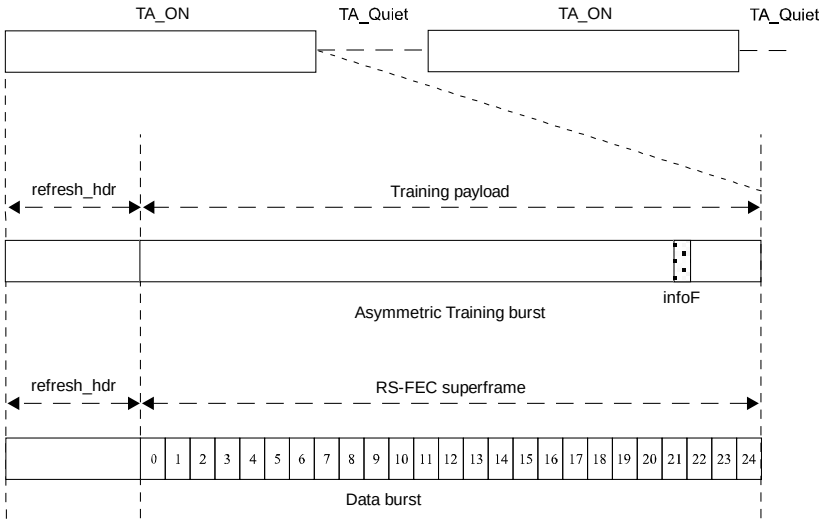


Figure 202–18—Asymmetric training/Data Mode timing and frame structure—HS_TX

202.3.7 PCS Detailed functions and state diagrams

202.3.7.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

202.3.7.2 State diagram parameters

202.3.7.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

IBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.

RFER_CNT_LIMIT
: TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
: TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.
The Link Interruption ordered set is defined in 46.3.4.

202.3.7.2.2 Variables

block_lock
: Boolean variable that is set TRUE when receiver acquires block delineation.

hi_rfer
: Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one rfer_timer interval.

pcs_data_mode
: Variable set by the PMA PHY Control function. See 202.4.4.1.

pcs_reset
: Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rf_valid
: Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

rs_fec_frame_done
: A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. It is set FALSE otherwise.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 202–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_data_active
: A Boolean variable that is set TRUE when the PHY PCS Receive function is operating in the data frame receive mode and set FALSE otherwise. This can be controlled by pre-defined timer after timing and frame synchronization is achieved.

rx_raw<71:0>
: Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

tdd_detect
: Set TRUE when the receiver has reliably detected TDD signaling. It is set FALSE otherwise.

tx_coded<64:0>
: Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 202–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_data_active
: A Boolean variable that is set TRUE during the TDD transmit mode, when PHY PCS is transmitting RS-FEC data frames. It is set FALSE otherwise.

tx_raw<71:0>
: Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

tx_qt_active
: A Boolean variable that is set TRUE during the TDD transmit mode, when the PHY is transmitting quiet signaling. It is set FALSE otherwise.

202.3.7.2.3 Timers

TDD_on_a_timer
: A timer used to control the duration for the Transmission of asymmetric training sequence during TRAINING1 and COUNTDOWN1 state of PHY Control state. A value of 560 ns for the LEADER PHY and a value of 8826.67 ns for the FOLLOWER PHY.

TDD_on_d_timer
: A timer used to control the duration for the Transmission of asymmetric data sequence during PCS_TEST and PCS_DATA state of PHY Control state. A value of 560 ns for the LEADER PHY and a value of 8826.67 ns for the FOLLOWER PHY.

TDD_on_s_timer
: A timer used to control the duration for the Transmission of symmetric PAM2 training sequence during TRAINING0 and COUNTDOWN0 state of PHY Control state. A value of 4480 ns is defined.

TDD_qt_a_timer
: A timer used to control the duration for the QUIET period of asymmetric training during TRAINING1 and COUNTDOWN1 state of PHY Control state. A value of 9040 ns for the LEADER PHY and a value of 773.33 ns for the FOLLOWER PHY.

TDD_qt_d_timer
A timer used to control the duration for the QUIET period during PCS_TEST and PCS_DATA state of PHY Control state. A value of 9040 ns for the LEADER PHY and a value of 773.33 ns for the FOLLOWER PHY.

TDD_qt_s_timer
A timer used to control the duration for the QUIET period of symmetric PAM2 training during TRAINING0 and COUNTDOWN0 state of PHY Control state. A value of 5120 ns is defined.

202.3.7.2.4 Functions

DECODE(rx_coded<64:0>)
In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 202.3.2.2.2

ENCODE(tx_raw<71:0>)
Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 202.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E}
Every case of the vector belongs to only one type.
Values: C; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x1E and seven valid control characters other than /E/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.
S; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.
T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a data/ctrl header of 0.
E; The vector does not meet the criteria for any other value.
A valid control character is one containing a control code specified in Table 202–3. A valid O code is one containing an O code specified in Table 202–3.

R_TYPE(rx_coded<64:0>)
Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT
Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E}
Every case of the vector belongs to only one type.
Values: C; The vector contains one of the following:
a) Eight valid control characters other than /O/, /S/, /T/, /E/;
b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
c) Two valid ordered sets.
S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.
A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 202–3. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 202–3.

T_TYPE(tx_raw<71:0>)
Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

202.3.7.2.5 Counters

rfer_cnt
Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt
Count number Reed-Solomon frames received during current period.

202.3.7.2.6 Messages

RX_FRAME
A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

202.3.7.3 State diagrams

The RFER monitor state diagram shown in Figure 202–19 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 202–20 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

The PCS 64B/65B Receive state diagram shown in Figure 202–21 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams.

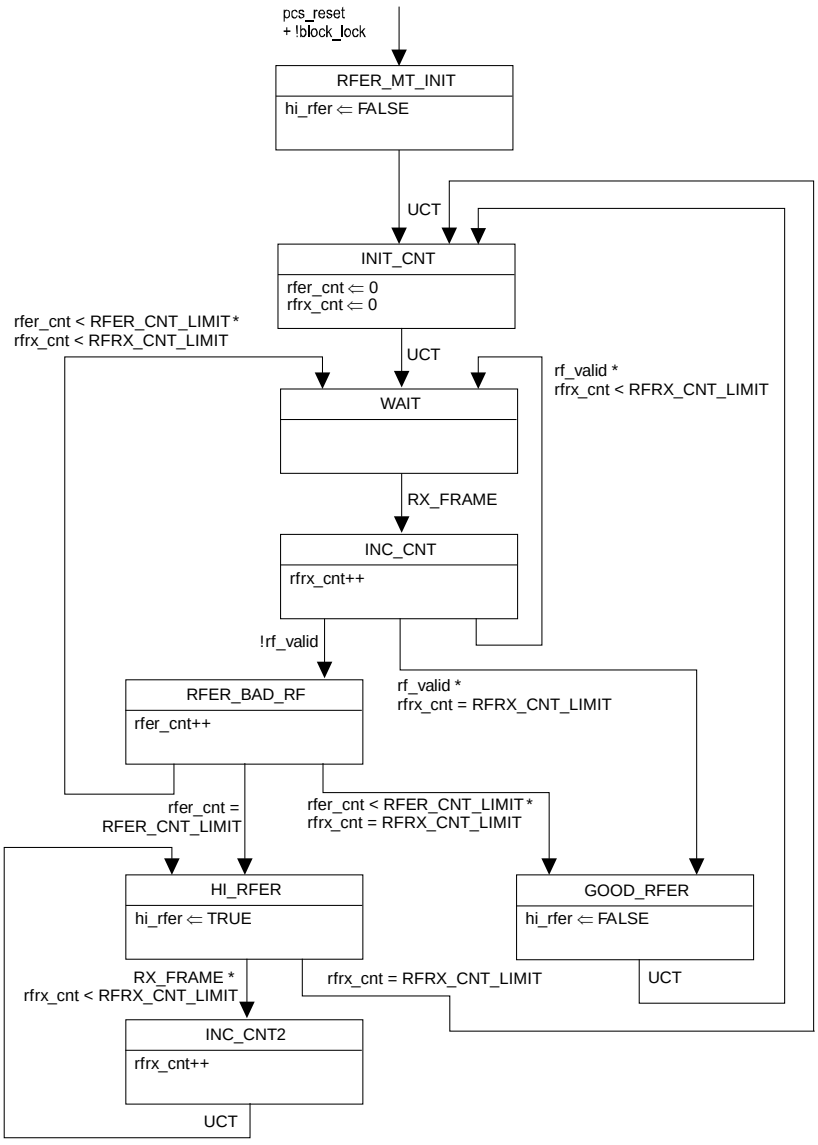


Figure 202–19—RFER monitor block state diagram

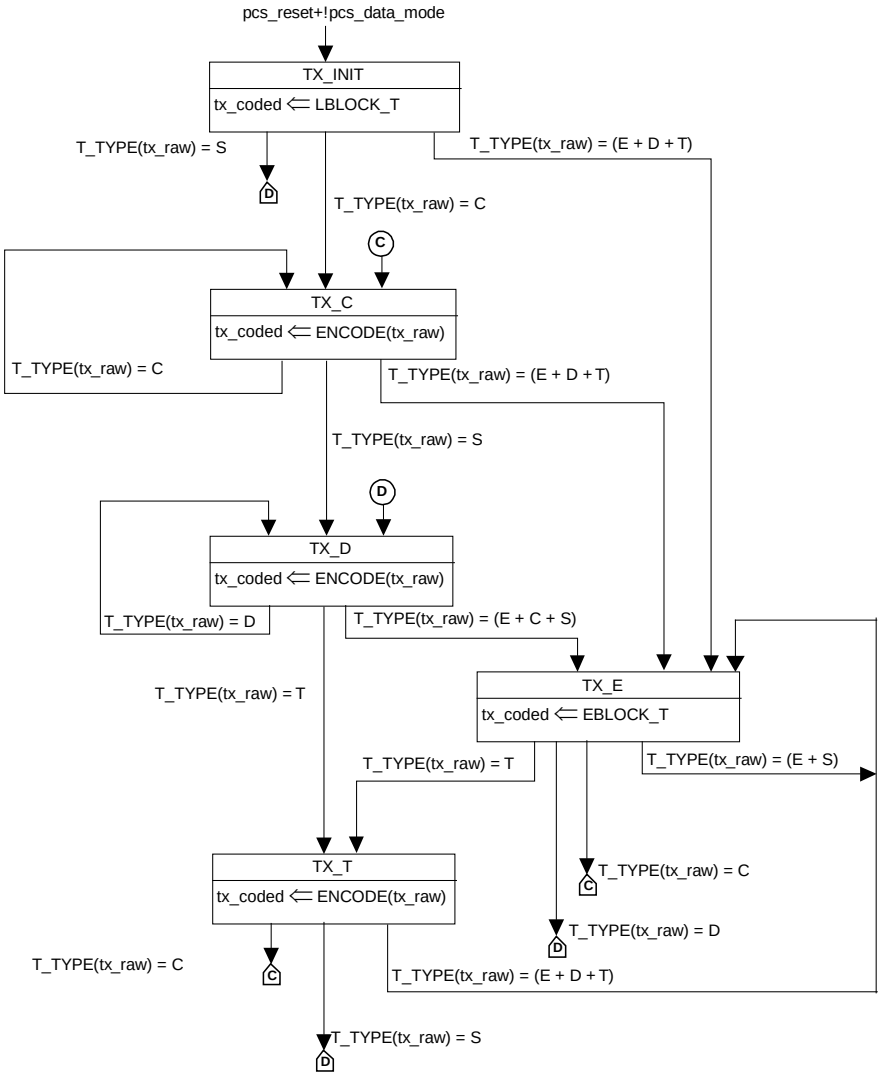


Figure 202–20—PCS 64B/65B Transmit state diagram

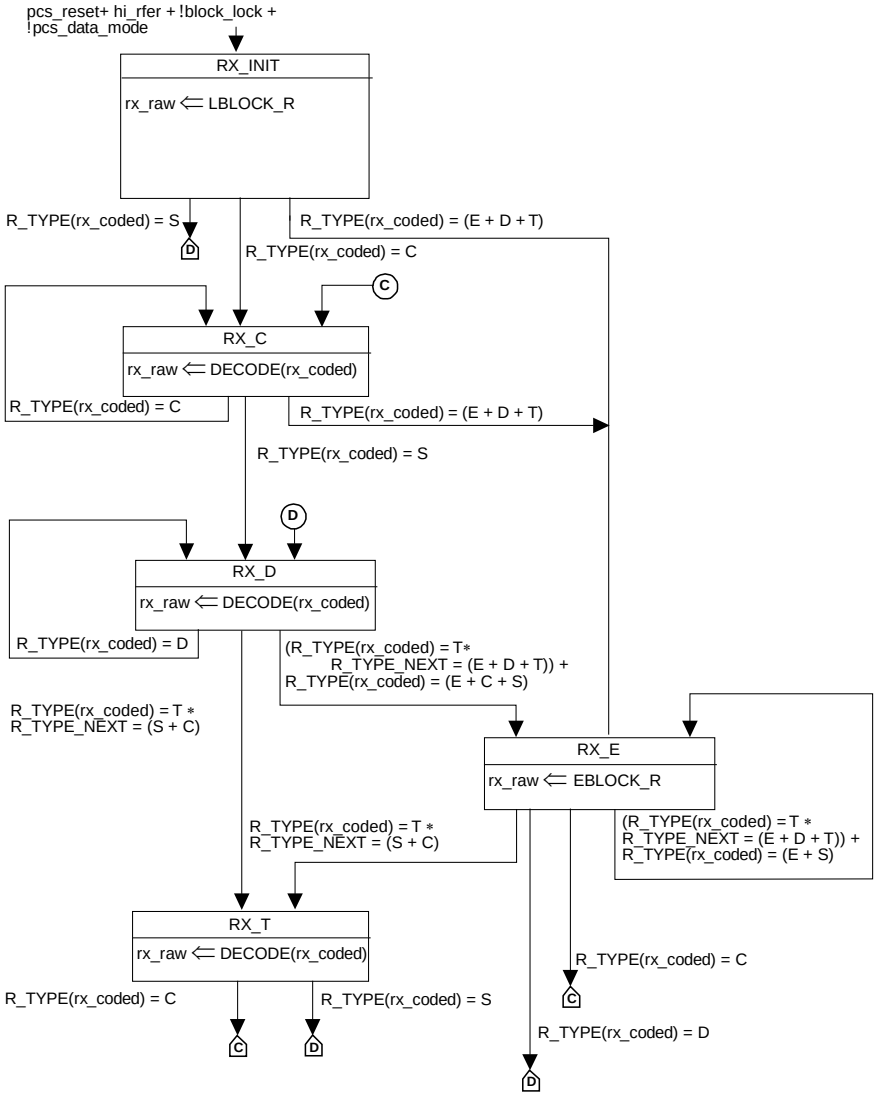


Figure 202–21—PCS 64B/65B Receive state diagram

202.3.8 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

202.3.8.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10 (TBD). A latch low view of this status is reflected in MDIO 3.2323.2 (TBD) and the inverse of this status is reflected in MDIO 3.2323.7 (TBD).

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8 (TBD). A latching low version of this status is reflected in MDIO bit 3.2324.6 (TBD).

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9 (TBD). A latching high version of this status is reflected in MDIO bit 3.2324.7 (TBD).

202.3.8.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

Editor's Note (to be removed prior to Working Group Ballot):

The descriptions in MDIO register 3.2324 need to be updated to align with Clause 202 as the current descriptions only point to Clause 149.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 202–19 is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

202.3.9 Operations, administration, and maintenance (OAM)

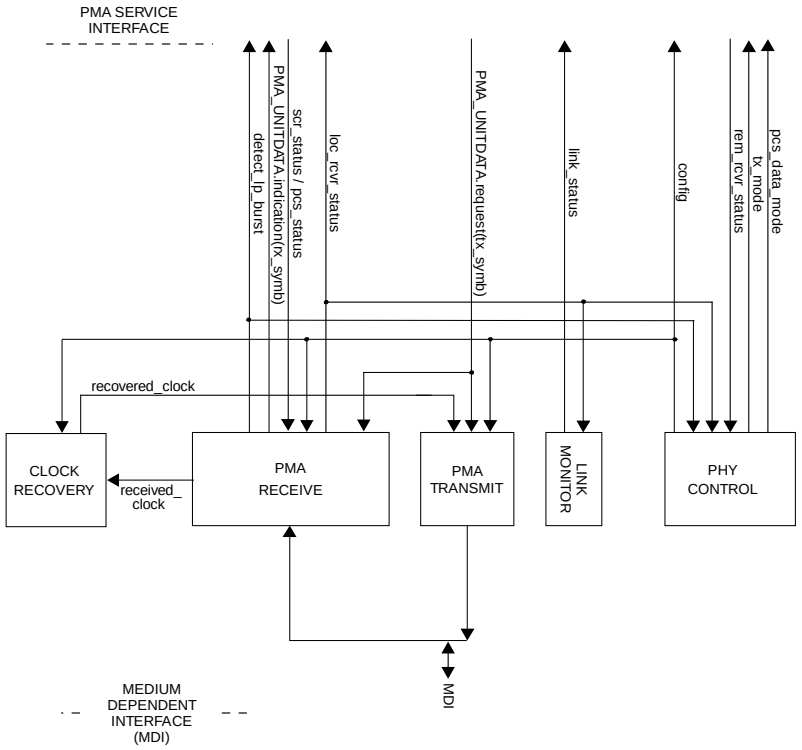
MultiGBASE-A operations, administration, and maintenance (OAM) is as specified for MultiGBASE-T1 PHYs in 149.3.9. OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one per TDD burst into the OAM fields in the HS_PATH and LS_PATH. OAM bits after the first ten per burst are reserved.

202.4 Physical Medium Attachment (PMA) sublayer

202.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 202.2.1 to the baseband medium specified in 202.7 or 202.8.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 202.9 or 202.10.



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

Figure 202–22—PMA reference diagram

202.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 202–22, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 202–22.

202.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 202–26), if link partner has already exited DISABLE_TRANSMITTER state.

202.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a two-level or four-level modulated signal on a single balanced pair of conductors or a single ended coaxial cable. When the PHY Control state diagram (see Figure 202–26) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI, followed by a ~~quiet~~ QUIET period to complete a TDD cycle. The PMA shall repeat such TDD cycles with the predefined timing parameters specified in 202.3.6. The signals generated by PMA Transmit shall comply with the electrical specifications given in 202.5.2.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source the transmit symbol clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of 202.5.2.3. The LEADER-FOLLOWER relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the recovered clock of 202.4.2.6 while meeting the jitter requirements of 202.5.2.3.

Editor's Note (to be removed prior to Working Group Ballot):

Need to add text to address transmit fault detection.

202.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

202.4.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM2 or PAM4 signals on the balanced pair or the single ended coaxial cable. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received into the PMA_UNITDATA.indication parameter rx_symb. The quality of

these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a -T1 link segment meeting the requirements of 202.7 or a -V1 link segment meeting the requirements of 202.8.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization. No echo cancellation is needed due to the TDD nature of the duplexing method.

The PMA Receive function uses the parameters pcs_status and scr_status, as well as the state of the equalization and estimation functions, to determine the quality of the receiver performance and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see Figure 202–26). Failing to receive link partner's consecutive TDD bursts could trigger deassertion of loc_rcvr_status. The SEND_Z signal during the TDD QUIET period alone shall not trigger the DUT to de-assert its loc_rcvr_status. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for signal inversions.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.193.7 (TBD).

202.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 202–26.

During PMA training (TRAINING and COUNTDOWN states in Figure 202–26), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the 96 bits starting after the *N_inf* th bit of the training payload specified in 202.3.5.3. The link partner is not required to decode every Infofield transmitted but is required to decode Infofields at a rate that enables the correct actions prior to the training phase transition.

The 12-octet Infofield shall include the fields in 202.4.2.4.2 through 202.4.2.4.8, also shown in Figure 202–23 and Figure 202–24. When PMA_state = 00, Infofield shall be transmitted at least 16 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octet 8	octets 9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	delay counter	PHY capability bits	CRC16

Figure 202–23—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	PhaseSwBC24	CRC16

Figure 202–24—Infofield COUNTDOWN format

202.4.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved ‹bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (i.e., the LSB of octet 1 is sent first).

202.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<T:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0 > and so forth.

202.4.2.4.3 PHY burst count (BC24)

The PHY burst count consists of 3 octets [Oct4<7:0>,Oct5<7:0>,Oct6,7:0>] and indicates the running count of PHY bursts sent LSB first. The BC24 continues to run uninterrupted for the duration of the link.

BC24 is defined to rollover to 0 after it reaches 16776959. BC24 could roll over in the case the LEADER has started long before the FOLLOWER sends the first responding burst.

202.4.2.4.4 Message Field

The Message Field is one octet. For both the LEADER and FOLLOWER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, training_phase<4:3>, reserved<2:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.

The two training_phase-indicator bits training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> =00 indicates SYMMETRIC TRAINING and training_phase<4:3>=01 indicates ASYMMETRIC TRAINING.

All possible Message Field settings are listed in Table 202–9 for the LEADER or FOLLOWER. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 202–9 for the LEADER, and the first or second row of Table 202–9 for the FOLLOWER. Moreover, for a given Message Fields setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

Table 202–9—Infofield message field valid LEADER or FOLLOWER settings

PMA_state<7:6>	loc_rcvr_status	training_phase<4:3>	reserved	reserved	reserved
00	0	00	0	0	0
00	1	00	0	0	0
01	1	00	0	0	0
00[2]	0	01	0	0	0
00	1	01	0	0	0
01	1	01	0	0	0

202.4.2.4.5 PHY capability bits

This multi-rate PHY supports bidirectional data transfer with 2.5 Gb/s, 5 Gb/s, or 10 Gb/s point-to-point transmission or reception in one direction and 100 Mb/s point-to-point reception or transmission in the other direction. The direction of asymmetry and high speed rate are determined at link startup. The management control configures the LEADER to negotiate with the FOLLOWER to configure it for the desired high speed data rate that the FOLLOWER is expected to use. The PHY capability and negotiated ~~speed~~ rate bits of the Infofield are used to establish the FOLLOWER rate and check for misconfiguration.

When PMA_state<7:6>= 00, then the Infofield [Oct9<7:0>,Oct10<7:0>] contains the PHY capability and negotiated ability bits. Each octet is sent LSB first.~~.~~ See Table 202–10 for the details of the field locations. As shown, these fields carry different values depending on the value of the burst count (BC24) LSB. See Tables 202-10a, and 202-10b, and 202-10c for details of how the fields are encoded.

Table 202–10—~~PHY capability bits~~

~~octet 9~~								~~octet 10~~							
~~0~~	~~1~~	~~2~~	~~3~~	~~4~~	~~5~~	~~6~~	~~7~~	~~0~~	~~1~~	~~2~~	~~3~~	~~4~~	~~5~~	~~6~~	~~7~~

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[2]This row can be skipped if not applicable.

~~VendorSpecificData~~

Table 202-10 – PHY capability and negotiated ability bits

		Octet 9								Octet 10							
		0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
BC24 LSB = 0	PHY_D / PHY_S Transmit and Receive Capability																
	Transmit Capability									Receive Capability							
		LS Rate		HS Rate						LS Rate		HS Rate					
		R	100 Mb/s	R	R	R	10 Gb/s	5 Gb/s	2.5 Gb/s	R	100 Mb/s	R	R	R	10 Gb/s	5 Gb/s	2.5 Gb/s
BC24 LSB = 1	PHY_D / PHY_S Negotiated Abilities																
	Vendor Specific Data									Direction	OAMEn	R	Negotiated Rates				

The transmit and receive capabilities depend on whether the PHY supports PHY_S, PHY_D or both capabilities. For example, PHY_S sets its HS TX capability and LS RX capability, and PHY_D set its HS RX capability and LS TX capability.~~):~~ ~~Oct10<5> 2.5 Gb/s capable, Oct10<6> 5 Gb/s capable, Oct10<7> 10 Gb/s capable.~~The capability bit field assignments are shown in Table 202-10a. A one in a field bit indicates that the PHY has that capability and a zero indicates it does not. All-zeros indicates that the field is not applicable to this PHY. For example, since a PHY_S has no HS RX capability it would set Oct10<7:2> to zero.

Table 202-10a – Rate field encoding

HS Rate		LS Rate	
000000	N/A	00	N/A
000001	2.5 Gb/s	01	100M
000010	5 Gb/s	10	RESERVED
000100	10 Gb/s	11	N/A
001000	RESERVED)		
010000	RESERVED		
100000	RESERVED		

~~Negotiated speed: 00 - 2.5 Gb/s, 01 - 5 Gb/s, 10 - 10 Gb/s~~The negotiated rate field encoding is shown in Table 202-10b. The LEADER selects the negotiated rates based on either management configure of register

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bits 1.xxx<5:1> or selecting the highest mutually supported advertised rate. In the latter case, the LEADER optionally sends the all-zeros negotiate rate code when it desires to see the FOLLOWER capabilities prior to determining the negotiated rate.

Table 202-10b—Negotiated rate field encoding

Code	TX	RX
00000	In progress	In progress
00001	100 Mbit/s	2.5 Gb/s
00010	100 Mbit/s	5 Gb/s
00011	100 Mbit/s	10 Gb/s
00100	Reserved	Reserved
00101	Reserved	Reserved
00110	2.5 Gb/s	100 Mbit/s
00111	5 Gb/s	100 Mbit/s
01000	10 Gb/s	100 Mbit/s
01001	Reserved	Reserved
…	…	…
11111	Reserved	Reserved

Table 202-10b – Negotiated rate field encoding

Code	LS RATE	HS RATE
00000	In progress	In progress
00001	100 Mbit/s	2.5 Gb/s
00010	100 Mbit/s	5 Gb/s
00011	100 Mbit/s	10 Gb/s
00100	Reserved	Reserved
00101	Reserved	Reserved
00110	Reserved	Reserved
00111	Reserved	Reserved
01000	Reserved	Reserved
01001	Reserved	Reserved
…	…	…
11111	Reserved	Reserved

Table 202-10C – Negotiated direction field encoding

Direction	LEADER	FOLLOWER
0	PHY_D	PHY_S
1	PHY_S	PHY_D

The LEADER uses the Direction bit to communicate the desired FOLLOWER PHY type as shown in Table 202-10c. A zero indicates that the FOLLOWER is requested to be a PHY_S and a one indicates that the FOLLOWER is requested to be a PHY_D.

OAMEn: The optional OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1.

PrecodeSel indicates the requested precoder and is available for 10 Gb/s Speed Capability only (see 202.3.2.2.19).

The capability bit values shall be considered as valid only when loc_rcvr_status bit is 1.

The criteria to set Negotiated Speed is TBD.

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202.4.2.4.6 TDD delay counter

When PMA_state<7:6>=00, then Oct8<7:0> contains TDD delay counter sent LSB first. The format of TDD delay counter is Oct8<0> = Reserved, Oct8<1:6> = delay_count<5:0>, and Oct8<7> = delay_count_valid. See Table 202–11 for the details.

Table 202–11—TDD delay counter

octet 8							
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
	delay_count						

Editor's Note (to be removed prior to Working Group Ballot):

The text in the following 4 paragraphs is repeated in 202.4.2.4.11. Need to identify what information is needed here.

After the LEADER detects the FOLLOWER TDD burst position, it should estimate the link segment delay, then set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to 1. Each LSB unit represents 5.333 ns delay (16 symbols at 3 GBd).

The FOLLOWER shall accept the received remote delay_count only when received remote delay_count_valid bit is set to 1. The FOLLOWER shall store this delay_count number.

As acknowledgment of the reception of this delay_count, the FOLLOWER shall send back its received delay count in its own delay_count field and set its delay_count_valid to 1, so the LEADER can confirm the exchange of this information is completed. When the LEADER or the FOLLOWER finishes the exchange of delay count, the negotiated speed, and the PrecodeSel, it shall set Negotiation_done signal to 1. The PHY Control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.

Starting from Asymmetric training and continuing through to the data mode, the FOLLOWER shall adjust its transmit burst position according to the stored delay_count.

202.4.2.4.7 Phase switch PHY burst count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>] contains the phase switch burst count (PhaseSwBC24) sent LSB first. PhaseSwBC24 indicates the burst count when the LEADER transmitter switches from current training phase to the next training phase or Data mode. PhaseSwBC24 shall be a minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state.

Since phase switch is always initiated from the LEADER, the PhaseSwBC24 value of FOLLOWER Infofield will be ignored. The LEADER will exit a COUNTDOWN state after sending the last burst (BC24=PhaseSwBC24-1), and receiving the last burst from the FOLLOWER. The FOLLOWER will exit a COUNTDOWN state after receiving the last burst (BC24=PhaseSwBC24-1) from the LEADER and finishing sending the last burst of its own.

202.4.2.4.8 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>)] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

202.4.2.4.9 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 202–25. In Figure 202–25 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 202–25, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

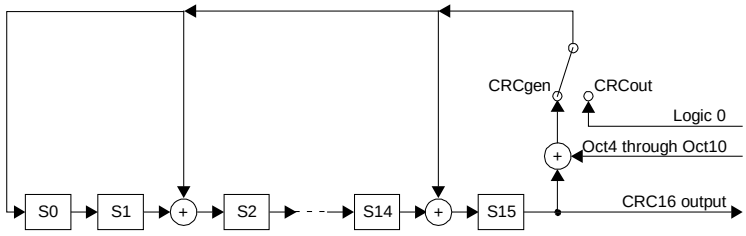

Figure 202–25—CRC16

202.4.2.4.10 PMA MDIO function mapping

Editor's Note (to be removed prior to Working Group Ballot):

Possible modifications to 149.4.2.4.9 may be required. Recommend adding text to describe references to register usage and naming.

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 202–12. Mapping of MDIO status variables to PMA status variables is shown in Table 202–13.

Table 202–12—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1 PMA control register	1.2309.14	PMA_transmit_disable

Table 202–13—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1 PMA status register	1.2310.1	PMA_receive_fault

202.4.2.4.11 Startup sequence

Editor's Note (to be removed prior to Working Group Ballot):

Table 149-15 provides some time limits on state transitions. It may be useful to apply here. TBD.

The startup sequence shall comply with the state diagram description given in Figure 202–26. PMA_CONFIG is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

When entering the TRAINING0 state, the FOLLOWER shall align the first symbol of the transmit PMA training frame to be on the transmit MDI 133.33 ns after the last PMA training payload symbol from the LEADER appears on the FOLLOWER input MDI. The FOLLOWER shall maintain this alignment while in the TRAINING0 state. The FOLLOWER Infofield burst count shall match the LEADER Infofield burst count from the previous PMA training frame.

In the TRAINING0 state, PAM2 transmission is used and PHY capabilities, PrecoderSel, and delay_count are exchanged with Infofields as specified in 202.4.2.4.5. The final negotiated speed mode will be determined by the LEADER. The FOLLOWER shall continue to maintain this alignment until it enters the TRAINING0 state.

At any COUNTDOWN or PCS_TEST state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT state and attempts a retrain.

When entering the TRAINING1 state, the FOLLOWER shall use the LEADER transmitted delay_count to align its transmit PMA training frame to be 176 ns - delay_count × 5.33 ns, after the last PMA training payload symbol from the LEADER appears on the FOLLOWER input MDI.

The LEADER link_fail_inhibit_timer is started when it detects the first FOLLOWER transmitted PMA training frame. The FOLLOWER link_fail_inhibit_timer is started when it sends first PMA training frame to the LEADER. The link_fail_inhibit_timer value is defined to be 97.5 ms, it is used to force a restart if the link up cannot be achieved within maximum allowed time.

The LEADER and FOLLOWER will move from TRAINING0 state to COUNTDOWN0 state, if local_rcvr_status and rem_rcvr_status are both asserted, and negotiation_done bit is OK.

202.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive link and communicates it via the variable link_status. Failure of the underlying receive link causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the link.

The Link Monitor function shall comply with the state diagram of Figure 202–28.

Upon power on reset, or release from power down, the PHY sets link_control = DISABLE. During this period, link_status = FAIL is asserted. When the PHY link_control is set to ENABLE, the Link Monitor state diagram begins monitoring the PMA. As soon as reliable transmission is achieved, with pcs_data_mode=TRUE, the variable link_ status = OK is asserted, upon which further PHY operations can take place.

202.4.2.6 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 202.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock for use when configured as the FOLLOWER.

202.4.3 MDI

Communication through the MDI is summarized in 202.4.3.1 and 202.4.3.2.

202.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The transmit path uses PAM2 for all refresh headers and during RS-FEC frame transmission for 100 Mb/s, 2.5 Gb/s or 5 Gb/s. The transmit path uses PAM4 for the 10 Gb/s RS-FEC frame transmission. During RS-FEC frame transmission, 10 Gb/s transmit path uses PAM4 while all other symbols transmitted within a burst use PAM2. PMA Transmit generates a pulse-amplitude modulated signal in the form shown in Equation (202–18). During RS-FEC frame transmission, 10 Gb/s transmit path uses PAM4 while all other symbols transmitted within a burst use PAM2.

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(202–18)

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT)$$

In Equation (202–18), a_n is the PAM4 modulation symbol from the set {–1, –1/3, +1/3, +1} or the PAM2 modulation symbol from the set {–1, +1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 202.5.2.

202.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as shown in Equation (202–19).

(202–19)

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t)$$

In Equation (202–19) $hR(t)$ denotes the symbol response of the overall impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

202.4.4 State variables

202.4.4.1 State diagram variables

config
: The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.
Values: LEADER or FOLLOWER.

link_control
: This variable is generated by management or set by default.
Values: ENABLE or DISABLE.

link_status
: The link_status parameter set by PMA Link Monitor state diagram.
Values: OK or FAIL.

loc_countdown_done
: This variable is only used by the LEADER. It is set to false when the PHY Control state diagram is

in the DISABLE_TRANSMITTER state or SILENT state, or after entering the new TRAINING state, and is set to TRUE once the LEADER finishes sending the last LEADER countdown Infofield and receiving the responding (last) Infofield from the FOLLOWER at the current TRAINING stage.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY at the current TRAINING stage. This variable is transmitted in the loc_rcvr_status bit of the Infofield by the local PHY.

Values:

OK: The receive link for the local PHY is operating reliably.

NOT_OK: Operation of the receive link for the local PHY is unreliable.

negotiation_done

During symmetric training phase, after loc_rcvr_status=1, the LEADER and FOLLOWER shall exchange capabilities, delay_count and negotiated speed, and then set negotiation_done bit.

Values:

OK: Negotiation is done, can move to COUNTDOWN0 state.

NOT_OK: Negotiation is not done, stay in TRAINING0 state.

pcs_data_mode

Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_-mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

pma_reset

Allows reset of all PMA functions. It is set by PMA Reset.

Values: ON or OFF.

PMA_state

Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.

Values:

00: TRAINING state.

01: COUNTDOWN state.

rem_countdown_done

This variable is only used by the FOLLOWER. It is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SLIENT state, or after entering the new TRAINING state, and is set to TRUE once the FOLLOWER receives the last countdown Infofield from the LEADER and finishes sending one Infofield from the FOLLOWER at the current TRAINING stage.

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. This variable is received in the loc_rcvr_status bit in the Infofield from the remote PHY. This variable is set to NOT_OK if the PCS has not decoded valid Infofields from the remote PHY.

Values:

OK: The receive link for the remote PHY is operating reliably.

NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

tdd_watchdog_status

Variable indicating the status of the TDD monitor. During normal operation, NOT_OK is assigned

when a TDD signal is not reliably detected within a moving time window equivalent to 10 complete TDD cycles.
Values:
OK: TDD burst is detected reliably.
NOT_OK: TDD burst is not detected reliably.

tx_mode
The PMA generates this variable continuously and passes it to the PCS via the PMA_TXMODE.indication primitive (see 202.2.1).
Values:
SEND_N: This value is continuously asserted when transmission of sequences of symbols representing a XGMII data stream take place.
SEND_TS: This value is continuously asserted when transmission of sequences of symbols representing the symmetric training sequences of symbols is to take place.
SEND_TA: This value is continuously asserted when transmission of sequences of symbols representing the asymmetric training sequences of symbols is to take place.
SEND_Z: This value is asserted when transmission of ~~zero~~ Z symbols is to take place.

202.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

link_fail_inhibit_timer
A timer used to determine the maximum amount of time the PHY Control stays in the TRAINING, COUNTDOWN, and PCS_TEST states. The timer shall expire 97.5 ms ± 0.5 ms after being started.
LEADER: This timer will be started when the LEADER PHY receives the first burst from the FOLLOWER.
FOLLOWER: This timer will be started when the FOLLOWER PHY sends the first burst to the LEADER.

minwait_timer
A timer used to determine the minimum amount of time the PHY Control stays in the SILENT and PCS_TEST states. The timer shall expire 975 μs ± 50 μs after being started.

202.4.5 State diagrams

The PHY Control state diagram is shown in Figure 202–26 and Figure 202–27.

The Link Monitor state diagram is shown in Figure 202–28.

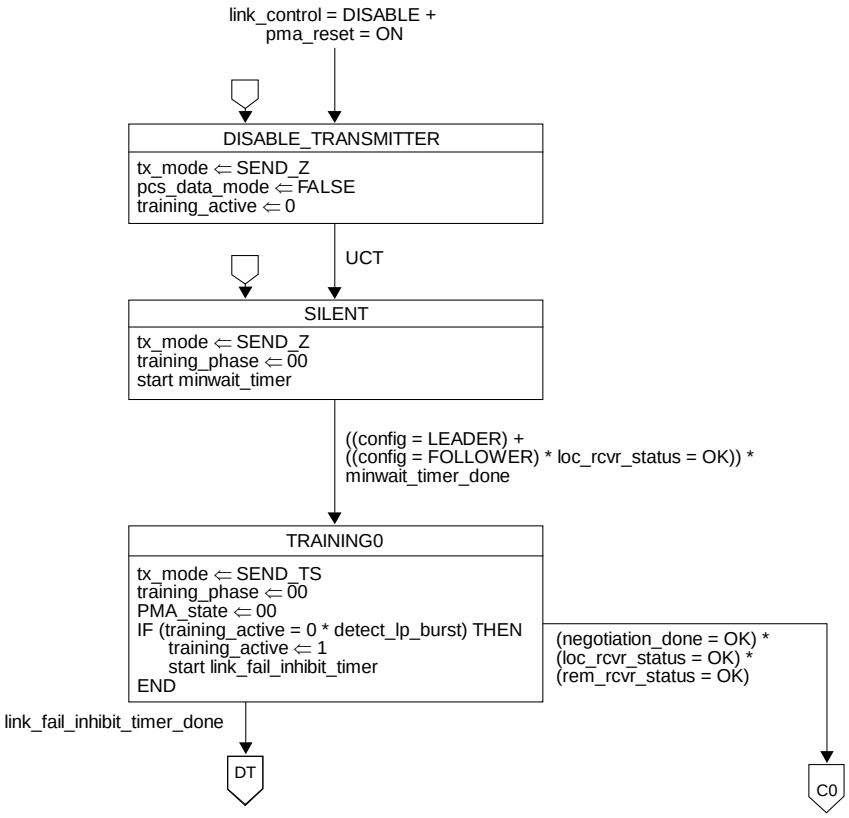

Figure 202–26—PHY Control state diagram, part a

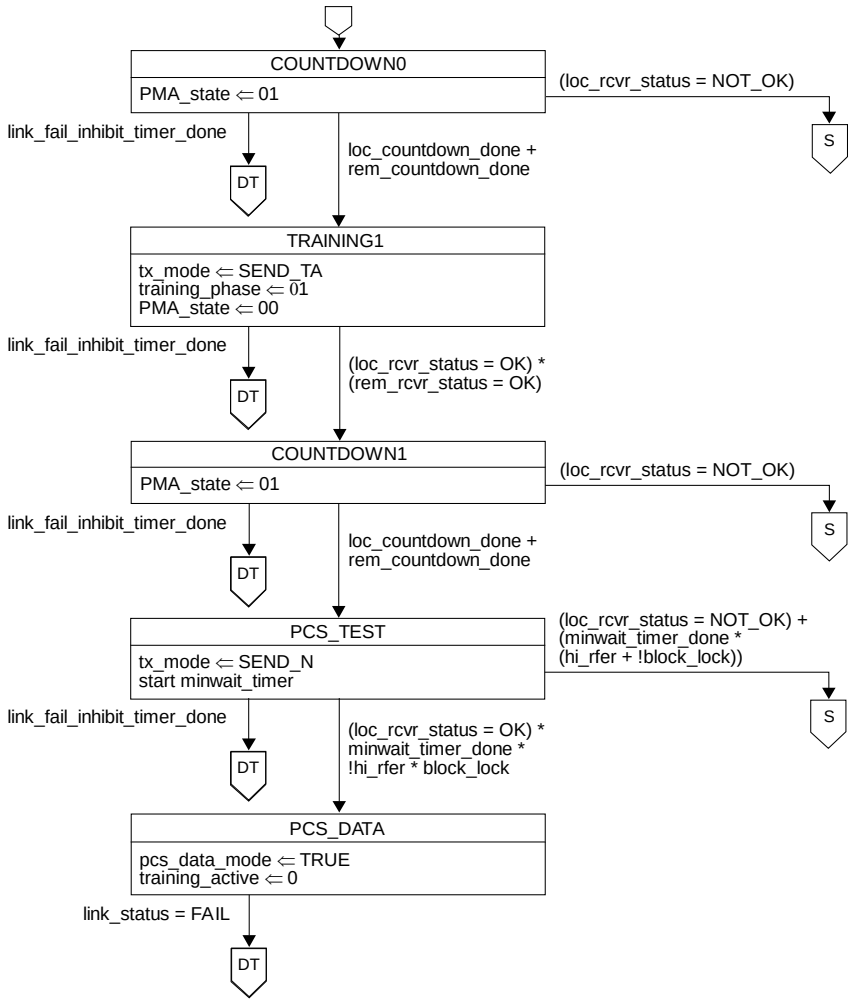

Figure 202–27—PHY Control state diagram, part b

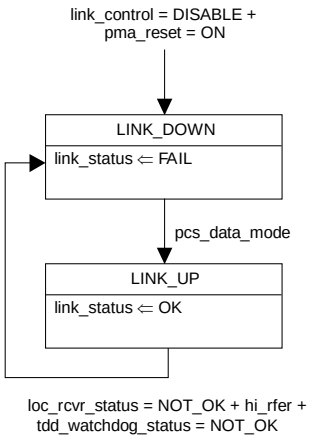

Figure 202–28—Link Monitor state diagram

202.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

202.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 202–14. If MDIO is not implemented, then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Table 202–14—MDIO management registers settings for test modes

Register value	Register description
000	Normal (non-test mode) operation
001	Test mode 1—Setting LEADER and FOLLOWER PHYs for transmit clock jitter test in linked mode

010	Test mode 2—Transmit MDI jitter test in LEADER mode
011	Test mode 3—Precoder test mode
100	Test mode 4—Transmitter distortion test
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test
110	Test mode 6—Transmitter droop test mode
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring

Test mode 1 enables testing of timing jitter on the LEADER and FOLLOWER transmitters. The LEADER and FOLLOWER PHYs are connected over a link segment defined in 202.7 or 202.8. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5. TX_TCLK_187.5 is equal to 187.5 MHz and is a divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous repeating pattern of {+1, -1} symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference.

Test mode 3 is for testing the precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the transmit precoder specified in 202.3.2.2.19, to be precoded according to the transmit precoder settings as determined by the value set in register 1.2313:10:9, or equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.

Test mode 4 is for transmitter distortion testing. When test mode 4 is enabled in PAM2 mode, the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (202–20) such that $A_n = Scr_n[0]$ (see Figure 202–4). All PHYs shall support transmission of this signal at 3 GBd. PHYs that support 5 Gb/s and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM4 mode, the PHY shall transmit the PCS scrambler generator polynomial per Equation (202–20) such that $A_n = Scr_n[0]$ and $B_n = Scr_n[3] \oplus Scr_n[8]$ (see Figure 202–4). PHYs that support 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

$$g(x) = 1 + x^9 + x^{11} \quad (202\text{–}20)$$

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit continuously with no quiet gap or refresh header and with transmit signal level corresponding to the normal mode of operation. The PCS Transmit will encode data as when tx_mode = SEND_N, and as if continuously receiving idle control characters from the

XGMII. The test applies to both the LEADER and FOLLOWER. The clock is sourced from a stable clock with 100 ppm accuracy for this test.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, the input to the RS-FEC is all-zero message symbols and the continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

202.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 202–29, Figure 202–30, and Figure 202–31, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

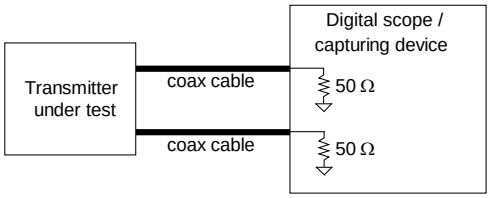

Figure 202–29—Transmitter test fixture 1 for -T1 transmitter droop, transmitter linearity, power spectral density, transmit power level, and MDI jitter measurements

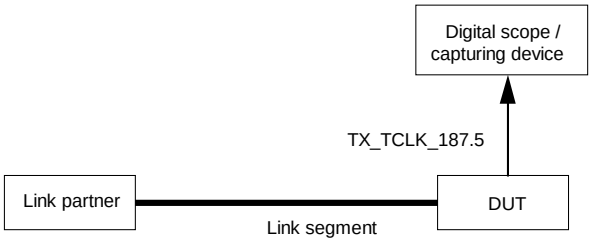

Figure 202–30—Transmitter test fixture 2 for -T1 and -V1 LEADER and FOLLOWER clock jitter measurement

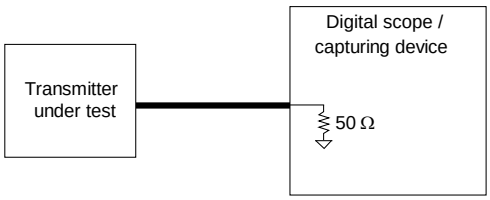

Figure 202–31—Transmitter test fixture 3 for -V1 transmitter droop, transmitter linearity, power spectral density, transmit power level, and MDI jitter measurements

202.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 202.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be ac-coupled (i.e., it presents a high dc common-mode impedance at the MDI). There may be various methods for ac-coupling in actual implementations.

When a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

202.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using transmitter test fixture 1 (see Figure 202–29) or test fixture 3 (see Figure 202–31), the magnitude of both the positive and negative droop shall be less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing.

202.5.2.2 Transmitter distortion

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 1 (see Figure 202–29) or transmitter test fixture 3 (see Figure 202–31) as appropriate to the MDI.

The peak distortion is determined by sampling the signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signal shall be at least 4000 transmitted symbols long and be sampled with the minimum 10x oversampling. The transmit baud rate may be reduced to 1 Gs/s by repeating the symbols using the same clock edge as in normal mode of operation.

The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM4 transmitters.

```
% Post processing pseudo-code for transmitter distortion
clear
Ns=2^11-1; % Scrambler length
```

```
Nc=70; % Canceller length
Modulation=2; % Choices are 2 or 4 for PAM2 and PAM4

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
   scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% Generate tm4 (test mode 4) for a given modulation
if Modulation==2
   tm4=2*scr-1;
else if Modulation==4
   tm4=ones(Ns,1);
   map=[-1;-1/3;1;1/3];
   DS=[scr,mod(circshift(scr,3) + circshift(scr,8),2)];
   data = 2*DS(:,1)+DS(:,2);
   for n=1:length(DS)
   tm4(n) =map(data(n)+1);
   end
else
   disp('Error: The code supports either PAM2 or PAM4')
   return
end

% Test mode4 matrix
for i=1:Nc
X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file

% Minimum of 4K TX symbols, 10X oversampling, high resolution capture
fid=fopen('TestMode4.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF at Nyquist
[A,B]=butter(1,1/10,'low');
tx=filter(A,B,tx);

% HPF (with this HPF, the 70-tap canceller residual linear error is 0.00
tx = filter([1,-1],[1,-0.98],tx);

% Select one period, 10x oversampling, a row vector
tx=tx((1:Ns*10)+2e3)'; % removes HPF transients

% Level normalization
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10
tx1=tx(n:10:end);
temp=xcorr(tx1,tm4); % Align data and test pattern
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);
coef=tx1/X; % Compute coefficients that minimize squared error in a cyclic
   block
```

```
err=tx1-coef*X; % Linear canceller
dist(n) = max(abs(err)); % Peak distortion
SNR(n)=std(tx)/std(err); % SNR
End

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist
```

202.5.2.3 Transmitter timing jitter and jitter at the MDI

The following measurements are performed for a PHY in LEADER mode:

1) The RMS jitter for jitter frequencies greater than 100 kHz measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1 shall be less than 1 ps when supporting 10 Gb/s, 2 ps when supporting 5 Gb/s/, and 4 ps when supporting 2.5 Gb/s.
2) Peak-to-peak of Time Interval Error measured in test mode 1 using test fixture 2 over a period of 100 µs shall be less than 10 ps when supporting 10 Gb/s, 20 ps when supporting 5 Gb/s, and 40 ps when supporting 2.5 Gb/s.

The following measurements are performed using test fixture 2 (see Figure 202–30) for a PHY in FOLLOWER mode:

1) The RMS jitter for jitter frequencies greater than 1 MHz measured in test mode 1 shall be less than 1 ps when supporting 10 Gb/s, 2 ps when supporting 5 Gb/s, and 4 ps when supporting 2.5 Gb/s.
2) Peak-to-peak of Time Interval Error over any period of 10 µs measured in test mode 1 over 50 overlapping periods of 10 µs each shall be less than 15 ps for 10 Gb/s, 30 ps for 5 Gb/s, and 60 ps for 2.5 Gb/s. The overlapping period of 5 µs is assumed.

202.5.2.4 Transmitter power spectral density (PSD) and power level

Transmitter power spectral density (PSD) and power level measurements are performed in test mode 5. The measured transmit power shall be in the range specified in Table 202–15 when using the same test fixture as used for PSD measurement. When tx_symb is “Z” the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm for frequencies above 10 MHz..

Table 202–15—Power levels

Transmit MAC data rate	Differential (balanced)		Single-ended (unbalanced)	
	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
100 Mb/s	0	2	-3	-1
2.5 Gb/s	0	2	-3	-1
5 Gb/s	2	4	-1	1
10 Gb/s	0	2	-3	-1

The power spectral density of the transmitter of -T1, measured into a 100 Ω differential load using test fixture 1 (see Figure 202–29), shall be between the upper and lower masks specified in Equation (202–21) and Equation (202–22).

The upper and lower masks for each MAC data rate are shown in Figure 202–32, Figure 202–33, and Figure 202–34. See Table 202–2 for the definition of *S*. See Table 202–16 for the definition of PSD mask *K* factor.

Table 202–16—PSD mask *K* factor

Transmit MAC data rate	*K*
100 Mb/s	0
2.5 Gb/s	0
5 Gb/s	0
10 Gb/s	2

(202–21)

$$UPSD(f) = \begin{cases} -89 - K & \text{dBm/Hz} \quad 40 < f \le 1200 \times S \\ -87 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 1200 \times S < f \le 3000 \times S \\ -80 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 3000 \times S < f \le 5000 \times S \end{cases}$$

(202–22)

$$LPSD(f) = \begin{cases} -93 - K & \text{dBm/Hz} \quad 40 < f \le 600 \times S \\ -92 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 600 \times S < f \le 2400 \times S \\ -86.4 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 2400 \times S < f \le 3500 \times S \end{cases}$$

where

f is the frequency in MHz

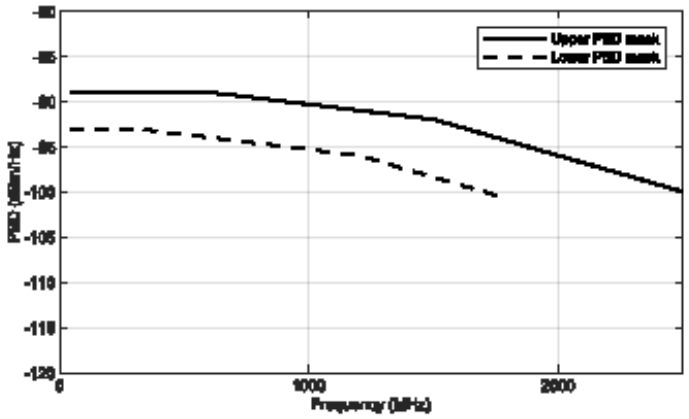

Figure 202–32—Transmitter Power Spectral Density for 100 Mb/s and 250 Mb/s MAC data rates, upper and lower masks

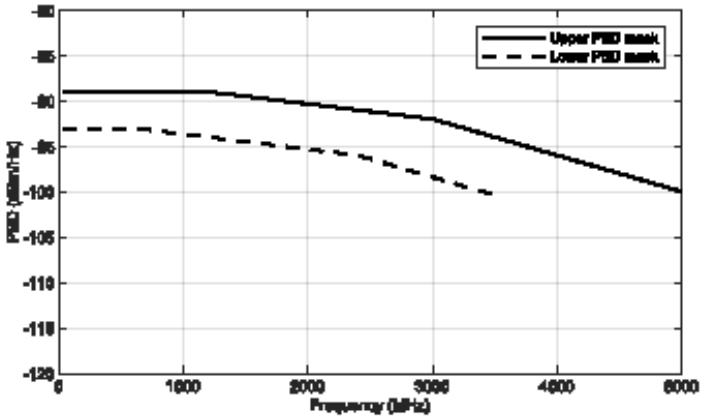

Figure 202–33—Transmitter Power Spectral Density for 5 Gb/s MAC data rate, upper and lower masks (TBD)

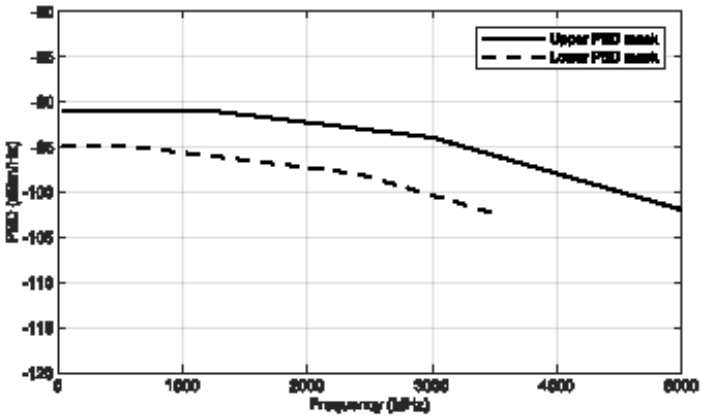

Figure 202–34—Transmitter Power Spectral Density for 10 Gb/s MAC data rate, upper and lower masks

For the power spectral density of -V1, with single ended termination of 50 Ω load and test fixture 3 (see Figure 202–31), both upper and lower PSD Masks are lower by 3 dB from Equation (202–21), Equation (202–22), Figure 202–32, Figure 202–33, and Figure 202–33.

202.5.2.5 Transmitter peak output

The transmit differential signal at the -T1 MDI should be less than the peak-to-peak values specified in Table 202–17 when measured with a 100 Ω termination. The transmit signal at the -V1 MDI should be less than the peak-to-peak values specified in Table 202–17 when measured with a 50 Ω termination. The limits in this clause apply to all transmitted symbol sequences, including SEND_N, SEND_TS, and SEND_TA.

Table 202–17—Transmitter peak-to-peak output

Transmit MAC data rate	-T1 MDI peak-to-peak output (V)	-V1 MDI peak-to-peak output (V)
100 Mb/s	1.3	0.65
2.5 Gb/s	1.3	0.65
5 Gb/s	1.5	0.75
10 Gb/s	1.7	0.85

202.5.2.6 Transmitter clock frequency

When using a local timing reference, the symbol transmission rate shall be within the range $6 \times S$ GBd ± 100 ppm with drift less than 1 ppm/sec).

When the FOLLOWER is using a recovered timing reference, the symbol transmission rate shall be within ± 10ppm of the recovered clock scaled by *S*.

202.5.3 Receiver electrical specifications

Editor's Note (to be removed prior to Working Group Ballot):

Coax signals are not differential at the MDI, so this clause may need to be reworded to include coax.

The PMA provides the Receive function specified in 202.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 202.7 or 202.8.

202.5.3.1 Receiver input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 202.5.2 and have passed through a link specified in 202.7 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion.

Single-ended signals received at the MDI that were transmitted from a remote transmitter within the specifications of 202.5.2 and have passed through a link specified in 202.8 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion.

This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

202.5.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver's tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 202–18. The minimum noise frequency is 10 MHz. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 202–35, with a link segment as defined in 202.7 for -T1 and shown in Figure 202–36, with a link segment as defined in 202.8 for -V1. The BER is expected to be less than 10^{-12}, and to satisfy this specification, the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

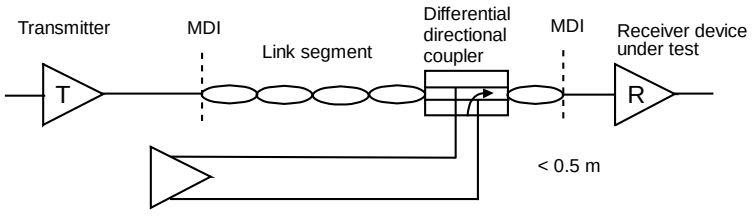

Figure 202–35—Broadband stationary noise rejection test setup, -T1

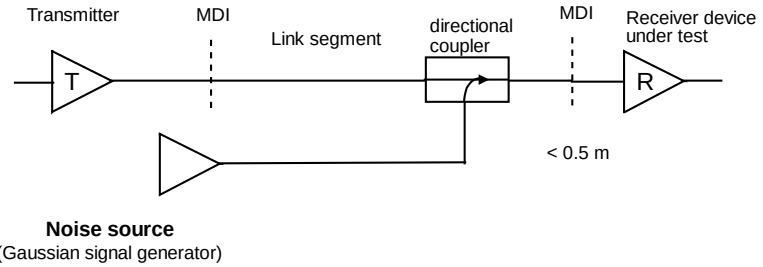

Figure 202–36—Broadband stationary noise rejection test setup, -V1

Table 202–18—Broadband stationary noise source, high speed

		Added noise at MDI (dBm/Hz)	
Transmit MAC data rate	**Noise bandwidth (MHz)**	**-T1**	**-V1**
2.5 Gb/s	1750	–140	-143
5 Gb/s	3500	–144	-147
10 Gb/s	3500	–148	-151

202.6 Management interface

MultiGBASE-A makes extensive use of the management functions that may be provided by the optional MDIO (see Clause 45).

202.7 Link segment characteristics, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. -T1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

202.7.1 Link transmission parameters

The transmission characteristics for a -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

202.7.1.1 Insertion loss

The insertion loss of a -T1 link segment shall meet the values determined using Equation (202–23).

(202–23)

$$\text{Insertion loss}(f) \le 0.322\sqrt{f} + 0.0019f + \frac{1}{\sqrt{f}} \quad \text{(dB)}$$

where

f is the frequency in MHz; $10 \le f \le 5000$

Equation (202–23) is plotted in Figure 202–37, which is provided for information only.

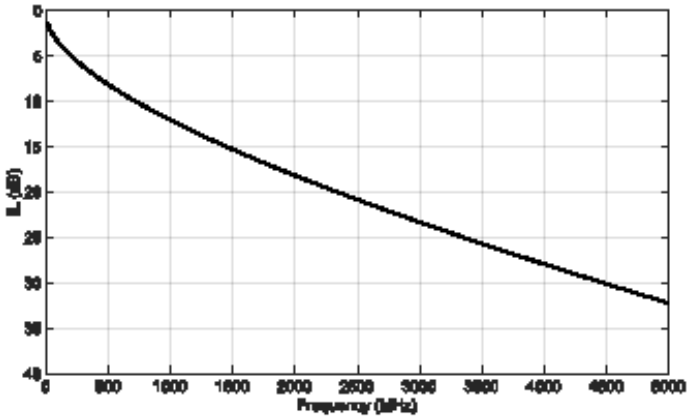

Figure 202–37—T1 link segment insertion loss

202.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of a -T1 link segment is 100 Ω.

202.7.1.3 Return loss

The return loss of a -T1 link segment shall meet the values determined using Equation (202–24).

(202–24)

$$RL(f) \geq \begin{cases} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left\langle \frac{f-500}{1500} \right\rangle & 500 \leq f < 2000 \\ 9.5 - 3\left\langle \frac{f-2000}{2500} \right\rangle & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{cases} \text{ (dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–24) is plotted in Figure 202–38, which is provided for information only.

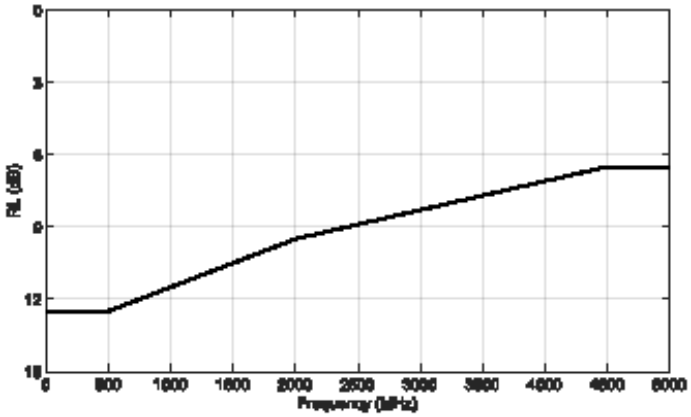

Figure 202–38—T1 link segment return loss

202.7.1.4 Coupling attenuation

The coupling attenuation of a -T1 link segment shall be as specified in 149.7.1.4.

202.7.1.5 Screening attenuation

The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5.

202.7.1.6 Maximum link delay

The maximum link delay of a -T1 link segment shall be 160 ns.

202.7.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

202.7.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -T1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -T1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–32).

$$\text{PSANEXT}(f) = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\text{AN}(f)_j}{10}} \text{ dB} \quad \text{(202–25)}$$

where the function $\text{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -T1 link segment j (1 to m) for the disturbed -T1 link segment.

The PSANEXT loss between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (202–33).

$$\text{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad \text{(dB)} \quad \text{(202–26)}$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (202–33) is plotted in Figure 202–44, which is provided for information only.

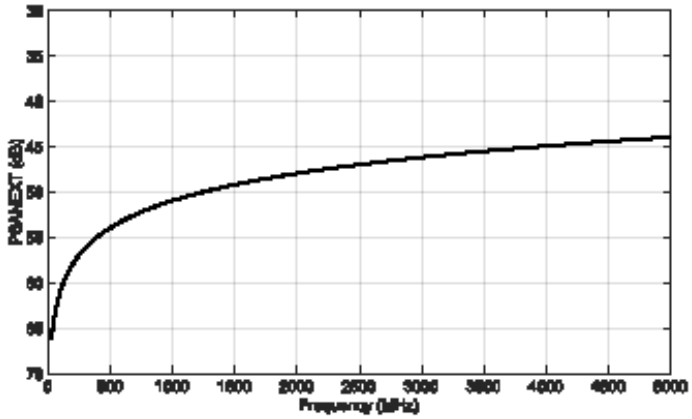

Figure 202–39—T1 link segment PSANEXT loss

202.7.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -T1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -T1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–34).

$$\mathrm{PSAACRF}(f) = \left(-10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AFEXT}(f)_j}{10}}\right) - \mathrm{IL}_d(f) \quad \mathrm{dB} \tag{202–27}$$

where

f is the frequency in MHz; $30 \le f \le 5000$

$\mathrm{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -T1 link segment j (1 to m) to the disturbed -T1 link segment in dB

$\mathrm{IL}_d(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (202–35).

$$\text{PSAACRF}(f) \geq 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad \text{(dB)} \tag{202–28}$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (202–35) is plotted in Figure 202–45, which is provided for information only.

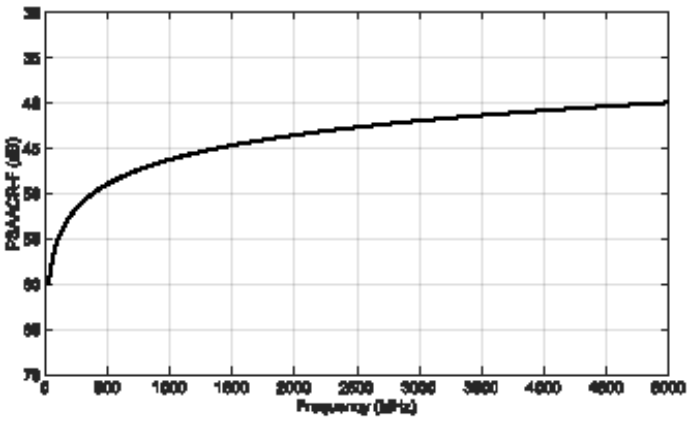

Figure 202–40—T1 link segment PSAACRF

202.8 Link segment characteristics, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial cable (-V1) that meet the requirements specified in this subclause. -V1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

202.8.1 Link transmission parameters

The transmission characteristics for a -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

202.8.1.1 Insertion loss

The insertion loss of a -V1 link segment shall meet the values determined using Equation (202–29).

(202–29)

$$\text{Insertion loss}(f) \leq 0.3 + 0.345\sqrt{f} + 0.000825f + \frac{0.48}{\sqrt{f}} \quad \text{(dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–29) is plotted in Figure 202–41, which is provided for information only.

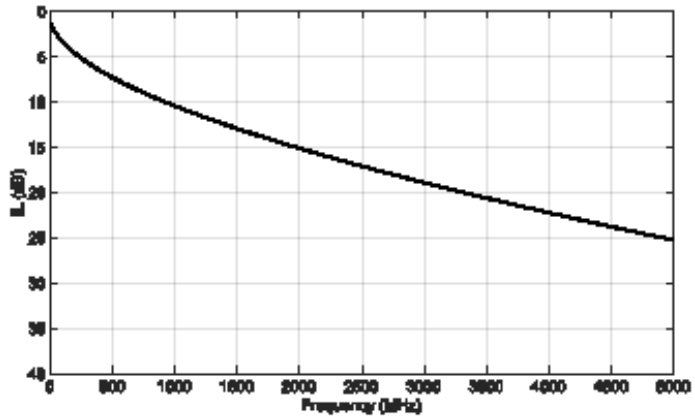

Figure 202–41—V1 link segment insertion loss

202.8.1.2 Single ended characteristic impedance

The nominal characteristic impedance of a -V1 link segment is 50 Ω.

202.8.1.3 Return loss

The return loss of a -V1 link segment shall meet the values determined using Equation (202–30).

(202–30)

$$RL(f) \geq \begin{cases} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left\langle \frac{f-500}{1500} \right\rangle & 500 \leq f < 2000 \\ 9.5 - 3\left\langle \frac{f-2000}{2500} \right\rangle & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{cases} \text{ (dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–30) is plotted in Figure 202–42, which is provided for information only.

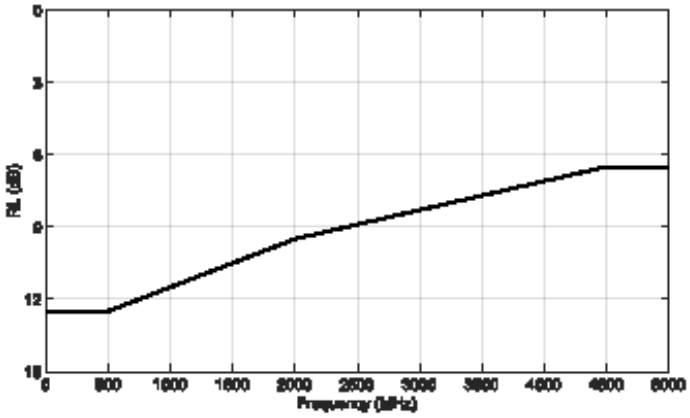

Figure 202–42—V1 link segment return loss

202.8.1.4 Coupling attenuation

Coupling attenuation is not defined for -V1 link segments.

202.8.1.5 Screening attenuation

The screening attenuation of a -V1 link segment, measured in accordance with ISO 19642-11, shall meet the values determined using Equation (202–31). Additional screening attenuation test methodologies are defined in Annex 149A.

(202–31)

$$Screening\ attenuation(f) \geq \left\{ \begin{array}{ll} 64 & 10 \leq f < 3000 \\ 54 & 3000 \leq f \leq 5000 \end{array} \right\} \text{ (dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–31) is plotted in Figure 202–43, which is provided for information only.

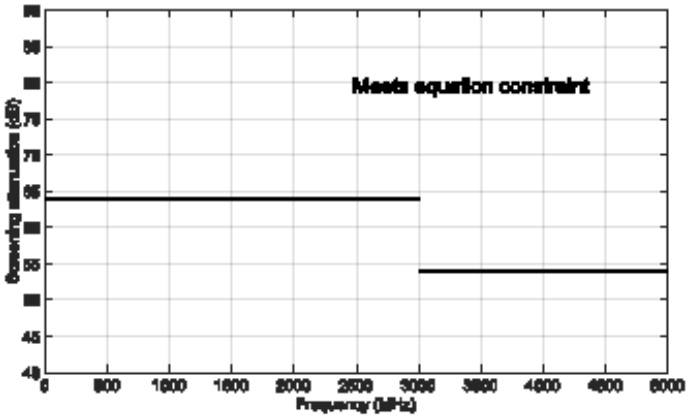

Figure 202–43—V1 link segment screening attenuation

202.8.1.6 Maximum link delay

The propagation delay of ~~maximum link delay of~~ a -V1 link segment shall ~~be~~ not exceed 160 ns.

202.8.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

202.8.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -V1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -V1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–32).

(202–32)

$$\mathrm{PSANEXT(f)} = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-AN(f)_j}{10}} \text{ dB}$$

where the function $AN(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -V1 link segment j (1 to m) for the disturbed -V1 link segment.

The PSANEXT loss between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (202–33).

(202–33)

$$\mathrm{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad \text{(dB)}$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (202–33) is plotted in Figure 202–44, which is provided for information only.

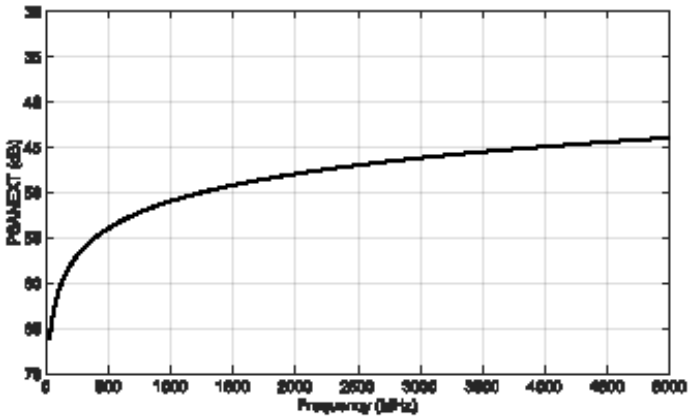

Figure 202–44—V1 link segment PSANEXT loss

202.8.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -V1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -V1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–34).

(202–34)

$$\mathrm{PSAACRF(f)} = \left(-10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AFEXT(f)}_j}{10}}\right) - \mathrm{IL_d(f)} \quad \mathrm{dB}$$

where

f is the frequency in MHz; $30 \le f \le 5000$

$\mathrm{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -V1 link segment j (1 to m) to the disturbed -V1 link segment in dB

$\mathrm{IL_d}(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (202–35).

(202–35)

$$\mathrm{PSAACRF}(f) \ge 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad \mathrm{(dB)}$$

where

f is the frequency in MHz; $30 \le f \le 5000$

Equation (202–35) is plotted in Figure 202–45, which is provided for information only.

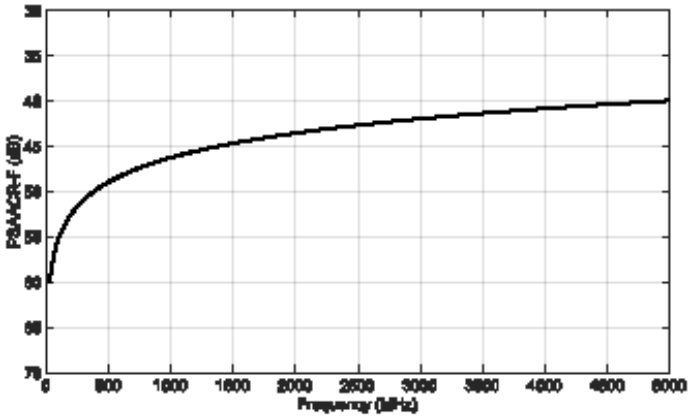

Figure 202–45—1 link segment PSAACRF

202.9 MDI specification, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

202.9.1 MDI connectors

The -T1 MDI connectors are as specified in 149.8.1.

202.9.2 MDI electrical specification

The electrical requirements specified in 202.5.2 and 202.5.3 shall be met when the PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors.

202.9.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -T1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (202–36). For the -T1 PMD, a nominal differential characteristic is impedance of 100 Ω is used.

(202–36)

$$MDI\_Return\_Loss(f) \geq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq Fmax$
$Fmax$ = TBD MHz for 100 Mb/s and 2.5 Gb/s data rate
= 4000 MHz for 5 Gb/s data rate
= 4000 MHz for 10 Gb/s data rate

Equation (202–36) is plotted in Figure 202–46, which is provided for information only.

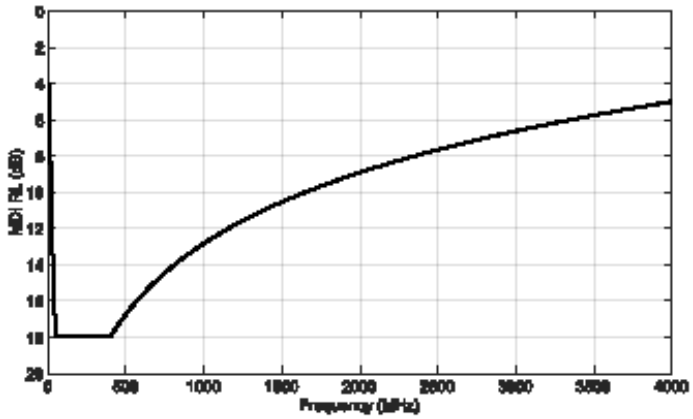

Figure 202–46—T1 MDI return loss using Equation (202–36)

202.9.3 MDI fault tolerance

The -T1 MDI fault tolerance shall comply with 96.8.3.

202.10 MDI specification, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial MDI (-V1) that meets the requirements specified in this subclause.

202.10.1 MDI connectors

The -V1 mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the -V1 mechanical interface is beyond the scope of this standard.

202.10.2 MDI electrical specifications

The electrical requirements specified in 202.5.2 and 202.5.3 shall be met when the PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable.

202.10.2.1 MDI return loss

The differential impedance at the -V1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -V1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (202–37). For the -V1 PMD, a nominal differential characteristic is impedance of 50 Ω is used.

(202–37)

$$MDI\_Return\_Loss(f) \geq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq Fmax$

Fmax
= TBD MHz for 100 Mb/s and 2.5 Gb/s data rate
= 4000 MHz for 5 Gb/s data rate
= 4000 MHz for 10 Gb/s data rate

Equation (202–37) is plotted in Figure 202–47, which is provided for information only.

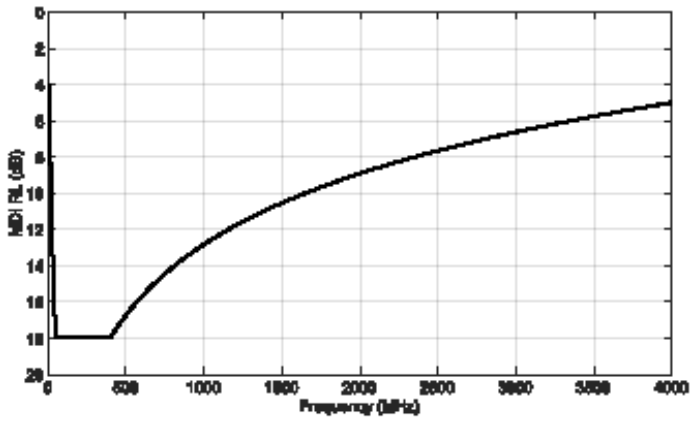

Figure 202–47—MDI return loss using Equation (202–37)

202.10.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 202–19, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

Table 202–19—Connection fault

Center conductor	Shield
No fault	Ground
MDI +	Ground
Ground	Ground
+50 V dc	Ground

202.11 Environmental specifications

202.11.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

202.11.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

202.11.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750–1

b) Electrical loads: ISO 16750–2, ISO 7637–2:2008, and ISO 8820–1

c) Mechanical loads: ISO 16750–3, ASTM D4728, and ISO 12103–1

d) Climatic loads: ISO 16750–4, IEC 60068–2–1, IEC 60068–2–27, IEC 60068–2–30, IEC 60068–2–38, IEC 60068–2–52, IEC 60068–2–64, and IEC 60068–2–78

e) Chemical loads: ISO 16750–5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

202.11.3 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21

b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21

c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3

d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

202.12 Delay constraints

Editor's Note (to be removed prior to Working Group Ballot):

Exceptions and modifications TBD.

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 202–20. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

Table 202–20—Delay Limits

Transmit MAC data rate	Bit times	Pause Quanta	Delay (ns)
100 Mb/s	1536	3	15 360
2.5 Gb/s	10 240	20	4096
5 Gb/s	13 824	27	2764.8
10 Gb/s	20 480	40	2048

202.13 Protocol implementation conformance statement (PICS) proforma for Clause 202, TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1[3]

202.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 202, TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

202.13.2 Identification

202.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

202.13.2.1

202.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-202x, Clause 202, TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

202.13.2.2

202.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

202.13.3

202.13.4 PICS proforma tables for TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

202.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

202.13.4.1

202.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]

202.13.4.2