NOTE—It is recommended that a FOLLOWER PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 201–42—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement, -V1

201.6.2 Transmitter electrical specifications

The MultiG+100M-T1/V1 PMA provides the Transmit function specified in 201.3.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high dc common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single-ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

201.6.2.1 Transmitter timing jitter

The allowable jitter varies with the PHY's data rate. The parameter *J* is used for scaling of the jitter, see Table 201–14.

Table 201–14—Jitter Scaling parameter

PHY type	*J*
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	2
2.5G+100MBASE-T1/V1	4

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both LEADER and FOLLOWER configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 201–38. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than *J* ps. The peak-to-peak value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10**J* ps. See Table 201–14 for the definition of *J*.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 6 ps and the RMS jitter shall be less than 3 ps when measured over jitter frequencies greater than 100 kHz. The peak-to-peak value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 60 ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

201.6.2.2 Transmit MDI random jitter in LEADER mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 201–15) and using test fixture 3 as shown in Figure 201–39 for -T1 and Figure 201–40 for -V1. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than J ps. See Table 201–14 for the definition of J. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than $10\times J$ ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

Table 201–15—Jitter test modes

Modulation	Bit 1.2313.1	Bit 1.2313.0	Test pattern
PAM4	0	0	Square wave: TX_TCLK_175
PAM4	0	1	JP03A (as specified in 94.2.9.1)
PAM4	1	0	JP03B (as specified in 94.2.9.2)
PAM2	1	1	0101 (as specified in 130.7.1.9)

201.6.2.3 Transmit MDI deterministic jitter in LEADER mode

Jitter measurements in this subclause are performed with the transmitter enabled in LEADER timing mode in test mode 2, with the patterns as defined by Table 201–15, and timed with a local clock.

To measure the peak-to-peak deterministic jitter (DJ_{pk-pk}) follow the steps as specified in 94.3.12.6.1, with the following modifications to step 5:

$f_n = 1 \times S$ MHz, $T = 68 / S$ ns. See Table 201–1 for the definition of S.

Using this method, DJ_{pk-pk} shall be less than $9\times J$ ps. See Table 201–14 for the definition of J.

To measure peak-to-peak even-odd jitter (EOJ_{pk-pk}) follow the steps as specified in 94.3.12.6.2.

Using this method, EOJ_{pk-pk} shall be less than $4\times J$ ps.

201.6.2.4 Transmitter clock frequency

~~The~~ In test mode 2 and using test fixture 3 as shown in Figure 201–39 for -T1 and Figure 201–40 for -V1, the symbol transmission rate of the LEADER PHY shall be within the range 5625 × *S* MHz ± 100 ppm. See Table 201–1 for the definition of *S*.

~~The~~ In test mode 2 and using test fixture 3 as shown in Figure 201–39 for -T1 and Figure 201–40 for -V1, the symbol transmission rate of the FOLLOWER PHY, when running off of a free-running clock, shall be within the range 5625 ⁄ 48 MHz +1/–20% and the short-term rate of frequency variation shall be less than 1% / second.

201.6.2.5 Transmitter linearity

Editor's Note (to be removed prior to Working Group Ballot):
Editorial Note: Consider what value of Np should be used in doing calculations to determine the SNDR.

With the transmitter in test mode 4, transmitting in MultiG mode, and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the test defined in 120D.3.1.2 shall be performed. The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2 for a 10G+100MBASE-T1/V1 PHY. For 5G+100MBASE-T1/V1 or 2.5G+100MBASE-T1/V1 PHYs, only levels corresponding to PAM2 modulation (-1 and +1) are relevant and ES1, ES2 and levels at ±1/3 are not applicable in the calculation of SNDR. The transmitter SNDR distortion, as specified in 120D.3.1.6, shall exceed 36 dB in 10G+100MBASE-T1/V1, 33 dB in 5G+100MBASE-T1/V1, and 30 dB in 2.5G+100MBASE-T1/V1 modes.

201.6.2.6 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the MultiG+100MBASE-T1/V1 PHYs shall be as specified in Table 201–16 and the power spectral density of the transmitter shall be between the upper and lower masks specified in Equation (201–9) and Equation (201–10). The PSD and power are measured using test fixture 4, shown in Figure 201–41, with a 100 Ω load for -T1 and shown in Figure 201–42, with a 50 Ω load for -V1. The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 201–43 for -T1 and in Figure 201–44 for -V1. When tx_symb is "Z" the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm. See Table 201–1 for the definition of *S*.

Table 201–16—Transmit Power, high speed mode

	Transmit power, -T1		Transmit power, -V1	
Transmit Rate	**Min (dBm)**	**Max (dBm)**	**Min (dBm)**	**Max (dBm)**
10 Gb/s	-1	2	-4	-1
5 Gb/s	-1	2	-4	-1
2.5 Gb/s	-4	-1	-7	-4

$$\mathrm{UpperPSD}(f) = \left\{ \begin{array}{cc} P_O & 0 < f \le 600 \times S \\ P_O + 1 - \dfrac{f}{600 \times S} & 600 \times S < f \le 3000 \times S \\ P_O + 8 - \dfrac{f}{250 \times S} & 3000 \times S < f \le 5500 \times S \end{array} \right\} \mathrm{dBm/Hz} \qquad (201\text{–}9)$$

$$\mathrm{LowerPSD}(f) = \left\{ \begin{array}{cc} P_O - 6 & 5 < f \le 400 \times S \\ P_O - 5 - \dfrac{f}{400 \times S} & 400 \times S < f \le 2000 \times S \\ P_O - \dfrac{f}{200 \times S} & 2000 \times S < f \le 3000 \times S \end{array} \right\} \mathrm{dBm/Hz} \qquad (201\text{–}10)$$

where

P_O is equal to -90 dBm/Hz for -T1
P_O is equal to -93 dBm/Hz for -V1
f is the frequency in MHz

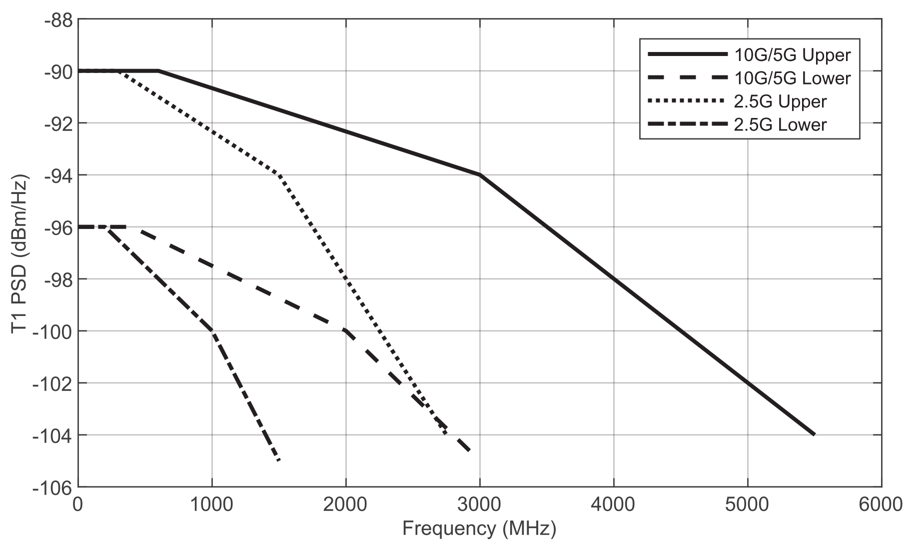

Figure 201–43—T1 MultiG Transmitter Power Spectral Density, upper and lower masks

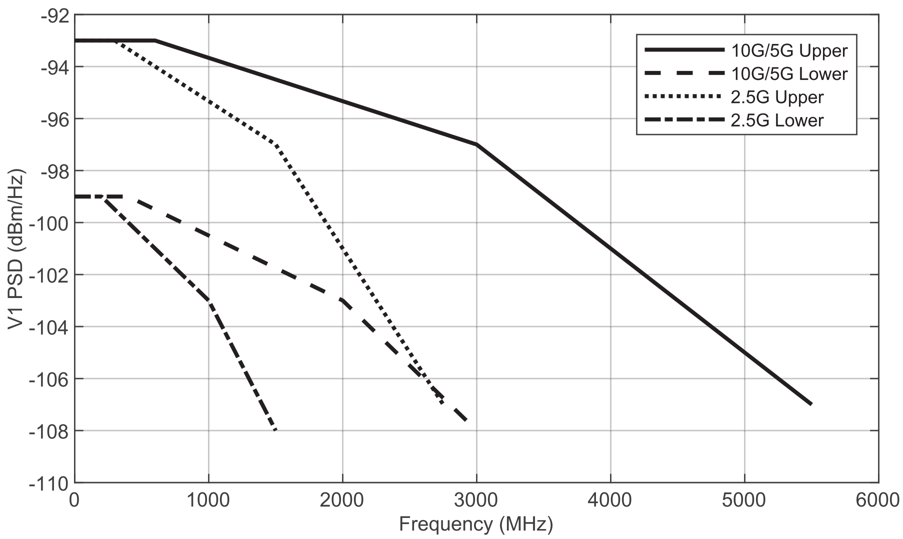

Figure 201–44—V1 MultiG Transmitter Power Spectral Density, upper and lower masks

201.6.2.7 Transmitter peak output

~~The~~ In test mode 5 (normal operation), the transmit signal of a MultiG+100MBASE-T1 transmitter measured ~~differentially~~ using test fixture 4, shown in Figure 201–41, with a 100 Ω ~~termination~~load for -T1 and shown in Figure 201–42, ~~and the single-ended transmit signal of a MultiG+100MBASE-V1 transmitter measured~~ with a 50 Ω ~~termination~~ load for -V1, shall be less than the peak-to-peak limits specified in Table 201–17 at the MDI. These limits apply to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

Table 201–17—Transmit peak-to-peak voltage limits, high speed mode

Transmit Rate	-T1 Max (V)	-V1 Max (V)
10 Gb/s	1.7	0.85
5 Gb/s	1.3	0.65
2.5 Gb/s	1.0	0.5

201.6.2.8 Maximum output droop

With the MultiG+100M-T1/V1 transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the magnitude of both the positive and negative droop shall be less than 30%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 10 ns after the zero crossing (6 ns period).