Table 201–19—MDIO management registers settings for test modes, low speed

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting LEADER and FOLLOWER PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in LEADER mode.
011	Test mode 3—Reserved
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the LEADER data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 3 {+1} baseband symbols followed by 3 {–1} symbols. These symbols are transmited with no Manchester encoding, generating a square wave with a period of 51.2 ns. The transmit symbols are timed from a free-running local clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the 100M+MultiGBASE-T1/V1 normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

201.7.1.1 Test fixtures

The test fixtures in 201.6.1.1 are defined for measuring the transmitter specifications for data communication only.

201.7.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 201.5.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high dc common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single-ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

201.7.2.1 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both LEADER and FOLLOWER configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 201–38. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than J ps. The peak-to-peak value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than $10 \times J$ ps. See Table 201–14 for the definition of J.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 50 ps. The peak-to-peak value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 500 ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

201.7.2.2 Transmit MDI random jitter in LEADER mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with a square wave pattern and using test fixture 3 as shown in Figure 201–39 for -T1 and Figure 201–40 for -V1. The square wave pattern is generated by transmitting constant 0 values as the input to the differential Manchester encoder. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than J ps. See Table 201–14 for the definition of J. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than $10 \times J$ ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

201.7.2.3 Transmit MDI deterministic jitter in LEADER mode

This test is not defined for the LS_PATH.

201.7.2.4 Transmitter clock frequency

The baseband symbol transmission rate of the LEADER PHY (prior to Manchester encoding) shall be within the range $5625/48$ MHz ± 100 ppm. The transmitter clock frequency can be measured at the MDI using test mode 2.

201.7.2.5 Transmitter Rise and Fall Time

The transmitter rise and fall time requirements specified in this subclause apply when the PHY_D is used to provide a reference clock for XTAL-less operation of PHY_S. Limiting the transmitter transition times reduces deterministic jitter of the derived reference at the receiving PHY.

The rise/fall transition time between 20% and 80% levels of the steady state voltage amplitude shall be less than 1.5 ns. The rise time and fall time is defined as measured at the MDI using ~~Test~~ test mode 2.

201.7.2.6 Transmitter linearity

With the transmitter in test mode 4, transmitting in ~~100M~~ 100 Mb/s mode, and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the transmit signal is captured per 85.8.3.3.4 with a minimum of M=14. The effective transmit baseband symbols, $x(n)$, is derived by noting that differential Manchester encoding includes an implicit nonlinear mapping. This nonlinear operation maps the transmitted PRBS13 bits d_{in} to another set of pseudo-random bits d_{out}, which in turn maps to the implicit transmit baseband symbols $x(n)$ according to Table 201–20.

Table 201–20—PRBS13 mapping table

Transmit Bits	Encoded Bits		Baseband Symbols
	previous	current	
$d_{in}(n)$=**PRBS13**	$d_{in}(n\text{-}1)$	$d_{in}(n)$	$x(n)$
0	0	1	-1
0	1	0	+1
1	0	0	-1
1	1	1	+1

Given the implicit transmit symbols $x(n)$, and the captured waveform $y(k)$, compute the linear fit pulse response $p(k)$ and the standard deviation of linear fit error $e(k)$ according to 85.8.3.3.5 and using N_p=100 and D_p=2.

The transmitter SNDR distortion is defined as: $\mathrm{SNDR} = 10\log_{10}\left(\frac{\sigma_p^2}{\sigma_e^2 + \sigma_n^2}\right)$

Where $\sigma_p^2 = \frac{1}{M}\sum_k p^2(\mathrm{k})$, and σ_e and σ_n are the standard deviation of $e(k)$ and noise, respectively.

The transmitter SNDR distortion shall exceed 30 dB.

201.7.2.7 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the 100M+MultiGBASE-T1/V1 PHYs shall be as specified in Table 201–21 and the power spectral density of the transmitter shall be between the upper and lower masks specified in Equation (201–11) and Equation (201–12). The PSD and power are measured using test fixture 4, shown in Figure 201–41, with a 100 Ω load for -T1 and shown in Figure 201–42, with a 50 Ω load for -V1. The upper and lower masks are shown in Figure 201–47 for -T1 and in Figure 201–49 for -V1. When tx_symb is “Z” the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm.

Table 201–21—Transmit Power, low speed mode

	Transmit power, -T1		Transmit power, -V1	
Transmit Rate	**Min (dBm)**	**Max (dBm)**	**Min (dBm)**	**Max (dBm)**
100M	-3	0	-6	-3

$$\mathrm{UpperPSD}(f) = \left\{\begin{array}{ll} P_O & 3 < f < 150 \\ P_O + 15 - \dfrac{f}{10} & 150 < f \le 260 \\ P_O - 11 & 260 < f \le 3500 \end{array}\right\} \mathrm{dBm/HZ} \qquad (201\text{–}11)$$

$$\mathrm{LowerPSD}(f) = \left\{\begin{array}{ll} P_O - 6 - \dfrac{90-f}{3} & 45 < f \le 90 \\ P_O - 6 - \dfrac{f-90}{4} & 90 < f \le 150 \end{array}\right\} \mathrm{dBm/HZ} \qquad (201\text{–}12)$$

where

P_O	is equal to –79 dBm/Hz for -T1
P_O	is equal to –82 dBm/Hz for -V1
f	is the frequency in MHz

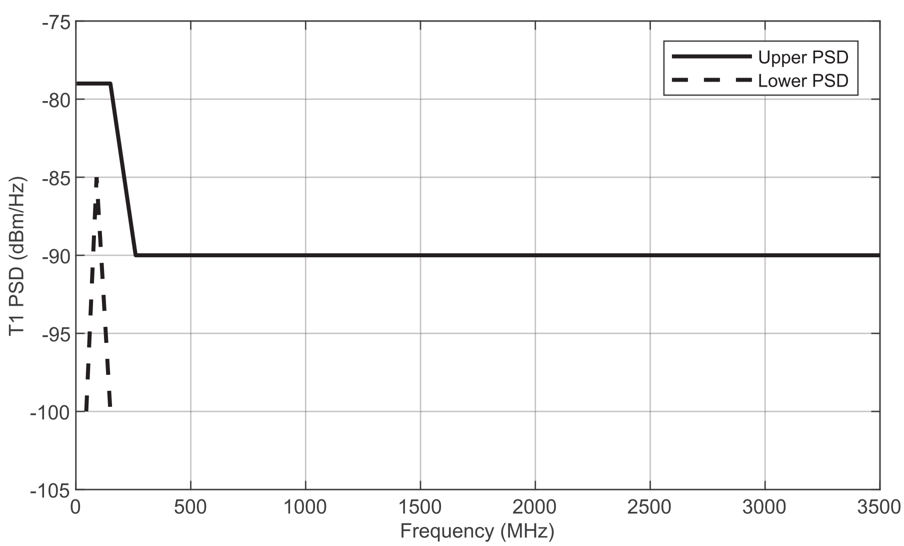

Figure 201–47—T1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

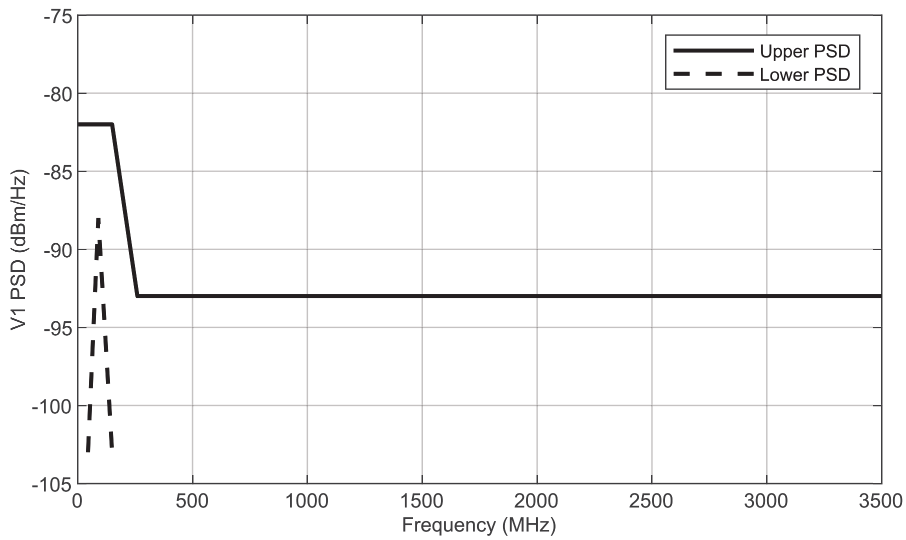

Figure 201–48—V1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

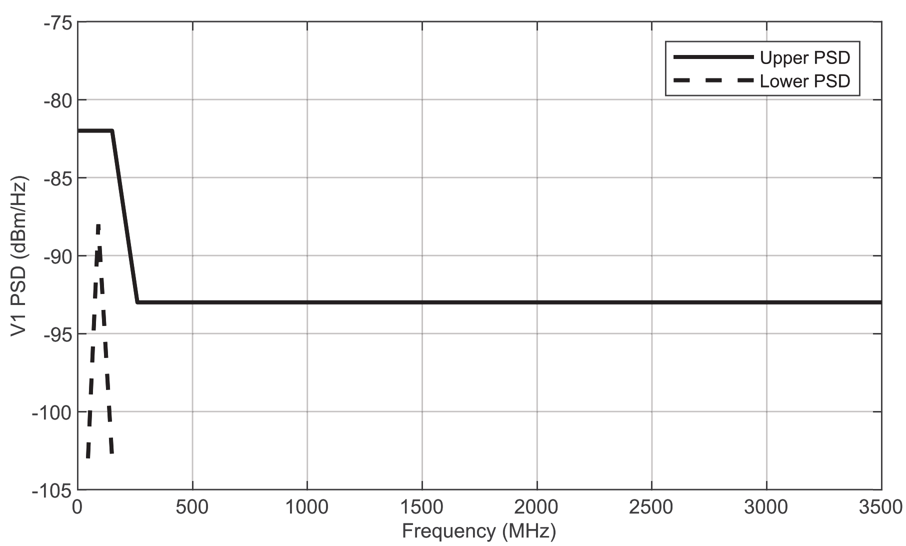

Figure 201–49—V1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

201.7.2.8 Transmitter peak output

When transmitting at a data rate of 100 Mb/s and measured using the -T1 test fixture 4, shown in Figure 201–41, with a 100 Ω ~~termination~~load, the differential transmit signal of a 100M+MultiGBASE-T1 transmitter shall be less than 1.0 V peak-to-peak at the MDI. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N~~.~~.

When transmitting at a data rate of 100 Mb/s and measured using the -V1 test fixture 4, shown in Figure 201–42, with a 50 ~~Ω termination~~Ω load, the transmit signal shall be less than 0.5 V peak-to-peak at the MDI. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

The transmitter peak output voltage can be measured at the MDI using test mode 5.

201.7.2.9 Maximum output droop

With the 100M+MultiGBASE-T1/V1 transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the magnitude of both the positive and negative droop shall be less than 30%, measured with respect to an initial value at 8 ns after the zero crossing and a final value at 14 ns after the zero crossing (6 ns period).

201.7.3 Receiver electrical specifications

The receiver electrical specifications for the low speed mode are specified in 201.6.3.

The broadband stationary noise rejection level is as specified in Table 201–22.

Table 201–22—Broadband stationary noise rejection, low speed

		Added noise at MDI (dBm/Hz)	
PHY type	**Noise bandwidth (MHz)**	**-T1**	**-V1**
100M+MultiGBASE	150	-126	-129

201.7.4 MDI

The MDI for the low speed mode is specified in 201.6.4.

201.8 Management interface

201.8.1 Support for Auto-Negotiation

MultiG+100M/100M+MultiGBASE-T1 PHYs optionally provide support for Auto-Negotiation. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

MultiG+100M/100M+MultiGBASE-V1 PHYs do not support Auto-Negotiation.

Auto-Negotiation, when implemented and enabled, is performed as part of the initial set-up of the link and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for MultiG+100M/100M+MultiGBASE-T1:

a) To negotiate which PHY types, including speed and direction, can be supported,
b) To determine the LEADER-FOLLOWER relationship between the PHYs at each end of the link.