IEEE P802.3dm™/D0.c

Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet

Prepared by the

LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2022 as amended by IEEE Std 802.3yy-20xx. The purpose of the amendment is to add Physical Layer (PHY) specifications and management parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation in one direction and 100 Mb/s operation in the other direction on automotive cabling in an automotive environment. Draft D0.c is prepared for Task Force review. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2022 adds Physical Layer (PHY) specifications and management parameters for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation in one direction and 100 Mb/s operation in the other direction on automotive cabling in an automotive environment.

Keywords: automotive Ethernet, 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1, IEEE 802.3dm™

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Participants

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Jon Lewis, *IEEE 802.3 Working Group Secretary*
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Introduction

This introduction is not part of IEEE Std 802.3dm-20xx, IEEE Draft Standard for Ethernet. Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. "Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications" was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3dm-202x publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

IEEE Std 802.3cy™-2023

Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and Annex 165A. This amendment adds Physical Layer specifications and management parameters for operation at 25 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3df™-2024

Amendment 9—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment includes Physical Layer specifications and management parameters for 400 Gb/s and 800 Gb/s operation.

IEEE Std 802.3-2022/Cor 1-2024

Corrigendum 1—This corrigendum includes changes to IEEE Std 802.3-2022 to correct the MDI return loss specifications in Clause 149 and Clause 165.

IEEE Std 802.3da™-2026

Amendment 10—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 188 through Clause 189. This amendment adds Physical Layer specifications and management parameters for enhancement of multidrop 10 Mb/s operation based on the 10BASE-T1S PHY specified in Clause 147 of IEEE Std 802.3-2022, and specifies optional provision of power over single balanced pair mixing segments. Additionally, this amendment includes additions and changes to Clause 148 to automatically allocate node IDs (Dynamic PLCA).

IEEE Std 802.3dk™-202x

Amendment 11—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 168. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s Ethernet optical interfaces for bidirectional operation over a single strand of single-mode fiber.

IEEE Std 802.3dg™-202x

Amendment 12—This amendment to IEEE Std 802.3-2022 specifies additions and appropriate modifications to add 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation, and associated optional provision of power, over a single balanced pair of conductors.

IEEE Std 802.3dm™-20xx

This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 200. This amendment adds Physical Layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation in one direction and 100 Mb/s operation in the other direction over a single balanced pair of conductors, or over a single coaxial cable.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

Contents

Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet

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Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

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1. Introduction

1.3 Normative references

Insert the following references in alphanumeric order:

ISO 19642–11:2023, Road vehicles—Automotive cables—Part 11: Dimensions and requirements for coaxial RF cables with a specified analogue bandwidth up to 6 GHz (20 GHz).

1.4 Definitions

Insert the following new definitions after 1.4.46 100 Gb/s Parallel Physical Interface (CPPI):

1.4.46a 100M+10GBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 10 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 201.)

1.4.46b 100M+10GBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 10 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 201.)

1.4.46c 100M+2.5GBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 2.5 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 201.)

1.4.46d 100M+2.5GBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 2.5 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 201.)

1.4.46e 100M+5GBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 5 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 201.)

1.4.46f 100M+5GBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 5 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 201.)

1.4.46g 100M+MultiGBASE: PHYs that belong to the set of specific asymmetric PHYs that transmit at 100 Mb/s and receive at speeds in excess of 1000 Mb/s, with concurrent transmission in both directions, including 100M+2.5GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-T1, 100M+5GBASE-V1, 100M+10GBASE-T1, and 100M+10GBASE-V1. (See IEEE Std 802.3, Clause 201.)

Insert the following new definitions after 1.4.62 10BROAD36:

1.4.62a 10G+100MBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 10 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 201.)

1.4.62b 10G+100MBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 10 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 201.

Change 1.4.88 as follows:

1.4.88 10 Gigabit Media Independent Interface (XGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation (including asymmetric PHYs with 100 Mb/s in the reverse direction). (See IEEE Std 802.3, Clause 46.)

Insert the following new definitions after 1.4.95 1G-EPON:

1.4.95a 2.5G+100MBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 2.5 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 201.)

1.4.95b 2.5G+100MBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 2.5 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 201.)

Insert the following new definitions after 1.4.178 50G-EPON:

1.4.178a 5G+100MBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 5 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 201.)

1.4.178b 5G+100MBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 5 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 201.)

Change 1.4.249 as follows:

1.4.249 coaxial cable interface: The electrical and mechanical interface to the ~~shared~~ coaxial cable medium either contained within or connected to the Medium Attachment Unit (MAU). Also known as the Medium Dependent Interface (MDI).

Insert the following new definitions after 1.4.405c* Multidrop Power Sourcing Equipment (MPSE*) (as modified by IEEE Std 802.3da-2026):

1.4.249a MultiG+100MBASE: PHYs that belong to the set of specific asymmetric PHYs that transmit at speeds in excess of 1000 Mb/s and receive at 100 Mb/s, with concurrent transmission in both directions, including 2.5G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-T1, 5G+100MBASE-V1, 10G+100MBASE-T1, and 10G+100MBASE-V1. (See IEEE Std 802.3, Clause 201.)

1.4.405b MultiGBASE-A: PHYs that belong to the set of specific asymmetric PHYs at speeds in excess of 1000 Mb/s in one direction and less than 1000 Mb/s in the other direction, including MultiGBASE-AT1 and MultiGBASE-AV1. (See IEEE Std 802.3, Clause 202.)

1.4.405c MultiGBASE-AT1: IEEE 802.3 Physical Layer specification for an asymmetric rate Ethernet full duplex point-to-point link operating at 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s in the other direction over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 202.)

1.4.405d MultiGBASE-AV1: IEEE 802.3 Physical Layer specification for an asymmetric rate Ethernet full duplex point-to-point link operating at 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s in the other direction over a single coaxial conductor. (See IEEE Std 802.3, Clause 202.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

ACT	Asymmetric Concurrent Transmission
TDD	Time Division Duplex

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "2.5GBASE-T1" as follows:

2.5G+100MBASE-T1/V1	Clause 201 2.5 Gb/s PAM2 transmit, 100 Mb/s DME receive
100M+2.5GBASE-T1/V1	Clause 201 100 Mb/s DME transmit, 2.5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "5GBASE-T1" as follows:

5G+100MBASE-T1/V1	Clause 201 5 Gb/s PAM2, 100 Mb/s DME receive
100M+5GBASE-T1/V1	Clause 201 100 Mb/s DME transmit, 5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "10GBASE-T1" as follows:

10G+100MBASE-T1/V1	Clause 201 10 Gb/s PAM4, 100 Mb/s DME receive
100M+10GBASE-T1/V1	Clause 201 100 Mb/s DME transmit, 10 Gb/s PAM4 receive

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "400GBASE-R" as follows:

MultiGBASE-A LS_PATH	Clause 202 MultiG PAM2 or PAM4 HS_PATH, 100 Mb/s PAM2

30.3.2.1.3 aPhyTypeList

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "2.5GBASE-T1" as follows:

2.5G+100MBASE-T1/V1	Clause 201 2.5 Gb/s PAM2 transmit, 100 Mb/s DME receive
100M+2.5GBASE-T1/V1	Clause 201 100 Mb/s DME transmit, 2.5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "5GBASE-T1" as follows:

5G+100MBASE-T1/V1	Clause 201 5 Gb/s PAM2, 100 Mb/s DME receive
100M+5GBASE-T1/V1	Clause 201 100 Mb/s DME transmit, 5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "10GBASE-T1" as follows:

10G+100MBASE-T1/V1	Clause 201 10 Gb/s PAM4, 100 Mb/s DME receive
100M+10GBASE-T1/V1	Clause 201 100 Mb/s DME transmit, 10 Gb/s PAM4 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "400GBASE-R" as follows:

MultiGBASE-A LS_PATH	Clause 202 MultiG PAM2 or PAM4 HS_PATH, 100 Mb/s PAM2

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "2.5GBASE-T1" as follows:

2.5G+100MBASE-T1	Single balanced pair of conductors PHY as specified in Clause 201
100M+2.5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 201
2.5G+100MBASE-V1	Coaxial Cable PHY as specified in Clause 201
100M+2.5GBASE-V1	Coaxial Cable PHY as specified in Clause 201

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "5GBASE-T1" as follows:

5G+100MBASE-T1	Single balanced pair of conductors PHY as specified in Clause 201
100M+5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 201
5G+100MBASE-V1	Coaxial Cable PHY as specified in Clause 201
100M+5GBASE-V1	Coaxial Cable PHY as specified in Clause 201

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "10GBASE-T1" as follows:

10G+100MBASE-T1	Single balanced pair of conductors PHY as specified in Clause 201
100M+10GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 201

10G+100MBASE-V1	Coaxial Cable PHY as specified in Clause 201
100M+10GBASE-V1	Coaxial Cable PHY as specified in Clause 201

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "802.9a" as follows:

MultiGBASE-AT1	Single balanced pair of conductors PHY as specified in Clause 202
MultiGBASE-AV1	Coaxial Cable PHY as specified in Clause 202

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "2.5GBASE-T1" as follows:

2.5G+100MBASE-T1	2.5G+100MBASE-T1 as specified in Clause 201
100M+2.5GBASE-T1	100M+2.5GBASE-T1 as specified in Clause 201
2.5G+100MBASE-V1	2.5G+100MBASE-V1 as specified in Clause 201
100M+2.5GBASE-V1	100M+2.5GBASE-V1 as specified in Clause 201

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "5GBASE-T1" as follows:

5G+100MBASE-T1	5G+100MBASE-T1 as specified in Clause 201
100M+5GBASE-T1	100M+5GBASE-T1 as specified in Clause 201
5G+100MBASE-V1	5G+100MBASE-V1 as specified in Clause 201
100M+5GBASE-V1	100M+5GBASE-V1 as specified in Clause 201

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "10GBASE-T1" as follows:

10G+100MBASE-T1	10G+100MBASE-T1 as specified in Clause 201
100M+10GBASE-T1	100M+10GBASE-T1 as specified in Clause 201
10G+100MBASE-V1	10G+100MBASE-V1 as specified in Clause 201
100M+10GBASE-V1	100M+10GBASE-V1 as specified in Clause 201

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the reserved row for 1.77 through 1.79 in Table 45-3 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, and IEEE Std 802.3dj-20xx) and change the reserved row for 1.2318 throug 1.2400 (as modified by IEEE Std 802.3dj-20xx) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
…		
1.77	Asymmetrical BASE-T1/V1 PMA/PMD extended ability	45.2.1.60f
1.~~77~~78 through 1.79	Reserved	
…		
1.2318	MultiGBASE-A PMA rate ability	45.2.1.250a
1.2319	MultiGBASE-A PMA rate negotiation	45.2.1.250b
1.2320	MultiGBASE-A PMA link partner rate negotiation	45.2.1.250c
1.2321 through 1.2400 ~~1.2318 through 1.2400~~		
…		

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45-7 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, and IEEE Std 802.3dj-20xx) as follows (unchanged table rows and most unchanged bit description lines not shown):.

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.7.~~7~~6:0	PMA/PMD type selection	7 6 5 4 3 2 1 0 … 0 0 1 1 1 1 0 1 = BASE-T1/V1 PMA/PMD[b] …	R/W
…			

[a]R/W = Read/Write, RO = Read only.
[b]If BASE-T1/V1 is selected, bits 1.2100.~~3~~4:0 are used to differentiate which BASE-T1/V1 PMA/PMD is selected.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert new rows in Table 45-9 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows (unchanged rows not shown):

Table 45–9—Transmit fault description location

PMA/PMD	Description location
…	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	201.5.2.2
100M+2.5GBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-V1, 100M+10GBASE-V1	201.5.2.2
…	

45.2.1.7.5 Receive fault (1.8.10)

Insert new rows in Table 45-10 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows and insert a new row at the end of the table(unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
…	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	201.5.2.3
100M+2.5GBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-V1, 100M+10GBASE-V1	201.5.2.3
…	
MultiGBASE-AT1, MultiGBASE-AV1	202.4.2.3

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Change the row for 1.11.11 in Table 45-19 as follows (unchanged rows not shown.):

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.11.11	BASE-T1/V1 extended abilities	1 = PMA/PMD has BASE-T1/V1 extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1/V1 extended abilities	RO
…			

[a]RO = Read only.

Change the title of 45.2.10.5 and the text as follows:

45.2.1.10.5 BASE-T1/V1 extended abilities (1.11.11)

When read as a one, bit 1.11.11 indicates that the PMA/PMD has BASE-T1/V1 extended abilities listed in register 1.18. When read as a zero, bit 1.11.11 indicates that the PMA/PMD does not have BASE-T1/V1 extended abilities.

Change the title of the following subsection as shown:

45.2.1.16 BASE-T1/V1 PMA/PMD extended ability register (1.18)

Change the title of the Table 45-19 and change row 2 and insert new row 3 (as modified by IEEE Std 802.3cy-2023, IEEE Std 802.3da-2026, and IEEE Std 802.3dg-202x) as follows (unchanged rows not shown)

Table 45–19—BASE-T1/V1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.18.15:13 ~~7~~	Reserved	Value always 0	RO
1.18.12	MultiGBASE-AT1 ability	1 = PMA/PMD is able to perform MultiGBASE-AT1 0 = PMA/PMD is not able to perform MultiGBASE-AT1	RO
1.18.11	MultiGBASE-AV1 abil-ity	1 = PMA/PMD is able to perform MultiGBASE-AV1 0 = PMA/PMD is not able to perform MultiGBASE-AV1	RO
1.18.10	MultiG+100M/ 100M+MultiGBASE-T1/V1 ability	1 = PMA/PMD is able to perform MultiG+100M/100M+MultiGBASE-V1 ability 0 = PMA/PMD is able to perform MultiG+100M/100M+MultiGBASE-T1	RO
…			

[a]RO = Read only.

Insert 45.2.1.16.aaaa before 45.2.1.16.aaa (as inserted by IEEE Std 802.3dg-202x) as follows:

45.2.1.16.aaaa MultiGBASE-AT1 ability (1.18.12)

When read as a one, bit 1.18.12 indicates that the PMA/PMD is able to operate as a MultiGBASE-AT1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.12 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AT1 PMA/PMD type as indicated in register 1.77.

45.2.1.16.aaab MultiGBASE-AV1 ability (1.18.11)

When read as a one, bit 1.18.11 indicates that the PMA/PMD is able to operate as a MultiGBASE-AV1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.11 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AV1 PMA/PMD type as indicated in register 1.77.

45.2.1.16.aaac MultiG+100M/100M+MultiGBASE-T1/V1 ability (1.18.10)

When read as a one, bit 1.18.10 indicates that the PMA/PMD is able to operate as a MultiG+100M/100M+MultiGBASE-V1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.10 indicates that the PMA/PMD is able to operate as a MultiG+100M/100M+MultiGBASE-T1 PMA/PMD type as indicated in register 1.77.

Insert 45.2.1.60f after 45.2.1.60e (as inserted by IEEE Std 802.3df-202x) as follows:

45.2.1.60f Asymmetric PMA/PMD extended ability register (Register 1.77)

The assignment of bits in the Asymmetric PMA/PMD extended ability register is shown in Table 45–58f.

Table 45–58f—Asymmetric PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.77.15:14	Reserved	Value always 0	RO
1.77.13	MultiGBASE-AV1 ability	1 = PMA/PMD is able to perform MultiGBASE-AV1 0 = PMA/PMD is not able to perform MultiGBASE-AV1	RO
1.77.13	MultiGBASE-AT1 ability	1 = PMA/PMD is able to perform MultiGBASE-AT1 0 = PMA/PMD is not able to perform MultiGBASE-AT1	RO
1.77.11	10G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-V1 0 = PMA/PMD is not able to perform 10G+100MBASE-V1	RO
1.77.10	100M+10GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-V1 0 = PMA/PMD is not able to perform 100M+10GBASE-V1	RO
1.77.9	10G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-T1 0 = PMA/PMD is not able to perform 10G+100MBASE-T1	RO
1.77.8	100M+10GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-T1 0 = PMA/PMD is not able to perform 100M+10GBASE-T1	RO
1.77.7	5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-V1 0 = PMA/PMD is not able to perform 5G+100MBASE-V1	RO
1.77.6	100M+5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-V1 0 = PMA/PMD is not able to perform 100M+5GBASE-V1	RO
1.77.5	5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-T1 0 = PMA/PMD is not able to perform 5G+100MBASE-T1	RO
1.77.4	100M+5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-T1 0 = PMA/PMD is not able to perform 100M+5GBASE-T1	RO

Table 45–58f—Asymmetric PMA/PMD extended ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.77.3	2.5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-V1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-V1	RO
1.77.2	100M+2.5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-V1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-V1	RO
1.77.1	2.5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-T1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-T1	RO
1.77.0	100M+2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-T1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-T1	RO

[a]R/W = Read/Write, RO = Read only

45.2.1.60f.1 MultiGBASE-AV1 (1.77.13)

When read as a one, bit 1.77.13 indicates that the PMA/PMD is able to operate as a MultiGBASE-AV1 PMA/PMD type.

When read as a zero, bit 1.77.13 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AV1 PMA/PMD type.

45.2.1.60f.2 MultiGBASE-AT1 (1.77.12)

When read as a one, bit 1.77.12 indicates that the PMA/PMD is able to operate as a MultiGBASE-AT1 PMA/PMD type.

When read as a zero, bit 1.77.12 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AT1 PMA/PMD type.

45.2.1.60f.3 10G+100MBASE-V1 (1.77.11)

When read as a one, bit 1.77.11 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.11 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-V1 PMA/PMD type.

45.2.1.60f.4 100M+10GBASE-V1 (1.77.10)

When read as a one, bit 1.77.10 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.10 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-V1 PMA/PMD type.

45.2.1.60f.5 10G+100MBASE-T1 (1.77.9)

When read as a one, bit 1.77.9 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.9 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-T1 PMA/PMD type.

45.2.1.60f.6 100M+10GBASE-T1 (1.77.8)

When read as a one, bit 1.77.8 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.8 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-T1 PMA/PMD type.

45.2.1.60f.7 5G+100MBASE-V1 (1.77.7)

When read as a one, bit 1.77.7 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.7 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-V1 PMA/PMD type.

45.2.1.60f.8 100M+5GBASE-V1 (1.77.6)

When read as a one, bit 1.77.6 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.6 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-V1 PMA/PMD type.

45.2.1.60f.9 5G+100MBASE-T1 (1.77.5)

When read as a one, bit 1.77.5 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.5 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-T1 PMA/PMD type.

45.2.1.60f.10 100M+5GBASE-T1 (1.77.4)

When read as a one, bit 1.77.4 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.4 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-T1 PMA/PMD type.

45.2.1.60f.11 2.5G+100MBASE-V1 (1.77.3)

When read as a one, bit 1.77.3 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.3 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-V1 PMA/PMD type.

45.2.1.60f.12 100M+2.5GBASE-V1 (1.77.2)

When read as a one, bit 1.77.2 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.2 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-V1 PMA/PMD type.

45.2.1.60f.13 2.5G+100MBASE-T1 (1.77.1)

When read as a one, bit 1.77.1 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.1 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-T1 PMA/PMD type.

45.2.1.60f.14 100M+2.5GBASE-T1 (1.77.0)

When read as a one, bit 1.77.0 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.0 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-T1 PMA/PMD type.

Change the title of the following subsection as shown:

45.2.1.214 BASE-T1/V1 PMA/PMD control register (Register 1.2100)

Change the title of the following table as shown. Replace the rows for bits 1.2100.13:4 and 1.2100.3:0 in Table 45–178 (as modified by IEEE Std 802.3cy-2023 and IEEE Std 802.3da-2026) as follows (unchanged rows not shown):

Change the subclause title and first sentence of 45.2.1.214.2 (as modified by IEEE Std 802.3da-2026) as follows:

45.2.1.214.2 Type selection (1.2100.4:0) ~~(1.2100.3:0)~~

Bits 1.2100.4:0 ~~1.2100.3:0~~ are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented.

Table 45–178—BASE-T1/V1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W[a]
…			
1.2100.13:5	Reserved	Value always 0	RO
1.2100.4:0	Type Selection	4 3 2 1 0 1 1 1 1 1 = MultiGBASE-AV1 1 1 1 1 0 = MultiGBASE-AT1 1 1 1 0 x = Reserved 1 1 0 1 1 = 10G+100MBASE-V1 1 1 0 1 0 = 100M+10GBASE-V1 1 1 0 0 1 = 10G+100MBASE-T1 1 1 0 0 0 = 100M+10GBASE-T1 1 0 1 1 1 = 5G+100MBASE-V1 1 0 1 1 0 = 100M+5GBASE-V1 1 0 1 0 1 = 5G+100MBASE-T1 1 0 1 0 0 = 100M+5GBASE-T1 1 0 0 1 1 = 2.5G+100MBASE-V1 1 0 0 1 0 = 100M+2.5GBASE-V1 1 0 0 0 1 = 2.5G+100MBASE-T1 1 0 0 0 0 = 100M+2.5GBASE-T1 0 1 1 x x = Reserved 0 1 0 1 x = Reserved 0 1 0 0 1 = Reserved 0 1 0 0 0 = 10BASE-T1M 0 0 1 1 1 = 25GBASE-T1 0 0 1 1 0 = 10GBASE-T1 0 0 1 0 1 = 5GBASE-T1 0 0 1 0 0 = 2.5GBASE-T1 0 0 0 1 1 = 10BASE-T1S 0 0 0 1 0 = 10BASE-T1L 0 0 0 0 1 = 1000BASE-T1 0 0 0 0 0 = 100BASE-T1	R/W

[a]R/W = Read/Write, RO = Read only

Insert the following new subclauses and tables after 45.2.1.250 and before 45.2.1.251 (as inserted by IEEE Std 802.3dj-202x) as follows:

45.2.1.250a MultiGBASE-A PMA rate ability (Register 1.2318)

The assignment of bits in the MultiGBASE-A PMA rate ability register is shown in Table 45–212a.

Table 45–212a—MultiGBASE-A PMA rate ability register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2318.15	MultiGBASE-A PHY_D 10 Gb/s RX ability	1 = PHY has MultiGBASE-A PHY_D 10 Gb/s RX ability 0 = PHY does not have MultiGBASE-A PHY_D 10 Gb/s RX ability	RO
1.2318.14	Reserved	Value always 0	RO
1.2318.13	MultiGBASE-A PHY_D 5 Gb/s RX ability	1 = PHY has MultiGBASE-A PHY_D 5 Gb/s RX ability 0 = PHY does not have MultiGBASE-A PHY_D 5 Gb/s RX ability	RO

Table 45–212a—MultiGBASE-A PMA rate ability register bit definitions *(continued)*

Bit(s)	Name	Description	R/W[a]
1.2318.12	MultiGBASE-A PHY_D 2.5 Gb/s RX ability	1 = PHY has MultiGBASE-A PHY_D 2.5 Gb/s RX ability 0 = PHY does not have MultiGBASE-A PHY_D 2.5 Gb/s RX ability	RO
1.2318.11:9	Reserved	Value always 0	RO
1.2318.8	MultiGBASE-A PHY_D 100 Mb/s TX ability	1 = PHY has MultiGBASE-A PHY_D 100 Mb/s TX ability 0 = PHY does not have MultiGBASE-A PHY_D 100 Mb/s TX ability	RO
1.2318.7	MultiGBASE-A PHY_S 10 Gb/s TX ability	1 = PHY has MultiGBASE-A PHY_S 10 Gb/s TX ability 0 = PHY does not have MultiGBASE-A PHY_S 10 Gb/s TX ability	RO
1.2318.6	Reserved	Value always 0	RO
1.2318.5	MultiGBASE-A PHY_S 5 Gb/s TX ability	1 = PHY has MultiGBASE-A PHY_S 5Gb/s TX ability 0 = PHY does not have MultiGBASE-A PHY_S 5Gb/s TX ability	RO
1.2318.4	MultiGBASE-A PHY_S 2.5 Gb/s TX ability	1 = PHY has MultiGBASE-A PHY_S 2.5Gb/s TX ability 0 = PHY does not have MultiGBASE-A PHY_S 2.5Gb/s TX ability	RO
1.2318.3:1	Reserved	Value always 0	RO
1.2318.0	MultiGBASE-A PHY_S 100 Mb/s RX ability	1 = PHY has MultiGBASE-A PHY_S 100 Mb/s RX ability 0 = PHY does not have MultiGBASE-A PHY_S 100 Mb/s RX ability	RO

[a]RO = Read only.

45.2.1.250a.1 MultiGBASE-A PHY_D 10 Gb/s RX ability (1.2318.15)

When read as a one, bit 1.2318.15 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 10 Gb/s. When read as a zero, bit 1.2318.15 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 10 Gb/s.

45.2.1.250a.2 MultiGBASE-A PHY_D 5 Gb/s RX ability (1.2318.13)

When read as a one, bit 1.2318.13 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 5 Gb/s. When read as a zero, bit 1.2318.13 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 5 Gb/s.

45.2.1.250a.3 MultiGBASE-A PHY_D 2.5 Gb/s RX ability (1.2318.12)

When read as a one, bit 1.2318.12 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.12 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 2.5 Gb/s.

45.2.1.250a.4 MultiGBASE-A PHY_D 100 Mb/s TX ability (1.2318.8)

When read as a one, bit 1.2318.8 indicates that the PHY supports operating in PHY_D mode at a transmit data rate of 100 Mb/s. When read as a zero, bit 1.2318.8 indicates that the PHY does not support operating in PHY_D mode at a transmit data rate of 100 Mb/s.

45.2.1.250a.5 MultiGBASE-A PHY_S 10 Gb/s TX ability (1.2318.7)

When read as a one, bit 1.2318.7 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 10 Gb/s. When read as a zero, bit 1.2318.7 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 10 Gb/s.

45.2.1.250a.6 MultiGBASE-A PHY_S 5 Gb/s TX ability (1.2318.5)

When read as a one, bit 1.2318.5 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 5 Gb/s. When read as a zero, bit 1.2318.5 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 5 Gb/s.

45.2.1.250a.7 MultiGBASE-A PHY_S 2.5 Gb/s TX ability (1.2318.4)

When read as a one, bit 1.2318.4 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.4 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 2.5 Gb/s.

45.2.1.250a.8 MultiGBASE-A PHY_S 100 Mb/s RX ability (1.2318.0)

When read as a one, bit 1.2318.0 indicates that the PHY supports operating in PHY_S mode at a receive data rate of 100 Mb/s. When read as a zero, bit 1.2318.0 indicates that the PHY does not support operating in PHY_S mode at a receive data rate of 100 Mb/s.

45.2.1.250b MultiGBASE-A PMA rate negotiation (Register 1.2319)

The assignment of bits in the MultiGBASE-A PMA supported rates register is shown in Table 45–212a.

Table 45–212b—MultiGBASE-A PMA rate negotiation register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2319.15:6	Reserved	Value always 0	RO
1.2319.5:4	Negotiated PHY_D Transmit rate	5 4 0 0 = Negotiation in progress 0 1 = 100 Mb/s PHY_D TX 1 x = Reserved	R/W
1.2319.3:1	Negotiated PHY_S Transmit rate	3 2 1 0 0 0 = Negotiation in progress 0 0 1 = 2.5 Gb/s PHY_S TX 0 1 0 = 5 Gb/s PHY_S TX 0 1 1 = Reserved 1 0 0 = 10 Gb/s PHY_S TX 1 0 1 = Reserved 1 1 x = Reserved	R/W
1.2319.0	Negotiated Direction	1 = PHY_D requested of FOLLOWER 0 = PHY_S requested of FOLLOWER	R/W

[a]RO = Read only, R/W = Read/Write.

45.2.1.250b.1 Negotiated PHY_D Transmit rate (1.2319.5:4)

When bits 1.2319:5:4 are 00 negotiation of the PHY_D transmit rate is in progress. When bits 1.2319:5:4 are 01 rate negotiation has selected a PHY_D transmit rate as described in Table 45–212b and the LEADER will request the FOLLOWER operate accordingly through Infofield exchange. The same PHY_S receive rate is selected.

45.2.1.250b.2 Negotiated PHY_S Transmit rate (1.2319.3:1)

When bits 1.2319:3:1 are 000 negotiation of the PHY_S transmit rate is in progress. When bits 1.2319:5:4 are not 000 rate negotiation has selected a PHY_S transmit rate as described in Table 45–212b and the LEADER will request the FOLLOWER operate accordingly through Infofield exchange. The same PHY_D receive rate is selected.

45.2.1.250b.3 Negotiated Direction (1.2319.0)

When bit 1.2319.0 is 1 the LEADER will operate in PHY_S mode and requests the FOLLOWER operate in PHY_D mode. When bit 1.2319.0 is 0 the LEADER will operate in PHY_D mode and requests the FOLLOWER operate in PHY_S mode

45.2.1.250c MultiGBASE-A PMA link partner rate negotiation (Register 1.2320)

The assignment of bits in the MultiGBASE-A PMA link partner rate negotiation register is shown in Table 45–212c.

Table 45–212c—MultiGBASE-A PMA link partner rate negotiation register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2320.15	Link partner PHY_D 10 Gb/s RX ability	1 = Link partner has MultiGBASE-A PHY_D 10 Gb/s RX ability 0 = Link partner does not have MultiGBASE-A PHY_D 10 Gb/s RX ability	RO
1.2320.14	Reserved	Value always 0	RO
1.2320.13	Link partner PHY_D 5 Gb/s RX ability	1 = Link partner has MultiGBASE-A PHY_D 5 Gb/s RX ability 0 = Link partner does not have MultiGBASE-A PHY_D 5 Gb/s RX ability	RO
1.2320.12	Link partner PHY_D 2.5 Gb/s RX ability	1 = Link partner has MultiGBASE-A PHY_D 2.5 Gb/s RX ability 0 = Link partner does not have MultiGBASE-A PHY_D 2.5 Gb/s RX ability	RO
1.2320.11:9	Reserved	Value always 0	RO
1.2320.8	Link partner PHY_D 100 Mb/s TX ability	1 = Link partner has MultiGBASE-A PHY_D 100 Mb/s TX ability 0 = Link partner does not have MultiGBASE-A PHY_D 100 Mb/s TX ability	RO
1.2320.7	Link partner PHY_S 10 Gb/s TX ability	1 = Link partner has MultiGBASE-A PHY_S 10 Gb/s TX ability 0 = Link partner does not have MultiGBASE-A PHY_S 10 Gb/s TX ability	RO
1.2320.6	Reserved	Value always 0	RO

Table 45–212c—MultiGBASE-A PMA link partner rate negotiation register bit definitions

Bit(s)	Name	Description	R/W[a]
1.2320.5	Link partner PHY_S 5 Gb/s TX ability	1 = Link partner has MultiGBASE-A PHY_S 5Gb/s TX ability 0 = Link partner does not have MultiGBASE-A PHY_S 5Gb/s TX ability	RO
1.2320.4	Link partner PHY_S 2.5 Gb/s TX ability	1 = Link partner has MultiGBASE-A PHY_S 2.5Gb/s TX ability 0 = Link partner does not have MultiGBASE-A PHY_S 2.5Gb/s TX ability	RO
1.2320.3:1	Reserved	Value always 0	RO
1.2320.0	Link partner PHY_S 100 Mb/s RX ability	1 = Link partner has MultiGBASE-A PHY_S 100 Mb/s RX ability 0 = Link partner does not have MultiGBASE-A PHY_S 100 Mb/s RX ability	RO

[a]RO = Read only.

45.2.1.250c.1 Link partner PHY_D 10 Gb/s RX ability (1.2320.15)

When read as a one, bit 1.2318.15 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 10 Gb/s. When read as a zero, bit 1.2318.15 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 10 Gb/s.

45.2.1.250c.2 Link partner PHY_D 5 Gb/s RX ability (1.2320.13)

When read as a one, bit 1.2318.13 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 5 Gb/s. When read as a zero, bit 1.2318.13 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 5 Gb/s.

45.2.1.250c.3 Link partner PHY_D 2.5 Gb/s RX ability (1.2320.12)

When read as a one, bit 1.2318.12 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.12 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 2.5 Gb/s.

45.2.1.250c.4 Link partner PHY_D 100 Mb/s TX ability (1.2318.8)

When read as a one, bit 1.2318.8 indicates that the link partner supports operating in PHY_D mode at a transmit data rate of 100 Mb/s. When read as a zero, bit 1.2318.8 indicates that the link partner does not support operating in PHY_D mode at a transmit data rate of 100 Mb/s.

45.2.1.250c.5 Link partner PHY_S 10 Gb/s TX ability (1.2320.7)

When read as a one, bit 1.2318.7 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 10 Gb/s. When read as a zero, bit 1.2318.7 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 10 Gb/s.

45.2.1.250c.6 Link partner PHY_S 5 Gb/s TX ability (1.2320.5)

When read as a one, bit 1.2318.5 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 5 Gb/s. When read as a zero, bit 1.2318.5 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 5 Gb/s.

45.2.1.250c.7 Link partner PHY_S 2.5 Gb/s TX ability (1.2320.4)

When read as a one, bit 1.2318.4 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.4 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 2.5 Gb/s.

45.2.1.250c.8 Link partner PHY_S 100 Mb/s RX ability (1.2320.0)

When read as a one, bit 1.2318.0 indicates that the link partner supports operating in PHY_S mode at a receive data rate of 100 Mb/s. When read as a zero, bit 1.2318.0 indicates that the link partner does not support operating in PHY_S mode at a receive data rate of 100 Mb/s.

46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

46.1 Overview

Change the third paragraph of 46.1 as follows:

The RS adapts the bit serial protocols of the MAC to the parallel encodings of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s (including asymmetric) PHYs. Though the XGMII is an optional interface, it is used extensively in this standard as a basis for specification. The 2.5 Gb/s, 5 Gb/s, and 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction) Physical Coding Sublayers (PCS) are specified to the XGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XGMII were implemented.

Change list item "a" in the fourth paragraph of 46.1 as follows:

a) It is capable of supporting at least one of the following rates of operation: 2.5 Gb/s, 5 Gb/s, or 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction).

46.1.1 Summary of major concepts

Change list item "i" in 46.1.1 as follows:

i) The XGMII is rate scalable and may support rates of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction).

46.1.2 Application

Change the second paragraph of 46.1.2 as follows:

This interface is used to provide media independence so that an identical media access controller may be used with all 2.5GBASE, ~~5GBASE, and 10GBASE~~ 100M+2.5GBASE, 2.5G+100MBASE, 5GBASE, 100M+5GBASE, 5G+100MBASE, 10GBASE, 100M+10GBASE, 10G+100MBASE, and MultiGBASE-A PHY types.

46.1.3 Rate of operation

Change the first paragraph of 46.1.3 as follows:

The XGMII supports MAC data rates of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s as defined within this clause. A compliant device may implement any subset of these rates in at least one direction. Symmetric ~~O~~operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35. The XGMII supports a MAC data rate of 100 Mb/s in one direction, for asymmetric operation, when at least one of the specified multigigabit rates is used in the other direction.

46.3 XGMII functional specifications

46.3.1 Transmit

46.3.1.1 TX_CLK (transmit clock)

Change the second paragraph of 46.3.1.1 as follows:

The TX_CLK frequency shall be 1/64 × f_{MAC} ± 100 ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal transmit bit rate.

46.3.2 Receive

46.3.2.1 RX_CLK (receive clock)

Change the second paragraph of 46.3.1.1 as follows:

The frequency of RX_CLK may be derived from the received data or the ~~it may be that of a~~ nominal clock (e.g., TX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be 1/64 × f_{MAC} ± 100 ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal receive bit rate.

46.6 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[3]

46.6.2 Identification

46.6.2.3 Major capabilities/options

Insert new row at end of table (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
ASM	Support of Asymmetric Multigigabit PHYs	46.1.2		O	Yes [ ] No [ ]

46.6.3 PICS proforma tables for Reconciliation Sublayer and 10 Gigabit Media Independent Interface

46.6.3.1 General

[3]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Change PICs items G1, G2, and G3, and insert new row G3a after row G3, as shown (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of 10 Gb/s MAC data rate in at least one direction	46.1.3	Support MAC data rate of 10 Gb/s	PHY:O.1	Yes [ ] N/A [ ]
G2	PHY support of 5 Gb/s MAC data rate in at least one direction	46.1.3	Support MAC data rate of 5 Gb/s	PHY:O.1	Yes [ ] N/A [ ]
G3	PHY support of 2.5 Gb/s MAC data rate in at least one direction	46.1.3	Support MAC data rate of 2.5 Gb/s	PHY:O.1	Yes [ ] N/A [ ]
G3a	Asymmetric support of 100 Mb/s	46.1.3	Support MAC data rate of 100 Mb/s in one direction when at least one of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s is supported in the other direction	ASM:M PHY:O	Yes [ ] N/A [ ]
…					

Change the title of Clause 98 as follows:

98. Auto-Negotiation for single-lane ~~differential-pair~~ media

98.1 Overview

Change the text of 98.1 as follows:

98.1.1 Scope

Clause 98 describes the ~~single-twisted-pair~~ Auto-Negotiation function ~~that allows~~ used on single-lane media to allow a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. Annex 98A describes the Selector Field that is used by Auto-Negotiation to identify the type of message being sent.

The objective of the ~~single-twisted-pair~~ Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. It has the additional objective of providing a common synchronization time between two devices prior to link training.

Single-lane ~~twisted-pair~~ Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC balanced signal. DME does not add packet or upper layer overhead to the network devices. DME is transferred in a half-duplex manner over the media ~~single-twisted-pair copper cable~~.

~~Single-twisted-pair~~ Auto-Negotiation for single-lane media does not test the link segment characteristics.

Single-lane Auto-Negotiation may be used with either differential balanced-pair media or with single-ended unbalanced media.

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The ~~single-twisted-pair~~ Auto-Negotiation function allows the identification of the operational mode of the link partner. Should multiple modes be present, management may select between the various offered modes. How such selection is done is beyond the scope of this standard.

98.1.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The ~~single-twisted-pair~~ Auto-Negotiation function is provided at the Physical Layer of the ISO/IEC OSI reference model as shown in Figure 98–2. A device that supports multiple modes of operation may advertise its capabilities using the ~~single-twisted-pair~~ Auto-Negotiation function. The actual transfer of information is observed only at the MDI.

98.2 Functional specifications

Change the text of 98.2 as follows (unchanged text and figures not shown):

The ~~single twisted-pair~~ Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PHY type, where more than one PHY type may exist. A management interface provides control and status of ~~single twisted-pair~~ Auto-Negotiation, but the presence of a management agent is not required.

Auto-Negotiation shall provide the following functions (as shown in Figure 98–1):

a) Transmit
b) Receive
c) Half duplex
d) Arbitration

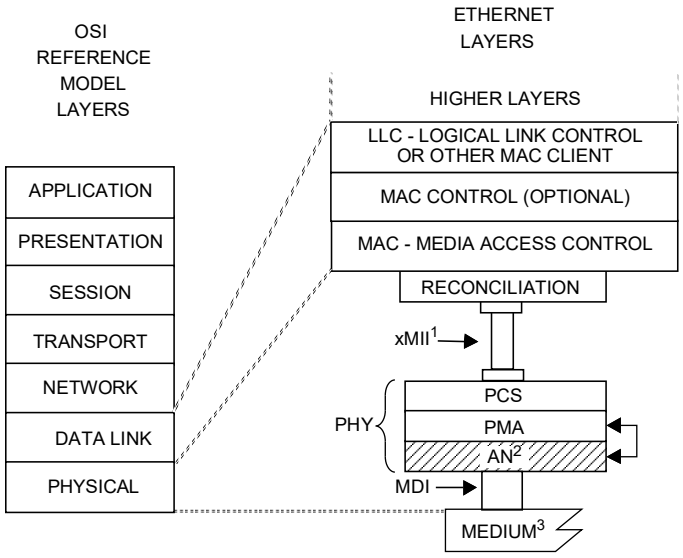
These functions shall comply with the state diagrams from Figure 98–7 through Figure 98–10. The ~~single twisted-pair~~ Auto-Negotiation functions shall interact with the technology-dependent PHYs through the Technology Dependent Interface (see 98.4).

98.2.1 Transmit function requirements

98.2.1.1 DME transmission

98.2.1.1.1 DME page encoding

Replace Figure 98-2 with the one that follows:



MDI = MEDIUM DEPENDENT INTERFACE
xMII = MEDIA INDEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
AN = AUTO-NEGOTIATION

NOTE 1—xMII is optional.
NOTE 2—Auto-Negotiation is optional. Auto-Negotiation communicates with the PMA sublayer through the PMA service interface messages PMA_LINK.request and PMA_LINK.indication.
NOTE 3—Medium is either a single-lane of differential balanced pair or unbalanced single-ended (e.g., coaxial)

Figure 98–2—Location of Auto-Negotiation function within the ISO/IEC OSI reference model

98.2.1.1.4 Transmitter peak differential output

Change the text of 98.2.1.1.4 as follows (unchanged text not shown):

~~When~~If used with a differential MDI and medium, when measured with 100 Ω termination, transmit differential signal at MDI shall be within range of 1 V ± 30% peak-to-peak.

If used with a single-ended unbalanced MDI and medium, when measured with 50 Ω termination, transmit signal at MDI shall be within range of 0.5 V ± 30% peak-to-peak.

98.2.1.2 Link codeword encoding

98.2.1.2.4 Technology Ability Field

Change the first paragraph of 98.2.1.1.4 as follows (unchanged text not shown):

Technology Ability Field (A[26:0]) is a 27-bit wide field containing information indicating supported technologies specific to the selector field value when used with the ~~single twisted-pair~~ Auto-Negotiation Ethernet. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector with ~~single twisted-pair~~ Auto-Negotiation Ethernet is described in 98B.3.

98.3 State diagram variable to Auto-Negotiation register mapping

Change the title of Table 98-7 as follows (unchanged rows not shown):

.

Table 98–7—State diagram variable to Single-lane ~~twisted-pair~~ media Auto-Negotiation MDIO register mapping

…

98.5 Detailed functions and state diagrams

98.5.1 State diagram variables

Insert new items at the end of the dashed list after the first paragraph of 98.5.1 as follows:

- 100M+2.5GigT1/V1; represents that the 100M+2.5GBASE-T1/V1 PMA is the signal source.
- 100M+5GigT1/V1; represents that the 100M+5GBASE-T1/V1 PMA is the signal source.
- 100M+10GigT1/V1; represents that the 100M+10GBASE-T1/V1 PMA is the signal source.
- 2.5GigT1+100MT1/V1; represents that the 2.5G+100MBASE-T1/V1 PMA is the signal source.
- 5GigT1+100MT1/V1; represents that the 5G+100MBASE-T1/V1 PMA is the signal source.
- 10GigT1+100MT1/V1; represents that the 10G+100MBASE-T1/V1 PMA is the signal source.

NOTE—If the priority resolution is an asymmetrical ability, the HCD values are complementary, e.g. if the HCD for a device is 100M+2.5GigT1, the HCD for its link partner would be 2.5Gig+100MT1.

Change the last sentence of the third paragraph of 98.5.1 as follows (unchanged text not shown):

The mapping between state diagram variables and ~~Single twisted-pair~~ Auto-Negotiation MDIO registers is shown in Table 98–7.

Change the title of 98.6 as follows:

98.6 Protocol implementation conformance statement (PICS) proforma for Clause 98, Auto-Negotiation for ~~Single Differential Pair~~ single-lane Media[4]

Change the first sentence of 98.6.1 as follows:

98.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 98, Auto-Negotiation for ~~Single Differential Pair~~ single-lane Media, shall complete the following protocol implementation conformance statement (PICS) proforma.

98.6.2 Identification

98.6.2.2 Protocol summary

Change the first row of the following table as follows (unchanged rows not shown):

Identification of protocol standard	IEEE Std 802.3-202x, Clause 98, Auto-Negotiation for Single Differential-Pair single-lane Media
…	

98.6.3 Major capabilities/options

Add two new rows at the end of the following table (unchanged rows not shown)

Item	Feature	Subclause	Value/Comment	Status	Support
…					
*DIFF	Differential balanced-pair media	98.1.1		O/2	Yes [ ] No [ ]
*UNB	Unbalanced single-ended media	98.1.1		O/2	Yes [ ] No [ ]

98.6.4 General

Change the second row of the following table as follows (unchanged rows not shown):l

Item	Feature	Subclause	Value/Comment	Status	Support
G1	Single-lane media ~~twisted-pair~~ Auto-Negotiation function	98.2	Provide Auto-Negotiation transmit, Auto-Negotiation receive, Auto-Negotiation half-duplex, and Auto-Negotiation arbitration	M	Yes [ ]
…					

[4] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

98.6.5 DME transmission

Change DME10 and add DME11 at the end of the following table (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
…					
DME10	Transmit differential signal at the MDI	98.2.1.1.4	Within range of 1 V ± 30% peak-to-peak when measured in reference to a 100 Ω termination	DIFF: M	Yes [ ]
DME11	Transmit signal at the MDI	98.2.1.1.4	Within range of 0.5 V ± 30% peak-to-peak when measured in reference to a 50 Ω termination	UNB: M	Yes [ ]

Insert new clauses and corresponding annexes as follows:

201. ACT proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1

201.1 Overview

This clause defines the type 100M+2.5GBASE, 2.5G+100MBASE, 100M+5GBASE, 5G+100MBASE, 100M+10GBASE, and 10G+100MBASE Physical Coding Sublayer (PCS) as well as the 100M+2.5GBASE-T1/V1, 2.5G+100MBASE-T1/V1, 100M+5GBASE-T1/V1, 5G+100MBASE-T1/V1, 100M+10GBASE-T1/V1, and 10G+100MBASE-T1/V1 Physical Medium Attachment (PMA) sublayers. Together, the corresponding PCS and PMA sublayers comprise a 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1,100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, and 10G+100MBASE-V1 Physical Layer device (PHY). Provided in this clause are functional and electrical specifications for the type 100M+2.5GBASE-T1/V1 PCS and PMA, 2.5G+100MBASE-T1/V1 PCS and PMA, 100M+5GBASE-T1/V1 PCS and PMA, 5G+100MBASE-T1/V1 PCS and PMA, 100M+10GBASE-T1/V1 PCS and PMA, and 10G+100MBASE-T1/V1 PCS and PMA.

The 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, and 10G+100MBASE-T1 PHYs are intended to be operated over a single balanced pair of conductors. The link segment specifications defined in 201.9 were derived from automotive requirements, but may also be used for non-automotive applications. The conductors supporting the operation of the 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, and 10G+100MBASE-T1 PHYs are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) allowing implementers to provide their own conductors to operate the 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, and 10G+100MBASE-T1 PHYs as long as the normative requirements included in 201.9 are met.

The 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, and 10G+100MBASE-V1 PHYs are intended to be operated over a single coaxial cable. The link segment specifications defined in 201.10 were derived from automotive requirements, but may also be used for non-automotive applications. The conductor supporting the operation of the 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, and 10G+100MBASE-V1 PHYs are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) allowing implementers to provide their own conductors to operate the 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, and 10G+100MBASE-V1 PHYs as long as the normative requirements included in 201.10 are met.

201.1.1 Nomenclature

The 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1 PHYs described in this clause represent 12 distinct PHY types that share the same PCS and PMA specifications subject to

frequency scaling, see Table 201–2 for additional information. In order to efficiently describe the 12 PHYs, the following nomenclature is used. See Figure 201–1 for block diagram.

HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter
PHY_D	Device containing LS_TX, HS_RX (100M+ MultiGBASE-T1/V1)
PHY_S	Device containing HS_TX, LS_RX (MultiG+100MBASE-T1/V1)

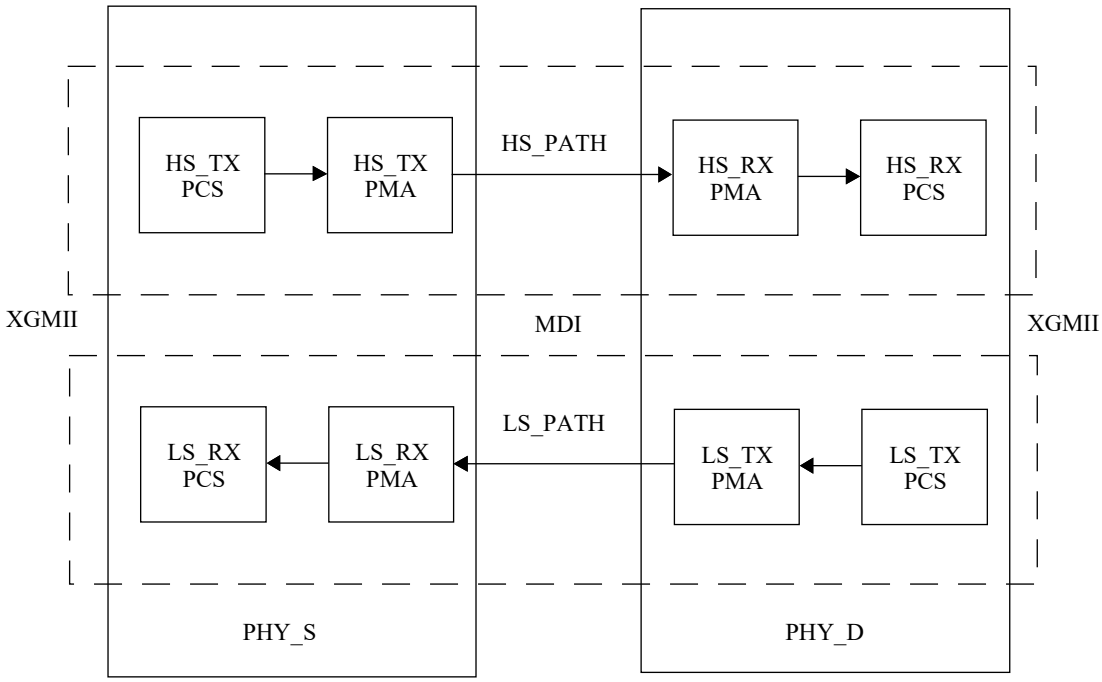


Figure 201–1—MultiG+100M/100M+MultiGBASE-T1/V1 block diagram

When talking about all PHYs communicating on a shielded, balanced, pair of conductors, regardless of transmit bit rate, use:

MultiG+100M/100M+MultiGBASE-T1

When talking about all PHYs communicating on a coaxial cable, regardless of transmit bit rate, use:

MultiG+100M/100M+MultiGBASE-V1

When talking about all PHYs, regardless of transmit bit rate or cable type, use:

MultiG+100M/100M+MultiGBASE-T1/V1

Additionally, for parameters that scale with the PHY's transmit bit rate, the parameter *S* is used for scaling, see Table 201–1. When incorporating Clause 149 requirements which use the scaling factor S by reference, refer to Table 201–1 rather than Table 149-1.

Table 201–1—Scaling parameter

PHY type	*S*
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	1
2.5G+100MBASE-T1/V1	0.5

The characteristics of each of the 12 PHY types are expanded in Table 201–2.

Table 201–2—PHY/PMD type definitions

PHY name	Transmit bit rate	Receive bit rate	Medium Interface
100M+2.5GBASE-T1	100 Mb/s	2.5 Gb/s	Differential (balanced)
2.5G+100MBASE-T1	2.5 Gb/s	100 Mb/s	Differential (balanced)
100M+5GBASE-T1	100 Mb/s	5 Gb/s	Differential (balanced)
5G+100MBASE-T1	5 Gb/s	100 Mb/s	Differential (balanced)
100M+10GBASE-T1	100 Mb/s	10 Gb/s	Differential (balanced)
10G+100MBASE-T1	10 Gb/s	100 Mb/s	Differential (balanced)
100M+2.5GBASE-V1	100 Mb/s	2.5 Gb/s	Single-ended (unbalanced)
2.5G+100MBASE-V1	2.5 Gb/s	100 Mb/s	Single-ended (unbalanced)
100M+5GBASE-V1	100 Mb/s	5 Gb/s	Single-ended (unbalanced)
5G+100MBASE-V1	5 Gb/s	100 Mb/s	Single-ended (unbalanced)
100M+10GBASE-V1	100 Mb/s	10 Gb/s	Single-ended (unbalanced)
10G+100MBASE-V1	10 Gb/s	100 Mb/s	Single-ended (unbalanced)

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

-T1 represents a single shielded balanced pair of conductors (i.e., differential)

-V1 represents a single-ended coaxial cable (i.e., unbalanced)

201.1.2 Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 to other standards

The relationship between a MultiG+100M/100M+MultiGBASE-T1/V1 PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 201–2. The PHY sublayers (shown shaded) in Figure 201–2 connect one Clause 4 Media Access Control (MAC) layer to the medium. The XGMII is defined in Clause 46.

Auto-Negotiation for all MultiG+100M/100M+MultiGBASE-T1/V1 PHYs is defined in Clause 98.

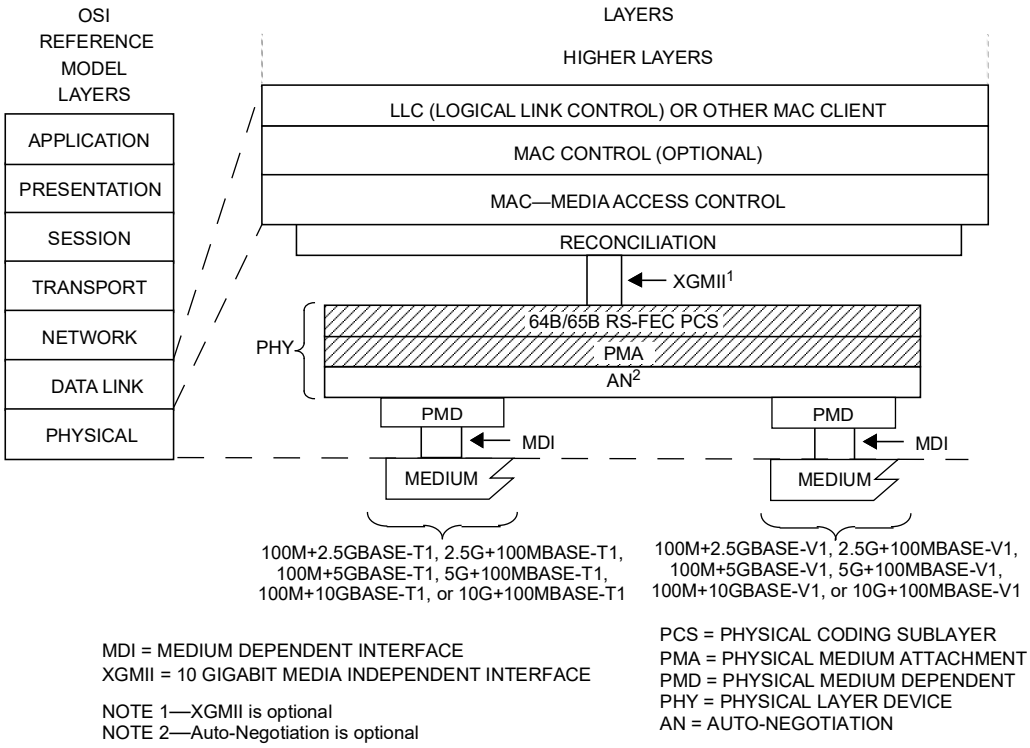


Figure 201–2—Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

201.1.3 Operation of MultiG+100M/100M+MultiGBASE-T1/V1

A MultiG+100MBASE-T1/V1 PHY is a PHY_S device which transmits at a bit rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s and receives at a 100 Mb/s bit rate. A 100M+MultiGBASE-T1/V1 PHY is a PHY_D device which transmits at a 100 Mb/s bit rate and receives at a bit rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s. Figure 201–3 shows a block diagram of the PHY_S device and Figure 201–4 shows a block diagram of the PHY_D device.

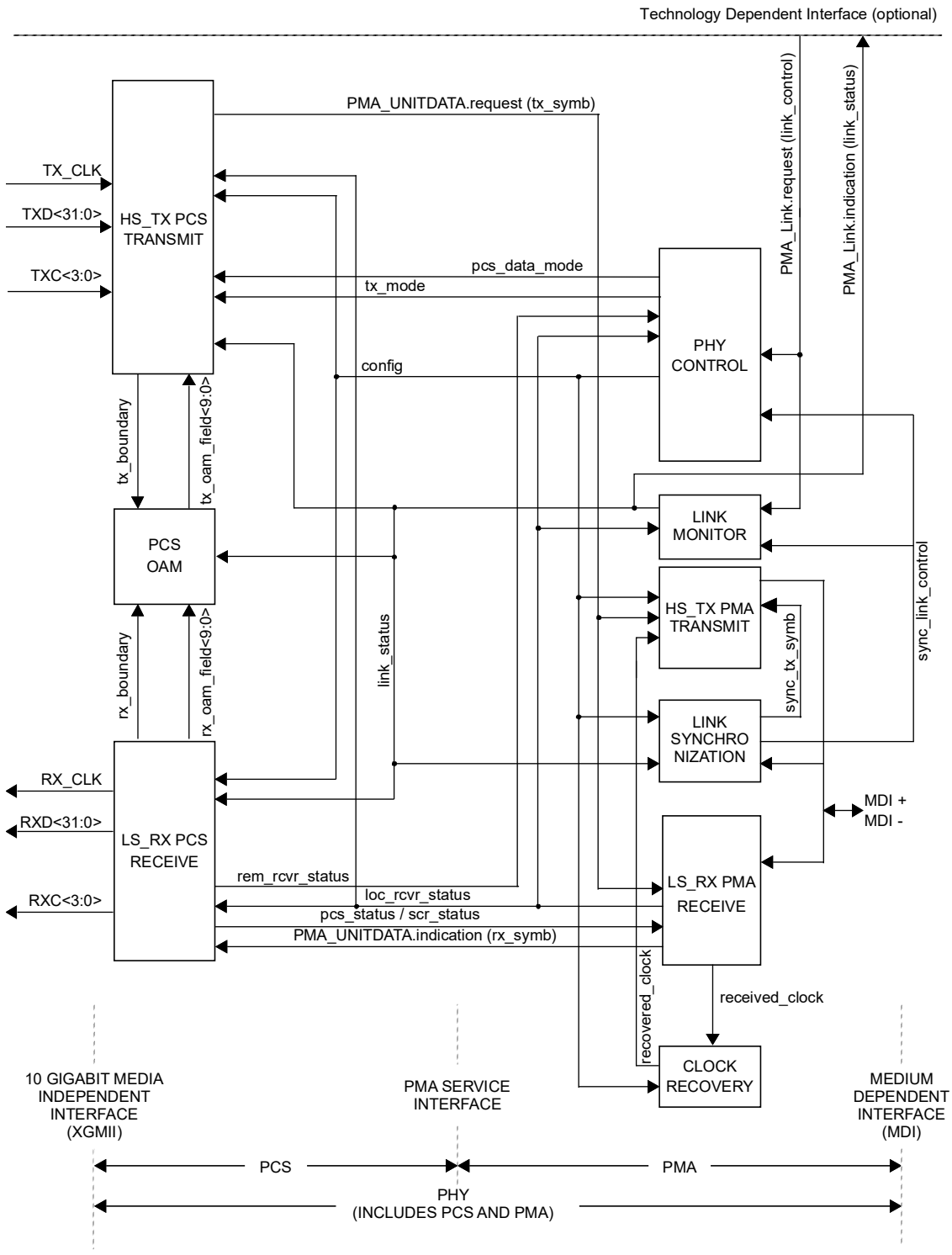
The PHY_S device includes the high speed transmit function and low speed receive function required for asymmetric operation over the link segment. The top-level arrangement of the PCS, PMA, synchronization, monitoring, and clock-recovery blocks is shown in Figure 201–3. While the block diagram illustrates data, status, and control flow among these elements, the detailed functional definitions are provided in the remainder of Clause 201.

The PHY_D device includes the low speed transmit function and high speed receive function required for asymmetric operation over the link segment. The top-level arrangement of the PCS, PMA, synchronization, monitoring, and clock-recovery blocks is shown in Figure 201–4. While the block diagram illustrates data, status, and control flow among these elements, the detailed functional definitions are provided in the remainder of Clause 201.

Auto-Negotiation (Clause 98) may optionally be used by MultiG+100M/100M+MultiGBASE-T1/V1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional.

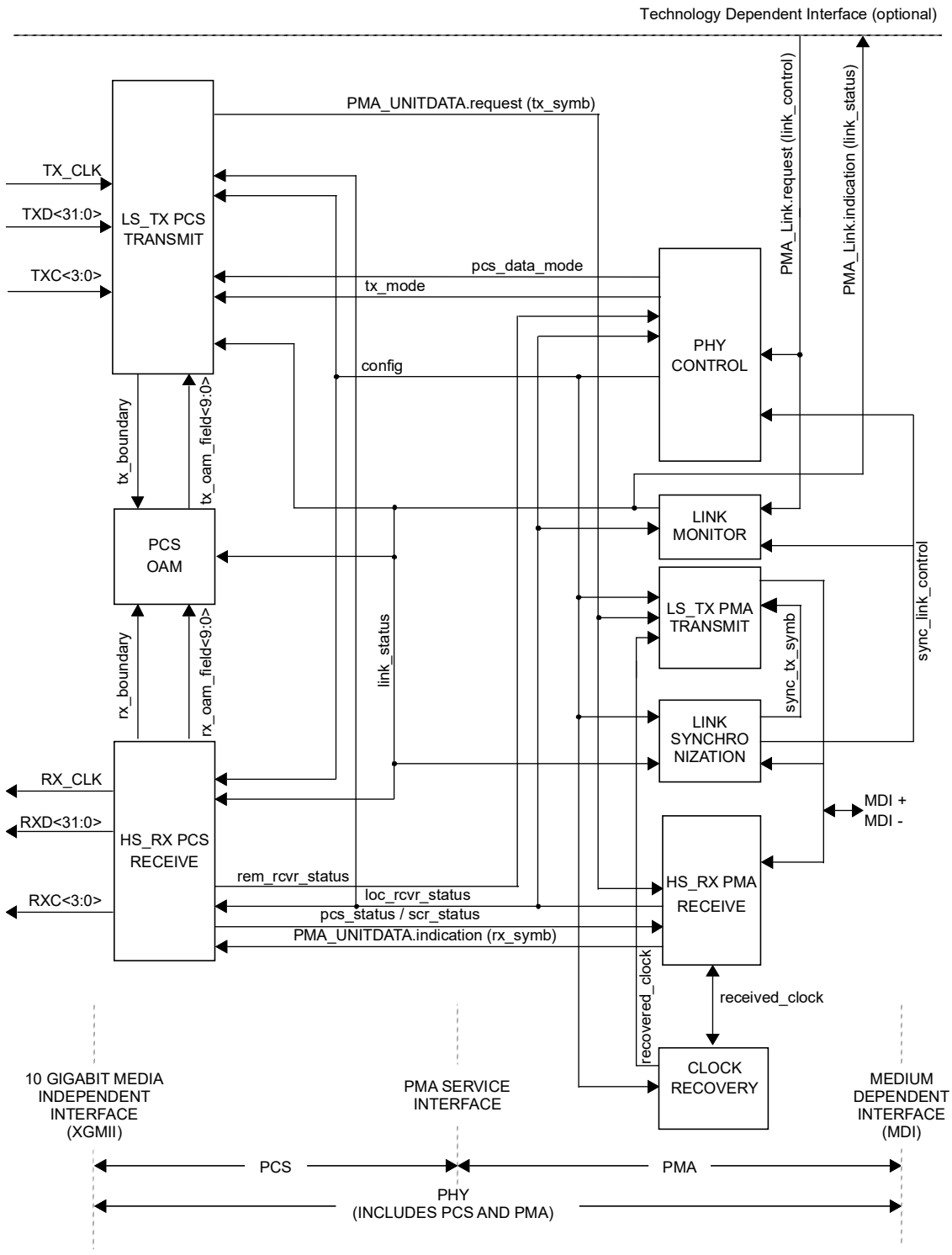
A MultiG+100M/100M+MultiGBASE-T1/V1 PHY can operate as LEADER or FOLLOWER, per runtime configuration. A LEADER PHY uses a local clock to determine the timing of transmitter operations. A FOLLOWER PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. The LEADER-FOLLOWER relationship is established by forced configuration in the Link Synchronization process (see 201.5.2.8), or by auto-negotiation if it is implemented and enabled.

NOTE-Annex K describes that the optional alternative terminology "leader"and "follower" which was formerly known as "master" and "slave".



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal by the HS_TX PMA TRANSMIT for loop timing.

Figure 201–3—PHY_S functional block diagram



NOTE—The recovered_clock arc,FOLLOWER only, is shown to indicate delivery of the received clock signal by the HS_TX PMA TRANSMIT for loop timing.

Figure 201–4—PHY_D functional block diagram

201.1.3.1 Physical Coding Sublayer (PCS), high speed path (HS_PATH)

For the high speed path, the HS_TX and HS_RX PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, to the 2.5G+100MBASE-T1/V1, 5G+100MBASE-T1/V1, or 10G+100MBASE-T1/V1 Physical Medium Attachment (PMA) sublayer. In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface. The HS_TX PCS is in the PHY_S and the HS_RX PCS is in the PHY_D.

The HS_PATH contains the PCS functions as specified in 149.3, except as modified by 201.3.

201.1.3.2 Physical Coding Sublayer (PCS), low speed path (LS_PATH)

For the low speed path, the LS_TX and LS_RX PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, to the 100M+2.5GBASE-T1/V1, 100M+5GBASE-T1/V1, or 100M+10GBASE-T1/V1 Physical Medium Attachment (PMA) sublayer. In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface. The LS_TX PCS is in the PHY_D and the LS_RX PCS is in the PHY_S.

For the low speed path, in normal mode, the PCS LS_TX receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and TXC<3:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block.

These 65-bit blocks are then aggregated into groups of four blocks. The contents of each group are contained in a vector tx_group4x65B. Next, 10 OAM bits and six vendor-specific bits are appended to form a 276-bit block. Each of these 276-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(50,46,6). The RS-FEC output frame consists of 300 bits. The duration of the frame is 2560 ns. These bits are exclusive OR'd with a degree 33 scrambler to create the 100M+MultiGBASE-T1/V1 payload. The LS_PATH contains the PCS functions as described in 201.4.2.2.

The tx_group4x65B <259:0> is defined as:

$$\text{tx\_group4x65B} \langle 65 \times i + j \rangle = \text{tx\_coded}_i \langle j \rangle$$

where i = 0 to 3, j = 0 to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded_0<64:0> is the first block transmitted.

The LS_RX PCS reverses the above process and presents eight XGMII data octets over two consecutive transfers on the XGMII service interface on RXD<31:0> and RXC<3:0>.

In the training mode (see 201.4.5), the LS_TX and LS_RX transmits and receives differential Manchester encoding (DME) training frames, to synchronize to the PHY frame (and advertises capabilities such as OAM). See 201.5.2.2.1 for details on the DME symbols.

Details of the PCS functions and state diagrams are covered in 201.4. The interface to the PMA is an abstract message-passing interface specified in 201.5.

201.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the PMD of a single balanced pair of conductors (T1) or a single coaxial cable (V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions.

For the HS_PATH, the PMA provides communications at 5625 × *S* MBd. See Table 201–1 for the definition of *S*. For the LS_PATH, the PMA provides communications at 117.1875 MBd.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of PHY Link Synchronization or optional Auto-Negotiation and provides the startup functions required for successful PHY operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

PMA functions and state diagrams are specified in 201.5. The electrical parameters of the PMA, i.e., test modes and electrical specifications for the transmitter and receiver, are specified in 201.6 and 201.7.

201.1.3.4 Link Synchronization

The Link Synchronization function is used when Auto-Negotiation is disabled or not implemented to detect the presence of the link partner, time and control link failure, and act as the data source for the PHY control state diagram. Link Synchronization operates in a half-duplex fashion. Link Synchronization is defined in 201.5.2.8.

201.1.4 Signaling, high speed path (HS_PATH)

HS_PATH signaling is performed by the HS_TX PCS generating continuous code-group sequences that the HS_TX PMA transmits over a single balanced pair of conductors (T1) or a single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between the HS_PATH and LS_PATH symbol streams.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for incorrect polarity in the connection for the single balanced pair of conductors (T1).

The PHY may operate in two basic modes: the normal data mode or the training mode.

In normal mode, the HS_TX PCS generates a continuous stream of PAM4 symbols that are transmitted via the HS_TX PMA at one of four voltage levels for 10Gb/s and PAM2 symbols that are transmitted via the HS_TX PMA at one of two voltage levels for 2.5Gb/s and 5Gb/s. In training mode, the PCS is directed to generate only PAM2 symbols for transmission by the HS_TX PMA.

201.1.5 Signaling, low speed path (LS_PATH)

LS_PATH signaling is performed by the LS_TX PCS generating continuous code-group sequences that the LS_TX PMA transmits over single balanced pair of conductors (T1) or single coaxial cable (V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to DME symbols in the transmit path. See 201.4.2.3 for details on the DME symbols.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between the HS_PATH and LS_PATH symbol streams.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

The PHY may operate in two basic modes: the normal data mode or the training mode.

The LS_TX PCS generates a continuous stream of bits that are transmitted via the LS_TX PMA in both training mode and normal mode.

201.1.6 Interfaces

All MultiG+100M/100M+MultiGBASE-T1/V1 PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not. The MDI for single balanced pair of conductors (T1) and single coaxial cable (V1), are different.

201.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

201.2 PHY_S and PHY_D service primitives and interfaces

PHY_S and PHY_D transfer data and control information across the following four service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) Technology Dependent Interface
c) PMA service interface
d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in 201.2.2 and the MDI is defined in 201.6.4.

201.2.1 Technology Dependent Interface

The following service primitives are used to exchange status indications and control signals across the Technology Dependent Interface, required in PHYs that implement Auto-Negotiation, as specified in 98.4:

PMA_LINK.request(link_control)
PMA_LINK.indication(link_status)

201.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation to enable and disable operation of the PMA, as specified in 98.4.2.

201.2.1.1.1 Semantics of the primitive

PMA_LINK.request(link_control)

The link_control parameter can take on one of two values: DISABLE, or ENABLE.

DISABLE Used by the Auto-Negotiation function to disable the PHY.

ENABLE Used by the Auto-Negotiation function to enable the PHY.

201.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

201.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 201.5.2.7, the PMA PHY Control function as defined in 201.5.2.6, and the PMA Receive function defined in 201.5.2.3 for both the HS_RX PMA and the LS_RX PMA.

201.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

201.2.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL No valid link established.

OK The Link Monitor function indicates that a valid MultiG+100M/100M+MultiGBASE-T1/V1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

201.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 201–32 Figure 149-33.

201.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

201.2.2 PMA service interface

The following service primitives are used to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication (pcs_data_mode)

The use of these primitives is illustrated in Figure 201–5 and Figure 201–6. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 201–5 and Figure 201–6.

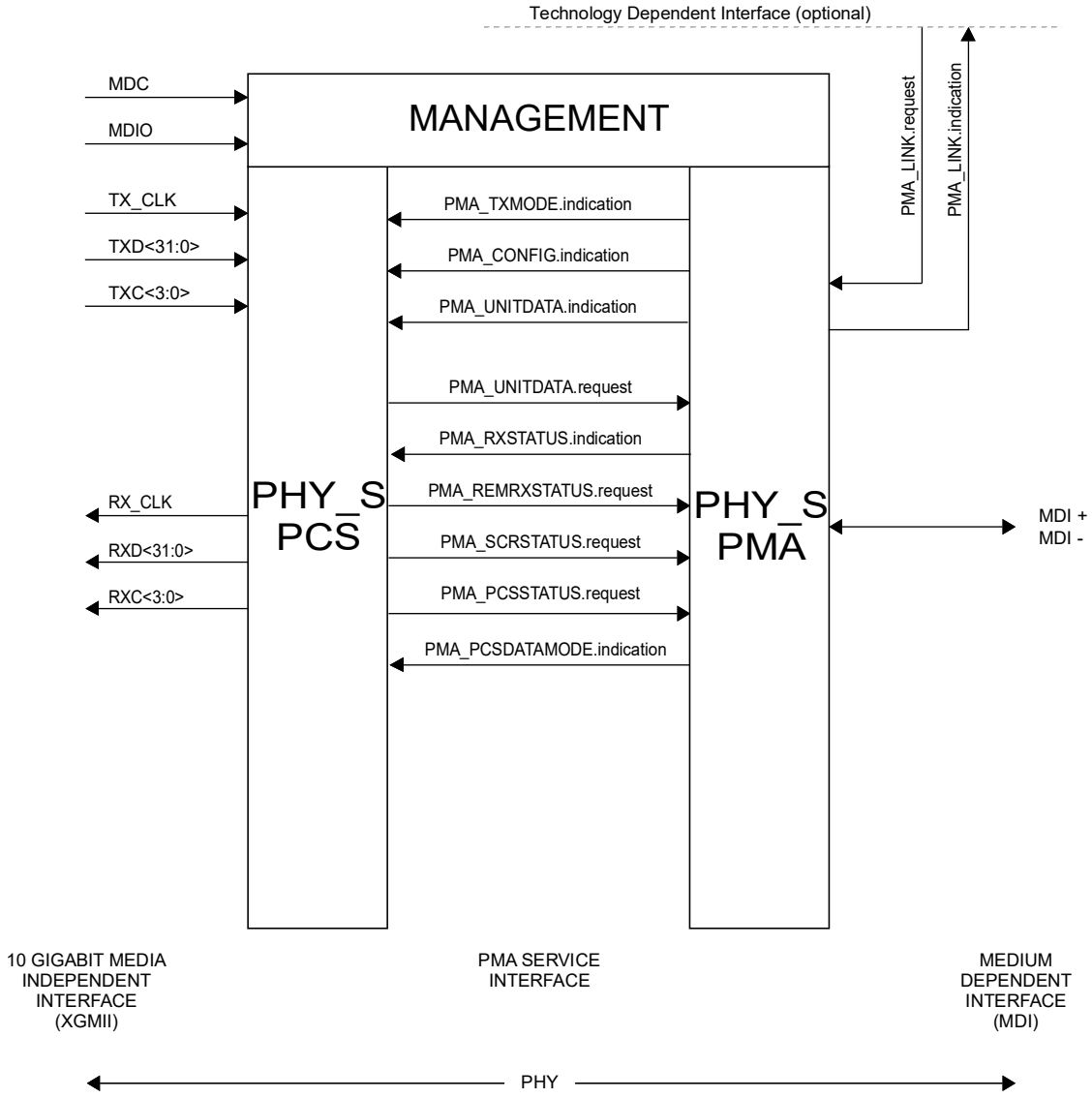


Figure 201–5—PHY_S service interfaces

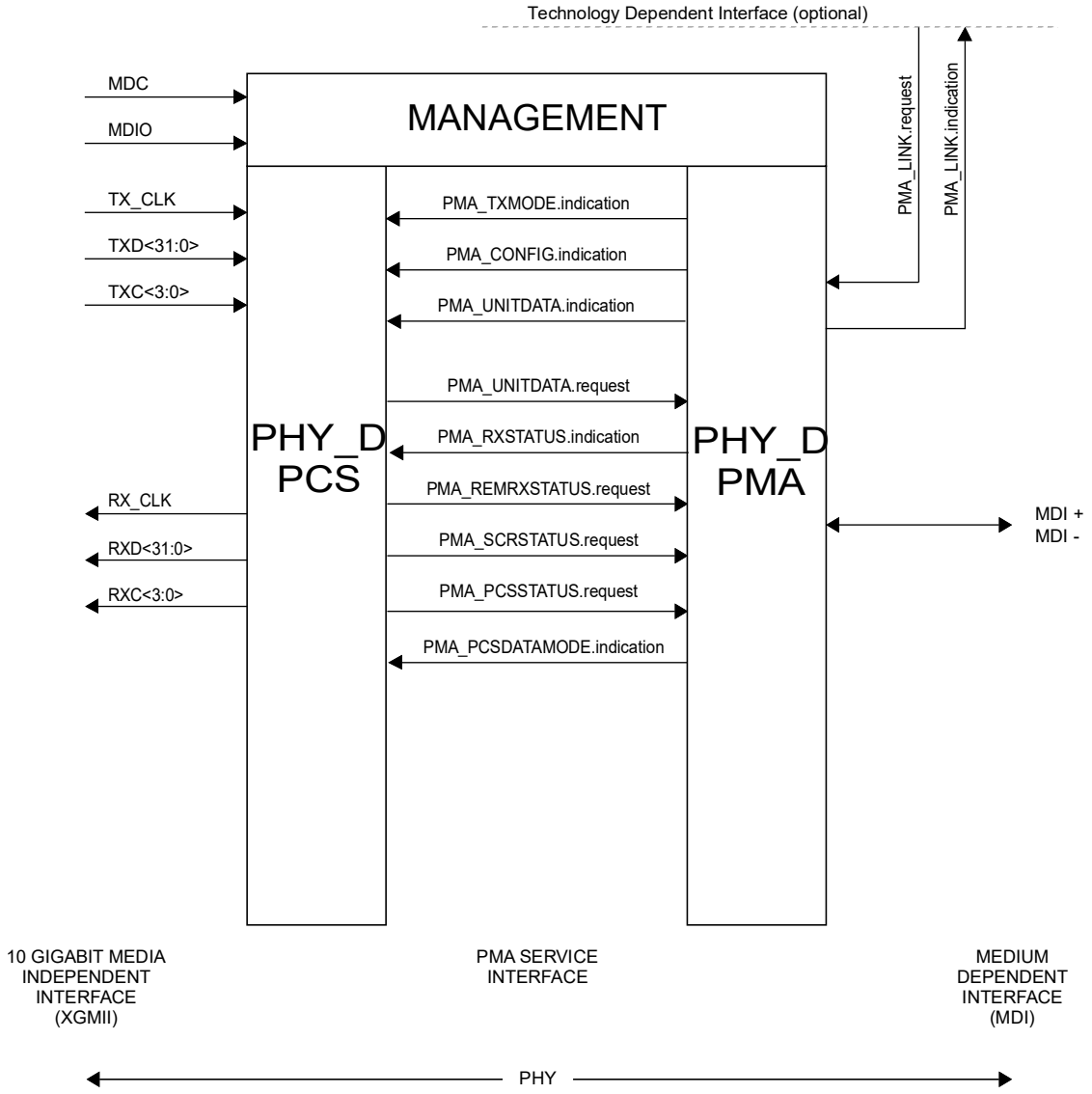


Figure 201–6—PHY_D service interfaces

201.2.2.1 PMA_TXMODE.indication

The transmitter normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

201.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.
SEND_T	This value is continuously asserted in case transmission of sequences of symbols representing the training mode is to take place.
SEND_Z	This value is continuously asserted in case transmission of Z symbols is required.

201.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

201.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 201.3.2.2 for the HS_TX and in 201.4.2.2 for the LS_TX.

201.2.2.2 PMA_CONFIG.indication

If the Auto-Negotiation process is enabled, PMA_CONFIG LEADER-FOLLOWER configuration is determined during Auto-Negotiation (see Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG LEADER-FOLLOWER configuration is predetermined to be LEADER or FOLLOWER via management control during initialization or via default hardware setup.

201.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PCS and PMA Transmit via the parameter config whether the PHY operates as a LEADER PHY or as a FOLLOWER PHY. The parameter config can take on one of the following two values of the form:

LEADER	This value is continuously asserted when the PHY operates as a LEADER PHY.
FOLLOWER	This value is continuously asserted when the PHY operates as a FOLLOWER PHY.

201.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

201.2.2.2.3 Effect of receipt

PCS and PMA Clock Recovery perform their functions in LEADER or FOLLOWER configuration according to the value assumed by the parameter config.

201.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 201.3.2.2 for the HS_TX and in 201.4.2.2 for the LS_TX to represent XGMII data and control streams or other sequences.

201.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI.

The HS_TX tx_symb may take on one of the following values:

{–1, –1/3, +1/3, +1}	in normal operation for 10G+100MBASE-T1/V1.
{–1, +1}	in normal operation for 2.5G+100MBASE-T1/V1 and 5G+100MBASE-T1/V1, and HS_PATH training frames.
Z	when Z symbols are to be transmitted in the following case: when PMA_TXMODE.indication is SEND_Z during PMA training.

The LS_TX tx_symb may take on one of the following values:

{0,1}	in normal operation.
Z	when Z symbols are to be transmitted in the following case: when PMA_TXMODE.indication is SEND_Z during PMA training.

201.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

201.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 201.6.2 for the HS_TX and 201.7.2 for the LS_TX.

201.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

201.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

201.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the HS_RX PMA_UNITDATA.indication primitive is 2812.5 MHz for 100M+2.5GBASE-T1/V1, and 5625 MHz for 100M+5GBASE-T1/V1 and 100M+10GBASE-T1/V1, as governed by the recovered clock. The nominal rate of the LS_RX PMA_UNITDATA.indication primitive is 117.1875 MHz; as governed by the recovered clock.

201.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

201.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the PCS descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode PCS descrambler has achieved synchronization.

201.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The training mode PCS descrambler has achieved synchronization.
NOT_OK	The training mode PCS descrambler is not synchronized.

201.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

201.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 201.5.2.3 for HS_RX and in 201.5.2.5 for LS_RX.

201.2.2.6 PMA_PCSSTATUS.request

PMA_PCSSTATUS.request is as described in 149.2.2.6.

201.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

201.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK — This value is asserted and remains true during reliable operation of the receive link for the local PHY.

NOT_OK — This value is asserted whenever operation of the link for the local PHY is unreliable.

201.2.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

201.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 201–3, Figure 201–4, Figure 201–7, Figure 201–8, Figure 201–31, 201.3.2.3, 201.4.2.3, and 201.5.2.6.1.

201.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

201.2.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK — The receive link for the remote PHY is operating reliably.

NOT_OK — Reliable operation of the receive link for the remote PHY is not detected.

201.2.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infofield messages received from the remote PHY during training.

201.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 201–31.

201.2.2.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

201.2.2.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

201.2.2.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

201.2.2.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 201.3.2.2 for HS_TX and 201.4.2.2 for LS_TX.

201.3 Physical Coding Sublayer (PCS) functions, high speed path (HS_PATH)

The PCS functions for HS_PATH are as specified for MultiGBASE-T1 PHYs in 149.3 with the exception that 2.5Gb/s and 5Gb/s use PAM2 instead of PAM4 in data mode and the differences noted in this subclause.

201.3.1 PCS service interface (XGMII)

The PCS service interface allows the MultiG+100MBASE-T1/V1 PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

201.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions, one of which is the HS_PATH and the other is the LS_PATH. This subclause discusses the HS_PATH. The HS_PATH PCS operating functions are the HS_TX PCS Transmit in the PHY_S device, and the HS_RX PCS Receive in the PHY_D device. All operating functions start immediately after the successful completion of the PCS Reset function.

The PHY_S PCS reference diagram, Figure 201–7 and the PHY_D PCS diagram, Figure 201–8, show how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 201–7 and Figure 201–8.

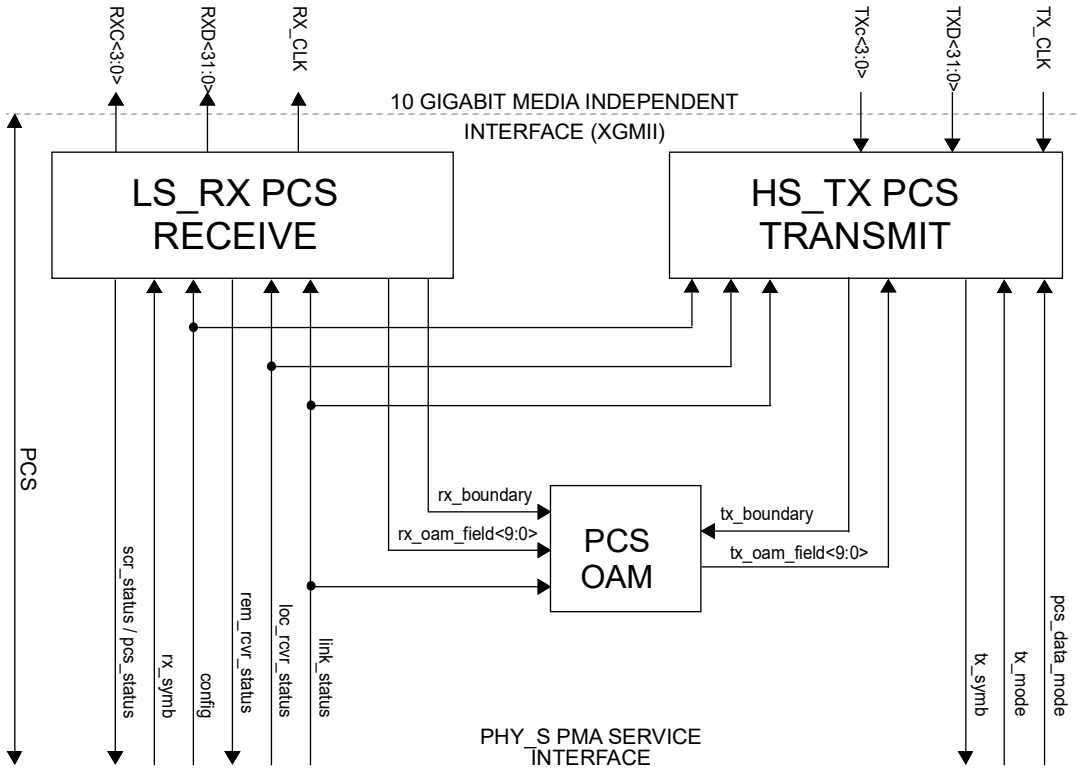


Figure 201–7—PHY_S PCS reference diagram

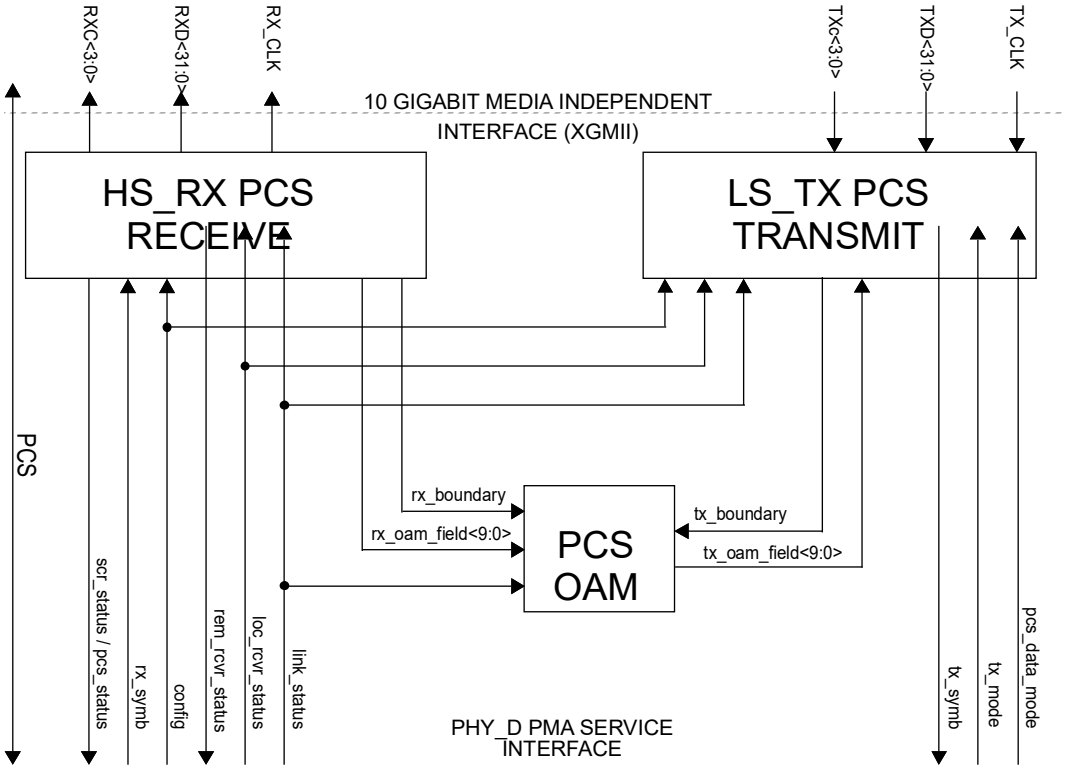


Figure 201–8—PHY_D PCS reference diagram

201.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 201.3.6.2.2).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

201.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 201–9 and to the PCS Transmit bit ordering in Figure 201–11 for 10Gb/s. The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 201–10 and to the PCS Transmit bit ordering in Figure 201–12 for 5 Gb/s and 2.5 Gb/s.

When communicating with the XGMII, the MultiG+100MBASE-T1/V1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take L groups of 50 65B blocks and append a 10-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC which adds L × 340 parity bits. The resulting L × 3600 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol for 10G and one at a time into a PAM2 symbol for 2.5G and 5G. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM4 symbol for 10G and a PAM2 symbol for 2.5G and 5G that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T, is 1000 / (5.625 × S) ps. See Table 201–1 for the definition of S.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a Z symbol at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 201.3.5.1 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {–1, +1}.

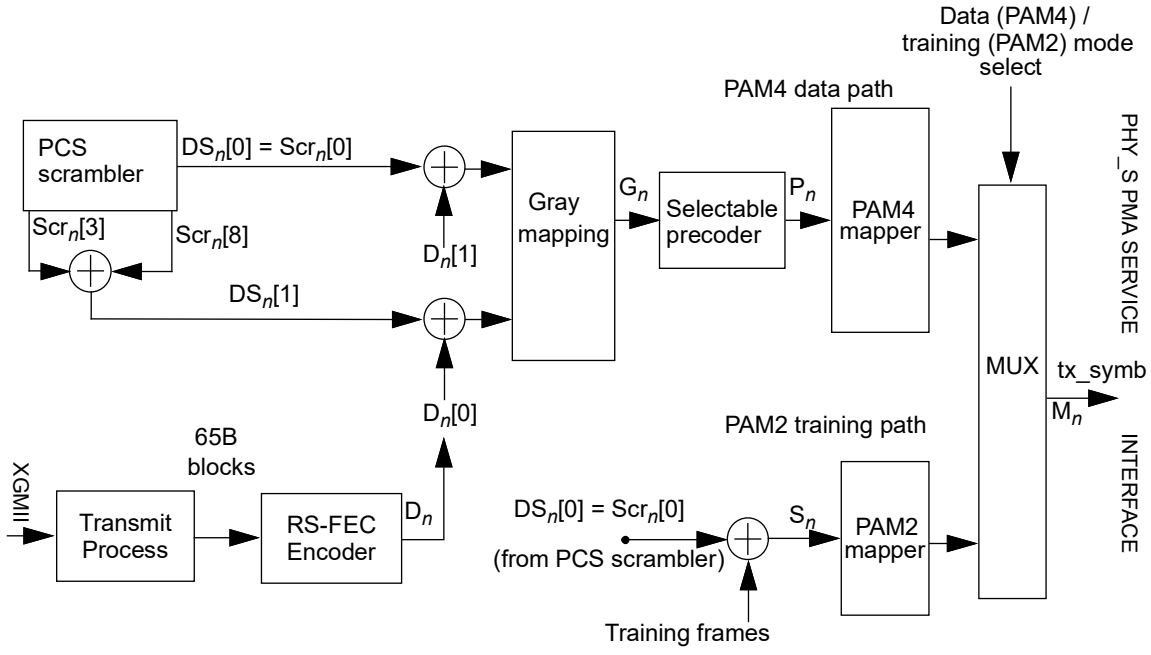
During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 201.5.2.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the 50 blocks of 65B encoded bits are appended with a 10-bit OAM field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes L-interleaved (L = 1, 2, or 4) Reed-Solomon encoders to generate and append 340 parity check bits to form 3600-bit (360,326) RS-FEC frames that are interleaved into an L-interleaved RS-FEC superframe.

Each RS-FEC input superframe consists of 3260 × L bits, or 326 × L Reed-Solomon message symbols. The interleaving function is integrated with the RS-FEC encoding, applying a round-robin interleaving scheme and distributing the 10-bit Reed-Solomon message symbols into L RS-FEC encoders. After encoding, the RS-FEC frames from each encoder are recombined into one single interleaved RS-FEC superframe, which consists of 360 × L symbols, or 3600 × L bits. The bits of the RS-FEC superframe are then scrambled by the PCS using an additive PCS scrambler, encoded in PAM4 symbols, and transferred to the PMA.

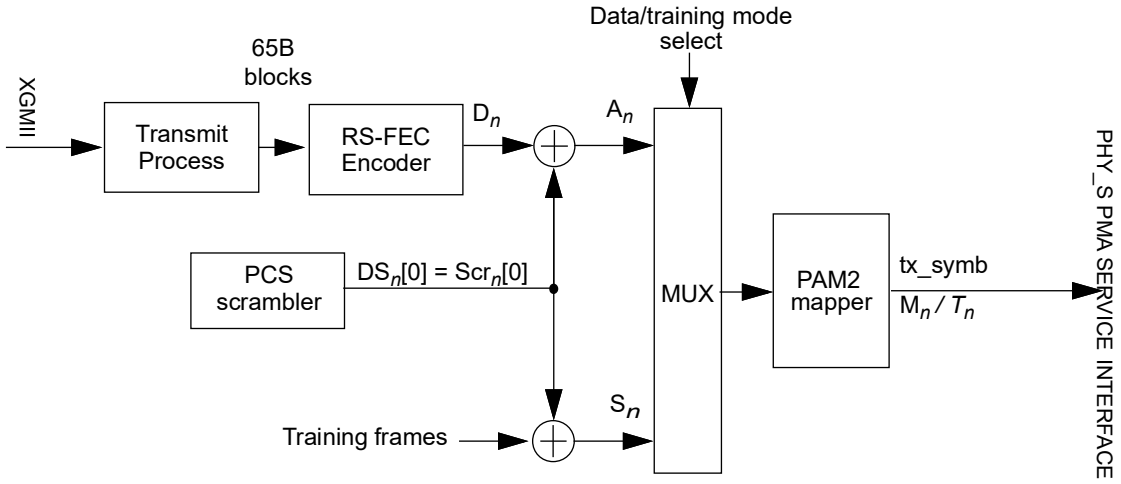
L is called the interleaving depth, and the possible choices of L are 1, 2, and 4. The interleaver settings requested in each direction of transmission may be different, and the value of L used by the transmitter is determined by the link partner and signaled during the PAM2 training mode Infofield exchange.

The block diagram of HS_TX PCS Transmit functions is shown in Figure 201–9 and Figure 201–10. .



NOTE —The S_n are from the training frame, and the MUX selects the PAM2 path while in PAM2 training states.

Figure 201–9—10 Gb/s HS_TX PCS Transmit function block diagram



NOTE 1 —The S_n are from the training frame, and the A_n are for the 2.5 Gb/s and 5 Gb/s HS_PATH.
NOTE 2 — The output of the PAM2 mapper is M_n in data mode and T_n in training mode.

Figure 201–10—2.5 Gb/s and 5 Gb/s HS_TX PCS Transmit function block diagram

201.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 201.3.2.2.2.

201.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 201–11 for 10G transmit, Figure 201–12 for 2.5G and 5G transmit, Figure 201–13 for 10G receive, and Figure 201–14 for 2.5G and 5G receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.

201.3.2.2.3 Notation conventions

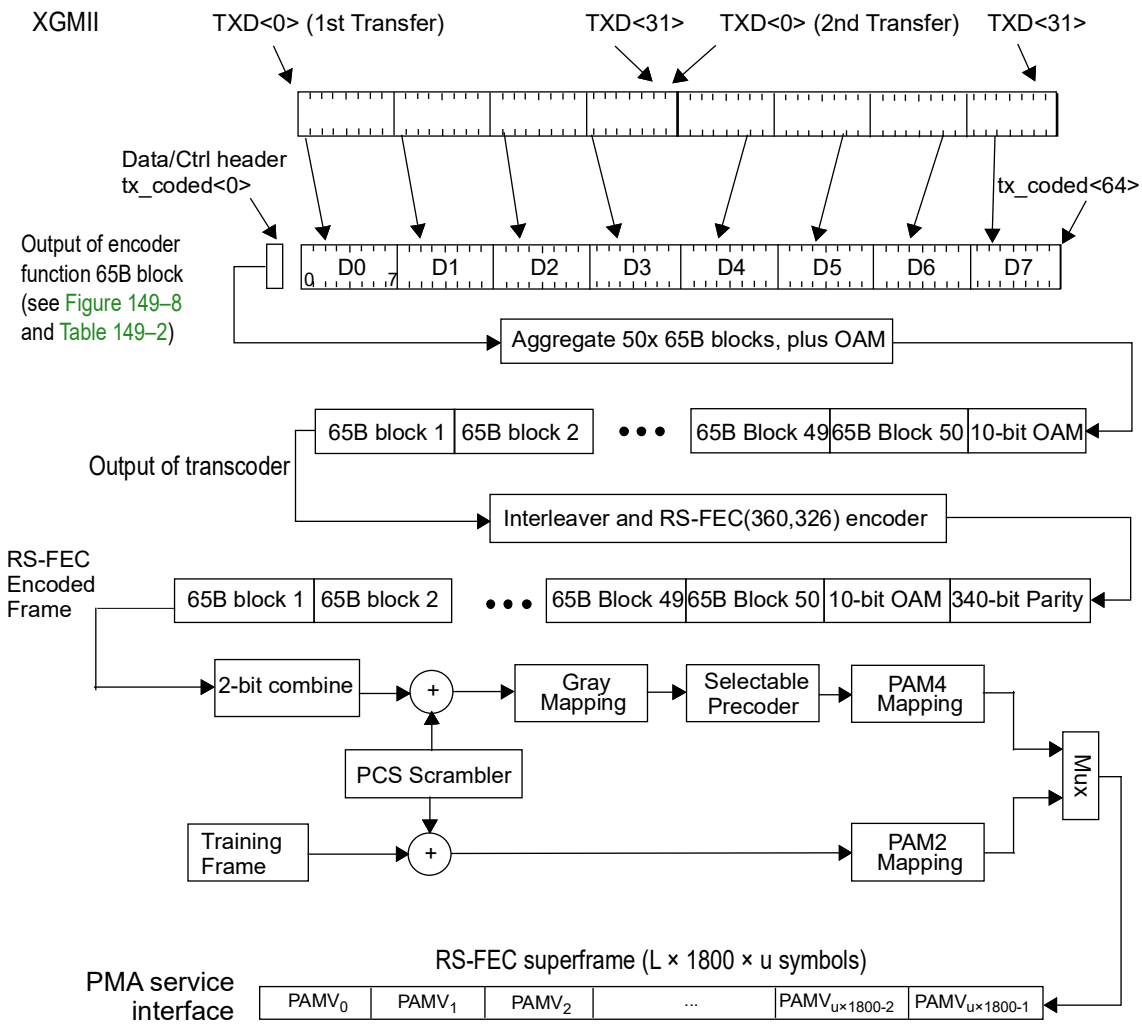
See 149.3.2.2.3.

201.3.2.2.4 Block structure

See 149.3.2.2.4.

201.3.2.2.5 Control codes

See 149.3.2.2.5.



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.
NOTE 2—Figure shown for L = 1.
NOTE 3—For PAM2 path, V=2 and u=2. For PAM4 path, V=4 and u=1.

Figure 201–11—PCS 10 Gb/s Transmit bit ordering for data mode and training mode, HS_TX

201.3.2.2.6 Ordered sets

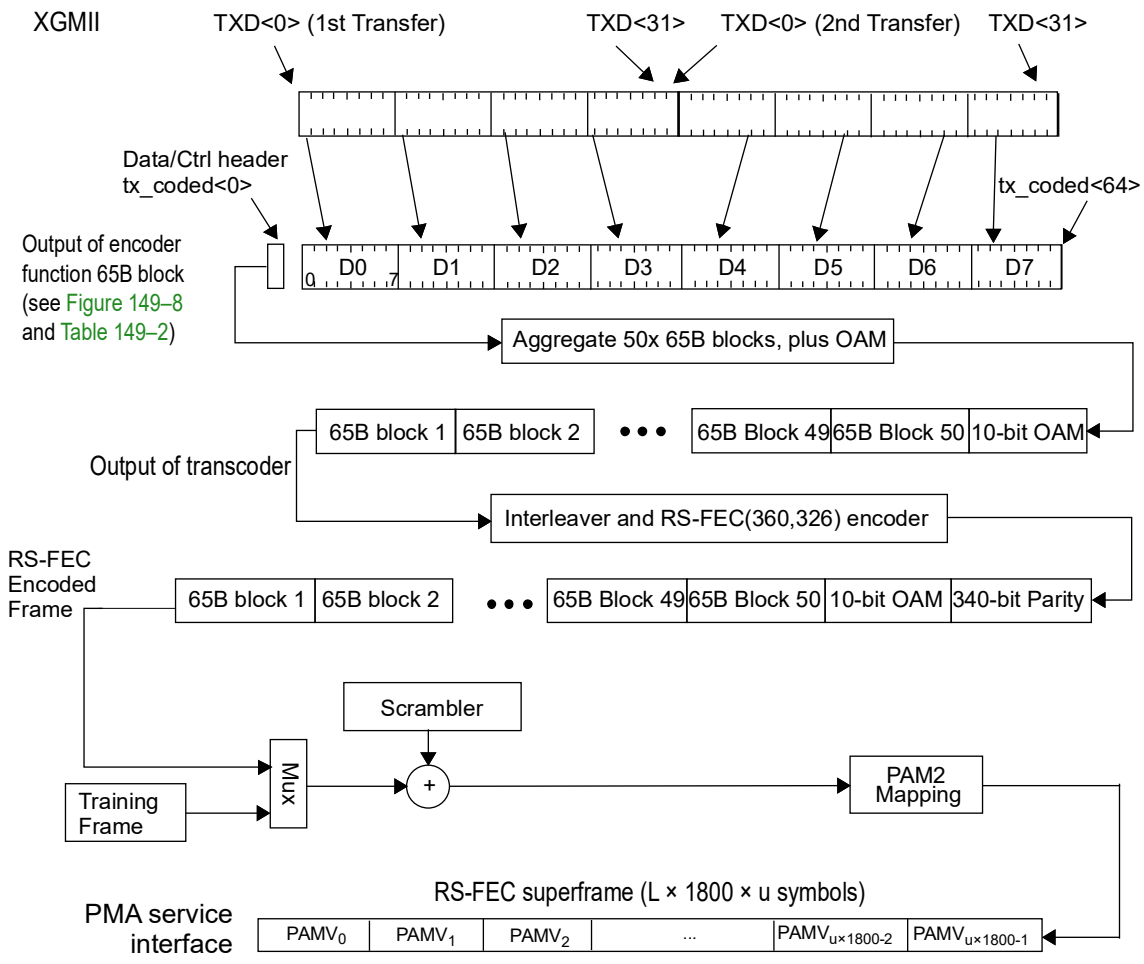
See 149.3.2.2.6. LPI, /LI/ is not used by MutltiG+100MBASE-T1/V1 PHYs.

201.3.2.2.7 Idle (/I/)

See 149.3.2.2.7.

201.3.2.2.8 Start (/S/)

See 149.3.2.2.9.



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.
NOTE 2—Figure shown for L = 1.
NOTE 3—For PAM2 path, V=2 and u=2.

Figure 201–12—PCS 5 Gb/s and 2.5 Gb/s Transmit bit ordering for data mode and training mode, HS_TX

201.3.2.2.9 Terminate (/T/)

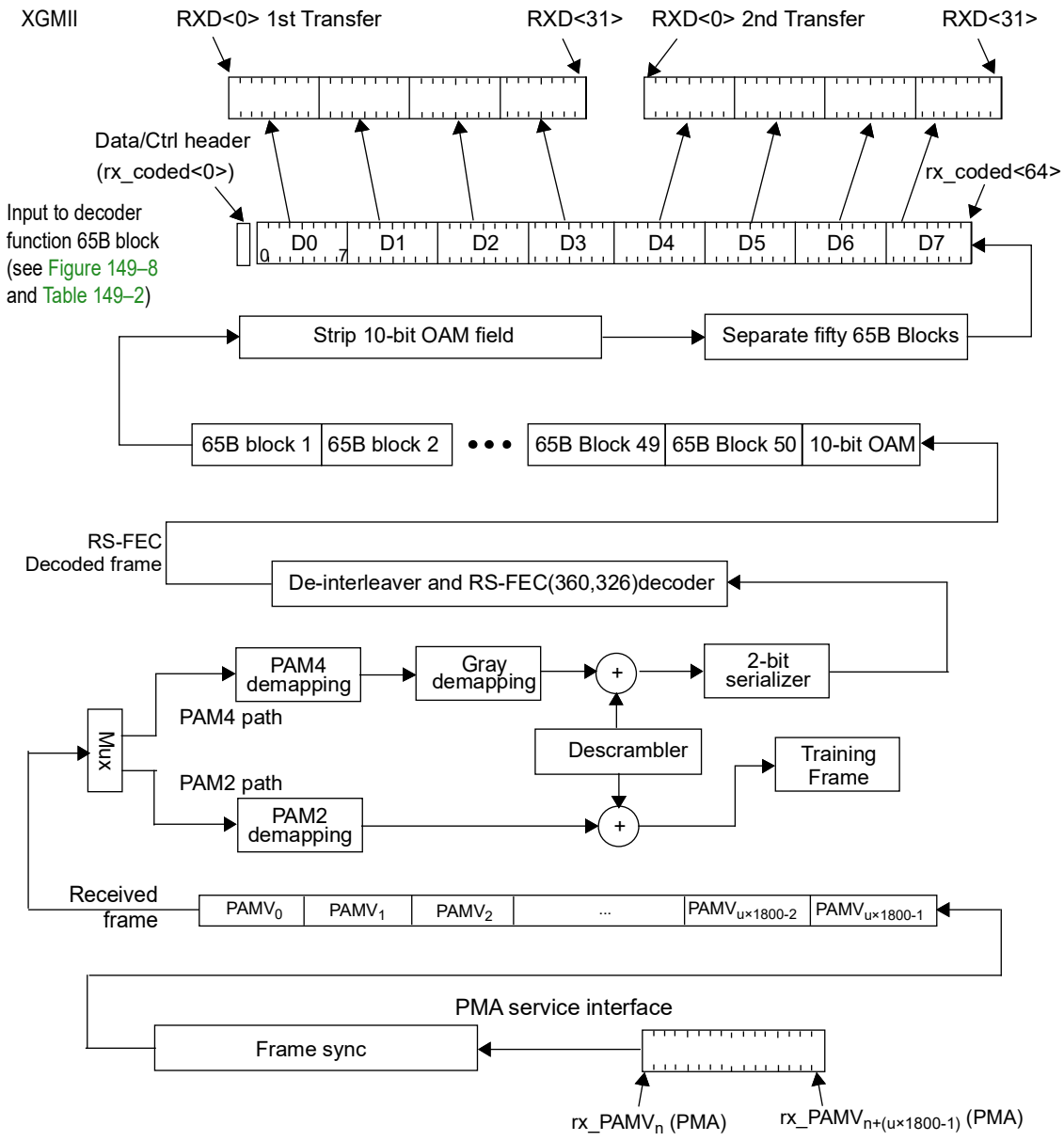
See 149.3.2.2.10.

201.3.2.2.10 Ordered set (/O/)

See 149.3.2.2.11.

201.3.2.2.11 Error (/E/)

See 149.3.2.2.12.



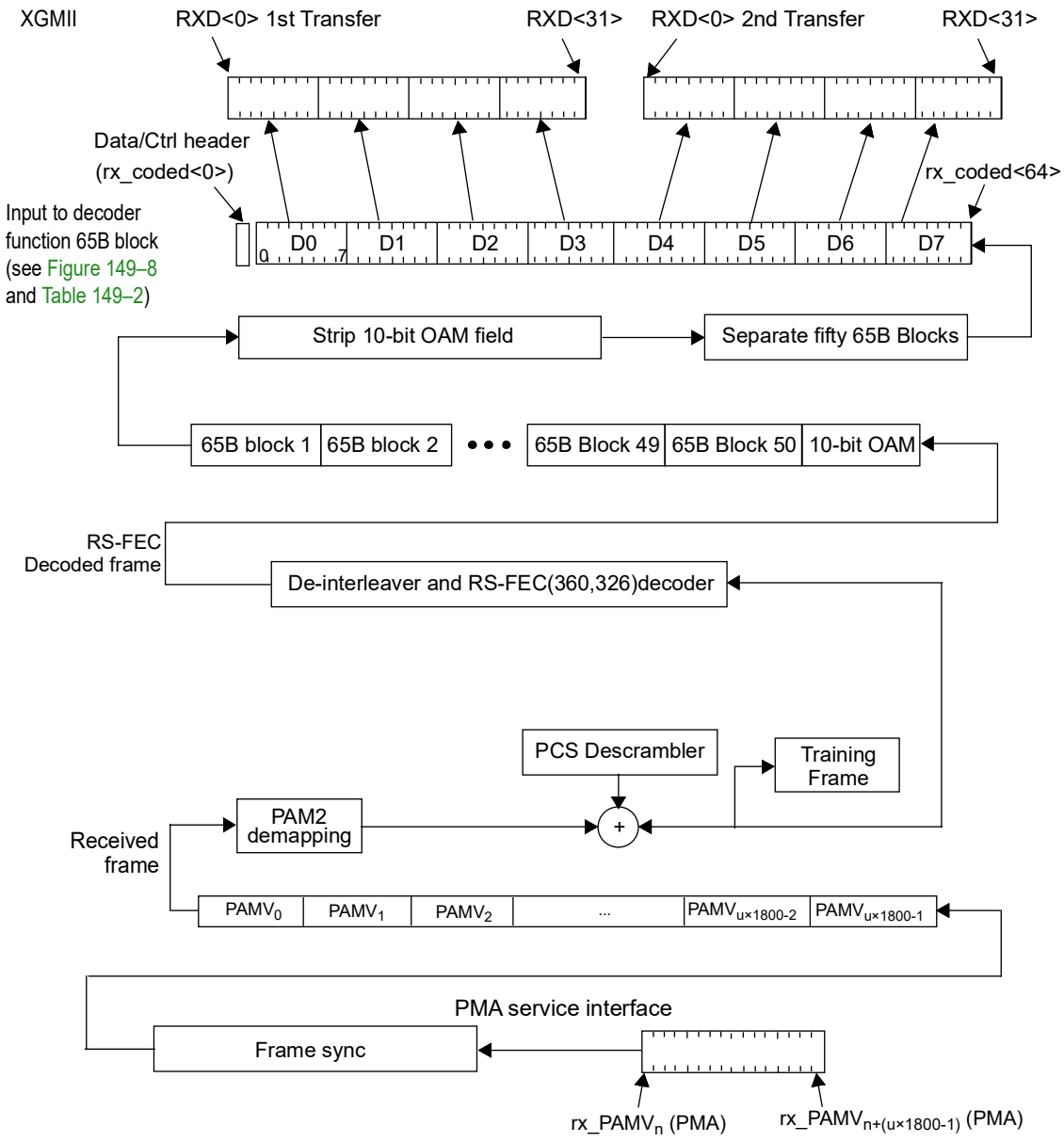
NOTE 1—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the XGMII.
NOTE 2—Figure shown for L = 1.
NOTE 3—For PAM2 path, V=2 and u=2. For PAM4 path, V=4 and u=1.

Figure 201–13—PCS 10 Gb/s Receive bit ordering for data mode and training mode, HS_RX

201.3.2.2.12 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 100 XGMII data transfers are encoded into an RS-FEC frame.

For PAM4 path HS_TX (10 Gb/s), it takes 1800 PMA_UNITDATA transfers to send an RS-FEC frame of data, and a XGMII to PMA transfer rate of exactly 1:18.



NOTE 1—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the XGMII.
NOTE 2—Figure shown for L = 1.
NOTE 3—For PAM2 path, V=2 and u=2. For PAM4 path, V=4 and u=1.

Figure 201–14—PCS 5G and 2.5G Receive bit ordering for data mode and training mode, HS_RX

For PAM2 path HS_TX (5 Gb/s and 2.5 Gb/s), it takes 3600 PMA_UNITDATA transfers to send an RS-FEC frame of data, and a XGMII to PMA transfer rate of exactly 1:36.

Therefore, for MultiG+100MBASE-T1/V1, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 1:18, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 201–18). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and PCS scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

201.3.2.2.13 RS-FEC framing and RS-FEC encoder

The resulting RS-FEC frame of 50 65B blocks, followed by the 10-bit OAM field and 340 parity bits is 3600 bits. See Figure 201–11 and Figure 201–12 for details on PCS bit ordering. See 201.3.2.2.16 for details on RS-FEC encoding.

The RS-FEC encoding takes the 3260-bit vector, consisting of tx_group50x65B, and the 10-bit OAM_field, and shall generate the 34 10-bit parity symbols (340 bits total).

201.3.2.2.14 RS-FEC superframe and round-robin interleaving

As specified in 149.3.2.2.15.

201.3.2.2.15 RS-FEC recombine

As specified in 149.3.2.2.16.

201.3.2.2.16 Reed-Solomon encoder

As specified in 149.3.2.2.17.

201.3.2.2.17 PCS scrambler PAM4

As specified in 149.3.2.2.18.

201.3.2.2.18 PCS scrambler PAM2

The bits of the interleaved RS-FEC superframe are presented as D_n, where n is an index indicating the symbol number, and are scrambled using an additive PCS scrambler. The scrambling sequence DS_n is equal to $Scr_n[0]$ defined in 201.3.4.

All incoming PAM2 path HS_RX (5 Gb/s and 2.5 Gb/s) data bits are D_n, which are represented in Figure 201–7 as $D_n[0]$. The DS_n are applied as an additive PCS scrambler sequence to each incoming data bit, D_n, to generate a single scrambled data bit, A_n, as shown in Equation (201–1).

$$A_n = DS_n \oplus D_n \quad (201–1)$$

201.3.2.2.19 Gray mapping for PAM4 encoding

As specified in 149.3.2.2.19.

201.3.2.2.20 Selectable precoder

As specified in 149.3.2.2.20 for PAM4 only.

201.3.2.2.21 PAM4 encoding

As specified in 149.3.2.2.21.

201.3.2.2.22 PAM2 encoding

The PCS Transmit process shall encode each output symbol to one of two PAM2 levels as specified in this subclause.

The PAM2 encoded symbols are denoted M(*n*), where:

n is an index indicating the symbol number.

Each consecutive output symbol, A_n, is mapped to one of two PAM2 levels and assigned to the PAM2 encoder output M(*n*).

Mapping from the output symbol A_n to a PAM2 encoded symbol M(*n*) is as follows:
0 maps to +1, and
1 maps to –1.

201.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 201–19 and the PCS Receive bit ordering in Figure 201–13 for 10 Gb/s and Figure 201–14 for 5 Gb/s and 2.5 Gb/s, including compliance with the associated state variables as specified in 201.3.6.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received symbols are demapped and descrambling is performed.

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into a 10-bit OAM field and 50 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 201–19). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the PCS descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor state diagram shown in Figure 201–17 monitors the received signal for high RS-FEC frame error ratio and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS

Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment bit every 450 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an Infofield, which is inserted in the 16th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

201.3.2.3.1 Frame and block synchronization

When operating in the data mode, a 100M+10GBASE-T1/V1 PHY's HS_RX PCS shall form a PAM4 stream from the PMA_UNITDATA.indication primitive as specified in 149.3.2.3.1.

When operating in the data mode, a 100M+2.5GBASE-T1/V1 PHY and a 100M+5GBASE-T1/V1 PHY's HS_RX PCS's each shall form a PAM2 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM2_0 to rx_PAM2_3599 (see Figure 201–13). It obtains block_lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

201.3.2.3.2 Frame and block synchronization

When operating in the data mode, a 100M+10GBASE-T1/V1 PHY's HS_RX PCS shall form a PAM4 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM4_0 to rx_PAM4_1799 (see Figure 201–13). It obtains block lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

When operating in the data mode, a 100M+2.5GBASE-T1/V1 PHY and a 100M+5GBASE-T1/V1 PHY's HS_RX PCS shall form a PAM2 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM2_0 to rx_PAM2_3599 (see Figure 201–13). It obtains block_lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

201.3.2.3.3 PCS descrambler

The descrambling process is as specified in 149.3.2.3.2, except Equation (149-6) shall be applied regardless of whether PHY_D is LEADER or FOLLOWER.

201.3.2.3.4 Invalid blocks

As specified in 149.3.2.3.3.

201.3.3 Test-pattern generators

As specified in 149.3.3.

201.3.4 PCS scrambler polynomials

The PCS scrambler shall employ Equation (149-6) as specified for $g_S(x)$ in 149.3.4. Equation (149-6) is applied regardless of whether PHY_S is LEADER or FOLLOWER.

201.3.5 HS_PATH PMA training frame

During PMA training, the training frames are embedded with indicators to establish alignment to the RS-FEC superframe composed of 16 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners.

For 10 Gb/s, the timing relationship among training frame, partial frame, RS-FEC frame, superframe, and partial PHY frame count (PFC24) are shown in Figure 201–16.

For 2.5 Gb/s and 5 Gb/s, the timing relationship among training frame, partial frame, RS-FEC frame, superframe, and partial PHY frame count (PFC24) are shown in Figure 201–15.

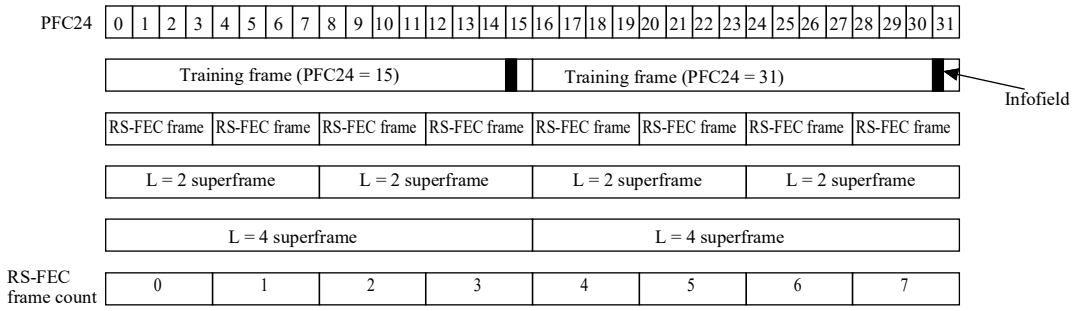


Figure 201–15—Timing relationship to PFC24 for 10G

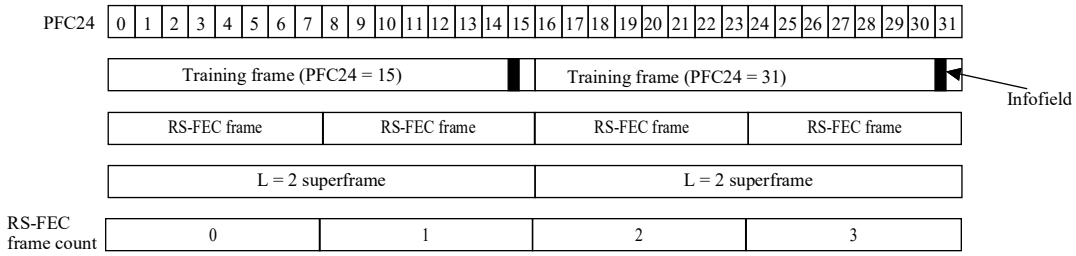


Figure 201–16—Timing relationship to PFC24 for 2.5G and 5G

PMA training frame encoding is based on the generation, at time n, of the bit S_n. The first bit is inverted in the first 15 partial PHY frames of each RS-FEC block. The first 96 bits of the 16th partial PHY frame are XORed with the contents of the Infofield. Each partial PHY frame is 450 bits long, beginning at S_n where (n mod 450) = 0. See Equation (201–2).

$$S_n = \begin{cases} Scr_n[0] \oplus InfoField_{(n \bmod 450)} & 6750 \le (n \bmod 7200) \le 6845 \\ Scr_n[0] \oplus 1 & \text{else if } (n \bmod 450) = 0 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad (201–2)$$

201.3.5.1 Generation of symbol Tn

The bit S_n is mapped to the transmit symbol T_n as follows, if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = –1$.

201.3.5.2 PMA training mode PCS descrambler polynomials

The PHY shall acquire PCS descrambler state synchronization to the PAM2 training sequence and report success through scr_status. For PCS descrambling, the high speed receiver employs the receiver PCS descrambler generator polynomial per 201.3.4.

201.3.6 Detailed functions and state diagrams

201.3.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

201.3.6.2 State diagram parameters

201.3.6.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

RFER_CNT_LIMIT
: TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
: TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.
The Link Interruption ordered set is defined in 46.3.4.

201.3.6.2.2 Variables

block_lock
: Boolean variable that is set TRUE when receiver acquires block delineation.

hi_rfer
: Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one RFRX_CNT_LIMIT interval.

pcs_data_mode
: Variable set by the PMA PHY Control function. See 201.5.2.6.2.

pcs_reset
: Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary

including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

rf_valid
Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

tx_coded<64:0>
Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

201.3.6.2.3 Timers

rfer_timer
Timer that is triggered every $\frac{125}{4 \times S}$ μs +1%, –25%. When the timer reaches its terminal count, rfer_timer_done = TRUE. See Table 201–1 for the definition of *S*.

201.3.6.2.4 Functions

DECODE(rx_coded<64:0>)
In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 149.3.2.2.2.

ENCODE(tx_raw<71:0>)
Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 201.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E}
This function classifies each 65-bit rx_coded vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.
A vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x1E and eight valid control characters other than /E/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.
S; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.
T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a data/ctrl header of 0.
E; The vector does not meet the criteria for any other value.

A valid control character is one containing a MultiGBASE-T1 control code specified in Table 149–2. A valid O code is one containing an O code specified in Table 149–2.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 72-bit tx_raw vector as belonging to one of the five types {C, S, T, D, E} depending on its contents. A vector belongs to only one type.

Values: C; The vector contains one of the following:
a) Eight valid control characters other than /O/, /S/, /T/, and /E/;
b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
c) Two valid ordered sets.
S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.
T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.
D; The vector contains eight data characters.
E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 149–2. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 149–2.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

T_TYPE_NEXT

Prescient end of packet check function. It returns the FRAME_TYPE of the tx_raw vector immediately following the current tx_raw vector.

201.3.6.2.5 Counters

rfer_cnt
: Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt
: Count number Reed-Solomon frames received during current period.

201.3.6.2.6 Messages

RX_FRAME
: A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

201.3.6.3 State diagrams

The RFER monitor state diagram shown in Figure 201–17 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 201–18 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

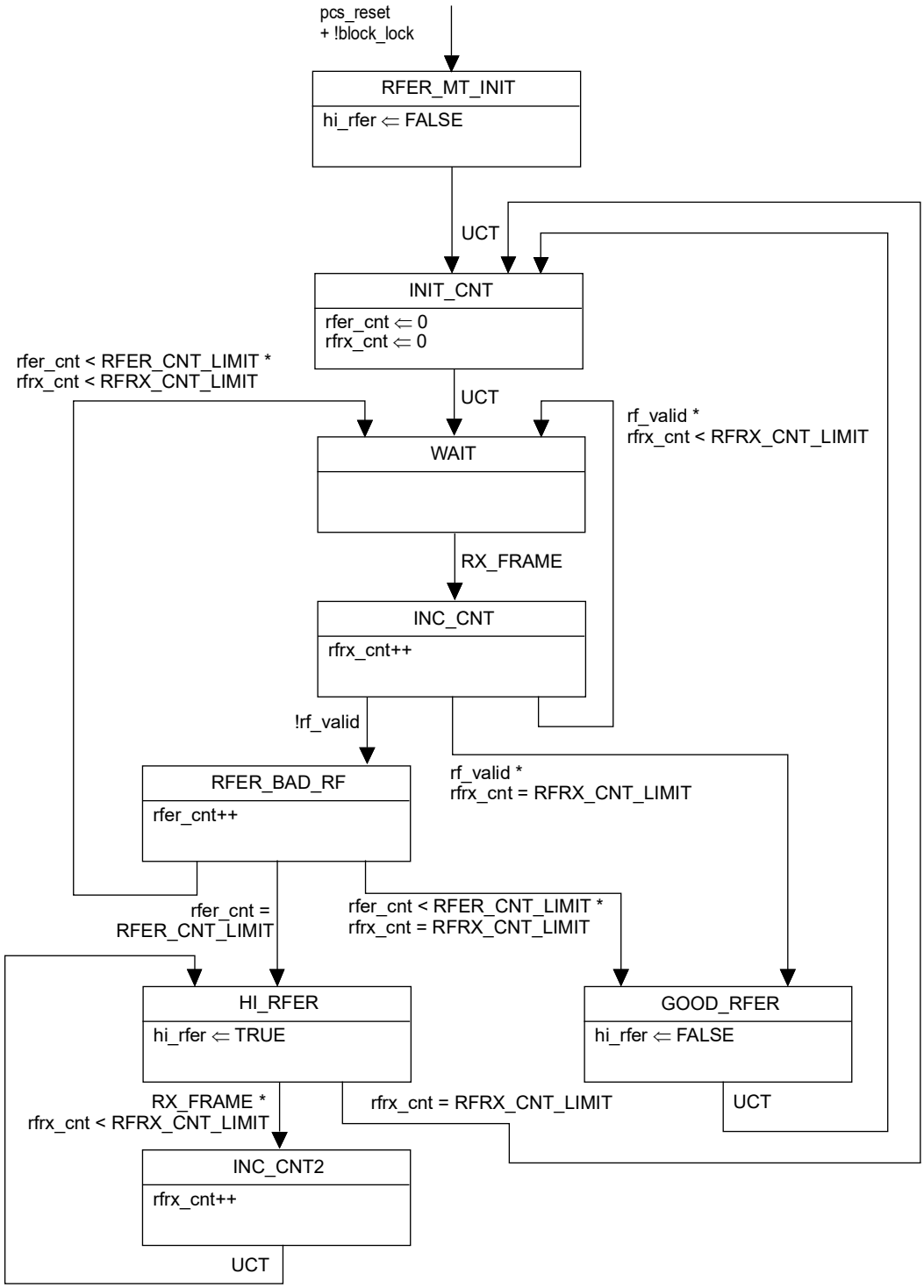


Figure 201–17—RFER monitor state diagram

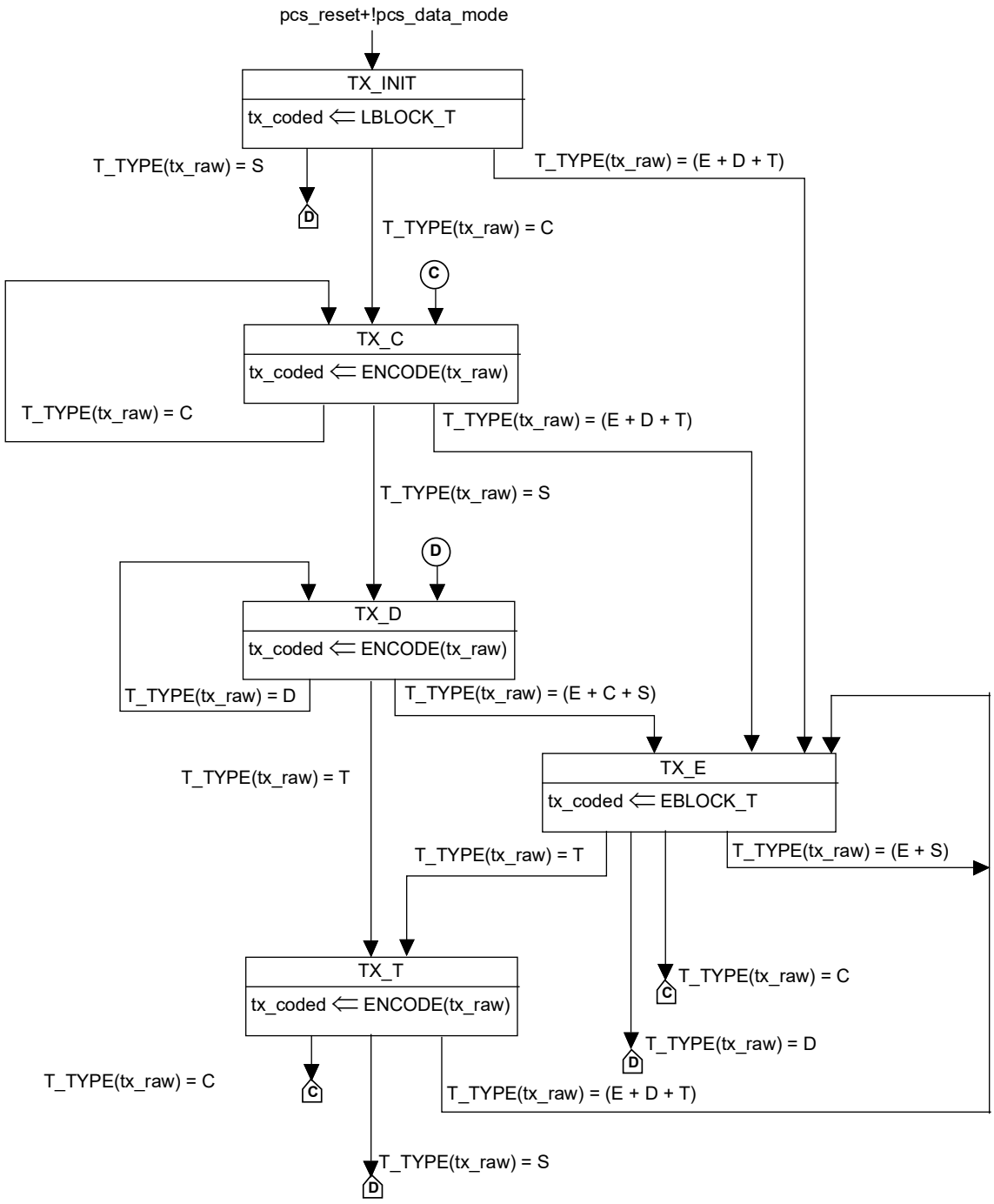


Figure 201–18—PCS 64B/65B Transmit state diagram

The PCS 64B/65B Receive state diagram is shown in Figure 201–19 and controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams.

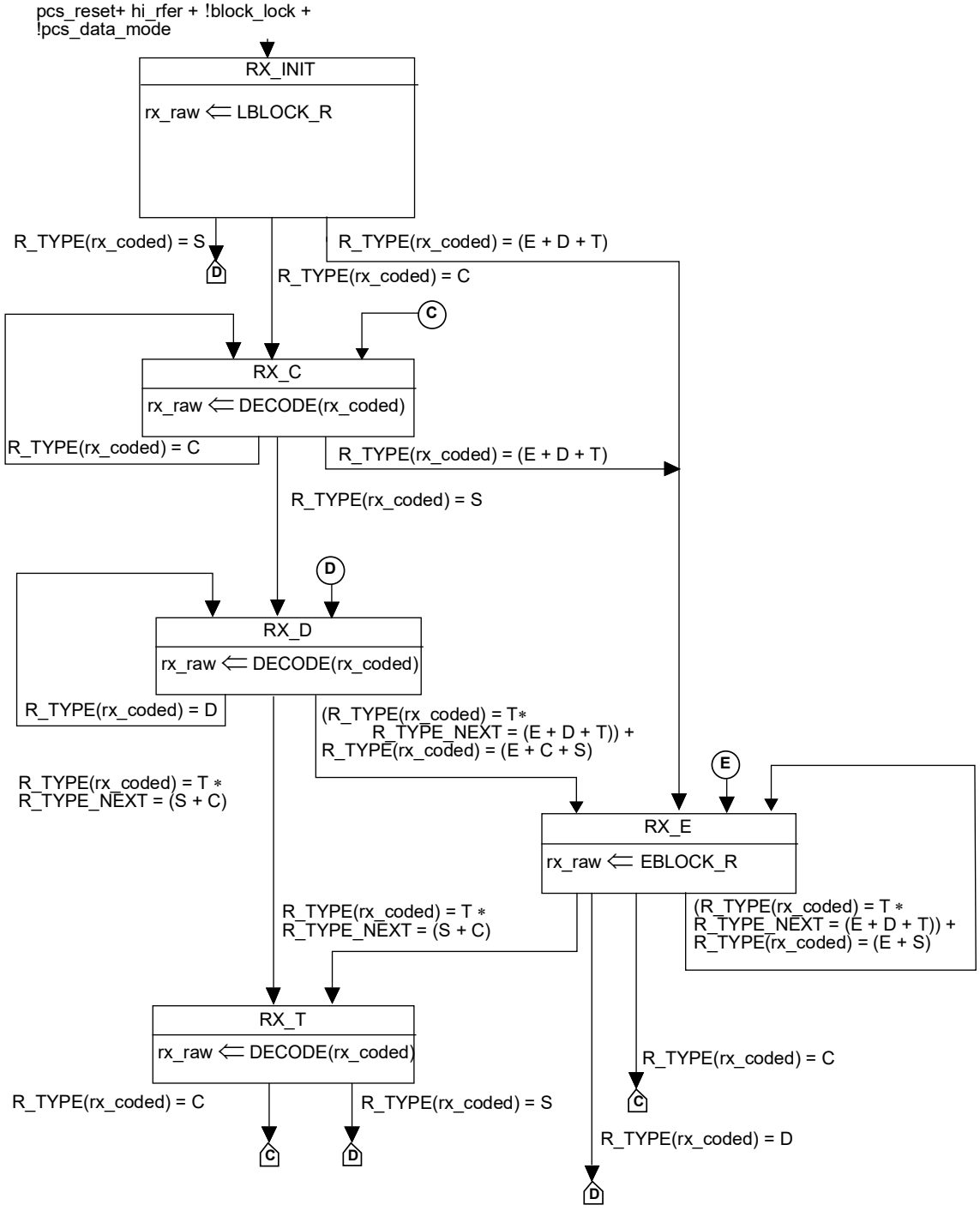


Figure 201–19—PCS 64B/65B Receive state diagram

201.3.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

201.3.7.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO bit 3.2323.2 and the inverse of this status is reflected in MDIO bit 3.2323.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

201.3.7.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 201–17) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

201.3.8 MultiG+100MBASE-T1/V1 operations, administration, and maintenance (OAM)

The MultiG+100MBASE-T1/V1 PCS level operations, administration, and maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. When OAM is implemented, behavior is defined in 149.3.9, including the state diagrams in Figure 149–24 and Figure 149–25.

The OAM frame data is carried in the OAM 10-bit field described in 201.3.2.2.13 for HS_PATH.

OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one at a time into the OAM field in each Reed Solomon frame in the HS_PATH and LS_PATH.

201.3.8.1 Definitions

The definitions for OAM are as defined in 149.3.9.1 for OAM frame, OAM symbol, OAM message, and OAM status.

OAM field: A 10-bit field in each RS-FEC frame reserved for the OAM symbol as described in 201.3.2.2.14.

201.3.8.2 Functional specifications

MultiG+100MBASE-T1/V1 OAM functions are the same as those defined for a MultiGBASE-T1 PHY in 149.3.9.2 with the exception that the MultiG+100MBASE-T1/V1 OAM frame structure, PHY health, and PHY health indicator are defined in 201.3.8.2.1.

201.3.8.2.1 MultiG+100MBASE-T1/V1 OAM frame structure

The MultiG+100MBASE-T1/V1 OAM frame structure is defined in 149.3.9.2.1 with the removal of Low Power Idle operation.

Each OAM frame is made up of 16 OAM symbols. Each of the first 14 symbols is made up of one octet of data, one framing bit, and one reserved bit. The last 2 symbols are the Reed-Solomon (16,14) parity symbols.

One OAM symbol is placed in the 10-bit OAM field in each PHY frame during normal power operation in the data mode. The sixteen OAM symbols are consecutively inserted into sixteen consecutive PHY frames. Once the sixteen symbols of the current OAM frame are inserted, the sixteen symbols of the next OAM frame are inserted. This process is continuous without any break in the insertion of OAM symbols.

When the PCS frame is operating in interleaved mode of 2x or 4x, the first symbol (OAM<0>) shall be inserted in the first RS frame in the superframe so that the full OAM frame can be packed into eight superframes in the 2x interleaved mode, and into four superframes in the 4x interleaved mode.

Bit 0 of each OAM symbol is the first bit transmitted in the 10-bit OAM field. Symbol 0 is the first symbol transmitted in each OAM frame.

The OAM frame boundary can be found at the receiver by looking at bit D8. The boundary is a 0 followed by thirteen 1's followed by two don't care.

If OAM is not implemented then the 10-bit OAM field shall be set to all 0's. If the link partner does not implement OAM, the 10-bit OAM field will remain static.

201.3.8.2.2 PHY health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame
- 01: Reserved
- 10: PHY SNR is marginal
- 11: PHY SNR is good

201.3.8.2.3 PHY health indicator

The PHY current health is sent to the link partner on a per OAM frame basis using the SNR<1:0> bits as described in 201.3.8.2.2. It lets the link partner have an early indication of potential problems that can cause the PHY to drop link or have high error rates.

201.3.8.3 State diagram variable to OAM register mapping

See 149.3.9.3.

201.3.8.4 Detailed functions and state diagrams

See 149.3.9.4.

201.4 Physical Coding Sublayer (PCS) functions, low speed path (LS_PATH)

201.4.1 PCS service interface (MII)

The LS_TX PCS service interface allows the 100M+MultiGBASE-T1/V1 PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46. The XGMII is running at 1/100th the rate of 10 Gb/s, 1/50th the rate of 5 Gb/s, and 1/25th the rate of 2.5 Gb/s.

201.4.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions, one of which is the LS_PATH and the other is the HS_PATH. This subclause discusses the LS_PATH. The LS_PATH PCS operating functions are the LS_TX PCS Transmit in the PHY_D device, and the LS_RX PCS Receive in the PHY_S device. All operating functions start immediately after the successful completion of the PCS Reset function.

The PHY_D PCS reference diagram, Figure 201–8, and PHY_S PCS reference diagram, Figure 201–7, show how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 201–8 and Figure 201–7.

201.4.2.1 PCS Reset function

The low data rate PCS reset function shall be as specified in 149.3.2.1.

201.4.2.2 PCS Transmit function

The PCS Transmit function shall comply with the PCS 64B/65B Transmit state diagram in Figure 149-16 and to the PCS Transmit bit ordering in Figure 201–21.

Dashed rectangles in Figure 149-16 are not part of the low speed PCS.

When communicating with the XGMII, the 100M+MultiGBASE-T1/V1 PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the eight XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take one group of four 65B blocks and append a 10-bit OAM field followed by a 6-bit vendor-specific field. When the 6-bit vendor-specific field is not used, it is recommended that it be set to 0x3F. This forms the input to RS-FEC which adds 24 parity bits. The resulting 300 bits are then scrambled. These bits

are then sent one bit at a time. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, *T*, is 1000 ÷ 117.1875 ns.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

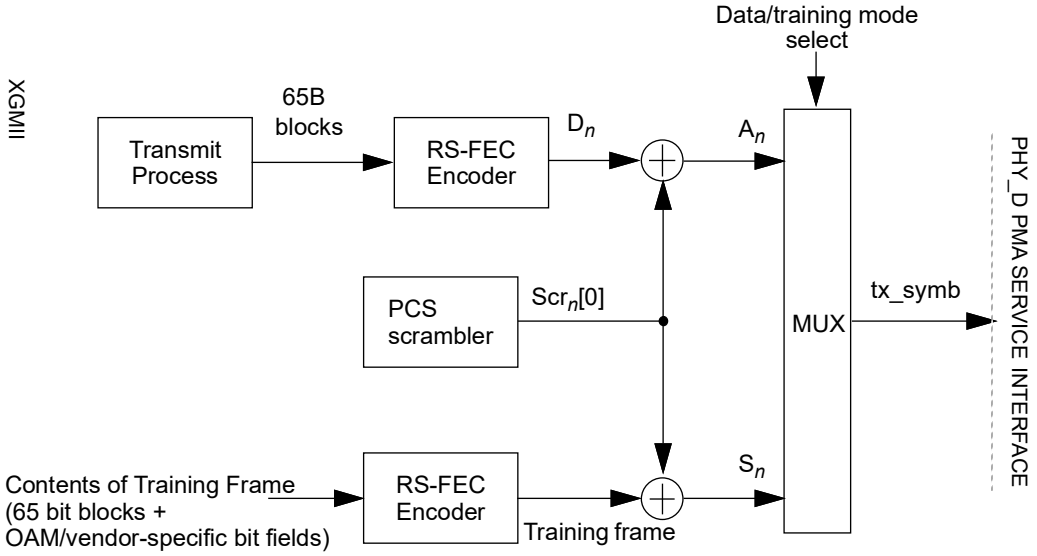
If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a Z symbol at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (S_n) defined in 201.4.5 to the PMA via the PMA_UNITDATA.request primitive.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 201.5.2.4.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, four blocks of 65B encoded bits are appended with a 10-bit OAM field followed by a 6-bit vendor specific field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes Reed-Solomon encoders to generate and append 24 parity check bits to form 300-bit (50,46, 6) RS-FEC frames.

A block diagram of the low speed path PCS Transmit functions is shown in Figure 201–20.



NOTE – The RS-FEC encoder for the data mode and training mode paths is the same (See 201.4.5), but are shown in separate chains for clarity.

Figure 201–20—PCS Transmit function block diagram for low speed path

201.4.2.2.1 Use of blocks

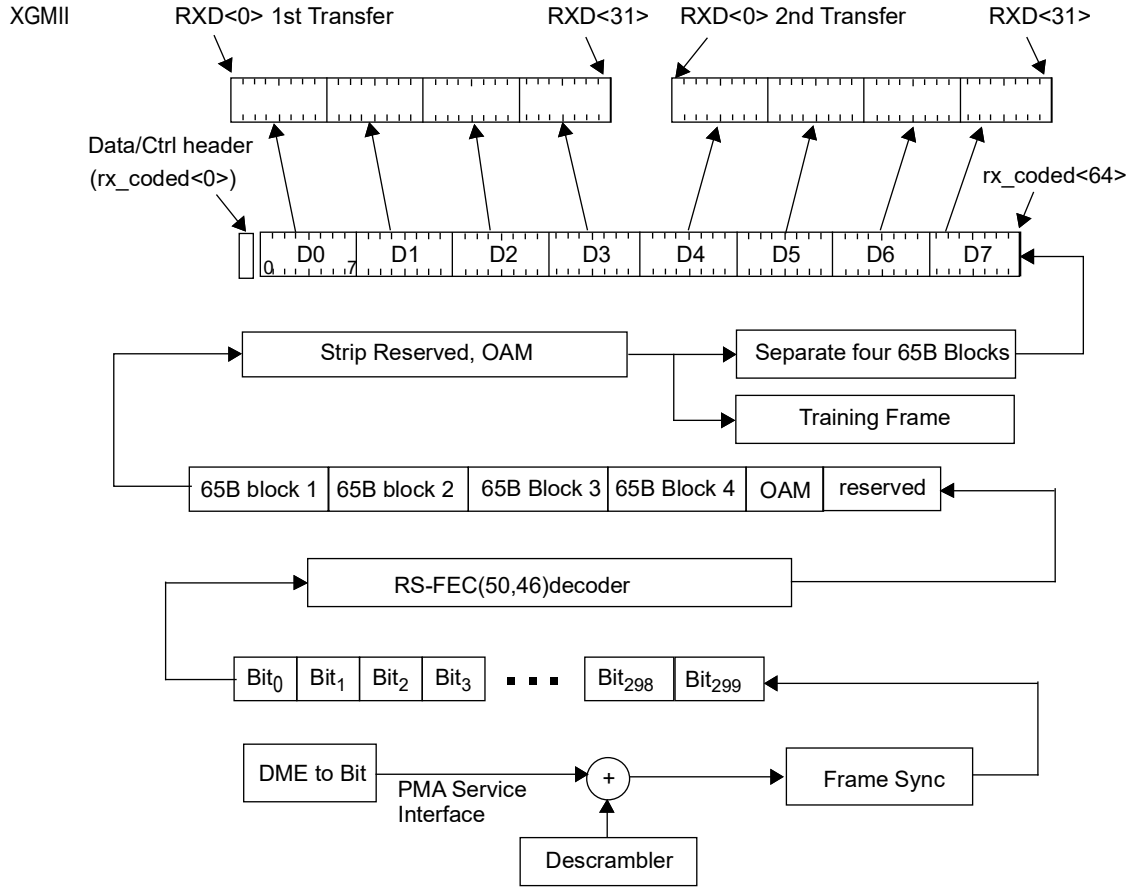
The PCS Transmit function maps XGMII signals into 65-bit blocks that are inserted into an RS-FEC frame. The PCS Receive function extracts the 65-bit blocks from the RS_FEC frame and maps them to the receiver XGMII interface. The PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS.

The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 201.4.2.2.

201.4.2.2.2 65B RS-FEC transmission code

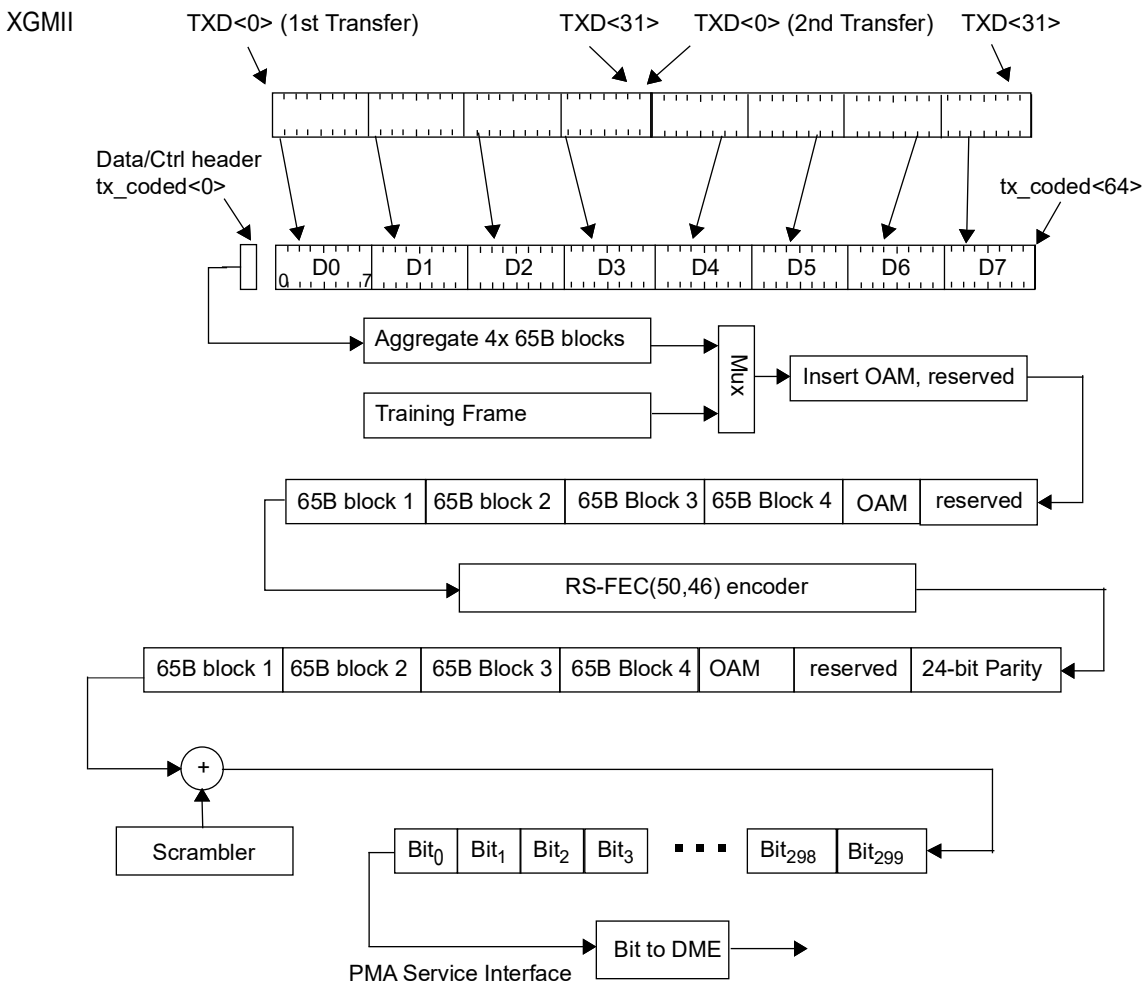
The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 201–21 for transmit and Figure 201–22 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.



NOTE 1—DME to bit mapping is done in the PMA.

Figure 201–22—PCS Receive bit ordering for data mode and training mode, LS_RX



NOTE 1—Bit to DME mapping is done in the PMA.

Figure 201–21—PCS Transmit bit ordering for data mode and training mode, LS_TX

201.4.2.2.3 Notation conventions

In all figures, for values shown as binary, the leftmost bit is the first transmitted bit.

The 64B/65B encoding, encodes eight data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7.

For 100M+MultiGBASE-T1/V1, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

201.4.2.2.4 Block structure

The low data rate block structure shall be as specified in 149.3.2.2.4

201.4.2.2.5 Control codes

The same set of control characters are supported by the XGMII and the LS_TX PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The LS_TX PCS encodes the start and terminate control characters implicitly by the block type field. The LS_TX PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The LS_TX PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to LS_TX control codes and XGMII control codes are specified in Table 149–2. The LPI Control character is not used by the 100M+MultiGBASE-T1/V1 PHY. All XGMII control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

201.4.2.2.6 Ordered sets

The low data rate ordered sets shall be as specified in 149.3.2.2.6.

201.4.2.2.7 Idle (/I/)

The low data rate ordered sets shall be as specified in 149.3.2.2.7.

201.4.2.2.8 Start (/S/)

The low data rate ordered sets shall be as specified in 149.3.2.2.9.

201.4.2.2.9 Terminate (/T/)

The low data rate ordered sets shall be as specified in 149.3.2.2.10.

201.4.2.2.10 Ordered set (/O/)

The low data rate ordered sets shall be as specified in 149.3.2.2.11.

201.4.2.2.11 Error (/E/)

The low data rate ordered sets shall be as specified in 149.3.2.2.12.

201.4.2.2.12 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. Eight XGMII data transfers are encoded into an RS-FEC frame. It takes 300 PMA_UNITDATA transfers to send an RS-FEC frame of data. Therefore, for 100M+MultiGBASE-T1/V1, if the PCS is connected to an

XGMII and PMA sublayer where the ratio of their transfer rates is exactly 2:75, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 149-16). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and PCS scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload

201.4.2.2.13 RS-FEC framing and RS-FEC encoder

The resulting RS-FEC frame of four 65B blocks, followed by ten OAM bits, six vendor-specific bits, and 24 parity bits is 300 bits. See Figure 201–21 and 201.4.2.2.14 for details on PCS bit ordering and RS-FEC encoding.

The RS-FEC encoding takes the 276-bit vector, consisting of tx_group4x65B, the ten OAM bits, and six vendor-specific bits, and shall generate the four 6-bit parity symbols (24 bits total).

201.4.2.2.14 Reed-Solomon encoder

The data frame is encoded using a Reed-Solomon encoder (see Figure 201–23) operating over the Galois Field GF (2^6) where the symbol size is six bits. The encoder processes forty-six 6-bit RS-FEC message symbols to generate four 6-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of fifty 6-bit RS-FEC symbols. The particular Reed-Solomon code is denoted as RS-FEC(50,46,6).

The code is based on the generating polynomial given by Equation (201–3).

$$g(x) = \prod_{j=0}^{3} (x - \alpha^j) = g_4x^4 + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (201–3)$$

In Equation (201–3), α, is a primitive element of the finite field defined by the primitive polynomial 0x43 = $x^6 + x + 1$.

Equation (201–4) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{45} to m_0.

$$m(x) = m_{45}x^{49} + m_{44}x^{48} + \ldots + m_1x^5 + m_0x^4 \quad (201–4)$$

Each message symbol m_i is the bit vector ($m_{i,5}$, $m_{i,4}$, ... $m_{i,1}$,$m_{i,0}$), which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<275:0> where
$m_{i,j}$ = tx_RSmessage <(45 – i) × 6 + j>, for i = 0 to 45, and j = 0 to 5.

tx_RSmessage<275:0> prior to RS-FEC(50,46) encoder is formed as follows:

tx_RSmessage<259:0> = tx_group4x65B<259:0>.
tx_RSmessage<269:260> = OAM_field<9:0>.
tx_RSmessage<275:270> = vendor-specific_fielld<5:0>.

The first symbol input to the encoder is m_{45}.

Equation (201–5) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_3 to p_0.

$$p(x) = p_3x^3 + p_2x^2 + p_1x + p_0 \quad (201–5)$$

Each parity symbol p_i is the bit vector $(p_{i,5}, p_{i,4}, \ldots p_{i,1}, p_{i,0})$, which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 201–23. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x, $c_{49} = m_{45}$ is transmitted first and the coefficient of the lowest power of x, $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

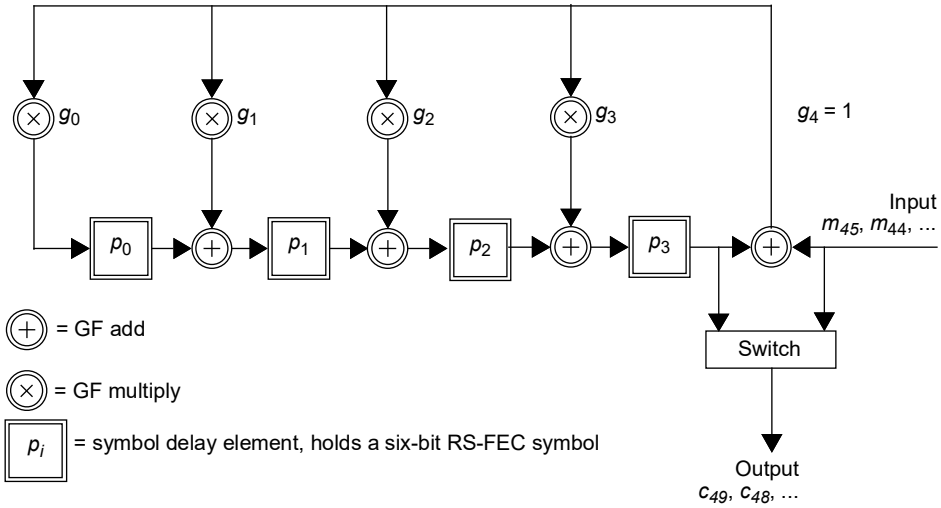


Figure 201–23—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 201–3.

Table 201–3—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(50, 46)
0	3
1	59
2	54
3	15
4	1

201.4.2.2.15 PCS scrambler

The bits of the RS-FEC frame are scrambled using an additive PCS scrambler. For each bit, D_n, a scrambler bit is generated from the PCS scrambler. The scrambler bit, DS_n, is equal to $Scr_n[0]$ of $g_M(x)$ defined in 201.4.4.

DS_n is applied as additive scrambler sequences to incoming data bits D_n to generate the scrambled data bit A_n as shown in Equation (201–6).

$$A_n = D_n \oplus DS_n \quad (201–6)$$

The parameter tx_symb is set to A_n for passing to the PMA when PHY control is in SEND_N mode.

201.4.2.2.16 Reed-Solomon encoder

As specified in 149.3.2.2.17.

201.4.2.2.17 PCS scrambler PAM4

As specified in 149.3.2.2.18.

201.4.2.2.18 PCS scrambler PAM2

The bits of the interleaved RS-FEC superframe are presented as D_n, where n is an index indicating the symbol number, and are scrambled using an additive PCS scrambler. The scrambling sequence DS_n is equal to $Scr_n[0]$ defined in 201.3.4.

All incoming PAM2 path HS_RX (5 Gb/s and 2.5 Gb/s) data bits are D_n, which are represented in Figure 201–7 as $D_n[0]$. The DS_n are applied as an additive PCS scrambler sequence to each incoming data bit, D_n, to generate a single scrambled data bit, A_n, as shown in Equation (201–7).

$$A_n = DS_n \oplus D_n \quad (201–7)$$

201.4.2.2.19 Gray mapping for PAM4 encoding

As specified in 149.3.2.2.19.

201.4.2.2.20 Selectable precoder

As specified in 149.3.2.2.20 for PAM4 only.

201.4.2.2.21 PAM4 encoding

As specified in 149.3.2.2.21.

201.4.2.2.22 PAM2 encoding

The PCS Transmit process shall encode each output symbol to one of two PAM2 levels as specified in this subclause.

The PAM2 encoded symbols are denoted M(n), where:

n is an index indicating the symbol number.

Each consecutive output symbol, A_n, is mapped to one of two PAM2 levels and assigned to the PAM2 encoder output M(n).

Mapping from the output symbol A_n to a PAM2 encoded symbol M(n) is as follows:
0 maps to +1, and
1 maps to –1.

201.4.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 149-18, and the PCS Receive bit ordering in Figure 201–22 including compliance with the associated state variables as specified in 149.3.7.2.2.

Dashed rectangles in Figure 149-18 are not part of the low speed PCS.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received symbols are demapped and descrambling is performed.

Following descrambling, the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into ten OAM bits and six Reserved bits and four 64B/65B blocks. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 149-18). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received training framing and signals the reliable acquisition of the PCS descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If forty consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment pattern every 300 symbols, which can be used to find the RS-Frame boundary. The PCS descrambler employs the generator polynomial per Equation (149–5). When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

201.4.2.3.1 Frame and block synchronization

When operating in the training and data modes, the receiving PCS shall form a bit stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from Bit_0 to Bit_{299} (see

Figure 201–22). PCS Receive obtains block_lock to the PHY frames during training using synchronization bits provided in the training frames.

201.4.2.3.2 PCS descrambler

The descrambling process is as specified in 149.3.2.3.2, except Equation (149-5) shall be applied regardless of whether PHY_S is LEADER or FOLLOWER.

201.4.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 149–2.
c) Any O code contains a value not in Table 149–2.
d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 201.4.2.2.14. If the check fails, the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

201.4.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode, it shall transmit continuously by setting zero input and any non-zero initial condition to the PCS scrambler.

When the receiver PCS is operating in test-pattern mode, it shall receive continuously as illustrated in Figure 201–22. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 in 201.6.1.

201.4.4 PCS scrambler polynomials

The PCS scrambler shall employ Equation (149-5) as specified for $g_M(x)$ in 149.3.4 regardless of whether PHY_S is LEADER or FOLLOWER.

201.4.5 PMA training frame

During PMA training, the PHY operates as shown in Figure 201–20 and Figure 201–21. The four 64B/65B blocks in the FEC frame are loaded with the internal training frame, consisting of three consecutive blocks of all zeros and the fourth block being a special control block, containing the Infofield. The structure of the Infofield is shown in Figure 201–30.

The fields in the Infofield are transmitted from left to right starting with C/D. The Block field as well as fields D0 through D6 are transmitted LSB first. Reserved bits in the Infofield represent unused values and shall be set to zero on transmit and ignored when received by the link partner.

The message and PHY capability fields are as specified in 201.5.2.5.3 and 201.5.2.5.4.

The four 65-bit blocks of the training frame, tx_group4x65B block, as defined in 201.1.3.2, are transmitted as described in 201.4.2.2.14. The four training frame 64B/65B blocks are then concatenated with the 10

OAM bits, six vendor-specific bits, and the 24 FEC parity bits, as shown in Figure 201–24. Zeros shall be transmitted in the OAM field of the training frame. Reserved bits shall be transmitted as defined by 201.5.2.4.1. RS-FEC parity bits are generated from the training frame contents by the RS-FEC encoder specified in 201.4.2.2.14.

After the training frame is assembled, it is scrambled and DME encoded as described in 201.4.2.2.15 and 201.5.2.2.1 respectively.

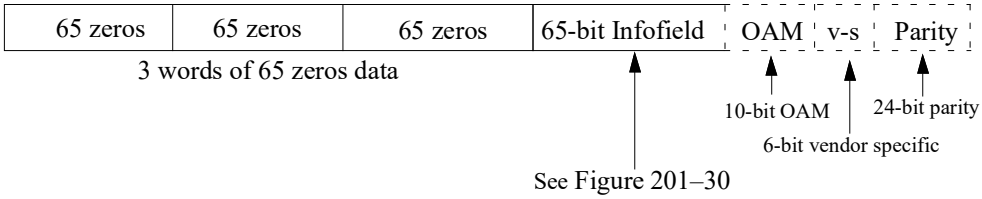


Figure 201–24—Training frame

S_n defines the training frame bit at time n, see Equation (201–8)

(201–8)

$$S_n = \begin{cases} Scr_n[0] \oplus \text{Infofield} & 195 \le (n \bmod 300) \le 259 \\ Scr_n[0] \oplus \text{OAM} & 260 \le (n \bmod 300) \le 269 \\ Scr_n[0] \oplus \text{6bit v-s} & 270 \le (n \bmod 300) \le 275 \\ Scr_n[0] \oplus \text{Parity} & 276 \le (n \bmod 300) \le 299 \\ Scr_n[0] & \text{otherwise} \end{cases}$$

201.4.5.1 PMA training mode PCS descrambler polynomials

The PHY shall acquire PCS descrambler state synchronization to the DME training sequence and report success through scr_status. For PCS descrambling, the low speed receiver employs the receiver PCS descrambler generator polynomial per 201.4.4. The resulting symbols are transferred to the PMA when PHY control is in SEND_T mode for DME encoding and transmission.

201.4.6 Detailed functions and state diagrams

Detailed functions and state diagrams are as specified for MultiGBASE-T1 PHYs in 149.3.7, except items enclosed in the dotted lines are not present in the MultiG+100M/100M+MultiGBASE-T1/V1 PHY.

201.4.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

201.4.7.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO bit 3.2323.2 and the inverse of this status is reflected in MDIO bit 3.2323.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

201.4.7.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 149–15) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

201.4.8 100M+MultiGBASE-T1/V1 operations, administration, and maintenance (OAM)

The MultiG+100MBASE-T1/V1 PCS level operations, administration, and maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. When OAM is implemented, behavior is defined in 149.3.9, including the state diagrams in Figure 149–24 and Figure 149–25.

The OAM frame data is carried in the OAM 10-bit field described in 201.4.2.2.13 for LS_PATH.

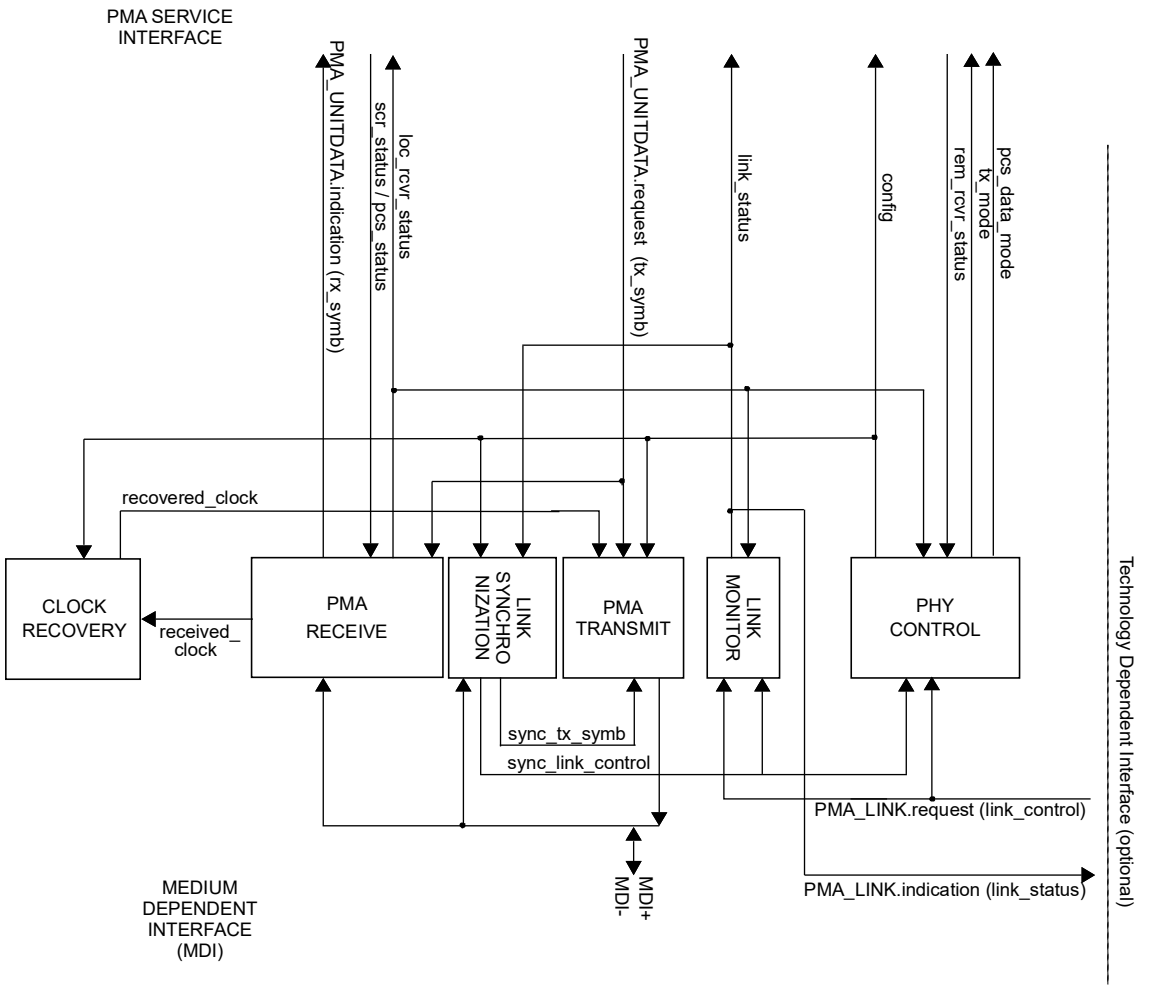
OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one at a time into the OAM field in each Reed Solomon frame in the HS_PATH and LS_PATH.

201.5 Physical Medium Attachment (PMA) sublayer

201.5.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 201.2.2 to the MultiG+100M/100M+MultiGBASE-T1 baseband medium, specified in 201.9 and to the MultiG+100M/100M+MultiGBASE-V1 baseband medium specified in 201.10.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 201.11 for -T1 and in 201.12 for -V1.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 201–25—PMA reference diagram

201.5.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 201–25, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 201–25.

201.5.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The MultiG+100M/100M+MultiGBASE-T1/V1 PMA takes no longer than 50 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 201–31).

201.5.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a four-level modulated signal for PAM4, a two-level modulated signal for PAM2, both for HS_TX, and a DME modulated signal for LS_TX on the single balanced pair of conductors for -T1 or the single coax for -V1. When the PHY Control state diagram (Figure 201–31) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 201.6.2 for HS_TX and in 201.7.2 for LS_TX.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 201.6.2.3 for HS_TX and 201.7.2.3 for LS_TX. The LEADER-FOLLOWER relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the recovered clock of 201.5.2.9 while meeting the jitter requirements of 201.6.2.3 for HS_TX and 201.7.2.3 for LS_TX.

A PHY_D shall support operation as LEADER, and may support operation as FOLLOWER. A PHY_S shall support operation as FOLLOWER, and may support operation as LEADER.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

201.5.2.2.1 Differential Manchester encoding (DME)

When tx_mode is not SEND_T or SEND_N, PMA_UNITDATA.request conveys the tx_symb variable, A_n, to the PMA, which can take on the values of 0 and 1.

When tx_mode is SEND_Z, see 201.7.2.5 for the encoding of "Z".

The scrambled data bit, A_n, shall be encoded using Differential Manchester Encoding (DME) as defined by the following rules.

The following rules apply to encode a bit to DME:

— A “clock transition” is always generated at the start of each bit symbol.
— A “data transition” in the middle of a nominal bit period is generated if the bit to be transmitted is a logical '1'. Otherwise, no transition is generated until the next bit symbol.

See Figure 201–26 and Table 201–4.

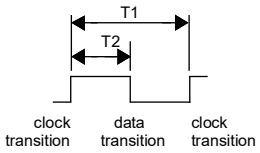


Figure 201–26—DME encoding scheme

Table 201–4—DME timings

Parameter name	Description	Nominal value[a]	Unit of measure
T1	Clock transition to clock transition	$8.5\overline{3}$	ns
T2	Clock transition to data transition (data = 1)	$4.2\overline{6}$	ns

[a]See 201.6.2.6 and 201.7.2.7 for details on bit timing tolerance.

201.5.2.3 PMA Receive function

The PMA Receive function includes a receiver for PAM4 and PAM2 for HS_RX and DME for LS_RX on the single balanced pair of conductors for -T1 or the single coax for -V1. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received at the MDI into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 201.9 for -T1 and of 201.10 for -V1.

The PMA Receive function uses the parameters pcs_status and scr_status, along with other applicable receiver status, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 201–31). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.250.7.

201.5.2.4 PHY Control Function, HS_PATH

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 201–31.

During PMA training (TRAINING and COUNTDOWN states in Figure 201–31), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the first 96 bits of the

16th partial PHY frame (bits 6750 to 6845). The Infofield is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM4 transition.

The 12-octet Infofield shall include the fields in 201.5.2.4.2 through 201.5.2.4.7, also shown in Figure 201–27 and Figure 201–28. For 10 Gb/s and 5 Gb/s, Infofield shall be transmitted at least 256 times with each change to octets 7 to 10. For 2.5 Gb/s, Infofield shall be transmitted at least 128 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 201–27—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 201–28—Infofield COUNTDOWN format

201.5.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

201.5.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0> and so forth.

201.5.2.4.3 Partial PHY frame count (PFC24)

The partial PHY frame count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 16 partial PHY frames per PHY frame and the Infofield is embedded within the 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 15.

PFC24 continues to run uninterrupted for the duration of the link. The resolution of PFC24 is large enough that it does not rollover during the allotted training time. However, it will rollover if allowed to run indefinitely. PFC24 is defined to rollover to 0 after it reaches 16 776 959.

201.5.2.4.4 Message Field

The Message Field is one octet. For the LEADER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_follower_tx<4>, reserved<3:0>}. For the FOLLOWER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 201–5 for the LEADER and Table 201–6 for the FOLLOWER. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 201–5 for the LEADER and the first or second row of Table 201–6 for the FOLLOWER. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 201–5—Infofield message field valid LEADER settings

PMA_state<7:6>	loc_rcvr_status	en_follower_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 201–6—Infofield message field valid FOLLOWER settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

201.5.2.4.5 PHY capability bits

When PMA_state<7:6> = 00, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 201–7 for the details.

The format of PHY capability bits is Oct10<2:1> = InterleaverDepth[1:0], Oct10<4:3> = PrecodeSel[1:0], Oct10<7> = OAMen, Oct8<7:0> = VendorSpecificData[7:0], and Oct9<7:0> = VendorSpecificData[15:8].

OAMen indicates MultiGBASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of optional capabilities by setting the corresponding capability bits.

Table 201–7—PHY capability bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	Reserved		Reserved		Reserved	Reserved	OAMen

The optional MultiGBASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1.

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining bits shall be reserved and set to 0.

201.5.2.4.6 Data switch partial PHY frame count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from SEND_T to SEND_N, which occurs at the start of an RS-FEC superframe. The last value of PFC24 prior to the transition is DataSwPFC24 – 1. DataSwPFC24 shall be set to an integer multiple of 16. When the value of DataSwPFC24 is a multiple of 16 the switch from SEND_T to SEND_N occurs on a PHY frame boundary. DataSwPFC24 shall be a minimum of 4081 and a maximum of 4785 from the current PFC24 value.

201.5.2.4.7 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 201–29. In Figure 201–29 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 201–29, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

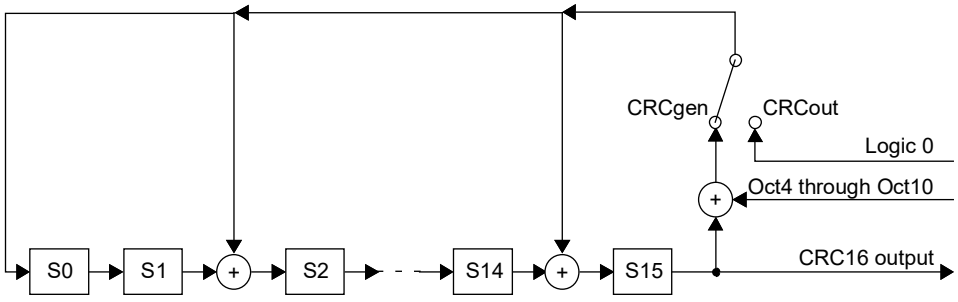


Figure 201–29—CRC16

201.5.2.4.8 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 201–8. Mapping of MDIO status variables to PMA status variables is shown in Table 201–9.

Table 201–8—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1/V1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1/V1 PMA control register	1.2309.14	PMA_transmit_disable

Table 201–9—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1/V1 PMA status register	1.2310.1	PMA_receive_fault

201.5.2.5 PHY Control function, LS_PATH

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 201–31.

During PMA training (TRAINING state in Figure 201–31), PHY Control information is exchanged between link partners with a 65-bit Infofield, which is XORed with bits 195 to 259 of the PMA training frame, see 201.4.5. The link partner is not required to decode every Infofield transmitted but is required to decode Infofields at a rate that enables the correct actions prior to the training to data mode transition.

The 65-bit Infofield shall include the fields in 201.5.2.5.2 through 201.5.2.5.6, also shown in Figure 201–30. Infofield shall be transmitted at least 128 times with each change to octets 5 to 8.

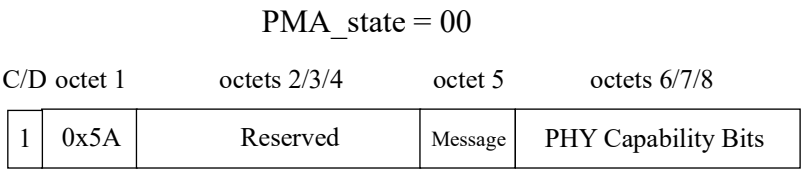


Figure 201–30—Infofield TRAINING format, LS_PATH

201.5.2.5.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

201.5.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 9 bits [C/D<0>, Octet 1<7:0>] and shall use the hexadecimal value 0x15A.

201.5.2.5.3 Message Field

The Message Field is one octet. For the LEADER, this field is represented by Oct5{PMA_state<7:6>, loc_rcvr_status<5>, en_follower_tx<4>, reserved<3:0>}. For the FOLLOWER, this field is represented by Oct5{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING.

All possible Message Field settings are listed in Table 201–5 for the LEADER and Table 201–6 for the FOLLOWER; however, the PMA_state<7:6> = 01 is not used by the LS_PATH. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 201–5 for the LEADER and the first or second row of Table 201–6 for the FOLLOWER. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

201.5.2.5.4 PHY capability bits

When PMA_state<7:6> = 00, then [Oct6<7:0>, Oct7<7:0>, Oct8<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 201–10 for the details.

Table 201–10—PHY capability bits, LS_PATH

octet 6								octet 7								octet 8							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	InterleaverDepth		PrecodeSel		Reserved	Reserved	OAMen

The format of PHY capability bits is Oct8<2:1> = InterleaverDepth[1:0], Oct8<4:3> = PrecodeSel[1:0], Oct8<7> = OAMen, Oct6<7:0> = VendorSpecificData[7:0], and Oct7<7:0> = VendorSpecificData[15:8].

OAMen indicates 100M+MultiGBASE-T1/V1 OAM capability enable. The PHY shall indicate the support of this OAM capability by setting the OAMen capability bit to 1.

The optional 100M+MultiGBASE-T1/V1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1. InterleaverDepth indicates the requested data mode interleaving depth. PrecodeSel indicates the requested precoder, available for 10G only.

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining PHY capability bits shall be reserved and set to 0.

201.5.2.5.5 Reserved fields

[Oct2<7:0>, Oct3<7:0>, Oct4<7:0>] contains a reserved field and are reserved for future use.

201.5.2.5.6 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 201–8. Mapping of MDIO status variables to PMA status variables is shown in Table 201–9.

201.5.2.6 PHY Control function, HS_PATH and LS_PATH

201.5.2.6.1 Startup Sequence

The startup sequence shall comply with the state diagram description given in Figure 201–31. If the Auto-Negotiation function is not implemented, or disabled (mr_autoneg_en = FALSE), PMA_CONFIG is predetermined to be LEADER or FOLLOWER via management control during initialization or via default hardware setup. The Auto-Negotiation function is optional for MultiG+100M/100M+MultiGBASE-T1/V1 PHYs. If the Auto-Negotiation function is implemented and enabled, Auto-Negotiation is the source of control (via link_control), PHY_D, PHY_S, and LEADER-FOLLOWER configuration; however, if Auto-Negotiation is either not enabled or is not implemented, the Link Synchronization function is the source of control (via sync_link_control) and LEADER-FOLLOWER configuration.

In the TRAINING state, PAM 2 transmission is used for the HS_PATH and DME is used for the LS_PATH. PHY capabilities are exchanged with Infofields as specified in 201.5.2.4.5.

At any time following the TRAINING state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control transitions to the TRAINING_FAILURE state and attempts a retrain.

The startup timing shall comply with Table 201–11 for PHY_S as LEADER and Table 201–12 for PHY_D as LEADER.

201.5.2.6.2 State diagram variables

auto_neg_imp
: This variable indicates if an optional Auto-Negotiation sublayer is associated with the PMA.
Values:
TRUE: An optional Auto-Negotiation sublayer is associated with the PMA.
FALSE: An optional Auto-Negotiation sublayer is not associated with the PMA.

Table 201–11—Startup timing maximums for PHY_S as LEADER

Timing interval	PHY_S (LEADER) Maximum time (ms)	PHY_D (FOLLOWER) Maximum time (ms)
Entry to SILENT state until en_slave_tx = 1 is transmitted	20 - 0.384	—
Entry to exit of SILENT state	—	20
Entry to exit of TRAINING state	29.475	29.091
Entry to exit of COUNTDOWN state	0.384	—
Entry to exit of TX_SWITCH state	—	0.384
Entry to exit of PCS_TEST state	0.525	0.525
Total (Entry to SILENT to exit of PCS_TEST state)	50	50

Table 201–12—Startup timing maximums for PHY_D as LEADER

Timing interval	PHY_D (LEADER) Maximum time (ms)	PHY_S (FOLLOWER) Maximum time (ms)
Entry to SILENT state until en_slave_tx = 1 is transmitted	20 - 0.384	—
Entry to exit of SILENT state	—	20
Entry to exit of TRAINING state	29.475	29.091
Entry to exit of COUNTDOWN state	—	0.384
Entry to exit of TX_SWITCH state	0.384	—
Entry to exit of PCS_TEST state	0.525	0.525
Total (Entry to SILENT to exit of PCS_TEST state)	50	50

config

The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.
Values: LEADER or FOLLOWER.

en_follower_tx

The en_follower_tx variable in the Infofield received by the FOLLOWER.
Values:

0: LEADER is not ready for the FOLLOWER to transmit.
1: LEADER is ready for the FOLLOWER to transmit.

infofield_complete

This variable indicates that a complete set of Infofield messages has been sent (see 201.5.2.4 for HS_PATH and 201.5.2.5 for LS_PATH.).
Values:

FALSE: A complete set of Infofield messages has not been sent since PMA_state changed.
TRUE: A complete set of Infofield messages has been sent.

link_control
This variable is defined in 201.2.1.1.1.

link_status
The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.
Values: OK or FAIL.

loc_countdown_done
This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to TRUE immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

loc_rcvr_status
Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.
Values:
OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin
This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.
Values:
OK: The local device has sufficient SNR margin.
NOT_OK: The local device does not have sufficient SNR margin.

pcs_data_mode
Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

phy_role
This variable indicates which side of the asymmetrical line the device is on.
Values:
PHY_S: MultiG+100MBASE-T1/V1 PHY.
PHY_D: 100M+MultiGBASE-T1/V1 PHY.

pma_reset
Forces reset of the PHY Control and Link Monitor state diagrams (see 201.5.2.1).
Values: ON or OFF.

PMA_state
Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.
Values:
00: TRAINING state
01: COUNTDOWN state

rem_countdown_done
This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state and is set to TRUE immediately after receiving the last bit of the DataSwPFC24–1 partial PHY frame.

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not.

Values:

OK: The receive link for the remote PHY is operating reliably.

NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

sync_link_control

This variable is defined in 201.5.2.8.1.

tx_mode

The PMA generates this variable continuously and passes it to the PCS via the PMA_TXMODE.indication primitive.

Values:

SEND_N: This value is continuously asserted when transmission of sequences of symbols representing a XGMII data stream take place.

SEND_T: This value is continuously asserted when transmission of sequences of symbols representing the training sequences of symbols is to take place.

SEND_Z: This value is continuously asserted in case transmission of Z symbols is required.

201.5.2.6.3 State diagram timers

All timers operate in the manner described in 14.2.3.2.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT and TRAINING states, and the minimum time it stays in PCS_TEST state before normal transition to the PCS_DATA state.

201.5.2.6.4 State diagrams

The PHY Control state diagram is shown in Figure 201–31.

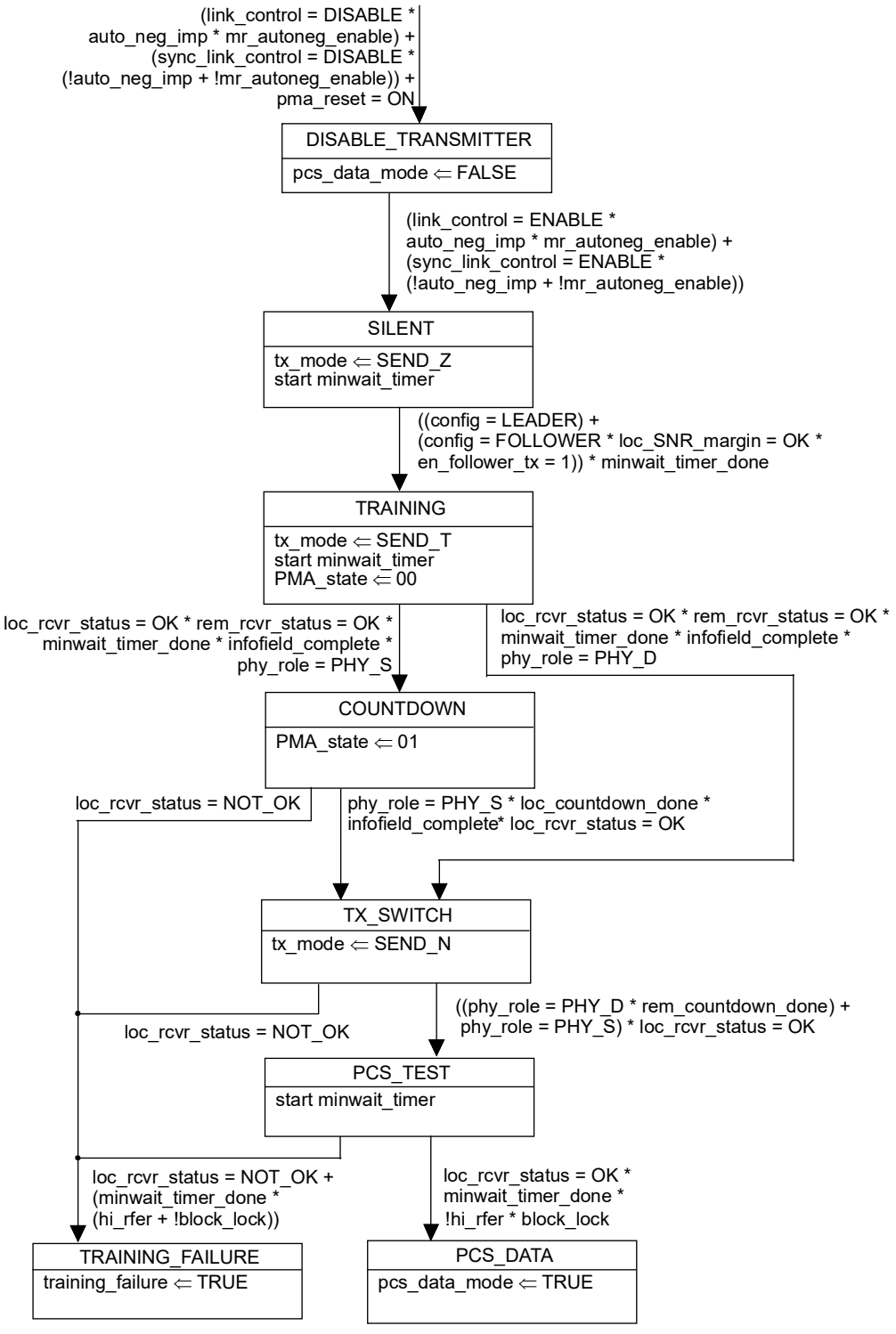


Figure 201–31—PHY Control state diagram

201.5.2.7 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the Auto-Negotiation (if enabled) or Link Synchronization (if Auto-Negotiation is not enabled) process.

The Link Monitor function shall comply with the state diagram of Figure 201–32.

Upon power on, reset, or release from power down, the Auto-Negotiation function sets link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. While in LINK_DOWN state, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote MultiG+100M/100M+MultiGBASE-T1/V1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state diagram begins monitoring the PCS and receiver lock status. When pcs_data_mode is TRUE, the variable link_status = OK is asserted.

201.5.2.7.1 State diagram variables

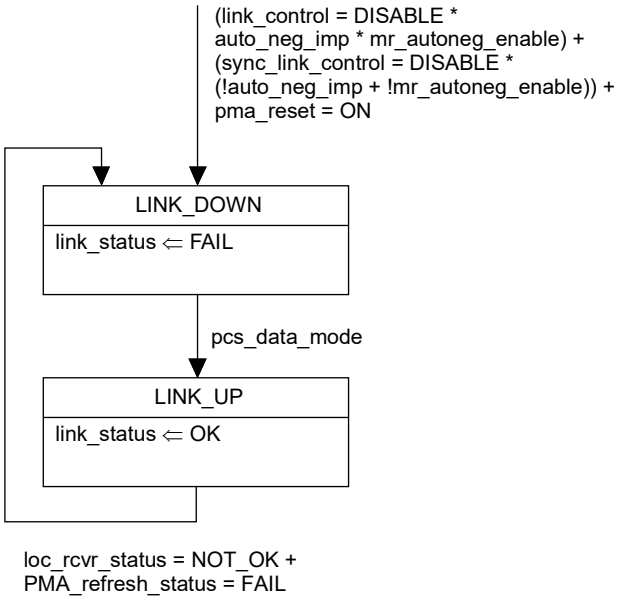
The variables defined in 201.5.2.6.2 apply to this clause.

201.5.2.7.2 State diagram timers

The variables defined in 201.5.2.6.3 apply to this clause.

201.5.2.7.3 State diagrams

The Link Monitor state diagram is shown in Figure 201–32.



NOTE—The variables link_control and link_status are designated as link_control_mGigT1 and link_status_mGigT1, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–7) if the optional Auto-Negotiation function is implemented.

Figure 201–32—Link Monitor state diagram

201.5.2.8 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function shall conform to the state diagram in Figure 201–35. This section describes and defines the function of Figure 201–35, the link synchronization process.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 201.5.2.2), and uses a signal, SEND_S. This signal is used by the LEADER and FOLLOWER to discover the link partner and synchronize the start of PMA training. The structure of the Link Synchronization signaling is shown in Figure 201–33.

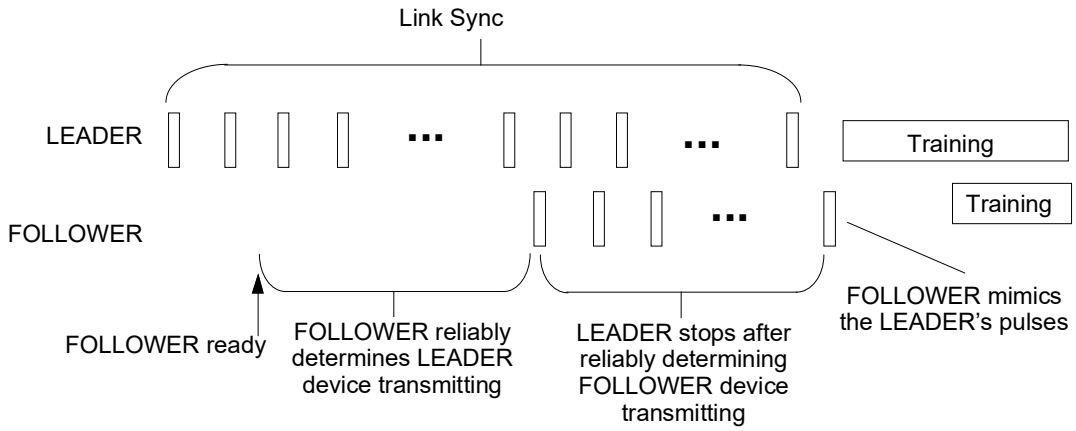


Figure 201–33—Link Synchronization signaling structure

A SEND_S pulse is defined to be a 4-bit pulse of 1001 mapped to DME symbols. The polarity of the DME symbols can be of either polarity and can vary between SEND_S pulses. At the LEADER and FOLLOWER, each DME symbol time is nominally 25.6/3 ns. See 201.6.2.6 and 201.7.2.7 for details on bit timing tolerance. See 201.5.2.2.1 for details on the DME symbols.

At the LEADER, SEND_S signal is defined to be a periodic signal with a SEND_S pulse (34.133 ns) followed by 116 DME symbol periods of quiet for a total of 120 DME symbol periods (1024 ns) per interval.

When the FOLLOWER detects a sufficient number of the LEADER's SEND_S pulses to determine that the LEADER is active, the FOLLOWER outputs one SEND_S pulse, with a delay following the detection of the LEADER's most-recent SEND_S pulse. For each subsequent SEND_S pulse detected from the LEADER, the FOLLOWER outputs one SEND_S pulse with timing as shown in Figure 201–34. This pattern repeats until the LEADER detects a sufficient number of the FOLLOWER's SEND_S pulses to determine that the FOLLOWER is active. The LEADER then enters the SILENT_WAIT state and stops transmitting SEND_S pulses as specified in Figure 201–35. Likewise, after the FOLLOWER determines that the LEADER has stopped transmitting SEND_S pulses, the FOLLOWER also enters the SILENT_WAIT state.

The SEND_S pulse timing is shown in Figure 201–34.

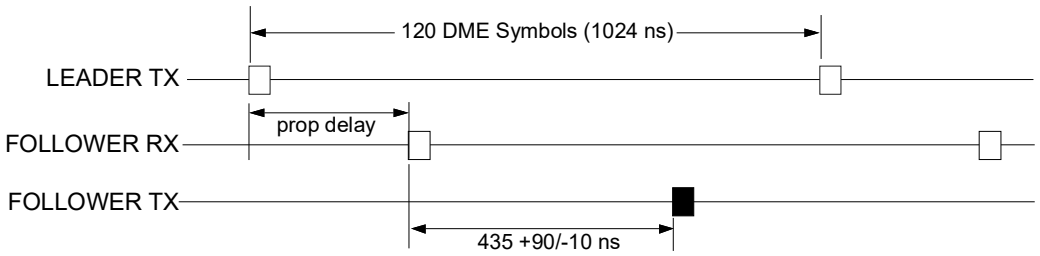


Figure 201–34—Link Synchronization timing

201.5.2.8.1 State diagram variables

force_config
: This variable indicates whether the PHY operates as a LEADER or as a FOLLOWER. The variable takes on one of the following values:
  LEADER: This value is continuously asserted when the PHY operates as a LEADER.
  FOLLOWER: This value is continuously asserted when the PHY operates as a FOLLOWER.

force_phy_type
: This variable indicates what speed the PHY is to operate when Auto-Negotiation is disabled or not implemented. The variable takes on one of the following values:
  10G+100M: If Auto-Negotiation is disabled or not implemented and 10G+100MBASE-T1/V1 is selected.
  5G+100M: If Auto-Negotiation is disabled or not implemented and 5G+100MBASE-T1/V1 is selected.
  2.5G+100M: If Auto-Negotiation is disabled or not implemented and 2.5G+100MBASE-T1/V1 is selected.
  100M+10G: If Auto-Negotiation is disabled or not implemented and 100M+10GBASE-T1/V1 is selected.
  100M+5G: If Auto-Negotiation is disabled or not implemented and 100M+5GBASE-T1/V1 is selected.
  100M+2.5G: If Auto-Negotiation is disabled or not implemented and 100M+2.5GBASE-T1/V1 is selected.
  Other values are implementation-dependent and beyond the scope of this clause.

link_status
: The link_status parameter is set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_enable:
: see 98.5.1.

mr_main_reset
: see 98.5.1.

power_on
: see 98.5.1.

quiet_detect
: A Boolean variable indicating whether the link partner has ceased sending SEND_S pulses.

TRUE: No SEND_S pulses have been detected at the specified times (for LEADER or FOLLOWER see Figure 201–34) within the preceding 5.1 µsec.
FALSE: At least one SEND_S pulse has been detected at the specified times (for LEADER or FOLLOWER see Figure 201–34) within the preceding 5.1 µsec

send_s_sigdet
A Boolean variable indicating whether sufficient SEND_S pulses were detected with proper spacing. The definition of sufficient pulses is implementation dependent.
Values:
TRUE: Sufficient SEND_S pulses have been detected.
FALSE: Sufficient SEND_S pulses have not been detected.

single_send_s_detect
A Boolean variable indicating whether a SEND_S pulse has been detected.
Values:
TRUE: SEND_S pulse detected.
FALSE: No SEND_S pulse detected.

sync_link_control
This variable indicates the data source for the PMA Transmit function.
Values:
DISABLE: The data source is the PHY Link Synchronization function (sync_tx_symb).
ENABLE: The data source is PMA_UNITDATA.request (tx_symb).

201.5.2.8.2 State diagram timers

break_link_timer_[HSM]
see 98.5.2.

follower_delay_timer
This timer is used to control the offset between the FOLLOWER detecting a SEND_S pulse from the LEADER and the FOLLOWER transmitting its SEND_S pulse reply as shown in Figure 201–33. Duration: 435 +90/-10 nsec.

leader_pause_timer
This timer is used to control the quiet time between SEND_S pulses from the LEADER. Duration: 116 DME symbol times.

fail_inhibit_timer
Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific technology link is first being established. A link will be considered “failed” only if the fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. This timer shall expire 50 ms after entering the LINK_GOOD_CHECK state.

pulse_timer
This timer is used to output the SEND_S pulse. Duration: 4 DME symbol times.

sigdet_wait_timer
This timer is used to control the wait time after transmitting or detecting the end of SEND_S. The timer shall expire 5 µs ± 0.15 µs after being started.

201.5.2.8.3 Messages

sync_tx_symb

The value of sync_tx_symb is set by the Link Synchronization state diagram and indicates the symbols sent from the PHY Link Synchronization block to PMA Transmit. The Link Synchronization block generates sync_tx_symb synchronously with every transmit clock cycle.

Values:

SEND_S: Transmit the SEND_S pulse defined in 201.5.2.8.

SEND_Z: This value is continuously asserted in case transmission of Z symbols is required.

201.5.2.8.4 State diagrams

The PHY Link Synchronization state diagram is shown in Figure 201–35.

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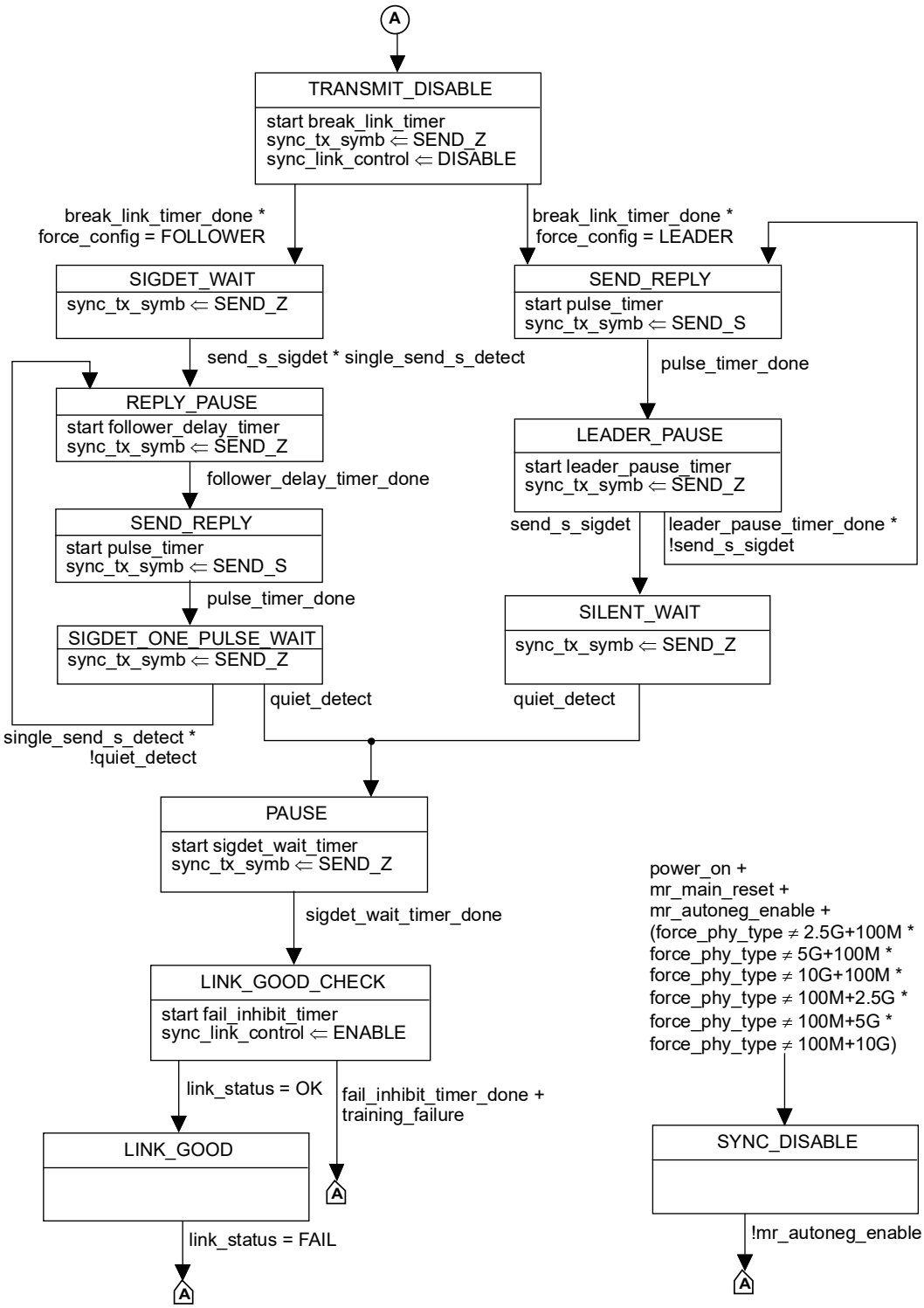


Figure 201–35—PHY Link Synchronization state diagram

201.5.2.9 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 201.5.2.3 for the HS_PATH and in 201.5.2.5 for the LS_PATH is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock.

201.5.2.10 MDI, T1

The MDI signals are as specified in 149.4.3, with the following exceptions:

1) The 100 Mb/s signaling uses DME instead of PAM4.
2) The 2.5 Gb/s signaling uses PAM2 instead of PAM4.
3) The 5 Gb/s signaling uses PAM2 instead of PAM4.

201.5.2.11 MDI, V1

The MDI signals are as specified in 149.4.3, with the following exceptions:

1) The signals are single ended instead of differential.
2) The 100 Mb/s signaling uses DME instead of PAM4.
3) The 2.5 Gb/s signaling uses PAM2 instead of PAM4.
4) The 5 Gb/s signaling uses PAM2 instead of PAM4.

201.6 PMA electrical specifications, high speed path

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests for the HS_PATH.

201.6.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 201–13. If MDIO is not implemented then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation

Test mode 1 enables testing of timing jitter on LEADER and FOLLOWER transmitters. LEADER and FOLLOWER PHYs are connected over a link segment defined in 201.9 for T1 links and 201.10 for V1 links. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 175.78125 MHz.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, when transmitting PAM4, the PHY shall transmit a continuous pattern of JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source. When test mode 2 is enabled, when transmitting PAM2, the PHY shall transmit a continuous pattern of 0101 with the transmitted symbols timed from its local clock source.

Test mode 3 is for testing the precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the transmit precoder specified in 149.3.2.2.20, to be

Table 201–13—MDIO management registers settings for test modes, high speed

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting LEADER and FOLLOWER PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in LEADER mode.
011	Test mode 3—Precoder test mode.
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

precoded according to the transmit precoder settings as determined by the value set in register 1.2313.10:9, or equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, a 10G+100MBASE-T1/V1 PHY shall transmit a continuous pattern of PRBS13Q (as specified in 120.5.11.2.1). When test mode 4 is enabled, a 2.5G+100MBASE-T1/V1 PHY or a 5G+100MBASE-T1/V1 PHY shall each transmit a continuous pattern of PRBS13 (as specified in 94.3.10.8).

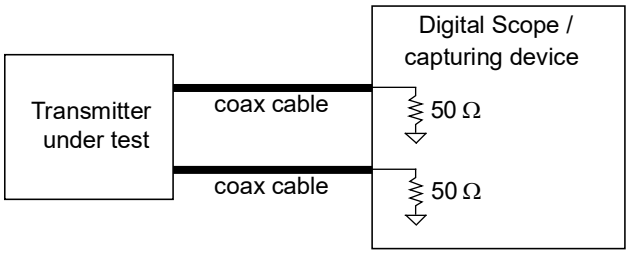
Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the LEADER data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of $128 \times S$ {+1} symbols followed by $128 \times S$ {–1} symbols with the transmitted symbols timed from its local clock source. See Table 201–1 for the definition of *S*.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the MultiG+100M/100M+MultiGBASE-T1/V1 normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

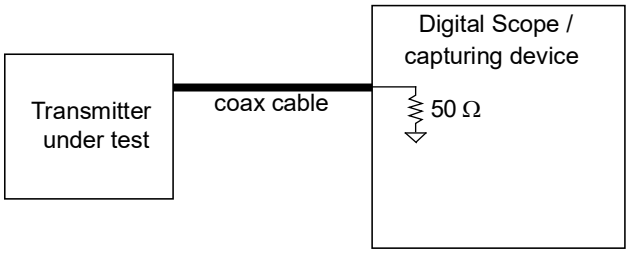
201.6.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 201–36, Figure 201–37, Figure 201–38, Figure 201–39, Figure 201–40, Figure 201–41, and Figure 201–42 in stated respective tests, are defined for measuring the transmitter specifications for data communication only.



NOTE—It is recommended that a FOLLOWER PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 201–36—Transmitter test fixture 1 for transmitter droop measurement and transmitter linearity measurement, -T1



NOTE—It is recommended that a FOLLOWER PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 201–37—Transmitter test fixture 1 for transmitter droop measurement and transmitter linearity measurement, -V1

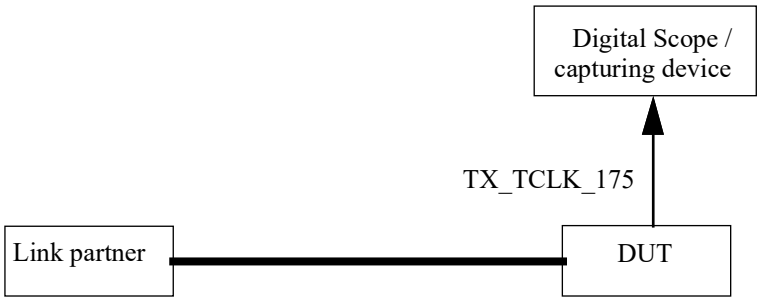


Figure 201–38—Transmitter test fixture 2 for LEADER and FOLLOWER clock jitter measurement, -T1 and -V1

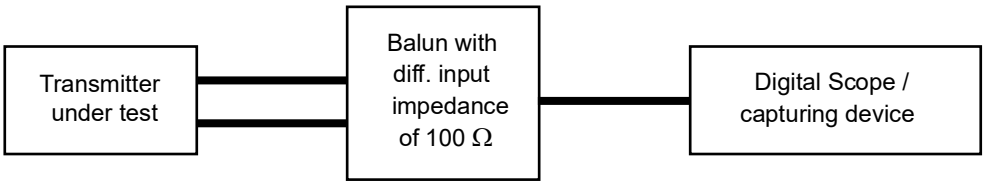


Figure 201–39—Transmitter test fixture 3 for MDI jitter measurement, -T1

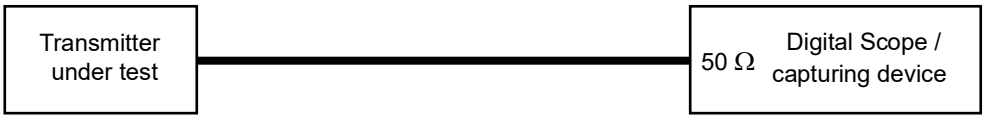
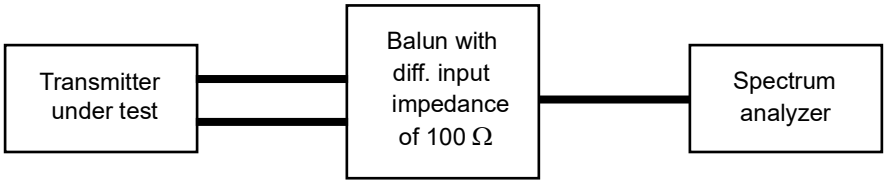


Figure 201–40—Transmitter test fixture 3 for MDI jitter measurement, -V1



NOTE—It is recommended that a FOLLOWER PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 201–41—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement, -T1

NOTE—It is recommended that a FOLLOWER PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 201–42—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement, -V1

201.6.2 Transmitter electrical specifications

The MultiG+100M-T1/V1 PMA provides the Transmit function specified in 201.3.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high dc common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single-ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

201.6.2.1 Maximum output droop

With the MultiG+100M-T1/V1 transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the magnitude of both the positive and negative droop shall be less than 30%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 10 ns after the zero crossing (6 ns period).

201.6.2.2 Transmitter linearity

Editor's Note (to be removed prior to Working Group Ballot):
Editorial Note: Consider what value of Np should be used in doing calculations to determine the SNDR.

With the transmitter in test mode 4, transmitting in MultiG mode, and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the test defined in 120D.3.1.2 shall be performed. The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2 for a 10G+100MBASE-T1/V1 PHY. For 5G+100MBASE-T1/V1 or 2.5G+100MBASE-T1/V1 PHYs, only levels corresponding to PAM2 modulation (-1 and +1) are relevant and ES1, ES2 and levels at ±1/3 are not applicable in the calculation of SNDR. The transmitter SNDR distortion, as specified in 120D.3.1.6, shall

exceed 36 dB in 10G+100MBASE-T1/V1, 33 dB in 5G+100MBASE-T1/V1, and 30 dB in 2.5G+100MBASE-T1/V1 modes.

201.6.2.3 Transmitter timing jitter

The allowable jitter varies with the PHY's data rate. The parameter *J* is used for scaling of the jitter, see Table 201–14.

Table 201–14—Jitter Scaling parameter

PHY type	*J*
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	2
2.5G+100MBASE-T1/V1	4

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both LEADER and FOLLOWER configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 201–38. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than *J* ps. The peak-to-peak value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10**J* ps. See Table 201–14 for the definition of *J*.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 6 ps and the RMS jitter shall be less than 3 ps when measured over jitter frequencies greater than 100 kHz. The peak-to-peak value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 60 ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

201.6.2.3.1 Transmit MDI random jitter in LEADER mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 201–15) and using test fixture 3 as shown in Figure 201–39 for -T1 and Figure 201–40 for -V1. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than *J* ps. See Table 201–14 for the definition of *J*. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 10×*J* ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

Table 201–15—Jitter test modes

Modulation	Bit 1.2313.1	Bit 1.2313.0	Test pattern
PAM4	0	0	Square wave: TX_TCLK_175
PAM4	0	1	JP03A (as specified in 94.2.9.1)
PAM4	1	0	JP03B (as specified in 94.2.9.2)
PAM2	1	1	0101 (as specified in 130.7.1.9)

201.6.2.3.2 Transmit MDI deterministic jitter in LEADER mode

Jitter measurements in this subclause are performed with the transmitter enabled in LEADER timing mode in test mode 2, with the patterns as defined by Table 201–15, and timed with a local clock.

To measure the peak-to-peak deterministic jitter ($DJ_{pk\text{-}pk}$) follow the steps as specified in 94.3.12.6.1, with the following modifications to step 5:

$f_n = 1 \times S$ MHz, $T = 68 / S$ ns. See Table 201–1 for the definition of *S*.

Using this method, $DJ_{pk\text{-}pk}$ shall be less than $9 \times J$ ps. See Table 201–14 for the definition of *J*.

To measure peak-to-peak even-odd jitter ($EOJ_{pk\text{-}pk}$) follow the steps as specified in 94.3.12.6.2.

Using this method, $EOJ_{pk\text{-}pk}$ shall be less than $4 \times J$ ps.

201.6.2.4 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the MultiG+100MBASE-T1/V1 PHYs shall be as specified in Table 201–16 and the power spectral density of the transmitter shall be between the upper and lower masks specified in Equation (201–9) and Equation (201–10). The PSD and power are measured using test fixture 4, shown in Figure 201–41, with a 100 Ω load for -T1 and shown in Figure 201–42, with a 50 Ω load for -V1. The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 201–43 for -T1 and in Figure 201–44 for -V1. When tx_symb is "Z" the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm. See Table 201–1 for the definition of *S*.

Table 201–16—Transmit Power, high speed mode

	Transmit power, -T1		Transmit power, -V1	
Transmit Rate	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
10 Gb/s	-1	2	-4	-1
5 Gb/s	-1	2	-4	-1
2.5 Gb/s	-4	-1	-7	-4

$$\text{UpperPSD}(f) = \left\{ \begin{array}{ll} P_O & 0 < f \le 600 \times S \\ P_O + 1 - \dfrac{f}{600 \times S} & 600 \times S < f \le 3000 \times S \\ P_O + 8 - \dfrac{f}{250 \times S} & 3000 \times S < f \le 5500 \times S \end{array} \right\} \text{dBm/Hz} \quad (201\text{–}9)$$

$$\text{LowerPSD}(f) = \left\{ \begin{array}{ll} P_O - 6 & 5 < f \le 400 \times S \\ P_O - 5 - \dfrac{f}{400 \times S} & 400 \times S < f \le 2000 \times S \\ P_O - \dfrac{f}{200 \times S} & 2000 \times S < f \le 3000 \times S \end{array} \right\} \text{dBm/Hz} \quad (201\text{–}10)$$

where

P_O is equal to -90 dBm/Hz for -T1
P_O is equal to -93 dBm/Hz for -V1
f is the frequency in MHz

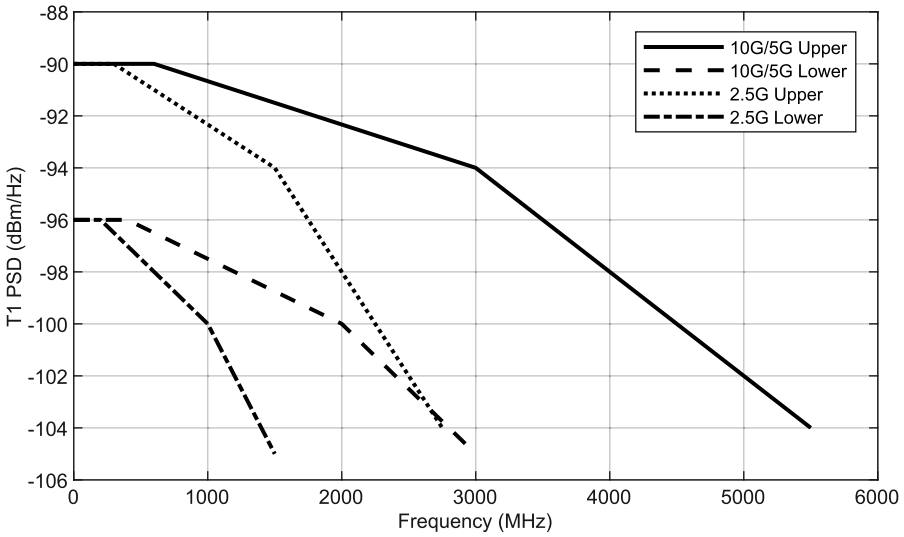


Figure 201–43—T1 MultiG Transmitter Power Spectral Density, upper and lower masks

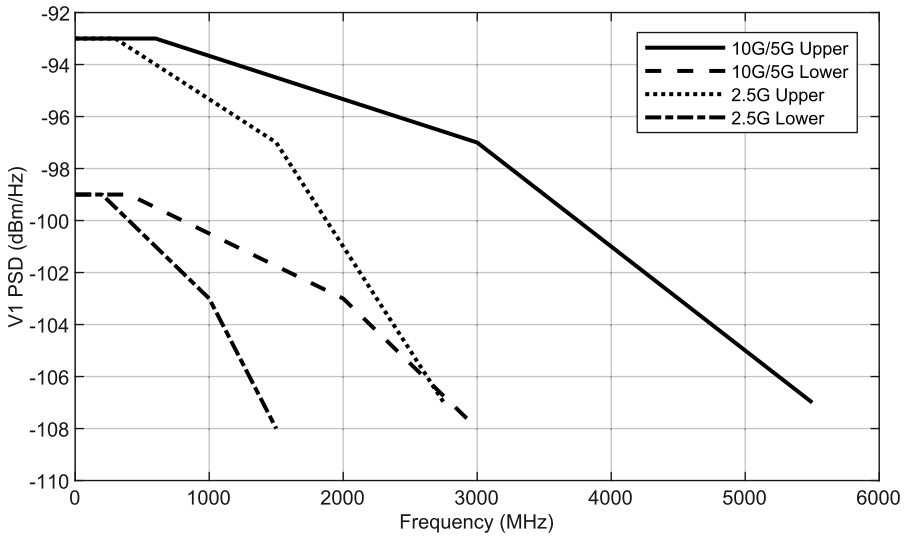


Figure 201–44—V1 MultiG Transmitter Power Spectral Density, upper and lower masks

201.6.2.5 Transmitter peak output

The transmit signal of a MultiG+100MBASE-T1 transmitter measured differentially with a 100 Ω termination, and the single-ended transmit signal of a MultiG+100MBASE-V1 transmitter measured with a 50 Ω termination shall be less than the peak-to-peak limits specified in Table 201–17 at the MDI. These limits apply to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

Table 201–17—Transmit peak-to-peak voltage limits, high speed mode

Transmit Rate	-T1 Max (V)	-V1 Max (V)
10 Gb/s	1.7	0.85
5 Gb/s	1.3	0.65
2.5 Gb/s	1.0	0.5

201.6.2.6 Transmitter clock frequency

The symbol transmission rate of the LEADER PHY shall be within the range 5625 × *S* MHz ± 100 ppm. See Table 201–1 for the definition of *S*.

The symbol transmission rate of the FOLLOWER PHY, when running off of a free-running clock, shall be within the range 5625⁄48 MHz +1/–20% and the short-term rate of frequency variation shall be less than 1% / second.

201.6.3 Receiver electrical specifications

The PMA provides the Receive function specified in 201.3.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 201.9 for -T1 and 201.10 for -V1.

201.6.3.1 Receiver differential input signals

The signal received at the MDI that was transmitted from a remote transmitter within the specifications of 201.6.2 and have passed through a link specified in 201.9 for -T1 and 201.10 for -V1 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

201.6.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver's tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 201–18. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 201–45, with a link segment as defined in 201.9 for -T1 and shown in Figure 201–46, with a link segment as defined in 201.10 for -V1. The BER is expected to be less than 10^{-12}, and to satisfy this specification, the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

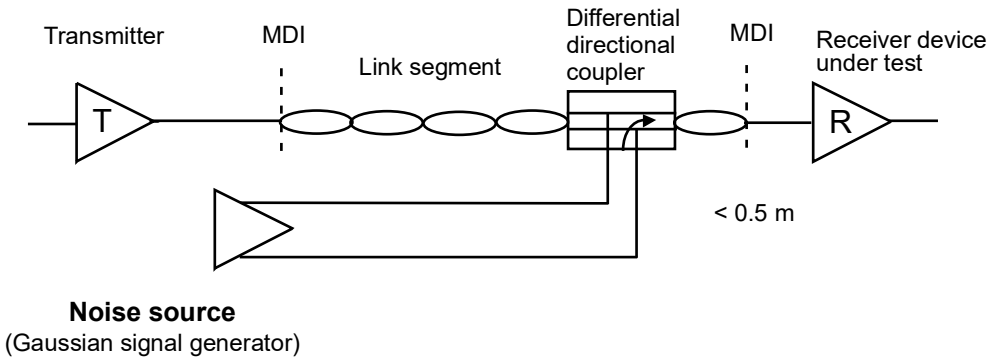


Figure 201–45—Broadband stationary noise rejection test setup, -T1

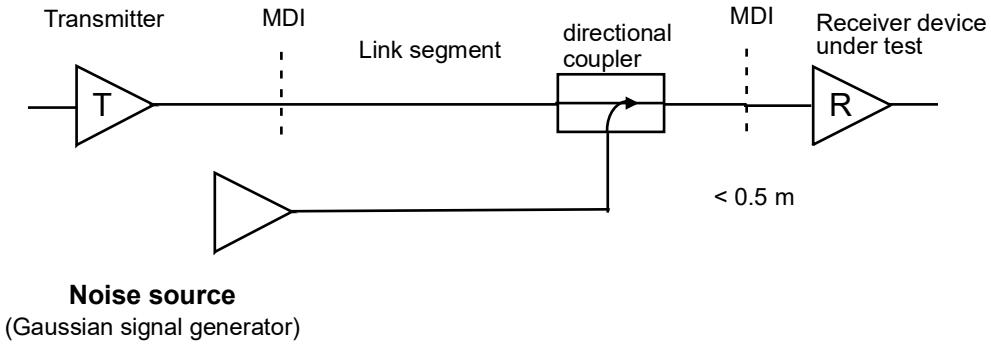


Figure 201–46—Broadband stationary noise rejection test setup, -V1

Table 201–18—Broadband stationary noise source, high speed

		Added noise at MDI (dBm/Hz)	
PHY type	**Noise bandwidth (MHz)**	**-T1**	**-V1**
10G+100MBASE	3500	–148	-151
5G+100MBASE	3500	–144	-147
2.5G+100MBASE	1750	–140	-143

Editor's Note (to be removed prior to SA Ballot):
Editorial Note: Contributors to consider whether to specify additional noise sources, such as line spectra from power management ICs, or other common self-noise from associated components.

201.6.4 MDI

Communication through the MDI is summarized in 149.4.3.1 and 149.4.3.2, with the exceptions listed in 201.5.2.10 for T1 links and with the exceptions listed in 201.5.2.11 for V1 links.

201.7 PMA electrical specifications, low speed path

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests for the low speed path.

201.7.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 201–19. If MDIO is not implemented then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Test mode 1 enables testing of timing jitter on LEADER and FOLLOWER transmitters. LEADER and FOLLOWER PHYs are connected over a link segment defined in 201.9 for T1 links and 201.10 for V1 links. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 175.78125 MHz.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, the PHY shall repeatedly transmit DME encoded ones.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled the PHY shall transmit a continuous pattern of PRBS13 (as specified in 94.3.10.8).

Table 201–19—MDIO management registers settings for test modes, low speed

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting LEADER and FOLLOWER PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in LEADER mode.
011	Test mode 3—Reserved
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the LEADER data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 3 {+1} baseband symbols followed by 3 {–1} symbols. These symbols are transmited with no Manchester encoding, generating a square wave with a period of 51.2 ns. The transmit symbols are timed from a free-running local clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the 100M+MultiGBASE-T1/V1 normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

201.7.1.1 Test fixtures

The test fixtures in 201.6.1.1 are defined for measuring the transmitter specifications for data communication only.

201.7.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 201.5.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high dc common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single-ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

201.7.2.1 Maximum output droop

With the 100M+MultiGBASE-T1/V1 transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the magnitude of both the positive and negative droop shall be less than 30%, measured with respect to an initial value at 8 ns after the zero crossing and a final value at 14 ns after the zero crossing (6 ns period).

201.7.2.2 Transmitter linearity

With the transmitter in test mode 4, transmitting in 100M mode, and using the transmitter test fixture 1 shown in Figure 201–36 for -T1 and Figure 201–37 for -V1, the transmit signal is captured per 85.8.3.3.4 with a minimum of M=14. The effective transmit baseband symbols, $x(n)$, is derived by noting that differential Manchester encoding includes an implicit nonlinear mapping. This nonlinear operation maps the transmitted PRBS13 bits d_{in} to another set of pseudo-random bits d_{out}, which in turn maps to the implicit transmit baseband symbols $x(n)$ according to Table 201–20.

Table 201–20—PRBS13 mapping table

Transmit Bits	Encoded Bits		Baseband Symbols
	previous	current	
$d_{in}(n)$=PRBS13	$d_{in}(n-1)$	$d_{in}(n)$	$x(n)$
0	0	1	-1
0	1	0	+1
1	0	0	-1
1	1	1	+1

Given the implicit transmit symbols $x(n)$, and the captured waveform $y(k)$, compute the linear fit pulse response $p(k)$ and the standard deviation of linear fit error $e(k)$ according to 85.8.3.3.5 and using N_p=100 and D_p=2.

The transmitter SNDR distortion is defined as: $\mathrm{SNDR} = 10\log_{10}\left(\frac{\sigma_p^2}{\sigma_e^2 + \sigma_n^2}\right)$

Where $\sigma_p^2 = \frac{1}{M}\sum_k p^2(\mathrm{k})$, and σ_e and σ_n are the standard deviation of $e(k)$ and noise, respectively.

The transmitter SNDR distortion shall exceed 30 dB.

201.7.2.3 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both LEADER and FOLLOWER configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 201–38. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than J ps. The peak-to-peak value of the LEADER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 10×J ps. See Table 201–14 for the definition of J.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 50 ps. The peak-to-peak value of the FOLLOWER TX_TCLK_175 jitter relative to an unjittered reference shall be less than 500 ps.

TX_TCLK_175 jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the capturing device shall be at least 200 MHz (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

201.7.2.4 Transmit MDI random jitter in LEADER mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with a square wave pattern and using test fixture 3 as shown in Figure 201–39 for -T1 and Figure 201–40 for -V1. The square wave pattern is generated by transmitting constant 0 values as the input to the differential Manchester encoder. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than *J* ps. See Table 201–14 for the definition of *J*. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 10×*J* ps. Jitter shall be measured over an interval of 1 ms ± 10%. The band-pass bandwidth of the measurement device shall be larger than 200 MHz. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error

201.7.2.5 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the 100M+MultiGBASE-T1/V1 PHYs shall be as specified in Table 201–21 and the power spectral density of the transmitter shall be between the upper and lower masks specified in Equation (201–11) and Equation (201–12). The PSD and power are measured using test fixture 4, shown in Figure 201–41, with a 100 Ω load for -T1 and shown in Figure 201–42, with a 50 Ω load for -V1. The upper and lower masks are shown in Figure 201–47 for -T1 and in Figure 201–48 for -V1. When tx_symb is "Z" the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm.

Table 201–21—Transmit Power, low speed mode

	Transmit power, -T1		Transmit power, -V1	
Transmit Rate	**Min (dBm)**	**Max (dBm)**	**Min (dBm)**	**Max (dBm)**
100M	-3	0	-6	-3

$$\text{UpperPSD}(f) = \begin{Bmatrix} P_O & 3 < f < 150 \\ P_O + 15 - \frac{f}{10} & 150 < f \le 260 \\ P_O - 11 & 260 < f \le 3500 \end{Bmatrix} \text{dBm/HZ} \qquad (201–11)$$

$$\text{LowerPSD}(f) = \left\{ \begin{array}{ll} P_O - 6 - \frac{90-f}{3} & 45 < f \le 90 \\ P_O - 6 - \frac{f-90}{4} & 90 < f \le 150 \end{array} \right\} \text{dBm/HZ} \qquad (201\text{–}12)$$

where

P_O is equal to –79 dBm/Hz for -T1
P_O is equal to –82 dBm/Hz for -V1
f is the frequency in MHz

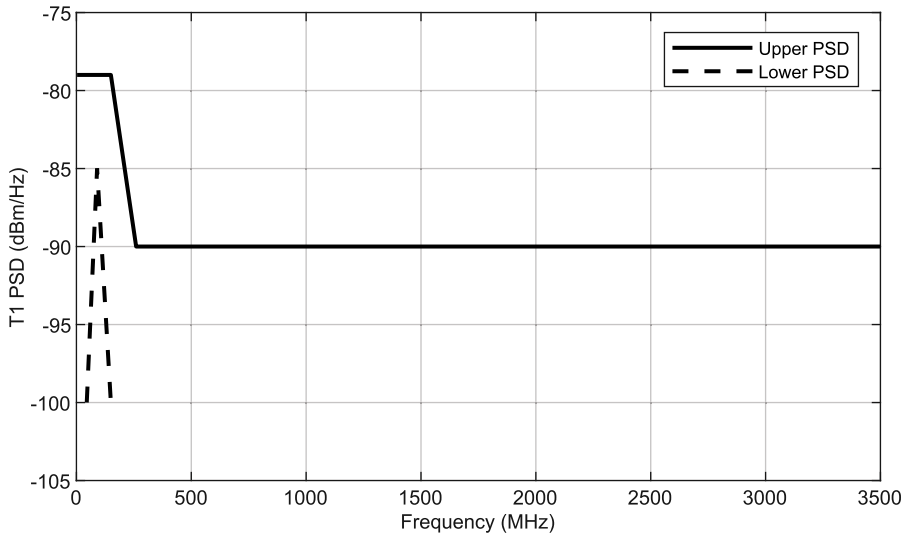


Figure 201–47—T1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

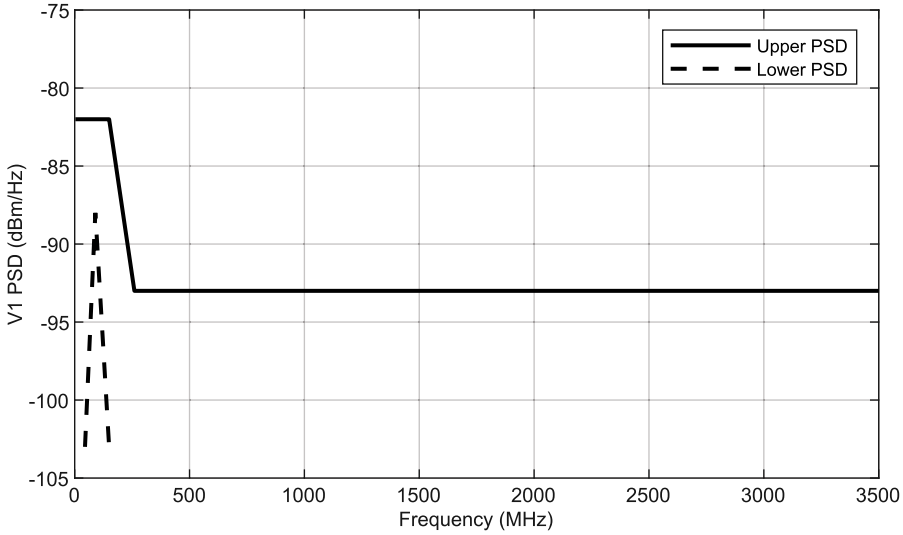


Figure 201–48—V1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

201.7.2.6 Transmitter peak output

When transmitting at a data rate of 100 Mb/s and measured with a 100 Ω termination, the differential transmit signal of a 100M+MultiGBASE-T1 transmitter shall be less than 1.0 V peak-to-peak at the MDI. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 100 Mb/s and measured with a 50 Ω termination, the transmit signal shall be less than 0.5 V peak-to-peak at the MDI. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

201.7.2.7 Transmitter clock frequency

The baseband symbol transmission rate of the LEADER PHY (prior to Manchester encoding) shall be within the range 5625⁄48 MHz ± 100 ppm.

201.7.2.8 Transmitter Rise and Fall Time

The transmitter rise and fall time requirements specified in this subclause apply when the PHY_D is used to provide a reference clock for XTAL-less operation of PHY_S. Limiting the transmitter transition times reduces deterministic jitter of the derived reference at the receiving PHY.

The rise/fall transition time between 20% and 80% levels of the steady state voltage amplitude shall be less than 1.5 ns. The rise time and fall time is defined as measured at the MDI using Test mode 2.

201.7.3 Receiver electrical specifications

The receiver electrical specifications for the low speed mode are specified in 201.6.3.

The broadband stationary noise rejection level is as specified in Table 201–22.

Table 201–22—Broadband stationary noise rejection, low speed

		Added noise at MDI (dBm/Hz)	
PHY type	**Noise bandwidth (MHz)**	**-T1**	**-V1**
100M+MultiGBASE	150	-126	-129

201.7.4 MDI

The MDI for the low speed mode is specified in 201.6.4.

201.8 Management interface

201.8.1 Support for Auto-Negotiation

MultiG+100M/100M+MultiGBASE-T1 PHYs optionally provide support for Auto-Negotiation. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

MultiG+100M/100M+MultiGBASE-V1 PHYs do not support Auto-Negotiation.

Auto-Negotiation, when implemented and enabled, is performed as part of the initial set-up of the link and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for MultiG+100M/100M+MultiGBASE-T1:

a) To negotiate which PHY types, including speed and direction, can be supported,
b) To determine the LEADER-FOLLOWER relationship between the PHYs at each end of the link.

201.9 Link segment characteristics, -T1

MultiG+100M/100M+MultiGBASE-T1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. The single shielded balanced pair of conductors supports an effective data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and simultaneously 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

201.9.1 Link transmission parameters

The transmission characteristics for the -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

201.9.1.1 Insertion loss

The insertion loss of each -T1 link segment shall meet the values determined using Equation (201–13).

$$\textit{Insertion loss(f)} \le -0.0015 + 0.001325f + 0.3645\sqrt{f} + \frac{1.1785}{\sqrt{f}}(\text{dB}) \qquad (201\text{–}13)$$

where

f is the frequency in MHz; $3 \le f \le \text{F}_{\text{max}}$

Fmax is given by Equation (201–14).

$$\text{F}_{\text{max}} = \begin{cases} 2000\ \text{MHz} & \text{for 2.5 Gb/s} \\ 4000\ \text{MHz} & \text{for 5 Gb/s and 10 Gb/s} \end{cases} \qquad (201\text{–}14)$$

The Insertion loss is illustrated in Figure 201–49.

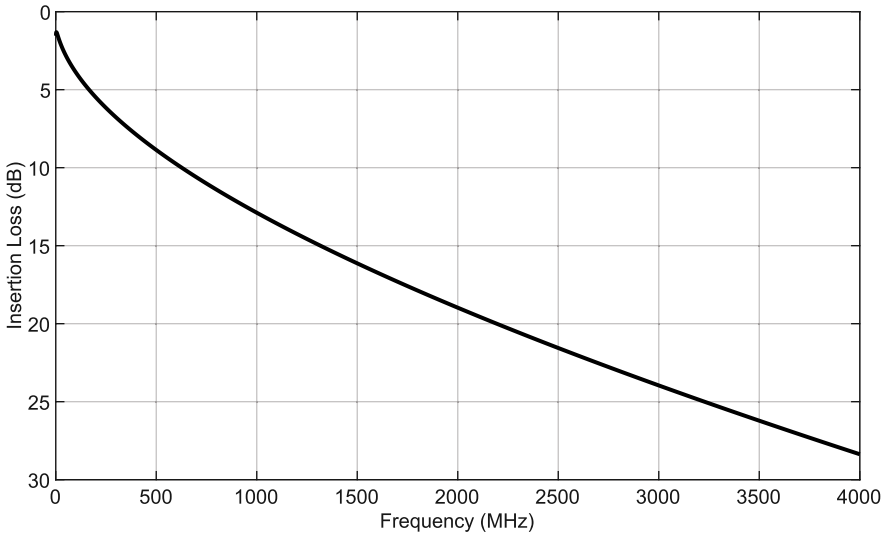


Figure 201–49—Insertion loss using Equation (201–13) for T1 and V1

201.9.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of the -T1 link segment is 100 Ω.

201.9.1.3 Return loss

The return loss of each -T1 link segment shall meet the values determined using Equation (201–15).

$$Return\ Loss(f) \geq \begin{cases} 18 & 3 \leq f < 400 \\ 16.5 - 11.5\log_{10}\left(\frac{f}{550}\right) & 400 \leq f < 3000 \\ 8 & 3000 \leq f < 4000 \end{cases} (\text{dB}) \qquad (201\text{–}15)$$

where

f is the frequency in MHz; $3 \leq f \leq 4000$

The Return loss is illustrated in Figure 201–50.

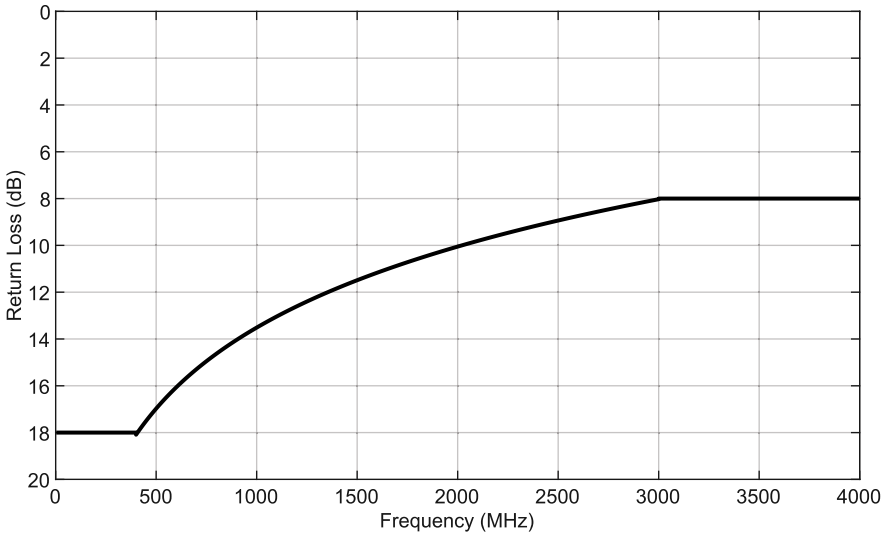


Figure 201–50—Return loss using Equation (201–15) for T1 and V1

201.9.1.4 Coupling attenuation

The coupling attenuation of each -T1 link shall be as specified in 149.7.1.4.

201.9.1.5 Screening attenuation

The screening attenuation of each -T1 link shall be as specified in 149.7.1.5.

201.9.1.6 Maximum link segment delay

The propagation delay of a -T1 link segment shall not exceed 160 ns at all frequencies between 3 MHz and Fmax MHz, see Equation (201–14) for the definition of Fmax.

201.9.2 Coupling parameters between link segments

The coupling parameters between link segments are described in 149.7.2.

201.9.2.1 Power sum alien near-end crosstalk (PSANEXT)

The PSANEXT shall be as specified in 149.7.2.1.

201.9.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The PSAACRF shall be as specified in 149.7.2.2.

201.10 Link segment characteristics, -V1

MultiG+100M/100M+MultiGBASE-V1 is designed to operate over a single coaxial cable (-V1) that meets the requirements specified in this subclause. The single coaxial cable supports an effective data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and simultaneously 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

201.10.1 Link transmission parameters

The transmission characteristics for the -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

201.10.1.1 Insertion loss

The insertion loss of each -V1 link segment shall meet the values determined using Equation (201–13).

The Insertion loss is illustrated in Figure 201–49.

201.10.1.2 Single ended characteristic impedance

The nominal characteristic impedance of the -V1 link segment is 50 Ω.

201.10.1.3 Return loss

The return loss of each -V1 is link segment shall meet the values determined using Equation (201–15).

The Return loss is illustrated in Figure 201–50.

201.10.1.4 Coupling attenuation

The coupling attenuation is not defined for coaxial cables.

201.10.1.5 Screening attenuation

The screening attenuation for each -V1 link segment shall meet the values determined using Equation (201–16). Screening attenuation is tested as specified in IEC 62153-4-7 using triaxial tube-in-tube method. Additional screening attenuation test methodologies are defined in Annex 149A.

$$\text{Screening attenuation}(f) \geq \begin{cases} 55 & 10 \leq f < 1000 \\ 50 & 1000 \leq f < 3000 \\ 45 & 3000 \leq f < 4000 \end{cases} \text{ (dB)} \qquad (201\text{–}16)$$

where

f is the frequency in MHz; $10 \le f \le 4000$

Screening attenuation is illustrated in Figure 201–51.

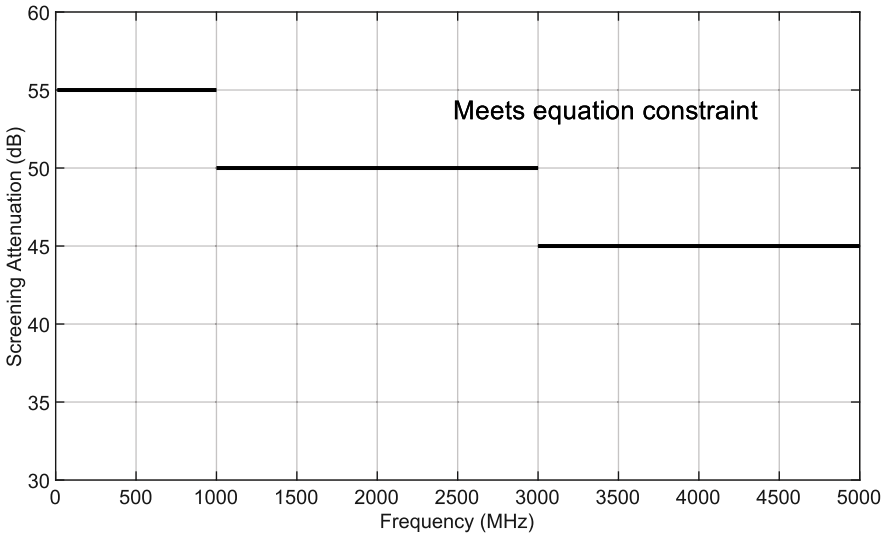


Figure 201–51—Screening attenuation using Equation (201–16) for V1

201.10.1.6 Maximum link segment delay

The propagation delay of a -V1 link segment shall not exceed 160 ns at all frequencies between 3 MHz and Fmax MHz, see Equation (201–14) for the definition of Fmax.

201.10.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

For implementations with multiple MultiG+100M/100M+MutiGBASE-V1 ports on the same MDI connector assembly, coupling between ports on the MDI connector is not considered to be part of the alien crosstalk specifications. For further information, see 149C.5.

201.10.2.1 Power sum alien near-end crosstalk (PSANEXT)

The unbalanced coax near-end crosstalk (NEXT) loss between the disturbed link segment and the disturbing link segment is specified to meet the bit error ratio objective by limiting the alien crosstalk at the near end of a link segment. Multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers. The power ANEXT loss is derived using Equation (97–25) over the frequency range 3 Mz to 4000 MHz.

The power sum ANEXT loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (201–17).

$$\text{PSANEXT loss}(f) \geq \min\left(60, 60 - 5\log_{10}\frac{f}{100}\right) \text{ dB} \quad (201\text{–}17)$$

where

f is the frequency in MHz; $3 \leq f \leq 4000$

PSANEXT is illustrated in Figure 201–52.

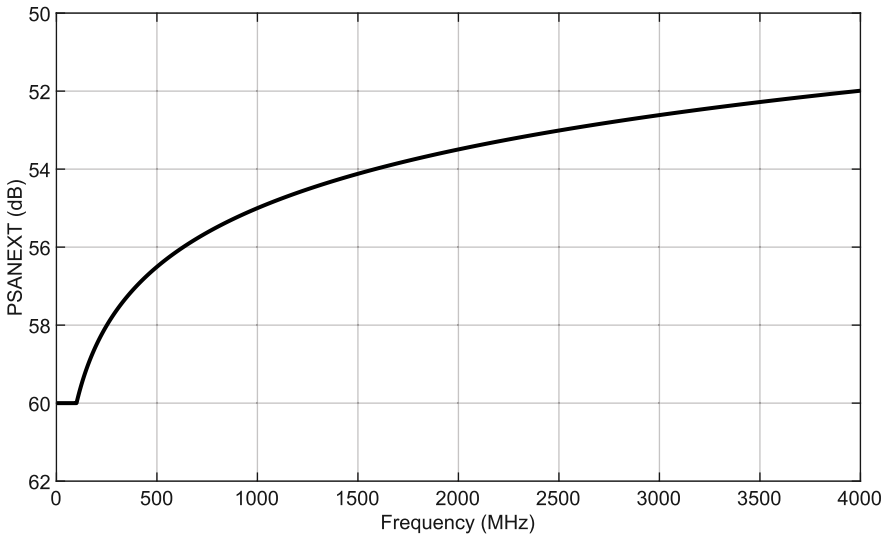


Figure 201–52—PSANEXT loss calculated using Equation (201–17)

201.10.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

In order to limit the alien crosstalk at the far-end of a link segment, the unbalanced coax cable-to-cable alien far-end crosstalk (FEXT) loss between the disturbed link segment and the disturbing link segment is specified to meet the bit error ratio objective. Multiple disturber attenuation to crosstalk ratio far-end ACRF is specified as the power sum of the individual alien ACRF disturbers to limit the total alien FEXT coupled into a link segment. The power AACRF is derived using Equation (97–27) over the frequency range 3 Mz to 4000 MHz.

The power sum AACRF loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (201–18).

$$\text{PSAACRF}(f) \geq \min\left(60, 60 - 5\log_{10}\frac{f}{100}\right) \text{ dB} \quad (201\text{–}18)$$

where

f is the frequency in MHz; $3 \leq f \leq 4000$

PSAACRF is illustrated in Figure 201–53.

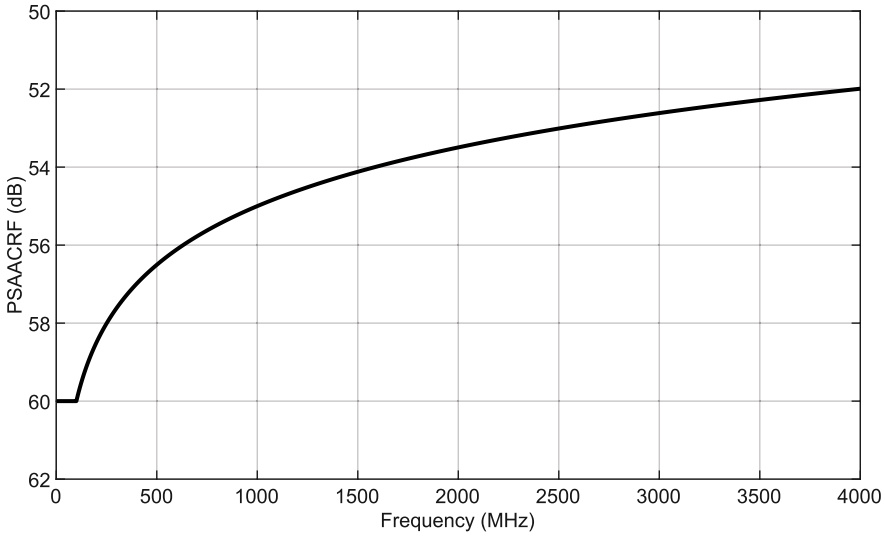


Figure 201–53—PSAACRF calculated using Equation (201–18)

201.11 MDI specification, T1

MultiG+100M/100M+MultiGBASE-T1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

201.11.1 MDI connectors

The MDI connectors are as specified in 149.8.1.

201.11.2 MDI electrical specification

201.11.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmit/receiver channel shall be such that any reflection due to signals incident upon the MDI from the cabling relative to the incident signal are per the relationship shown in Equation (201–19). For the -T1 PMD, a nominal differential characteristic is impedance of 100 Ω is used.

$$MDI\_Return\_Loss(f) > \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \le f < 50 \\ 18 & 50 \le f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \le f < Fmax \end{cases} \text{(dB)} \qquad (201–19)$$

where

f is the frequency in MHz; $10 \le f \le F_{max}$

For 10G-T1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 4000 MHz.

For 5G-T1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 4000 MHz.

For 2.5G-T1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 2000 MHz.

The MDI return loss for 10G-T1 and 5G-T1 is illustrated in Figure 201–54.

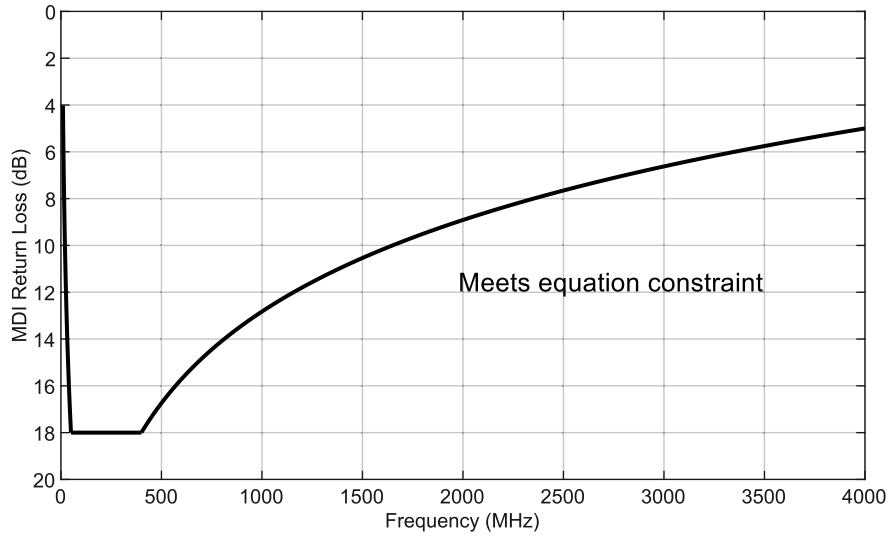


Figure 201–54—-T1 MDI return loss using Equation (201–19)

201.11.3 MDI fault tolerance

The MDI fault tolerance shall comply with 96.8.3.

201.12 MDI specification, V1

MultiG+100M/100M+MultiGBASE-V1 is designed to operate over a single coaxial cable MDI (-V1) that meets the requirements specified in this subclause.

201.12.1 MDI connectors

Where coaxial cabling is used, the mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the mechanical interface is beyond the scope of this standard.

201.12.2 MDI electrical specification

201.12.2.1 MDI return loss

The differential impedance at the -V1 MDI for each transmit/receiver channel shall be such that any reflection due to signals incident upon the MDI from the cabling relative to the incident signal are per the

relationship shown in Equation (201–20). For the -V1 PMD, a nominal differential characteristic is impedance of 50 Ω is used.

$$MDI\_Return\_Loss(f) > \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \le f < 50 \\ 18 & 50 \le f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \le f < Fmax \end{cases} \text{(dB)} \qquad (201–20)$$

where

f is the frequency in MHz; $10 \le f \le \mathrm{F_{max}}$

For 10G-V1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 4000 MHz.

For 5G-V1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 4000 MHz.

For 2.5G-V1 the maximum applicable frequency, *Fmax*, for the MDI return loss is 2000 MHz.

The MDI return loss for 10G-V1 and 5G-V1 is illustrated in Figure 201–55.

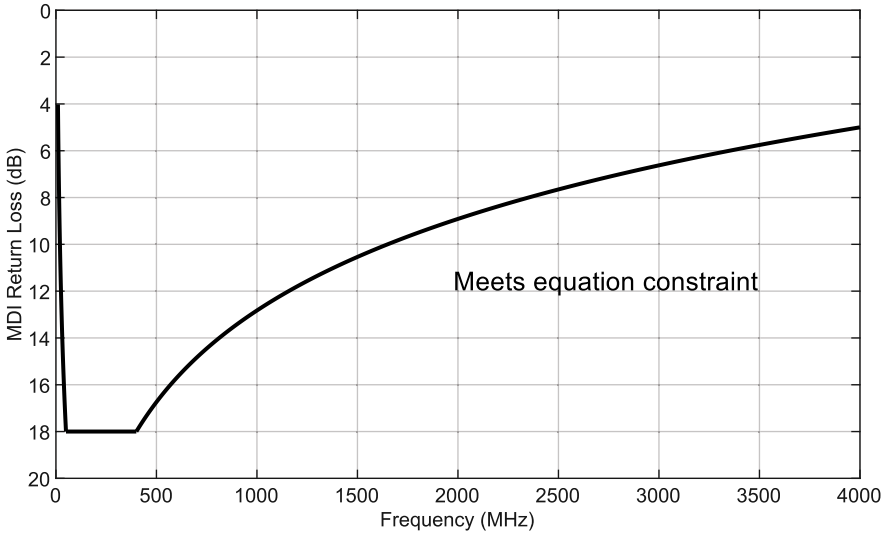


Figure 201–55—-V1 MDI return loss using Equation (201–20)

201.12.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 201–23, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI shall also withstand, without damage, high-voltage transient noises and ESD per application requirements.

Table 201–23—Connection fault, -V1

Center Conductor	Shield
No fault	Ground
MDI+	Ground
Ground	Ground
+50 V dc	Ground

201.13 Environmental specifications

The environmental specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.

201.13.1 General safety

The general safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.1.

201.13.2 Network safety

The network safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.

201.13.2.1 Environmental safety

The environmental safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.1.

201.13.3 Electromagnetic compatibility

The electromagnetic compatibility safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.2.

201.14 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network.

The HS_PATH delays for an implementation of the PHY (local XGMII to remote XGMII link delay minus the link segment propagation delay) shall not exceed the limits shown in Table 201–24. The data delay is measured from the input of a given unit of data at the PHY_S XGMII to the presentation of the same unit of data by the PHY_D XGMII.

The LS_PATH delays for an implementation of the PHY (local XGMII to remote XGMII link delay minus the link segment propagation delay) shall not exceed the limits shown in Table 201–24. The data delay is measured from the input of a given unit of data at the PHY_D XGMII to the presentation of the same unit of data by the PHY_S XGMII.

Table 201–24—Delay Limits

PATH	Interleave	Bit times	Pause Quanta	Delay (ns)
2.5G+100MBASE-T1/V1	1x	10 240	20	4096
5G+100MBASE-T1/V1	1x	10 240	20	2048
5G+100MBASE-T1/V1	2x	13 824	27	2764.8
10G+100MBASE-T1/V1	1x	10 240	20	1024
10G+100MBASE-T1/V1	2x	13 824	27	1382.4
10G+100MBASE-T1/V1	4x	20 480	40	2048
100M+MultiGBASE-T1/V1	—	512	1	5120

See Annex 201 for informative guidance on the allocation of delay between the transmit and receive portions of the PHY.

201.15 Protocol implementation conformance statement (PICS) proforma for Clause 201, ACT proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1[5]

201.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 201, ACT proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

[5]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

201.15.2 Identification

201.15.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

201.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-202x, Clause 201, ACT proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

201.15.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

201.15.4 PICS proforma tables for ACT proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1,

10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1

201.15.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

201.15.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]

202. TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

202.1 Overview

MultiGBASE-A PHYs support multiple rate options. They features baud commonality across high speed and low speed implementations. The PHYs use the same TDD cycle for all data rates (see 202.3), as well as use the same base FEC with different shortening parameters for the high speed and low speed directions.

202.1.1 Nomenclature

Editor's Note (to be removed prior to Working Group Ballot):

Need to add some explanation of TDD bursts, LEADER vs. FOLLOWER behavior, and TDD burst structure in US/DS direction as this is implied but not given much context in other parts of the text. For example needs to be defined that bursts are non-overlapping at the receiver, US bursts include one RS-FEC frame, DS bursts include 25 RS-FEC frames, etc. diagram of overall burst structure (refresh header plus data payload).

The MultiGBASE-AT1 and MultiGBASE-AV1 PHYs described in this clause represent two distinct PHY types that share the same PCS and PMA specifications subject to frequency scaling. In order to efficiently describe the two PHYs, the following nomenclature is used.

HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter
PHY_D	LS_TX, HS_RX mode of operation (high speed XGMII destination)
PHY_S	HS_TX, LS_RX mode of operation (high speed XGMII source)

When talking about the asymmetric PHY communicating on a shielded, balanced, pair of conductors, use:

MultiGBASE-AT1

When talking about the asymmetric PHY communicating on a coaxial cable, use:

MultiGBASE-AV1

When talking about all PHYs, regardless of transmit bit rate or cable type, use:

MultiGBASE-A

The six modes of operation and MAC data rate combinations for each of the two PHY types are shown in Table 202–1.

Table 202–1—PHY/PMD type definitions

PHY name	Medium interface	Mode of operation	Transmit MAC data rate	Receive MAC data rate
MultiGBASE-AT1	Differential (balanced)	PHY_D	100 Mb/s	2.5 Gb/s
			100 Mb/s	5 Gb/s
			100 Mb/s	10 Gb/s
		PHY_S	2.5 Gb/s	100 Mb/s
			5 Gb/s	100 Mb/s
			10 Gb/s	100 Mb/s
MultiGBASE-AV1	Single-ended (unbalanced)	PHY_D	100 Mb/s	2.5 Gb/s
			100 Mb/s	5 Gb/s
			100 Mb/s	10 Gb/s
		PHY_S	2.5 Gb/s	100 Mb/s
			5 Gb/s	100 Mb/s
			10 Gb/s	100 Mb/s

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

-T1 represents a single shielded balanced pair of conductors (i.e., differential)
-V1 represents a single coaxial cable (i.e., unbalanced)

Additionally, for parameters that scale with the PHY's supported MAC data rate, the parameter *S* is used for scaling as shown in Table 202–2.

Table 202–2—Scaling parameters

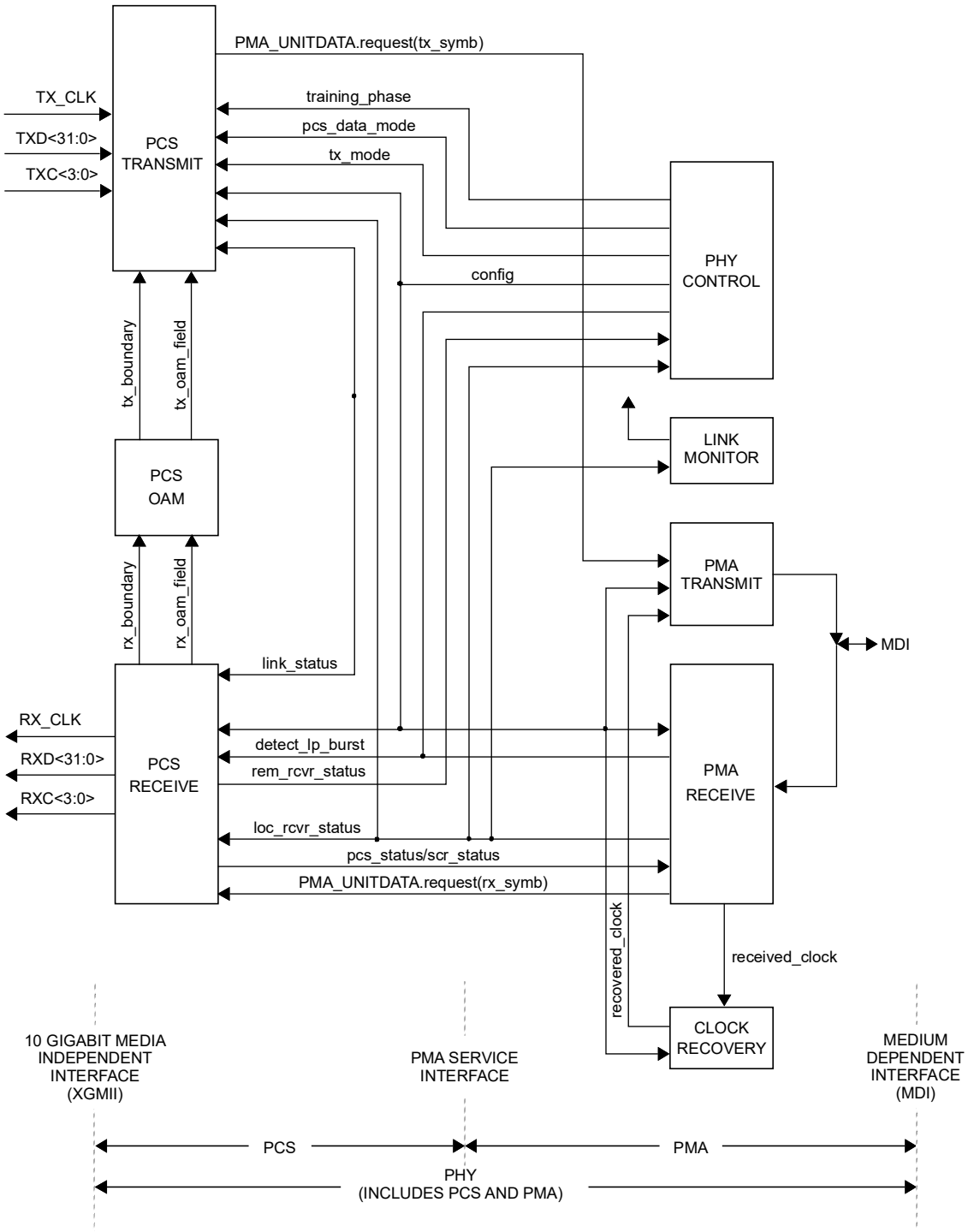
Transmit MAC data rate	*S*
100 Mb/s	0.5
2.5 Gb/s	0.5
5 Gb/s	1
10 Gb/s	1

202.1.2 Relationship of MultiGBASE-A to other standards

Editor's Note (to be removed prior to Working Group Ballot):

May be added by Editor based on project details.

202.1.3 Operation of MultiGBASE-A



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

Figure 202–1—Functional block diagram

202.1.3.1 Physical Coding Sublayer (PCS) in PHY_S mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 1-bit OAM field is appended to form a 976-bit block. A number, L (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 4 for 10 Gb/s), of these 976-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC(128,122,8) and the round-robin interleaving as described in 202.3.2.2.15. The RS-FEC output superframe consists of L × 1040 bits. The duration of the superframe is 1024 / 3 ns.

NOTE—Duration = L × 1024 bits / bits per symbol / baud rate. For 10 Gb/s, Duration = 4 × 1024 / 2 / 6 GBd; for 5 Gb/s, Duration = 2 × 1024 / 1 / 6 GBd; for 2.5 Gb/s, Duration= 1 × 1024 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the HS_TX payload. The PCS Transmit functions are described in 202.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where i = 0 to 14, j = 0 to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded_0<64:0> is the first block transmitted.

In the training mode (see 202.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 202.3. The interface to the PMA is an abstract message-passing interface specified in 202.4.

202.1.3.2 Physical Coding Sublayer (PCS) in PHY_D mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in normal mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 17-bit OAM field is appended to form a 992-bit block. Each of these 992-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(130,124,8). The RS-FEC output frame consists of 1040 bits. The duration of the frame is 1040 / 3 ns.

NOTE—Duration = 1040 bits / bits per symbol / baud rate = 1040 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the LS_TX payload. The PCS Transmit functions are described in 202.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}<65 \times i + j> = \text{tx\_coded}_i<j>$$

where i = 0 to 14, j = 0 to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded0<64:0> is the first block transmitted.

In the training mode (see 202.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 202.3. The interface to the PMA is an abstract message-passing interface specified in 202.4.

202.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto a single balanced pair of conductors (-T1) or a single coaxial cable (-V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides communications at $6 \times S$ GBd. See Table 202–2 for the definition of S.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled and provides the startup functions required for successful operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link and communicates this status to other functional blocks. A failure of the receive link causes the data mode operation to stop and startup functions to restart.

PMA functions and state diagrams are specified in 202.4 and 202.5. The electrical parameters of the PMA (i.e., test modes and electrical specifications for the transmitter and receiver) are specified in 202.5.

202.1.4 LS_PATH signaling

LS_PATH signaling is performed by the LS_TX PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling in opposite directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the normal data mode or the training mode.

In both normal mode and training mode, the LS_TX PCS generates a continuous stream of PAM2 symbols that are transmitted via the PMA at one of two voltage levels (see Figure 202–26).

202.1.5 HS_PATH signaling

HS_PATH signaling is performed by the HS_TX PCS generating continuous code-group sequences that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling in opposite directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the normal data mode or the training mode.

In normal mode, the HS_TX PCS generates a continuous stream of either PAM4 symbols that are transmitted via the PMA at one of four voltage levels for 10 Gb/s or PAM2 symbols that are transmitted via the PMA at one of two voltage levels for 2.5 Gb/s and 5 Gb/s. In training mode, the HS_TX PCS is directed to generate only PAM2 symbols for transmission by the PMA (see Figure 202–26).

202.1.6 Interfaces

All MultiGBASE-A PHY implementations are compatible at the XGMII, if implemented. Implementation of the XGMII is optional. All MultiGBASE-AT1 PHY implementations are compatible at the -T1 MDI. All MultiGBASE-AV1 PHY implementations are compatible at the -V1 MDI. The MDI for a single balanced pair of conductors (-T1) and a single coaxial cable (-V1) are different. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

202.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

202.2 Service primitives and interfaces

MultiGBASE-A transfers data and control information across the following three service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) PMA service interface
c) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46. The PMA service interface is defined in 202.2.1. The -T1 MDI is defined in 202.9. The -V1 MDI is defined in 202.10.

202.2.1 PMA service interface

MultiGBASE-A uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication(pcs_data_mode)
PMA_DET_LP_BURST.indication(detect_lp_burst)

The use of these primitives is illustrated in Figure 202–2. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 202–2.

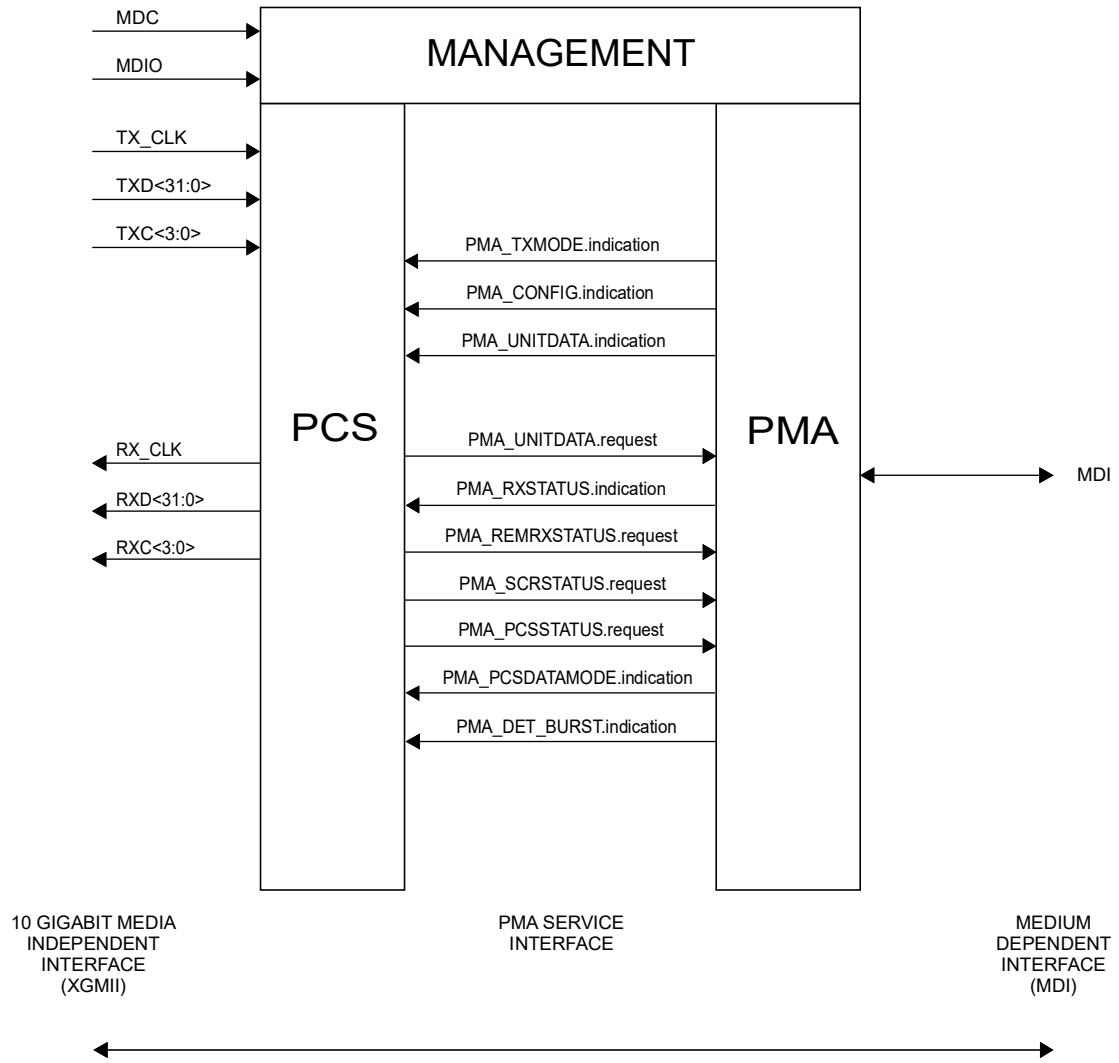


Figure 202–2—MultiGBASE-A service interface

202.2.1.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE-A link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

202.2.1.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.

SEND_TS This value is continuously asserted in case transmission of sequences of symbols representing the TDD symmetric training mode is to take place. LS_TX and HS_TX send at 3 GBd with PAM2 TDD training frames.

SEND_TA This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. LS_TX sends at 3 GBd with PAM2 TDD training frames. HS_TX sends at 3 GBd or 6 GBd with PAM2 TDD training frames.

SEND_Z This value is continuously asserted in case transmission of zero symbols is required.

202.2.1.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

202.2.1.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 202.3.2.2.

202.2.1.2 PMA_CONFIG.indication

PMA_CONFIG FOLLOWER-LEADER configuration is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

202.2.1.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PHY functions via the parameter config whether the PHY operates as the LEADER or FOLLOWER. The parameter config can take on one of the following two values of the form:

LEADER This value is continuously asserted when the PHY operates as the LEADER.

FOLLOWER
This value is continuously asserted when the PHY operates as the FOLLOWER.

202.2.1.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

202.2.1.2.3 Effect of receipt

PCS and PMA perform their functions in the LEADER or FOLLOWER configuration according to the value of the parameter config.

202.2.1.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 202.3.2.2 to represent XGMII data and control streams or other sequences.

202.2.1.3.1 Semantics of the primitive

Editor's Note (to be removed prior to Working Group Ballot):

Need to confirm if tx_symb is really sending "0" or if there is another definition intended similar to Tx disable.

PMA_UNITDATA.request(tx_symb)

The PMA_UNITDATA.request primitive conveys the value of the symbol to be transmitted over the MDI via the tx_symb parameter. The tx_symb may take on one of the following values:

{–1, –1/3, +1/3, +1}	in normal operation for 10 Gb/s mode's data payload.
{-1, +1}	in training mode and in normal operation for all refresh header, 2.5 Gb/s mode, and 5 Gb/s mode data payloads.
0	when zeros are to be transmitted in the following two cases: 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and 2) after data mode is reached, the transmit function is in the QUIET period.

202.2.1.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

202.2.1.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 202.5.2.

202.2.1.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

202.2.1.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception, the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock.

202.2.1.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive, as governed by the recovered clock, is 3 GHz for 100 Mb/s and 2.5 Gb/s receive modes and 6 GHz for 5 Gb/s and 10 Gb/s receive modes.

202.2.1.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

202.2.1.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the PCS descrambler has achieved synchronization.

202.2.1.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

OK	The PCS descrambler has achieved synchronization.
NOT_OK	The PCS descrambler is not synchronized.

202.2.1.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

202.2.1.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 202.4.2.3 and 202.4.2.4.

202.2.1.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

202.2.1.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values of the form:

OK	The PCS is operating reliably in the data mode.
NOT_OK	The PCS is not operating reliably in the data mode.

202.2.1.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

202.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 202.4.2.3 and 202.4.4.1.

202.2.1.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criteria for setting the parameter loc_rcvr_status is left to the implementer. For example, it can be based on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

202.2.1.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK — This value is asserted and remains true during reliable operation of the receive link for the local PHY.

NOT_OK — This value is asserted whenever operation of the link for the local PHY is unreliable.

202.2.1.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

202.2.1.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 202–2, 202.3.2.3, 202.4.2.4, and 202.5.

202.2.1.8 PMA_REMRXSTATUS.request

Editor's Note (to be removed prior to Working Group Ballot):

Needs review.

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

202.2.1.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK — The receive link for the remote PHY is operating reliably.

NOT_OK — Reliable operation of the receive link for the remote PHY is not detected.

202.2.1.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request message to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infofield messages received from the remote PHY during training.

202.2.1.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 202–26.

202.2.1.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

202.2.1.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

202.2.1.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

202.2.1.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 202.3.2.2.

202.2.1.10 PMA_DET_LP_BURST.indication(detect_lp_burst)

Editor's Note (to be removed prior to Working Group Ballot):

TBD.

This primitive is generated by PMA Receive to indicate it has detected a burst from link partner. The parameter detect_lp_burst conveys to the PCS Receive function and PHY Control.

202.2.1.10.1 Semantics of the primitive

Editor's Note (to be removed prior to Working Group Ballot):

TBD.

PMA_DET_LP_BURST.indication(detect_lp_burst)

PMA_DET_LP_BURST.indication specifies to PCS Receive and PHY Control via the parameter detect_lp_burst that the TDD burst has been detected. Set to FALSE when the PMA detected the burst has ended (PMA could use timer timeout to terminate this detection signal).

202.2.1.10.2 When generated

PMA Receive generates PMA_DET_LP_BURST.indication messages to indicate a change in detect_lp_burst.

202.2.1.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 202–26.

202.3 Physical Coding Sublayer (PCS) functions

202.3.1 PCS service interface (XGMII)

The PCS service interface allows the PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

202.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram (see Figure 202–3) shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 202–3.

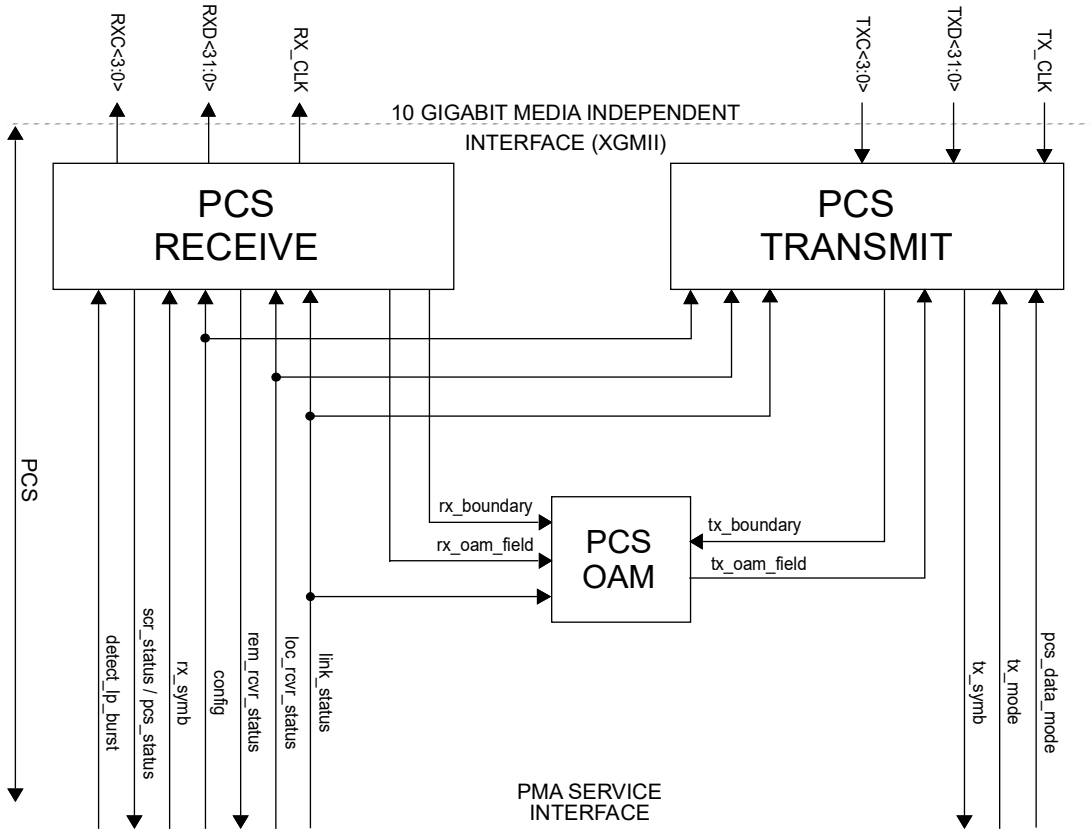


Figure 202–3—PCS reference diagram

202.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of following conditions occur:

a) Power on (see 202.3.7.2.2)
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15 (TBD).

202.3.2.2 PCS Transmit function

PCS Transmit function block diagram is shown in Figure 202–4. The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 202–20 and to the PCS Transmit bit ordering in Figure 202–5 for the LS_TX or Figure 202–6 for the HS_TX.

Dashed rectangles in Figure 202–6 indicate the data path of PAM2 or PAM4 signals. Only one of them shall be chosen for a particular operational speed mode.

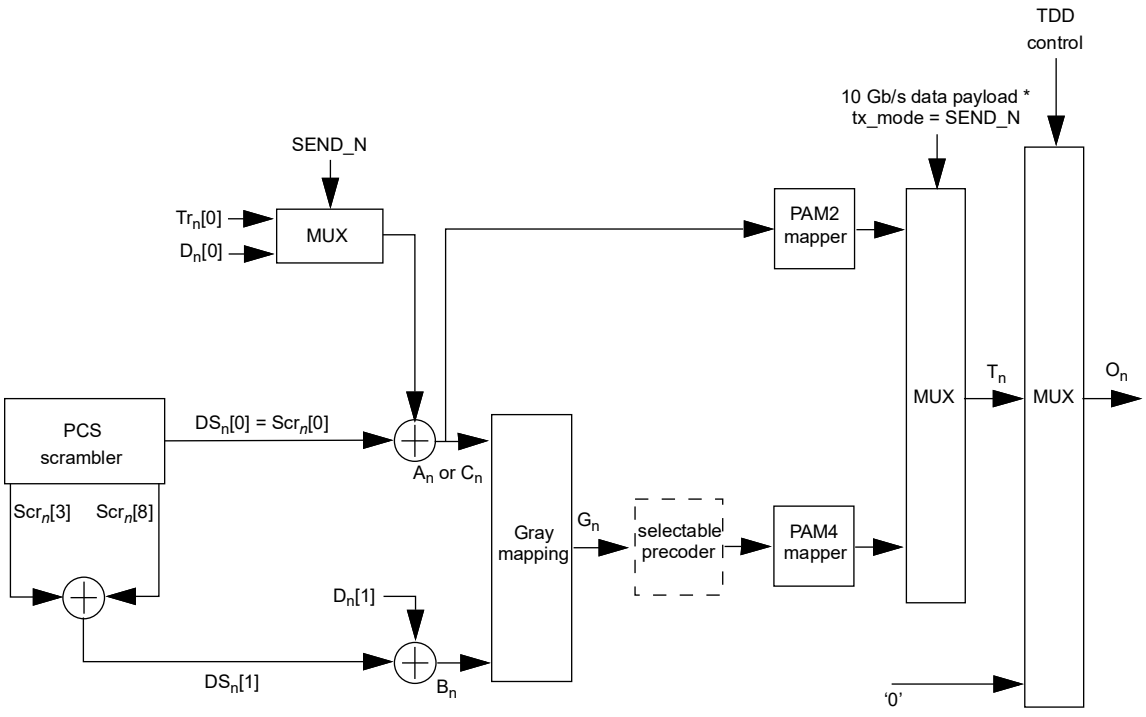


Figure 202–4—PCS Transmit function block diagram

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals.

Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

For LS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the LS_TX PCS Transmit process take 1 group of 15 65B blocks and append a 17-bit OAM field to it, shown in Figure 202–5. This forms the input to the RS_FEC(130,124) which adds 48 parity bits. The resulting 1040 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. Transmit data-units are sent to the LS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For HS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the HS_TX PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC(128,122) superframe which adds L × 64 parity bits, shown in Figure 202–6. 25 such superframes are formed for one data payload. L = 1 for 2.5 Gb/s and L = 2 for 5 Gb/s. For 2.5 Gb/s and 5 Gb/s PAM2 transmission, the resulting L × 1024 × 25 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. L = 4 for 10 Gb/s PAM4 transmission. The resulting L × 1024 × 25 bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol. Transmit data-units are sent to the HS_TX PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a PAM2 or PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T, is 1000 / (6 × S) ps. See Table 202–2 for the definition of S.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a vector of zeros at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_TS or SEND_TA, PCS Transmit shall generate a sequence (O_n) defined in 202.3.5 to the PMA via the PMA_UNITDATA.request primitive. These code-groups are used for training mode and only transmit the values {-1, +1}.

During training mode, an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes request for remote transmitter settings (see 202.4.2.4).

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the normal mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. For LS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 17-bit OAM field to form the RS-FEC input frame. During data encoding, LS_TX PCS Transmit utilizes Reed-Solomon encoders to generate and append 48 parity check bits to form 1040-bit (130,124) RS-FEC frames. For HS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 1-bit OAM field to form the RS-FEC input frame. During data encoding, HS_TX PCS Transmit utilizes L-interleaved (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, or L = 4 for 10 Gb/s)

Reed-Solomon encoders to generate and append 48 parity check bits to form 1024-bit (128,122) RS-FEC frames that are interleaved into an L-interleaved RS-FEC superframe.

Editor's Note (to be removed prior to Working Group Ballot):

L interleaving and Superframe structure - TBD (similar to 802.3ch format).

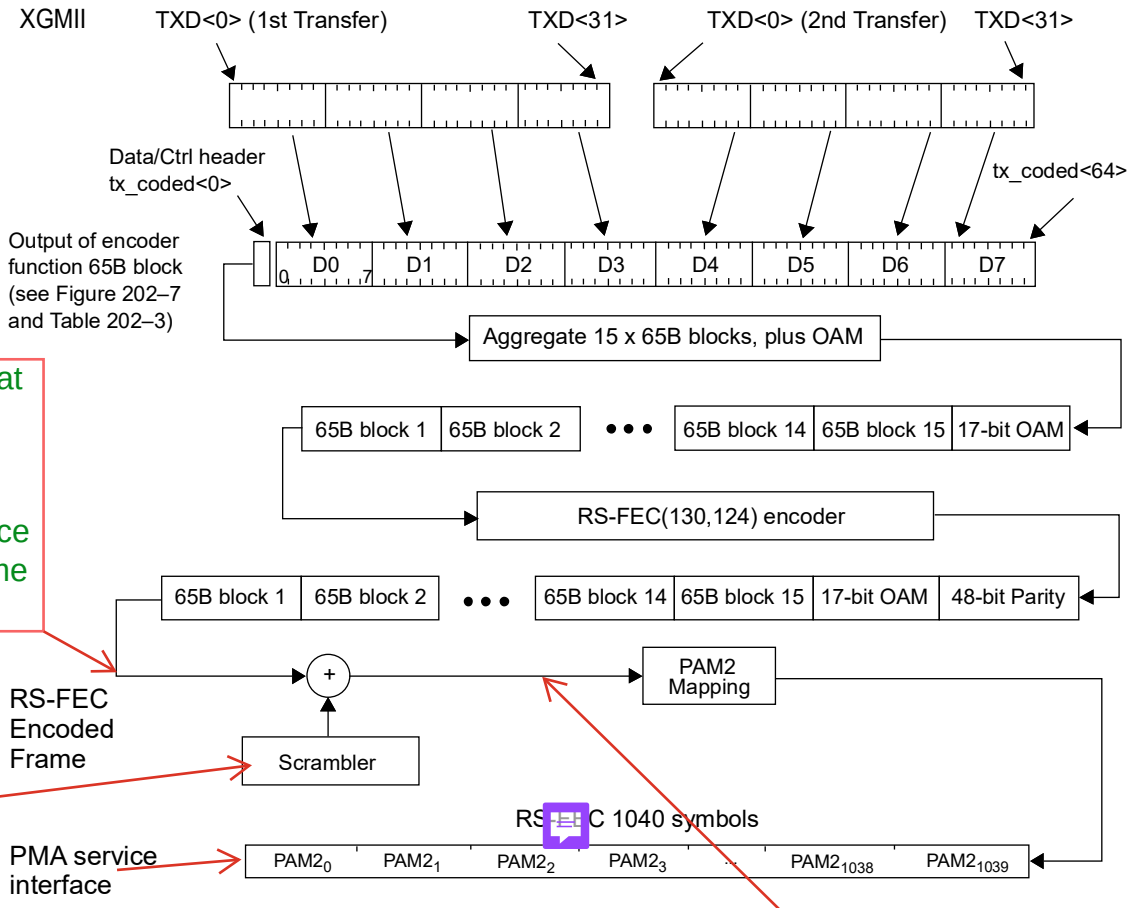
202.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2/PAM4 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 202.3.2.2.2.

202.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 202–5 for LS_TX, Figure 202–6 for HS_TX, Figure 202–10 for LS_RX, and Figure 202–11 for HS_RX. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 202.3.2.2.4 for information on how blocks containing control characters are mapped.



NOTE—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

Figure 202–5—LS_TX PCS Transmit bit ordering

Add a selector at this point for generating training frames payloads in place of RS-FEC frame payloads.

Refresh header bit generator

PRBS-11 Scrambler

Add a block of *N_r* scrambled refresh header bits in front of the scrambled N_p=1040-bit RS-FEC Encoded Frame.This combined block of bits is then sent to the PAM2 Mapping.

For consistency with HS_TX it might be better to have separate PAM2 mapping and just concatenate the symbol blocks, so suggest updating Figure 202-6 first and then update Figure 202-5 in a similar but simplified method.

Refresh header	Payload	Quiet Symbols
N_r PAM2 symbols	N_p PAM2 symbols	N_z Z symbols

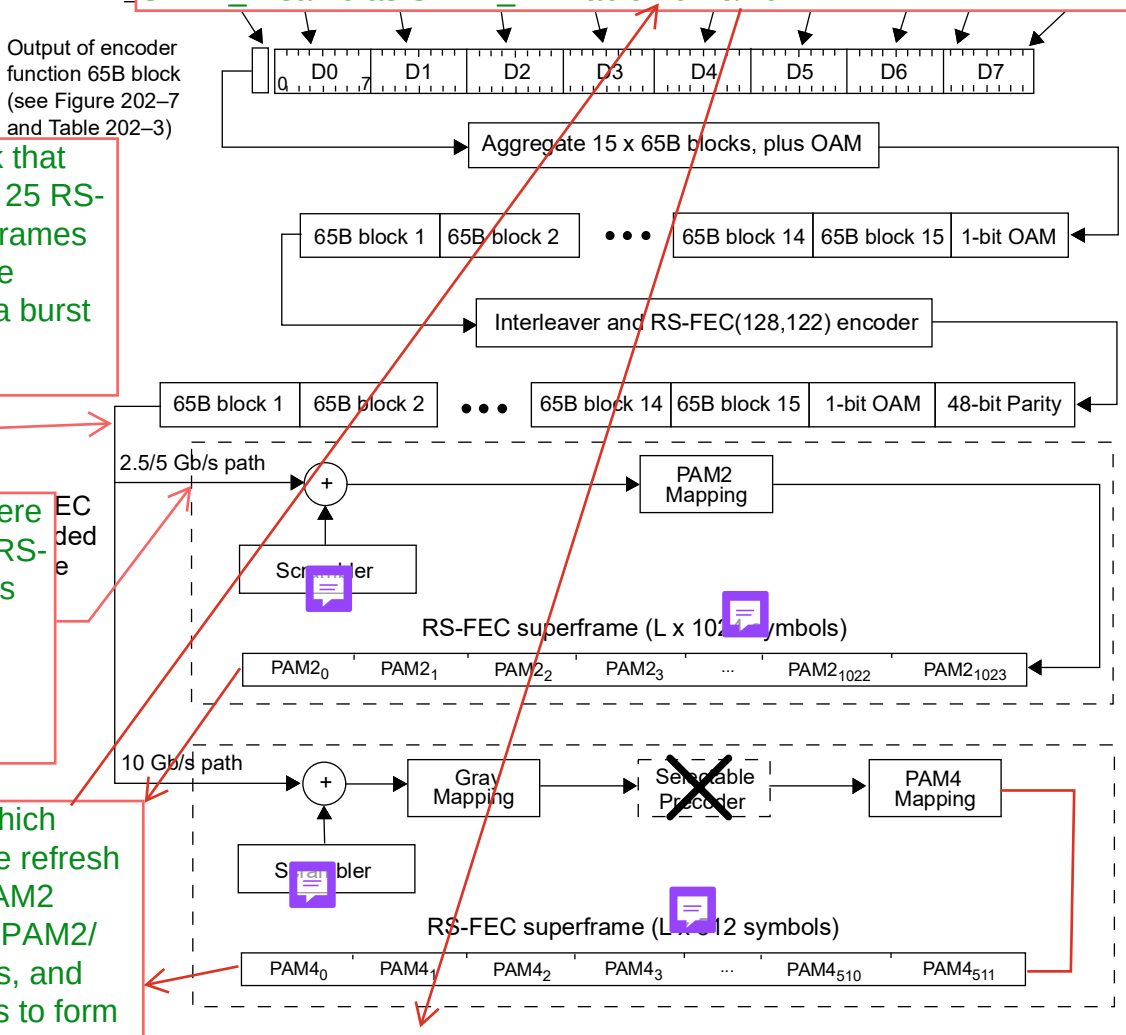
Total symbols per TDD cycle = N_r+N_p+N_z
SEND_TS uses 560 + 12880 + 15360 Table 202-5
SEND_TA uses 624 + 1040 + 27136 Table 202-5
SEND_N uses 624 + 1040 + 27136 Table 202-5

Refresh header
N_r PAM2 symbols

Payload
N_p PAM2 symbols

Quiet Symbols
N_z Z symbols

Total symbols per TDD cycle = N_r+N_p+N_z
SEND_TS 560 + 12880 + 15360 Table 202-6/Table 202-7
SEND_TA 2.5G 480 + 25600 + 2720 Table 202-6
SEND_TA 5G/10G 960 + 51200 + 5440 Table 202-7
SEND_N same as SEND_TA Table 202-6/202-7



Add a block that aggregates 25 RS-FEC superframes to create the payload of a burst

Add a selector here between the 25 RS-FEC superframes and the training payload bit generator

Add a block which aggregates the refresh header N_r PAM2 symbols, N_p PAM2/ PAM4 symbols, and N_z Z symbols to form the complete burst.

—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

NOTE 3—Either the PAM2 or PAM4 path is chosen.

Figure 202–6—HS_TX PCS Transmit bit ordering

Refresh header bit generator

PRBS-11 Scrambler

The scrambled refresh header bits go through PAM2 mapping (similar to 2.5/5 Gb/s path) to produce the refresh header N_r PAM2 symbols.

The N_r PAM2 symbols should then be concatenated with the payload N_p PAM2/PAM4 symbols and N_z Z symbols to form the burst that will be sent to the PMA.

202.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D0 to D7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O0 or O4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S0 or S4 for the same reason. The control character for terminate is labeled as T0 to T7.

The two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

202.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks is shown in Figure 202–7. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, D_0 through D_7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

Input data	data ctrl header	**Block payload**							
Bit position: / **Data block format:**	0	1							64
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		Block							
$C_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0\ C_1\ C_2\ C_3/O_4\ D_5\ D_6\ D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0\ C_1\ C_2\ C_3/S_4\ D_5\ D_6\ D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/S_4\ D_5\ D_6\ D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/O_4\ D_5\ D_6\ D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ D_7$	1	0x78	D_1	D_2	D_3	D_4		D_5	D_6	D_7
$O_0\ D_1\ D_2\ D_3/C_4\ C_5\ C_6\ C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0\ C_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ T_1\ C_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ T_2\ C_3/C_4\ C_5\ C_6\ C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ T_3/C_4\ C_5\ C_6\ C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/T_4\ C_5\ C_6\ C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ T_5\ C_6\ C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ T_6\ C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0\ D_1\ D_2\ D_3/D_4\ D_5\ D_6\ T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

Figure 202–7—64B/65B block formats for MultiGBASE-A

202.3.2.2.5 Control codes

All control characters are supported by both the XGMII and the PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The PCS encodes the start and terminate control characters implicitly by the block type field. The PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to MultiGBASE-A control codes and XGMII control codes are specified in Table 202–3.

Table 202–3—MultiGBASE-A control codes

Control character	Notation	XGMII control code	Control code	O code
idle	/I/	0x07	0x00	—
start	/S/	0xFB	Encoded by block type field	—
terminate	/T/	0xFD	Encoded by block type field	—
error	/E/	0xFE	0x1E	—
Sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0		0x1C	0x2D	reserved0
reserved1		0x3C	0x33	reserved1
reserved2		0x7C	0x4B	reserved2
reserved3		0xBC	0x55	reserved3
reserved4		0xDC	0x66	reserved4
reserved5		0xF7	0x78	reserved5
Signal ordered set[a]	/Fsig/	0x5C	Encoded by block type field plus O code	0xF

[a]Reserved for INCITS T11 Fibre Channel use.

202.3.2.2.6 Ordered sets

Editor's Note (to be removed prior to Working Group Ballot):

"remote fault" is not used in the document. Suggest to delete?

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and Local Fault status. Ordered sets consist of a control character followed by three data characters.

Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 202–3 for the mappings

202.3.2.2.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

202.3.2.2.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

202.3.2.2.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

202.3.2.2.10 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

202.3.2.2.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 202.3.7.2.4 for further information.

202.3.2.2.12 Transmit process

The LS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. It takes 1040 PMA_UNITDATA transfers to send an RS-FEC frame of data.

The HS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. L × 30 XGMII data transfers are encoded into an RS-FEC superframe. For 2.5 Gb/s and 5 Gb/s mode, it takes L × 1024 PMA_UNITDATA PAM2 transfers to send an RS-FEC superframe of data. For 10 Gb/s mode, it takes L × 512 PMA_UNITDATA PAM4 transfers to send an RS-FEC superframe of data. Where the XGMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 202–20). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the transcoder and scrambler. Tx_coded<0> contains the data/ctrl header and the remainder of bits contain the block payload.

202.3.2.2.13 RS-FEC framing and RS-FEC encoder

For LS_TX transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 17-bit OAM/Reserved field and 48 parity bits is 1040 bits. See Figure 202–5 and 202.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

For HS_TX transmission, the resulting RS-FEC frame of 15 65B blocks, followed by the 1-bit OAM/Reserved field and 48 parity bits is 1024 bits. See Figure 202–6 and 202.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

202.3.2.2.14 RS-FEC superframe and round-robin interleaving

The interleaver depth L of the transmitter shall be predefined for each speed. When the defined interleaving depth L = 1, there is no interleaving, and the RS-FEC superframe is the same as the RS-FEC frame.

When the defined interleaving depth L > 1, the round-robin interleaving scheme shown in Figure 202–8 shall be applied.

100 Mb/s mode supports L = 1.

2.5 Gb/s mode supports L = 1.

5 Gb/s mode supports L = 2.

10 Gb/s mode supports L = 4.

The HS_TX PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 976 × L bits, or 122 × L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are as follows:

$$m_{122 \times \mathrm{L}-1}, m_{122 \times \mathrm{L}-2}, \ldots m_1, m_0$$

These message symbols are distributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message symbols from the superframe. Otherwise, the RS-FEC encoder operates exactly the same as specified in 202.3.2.2.16.

202.3.2.2.15 RS-FEC recombine

The L encoded RS-FEC frames are combined into an interleaved RS-FEC superframe when the PCS operates as a HS_RX. The output symbols are as follows:

$$m_{122 \times \mathrm{L}-1}, m_{122 \times \mathrm{L}-2}, \ldots, m_1, m_0, p_{1,5}, \ldots, p_{\mathrm{L},5}, \ldots, p_{1,0}, \ldots, p_{\mathrm{L},0}$$

where $p_{i,r}$ is the r^{th} parity symbol of the i^{th} encoder.

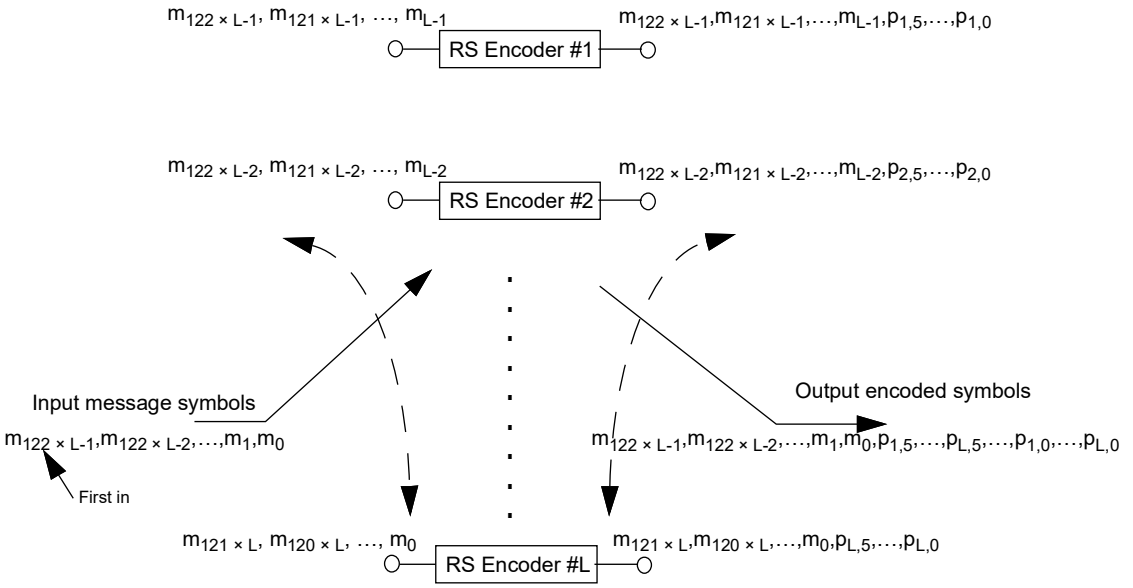


Figure 202–8—Interleaving block diagram with interleaving depth *L*

202.3.2.2.16 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field GF(2^8) where the symbol size is 8 bits. For the LS_PATH, the encoder processes k 8-bit RS FEC message symbols to generate (130-k) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. For the HS_PATH, the encoder processes k 8-bit RS FEC message symbols to generate (128-k) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 128 8-bit RS-FEC symbols. k = 124 is adopted for the LS_PATH and k = 122 is adopted for the HS_PATH. For the purposes of this clause, the respective particular Reed-Solomon code is denoted as RS-FEC(n,k), where n designates the FEC code block with n = 130 for the LS_PATH and n = 128 for the HS_PATH.

The code is based on the generating polynomial shown in Equation (202–1).

$$g(x) = \prod_{j=0}^{n-k-1}(x-\alpha^j) = g_{n-k}x^{n-k} + g_{129-k}x^{129-k} + \ldots + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (202\text{–}1)$$

In Equation (202–1), α is a primitive element of the finite field defined by the primitive polynomial $0x11D = x^8 + x^4 + x^3 + x^2 + 1$.

Equation (202–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0.

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1x^{n-k+1} + m_0x^{n-k} \quad (202\text{–}2)$$

Each message symbol m_i is the bit vector ($m_{i,7}$, $m_{i,6}$, …, $m_{i,1}$, $m_{i,0}$), which is identified with the element of the finite field $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<(8 × k - 1):0>.

For LS_TX, $m_{i,j}$ = tx_RSmessage<(123 - i) × 8 + j>, for i = 0 to 123, and i = 0 to 7.

tx_RSmessage<991:0> prior to RS-FEC(130,124) encoder is formed as follows:

tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<991:975> = OAM_field<16:0>.

For HS_TX, $m_{i,j}$ = tx_RSmessage<(121 - i) × 8 + i>, for i = 0 to 121, and i = 0 to 7.

tx_RSmessage<975:0> prior to RS-FEC(128,122) encoder is formed as follows for L = 1 (see 202.3.2.2.14):

tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<975> = OAM_field<0>.

For L = 2 and L = 4, see both 202.3.2.2.14 and 202.3.2.2.15.

The first symbol input to the encoder is $m_{k\text{-}1}$.

Equation (202–3) defines the parity polynomial $p(x)$ whose coefficients are the message symbols $p_{n\text{-}k\text{-}1}$ to p_0.

$$p(x) = p_{n-k-1}x^{n-k-1} + p_{130-k-2}x^{n-k-2} + \ldots + p_2x^2 + p_1x + p_0 \quad (202\text{–}3)$$

Each parity symbol p_i is the bit vector ($p_{i,7}$, $p_{i,6}$, …, $p_{i,1}$, $p_{i,0}$), which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 202–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x (e.g., $c_{129} = m_{k\text{-}1}$) is transmitted first and the coefficient of the lowest power of x (e.g., $c_0 = p_0$) is transmitted last. The first bit transmitted from each symbol is bit 0.

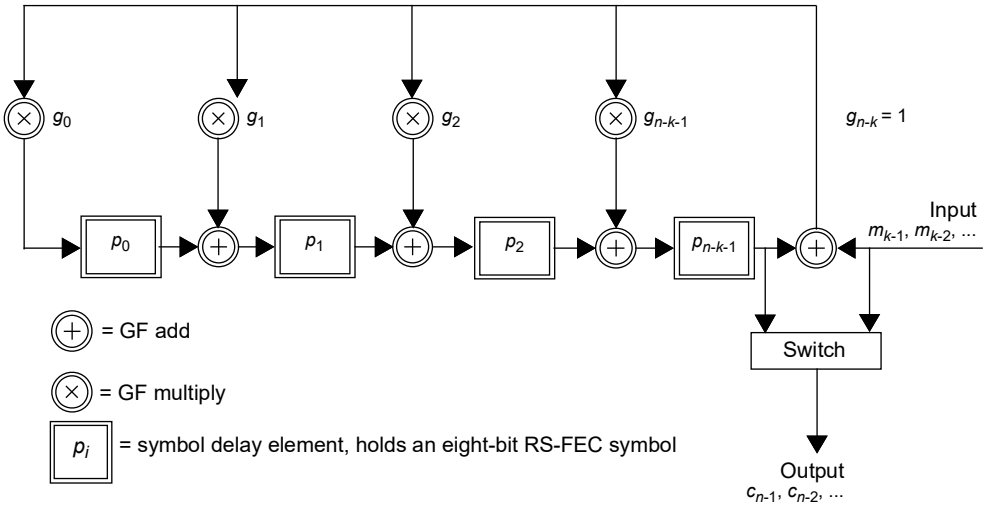


Figure 202–9—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 202–4.

Table 202–4—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(130,124)	RS-FEC(128,122)
0	38	38
1	227	227
2	32	32
3	218	218
4	1	1
5	63	63
6	1	1

202.3.2.2.17 PCS scrambler

PAM2 encoding is used for the refresh header (see 202.3.5) at all symbol rates. Consequently, the scrambled header data stream, C_n, is shown in Equation (202–4).

$$C_n = \begin{cases} DS_n[0] \oplus Tr_n[0] & \text{tx\_mode ! = SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad 0 \le n \le N\_r - 1 \qquad (202\text{–}4)$$

where

$DS_n[0]$ is produced using the scrambler defined in 202.3.4.1

PAM2 symbols are used for rates less than 10 Gb/s. The scrambled data stream, A_n, for PAM2 is shown in Equation (202–5). Bit $DS_n[0]$ is produced using the scrambler defined in 202.3.4.2. It is applied as an additive scrambler sequence to incoming data bit Dn[0] (LSB) to generate the scrambled data bit, A_n.

$$A_n = \begin{cases} DS_n[0] \oplus Tr_n[0] & \text{tx\_mode ! = SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1 \qquad (202\text{–}5)$$

For 10 Gb/s interfaces using PAM4 coding, the burst data bits of the interleaved RS-FEC superframe are grouped into pairs. Each pair of bits, $D_n[0]$ and $D_n[1]$, where n is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the PCS scrambler. The first least significant bit (LSB) bit is $DS_n[0]$ equal to $Scr_n[0]$ defined in 202.3.4. The second most significant (MSB) bit is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$.

Bits $DS_n[0]$ and $DS_n[1]$ in Equation (202–6) and Equation (202–7) are produced using the scrambler defined in 202.3.4.2. They are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$.

$$A_n = \begin{cases} DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1 \qquad (202\text{–}6)$$

$$B_n = \begin{cases} DS_n[1] \oplus D_n[1] & N\_r \le n \le N\_r + N\_p - 1 \end{cases} \qquad (202\text{–}7)$$

202.3.2.2.18 Gray mapping for PAM4 encoding

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where A_n is the bit arriving first, and n is an index indicating the symbol number, to Gray-coded symbols $G(n)$ with one of four levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

When receiving at 10 Gb/s in the PAM4 transmission period, the PCS Receive process shall map Gray-coded PAM4 symbols $G(n)$, with one of four levels, to pairs of bits, $\{A_n, B_n\}$, where A_n is considered to be the first bit as follows:

0 maps to {0, 0},
1 maps to {0, 1},
2 maps to {1, 1}, and
3 maps to {1, 0}.

202.3.2.2.19 PAM4 encoding

Editor's Note (to be removed prior to Working Group Ballot):

Deleting clause "202.3.2.2.19 Selectable precoder" during d0pb means that text referencing a precoder and other text needs to be adjusted (e.g., replace "precoder output symbol" with "Gray-coded" symbol. Diagrams should be checked, too.

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall encode each precoder output symbol to one of four PAM4 levels as specified in this clause.

The PAM4 encoded symbols are denoted $M(n)$, where n is an index indicating the symbol number.

Each consecutive precoder output symbol, $P(n)$, is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output $M(n)$.

Mapping from the precoder output symbol $P(n)$ to a PAM4 encoded symbol $M(n)$ is as follows:

0 maps to -1,
1 maps to -1/3,
2 maps to +1/3, and
3 maps to +1.

202.3.2.2.20 PAM2 mapping

During the PAM2 transmission period, the PCS Transmit process sends out PAM2 symbols according to following mapping:

Input bit S_n is mapped to the transmit symbol T_n as follows: if $S_n = 0$, then $T_n = +1$, if $S_n = 1$, then $T_n = -1$.

202.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 202–21 and the PCS Receive bit ordering in Figure 202–10 for the LS_RX and Figure 202–11 for the HS_RX, including compliance with the associated state variable as specified in 202.3.7.2.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM2 or PAM4 symbols are demapped and descrambling is performed according to rules.

Following descrambling, the *L*-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For LS_RX, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks. For HS_RX, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each burst, the 25 superframes can form a 25-bit OAM field for 2.5 Gb/s mode, a 50-bit OAM field for 5 Gb/s mode, and a 100-bit OAM field for 10 Gb/s mode.

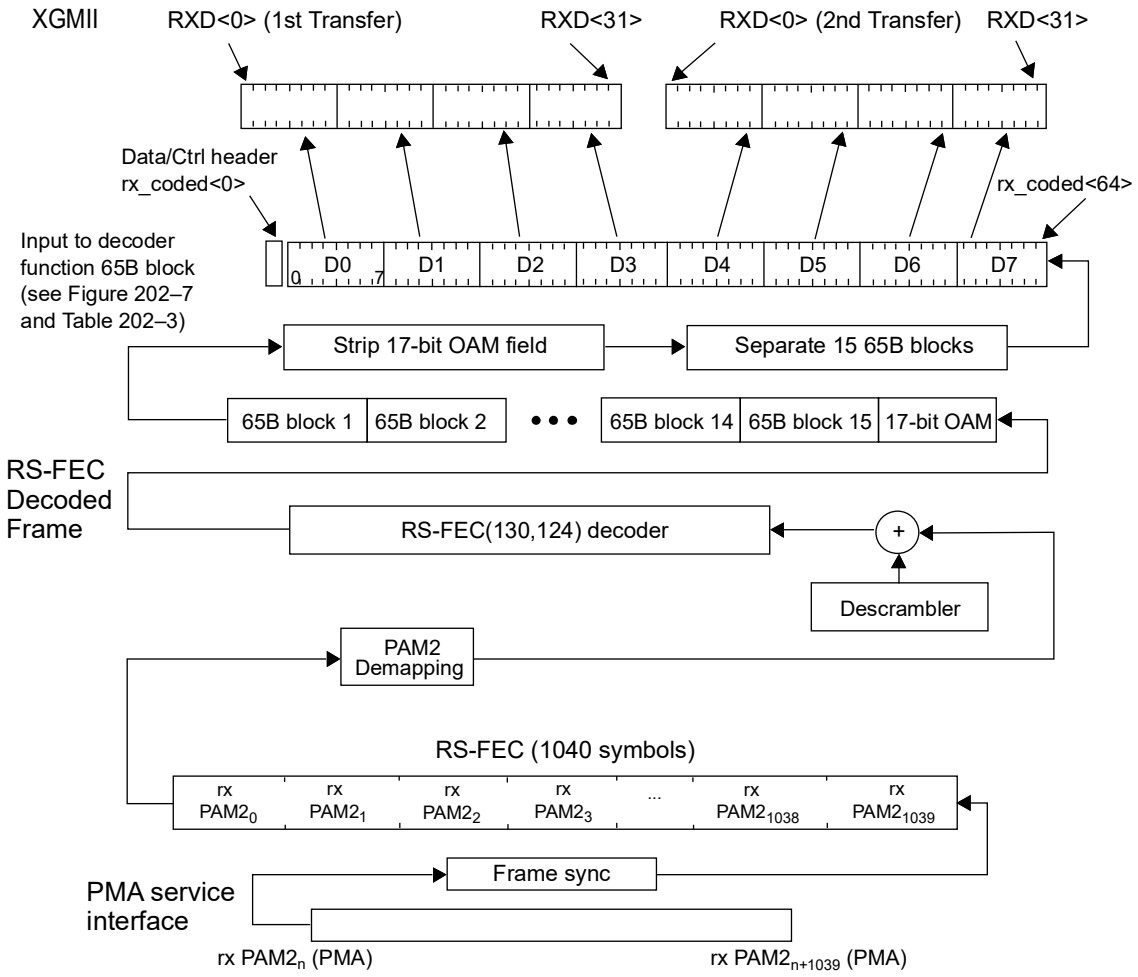
This process generates the 64B/65B block vector rx_coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 202–21). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 (TBD) consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi _rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

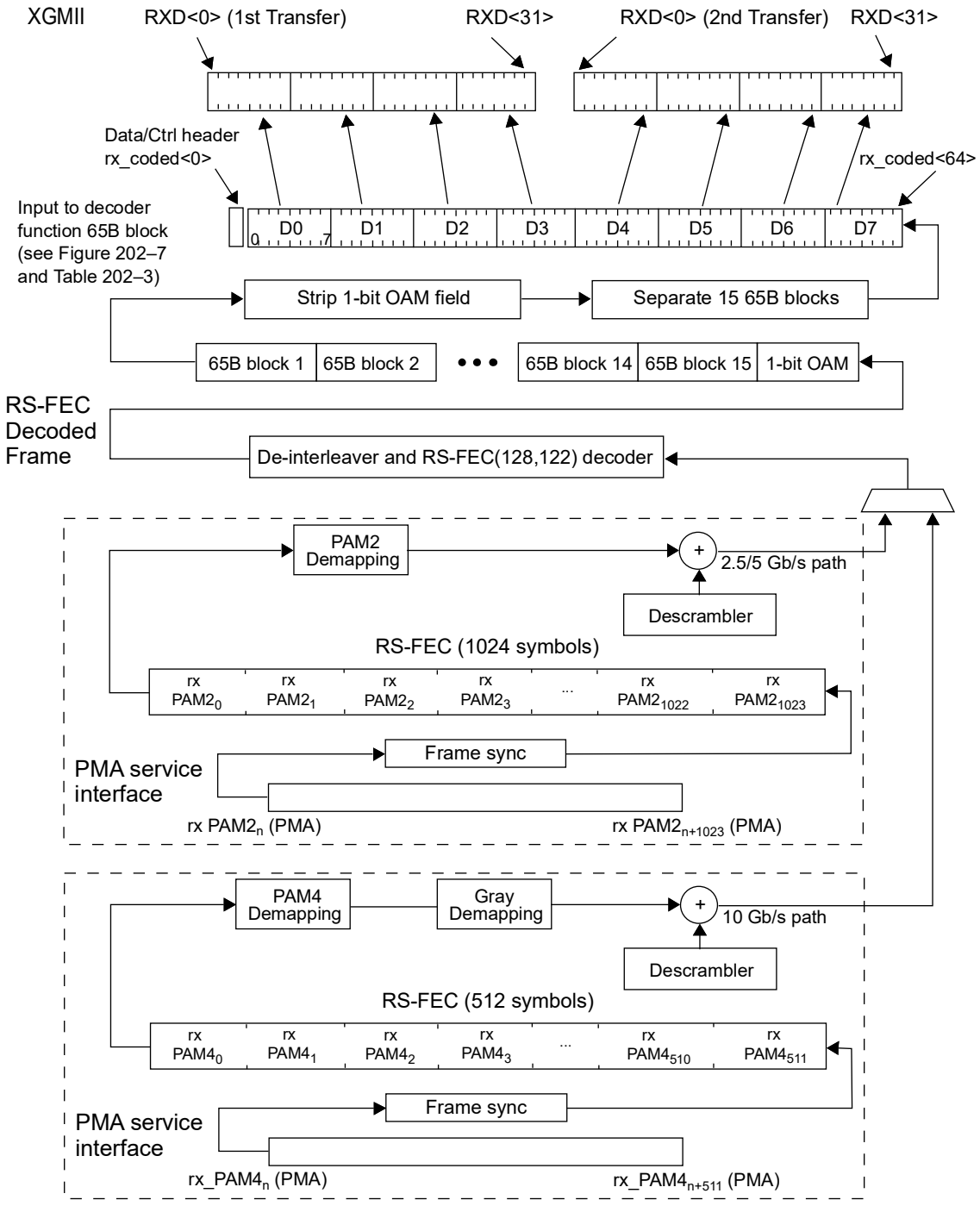
When the receiver is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status).

When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process when PHY Control is in PCS_TEST or PCS_DATA state. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header (see 202.3.5). It also includes training payload which has an Infofield, inserted in the N_inf^{th} bit of the training payload (see 202.3.5.3). When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.



NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

Figure 202–10—LS_RX PCS Receive bit ordering



NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

NOTE 2—Figure shown for L = 1.

NOTE 3—Either the PAM2 or PAM4 path is chosen.

Figure 202–11—HS_RX PCS Receive bit ordering

202.3.2.3.1 Frame and block synchronization

When operating in 100 Mb/s, 2.5 Gb/s, or 5 Gb/s data mode, the receiving PCS shall form a PAM2 stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM2_0 to rx_PAM2_1023 (see Figure 202–10 for LS_RX or Figure 202–11 for HS_RX). When operating in 10 Gb/s data mode, the receiving PCS shall form a PAM4 stream from PMA_UNITDATA.indication primitive by concatenating requests in order from rx_PAM4_0 to rx_PAM4_511 (see Figure 202–10).

The receiving PCS obtains block_lock to the PHY frames during training using synchronization sequence and Infofield provided in the training frames.

202.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For descrambling, the LEADER PHY shall employ the receiver descrambler generator polynomial per Equation (202-6) and the FOLLOWER PHY shall employ the receiver descrambler generator polynomial per Equation (202-5).

202.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 202–3.
c) Any O code contains a value not in Table 202–3.
d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 202.3.2.2.13. If the check fails, the RS-FEC frame is invalid. The R_BLOCK_ TYPE of an invalid block is set to E.

202.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, channel, and remote receiver.

When the transmit PCS is operating in test-pattern mode, it shall transmit TDD bursts as illustrated in Figure 202–5 or Figure 202–6, with the input to the RS-FEC encoder set to zero and the initial condition of the PCS scrambler set to any non-zero value. This has the same effect as setting the input to the PCS scrambler to zero.

When the receiver PCS is operating in test-pattern mode, it shall receive TDD bursts as illustrated in Figure 202–10 or Figure 202–11. The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero. However, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 (TBD) in 202.5.1.

202.3.4 PCS scrambler polynomials

The TDD bursts use different scrambler polynomials for the refresh_hdr and the burst payload. The scrambler used for the refresh_hdr, as well as some test modes, is defined in 202.3.4.1 The payload scrambler used for burst payloads is defined in 202.3.4.2.

202.3.4.1 PRBS11 scrambler polynomial

The refresh header specified in 202.3.5 shall be scrambled from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 202–12. This implements the generator polynomial shown in Equation (202–8), which is the same as Equation (72–1).

$$G(x) = 1 + x^9 + x^{11} \tag{202–8}$$

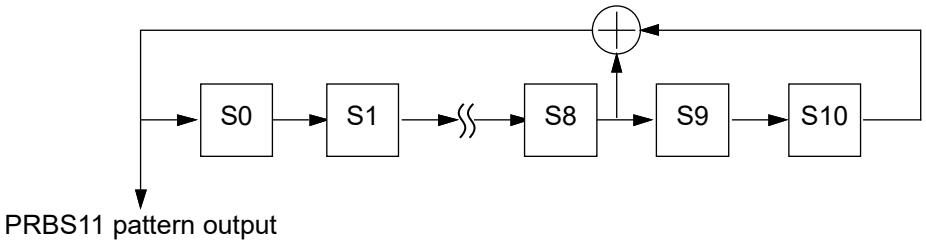


Figure 202–12—PRBS11 pattern generator

202.3.4.2 PRBS33 scrambler polynomials

The PCS Transmit function employs additive scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value LEADER, PCS Transmit shall employ Equation (202–9) as the transmitter scrambler generator polynomial.

$$g_M(x) = 1 + x^{13} + x^{33} \tag{202–9}$$

If the PMA_CONFIG.indication message assumes the value FOLLOWER, PCS Transmit shall employ Equation (202–10) as the transmitter scrambler generator polynomial.

$$g_S(x) = 1 + x^{20} + x^{33} \tag{202–10}$$

An implementation of the LEADER PCS and FOLLOWER PCS transmitter scramblers by linear-feedback shift registers is shown in Figure 202–13. The bits stored in the shift register delay line at time *n* are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case, shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the payload of PMA training frames and data mode frames and shall stop during QUIET and refresh headers.

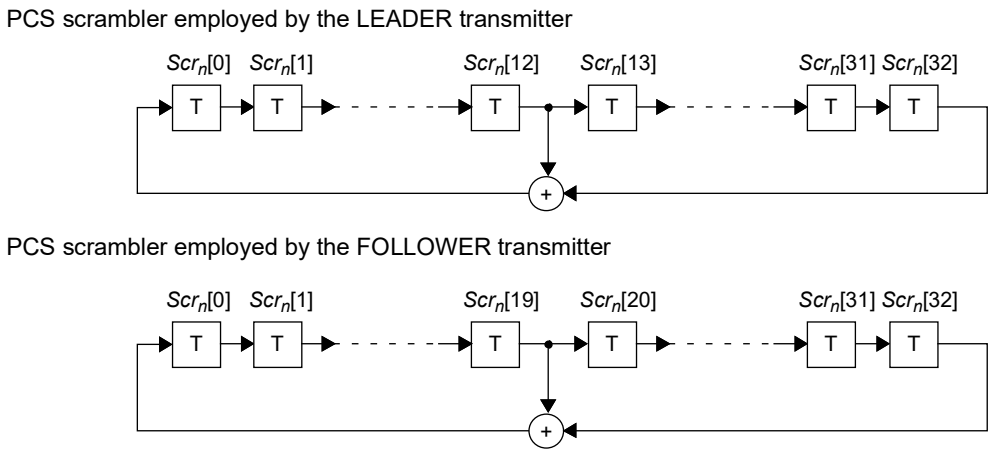


Figure 202–13—Realization of PCS scramblers by linear feedback shift registers

202.3.5 PMA training frame

Each PMA training frame includes a refresh header followed by a training payload.

Refresh header (refresh_hdr) is a sequence of PAM2 symbols with length of N_r symbols. Training payload is a sequence of PAM2 symbols with length of N_p symbols. The refresh header bits are all zeros except for the final 64 bits (see 202.3.5.2.1).

An 11-bit scrambler (see 202.3.5.2.1) is used to scramble the refresh_hdr. This scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

The training payload data sequence bits are all zeros, with the exception that a 96-bit Infofield is started at N_inf^{th} symbol of the training payload. This training data sequence $S\_t_{(n)}$ is defined in Equation (202–13).

The 33-bit scrambler (see 202.3.4) is used to scramble the training payload. Once started at the beginning of the training payload of the first training burst, this scrambler shall continue to run uninterrupted for each symbol during training payloads and shall stop during the QUIET period and refresh headers.

The Infofield is used to exchange messages between link partners during the startup training.

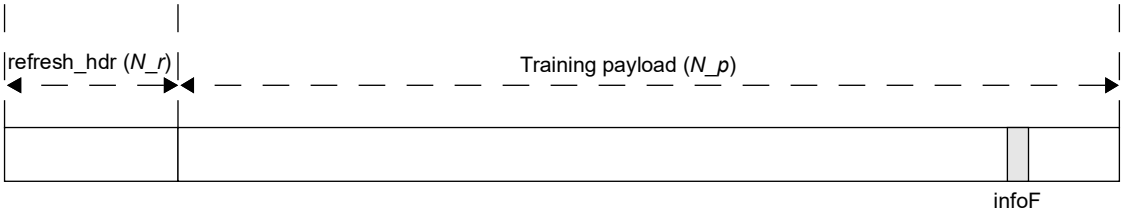


Figure 202–14—PMA Training frame

202.3.5.1 Refresh header and training payload length

The lengths for refresh_hdr and training payload are described in Table 202–5, Table 202–6, and Table 202–7.

Table 202–5—*N_r* and *N_p* value for 100 Mb/s mode transmission

tx_mode	refresh_header *N_r*(symb)	training_payload *N_p*(symb)
SEND_TS	560	12 880
SEND_TA	624	1024
SEND_N	624	1024

Table 202–6—*N_r* and *N_p* value for 2.5 Gb/s mode transmission

tx_mode	refresh_header *N_r*(symb)	training_payload *N_p*(symb)
SEND_TS	560	12 880
SEND_TA	480	26 000
SEND_N	480	26 000

Table 202–7—*N_r* and *N_p* value for 5 Gb/s mode and 10 Gb/s mode transmission

tx_mode	refresh_header *N_r*(symb)	training_payload *N_p*(symb)
SEND_TS	560	12 880
SEND_TA	960	52 000
SEND_N	960	52 000

202.3.5.2 Refresh header and training payload data bits generation

N_b is the number of bits in the training payload. *N_inf* is the bit position where Infofield starts within the training payload. The first bit of the training frame starts at bit 0, with $0 \le n \le N\_r$ - 1 consisting of the refresh header. Per Equation (202–13), $S\_t_{(n)}$ is all zeros from the end of the refresh header to the beginning of the Infofield, followed by the 96-bit Infofield, then followed by all zeros from the end of the Infofield to the end of the training payload, which is the end of the burst.

$$N\_b = N\_p \tag{202–11}$$

$$N\_inf = N\_b - 256 \tag{202–12}$$

$$S\_t_{(n)} = \begin{cases} refresh\_hdr(n) & 0 \le n \le N\_r - 1 \\ 0 & N\_r \le n \le N\_r + N\_inf - 1 \\ Infofield(n - [N\_r + N\_inf]) & N\_r + N\_inf \le n \le N\_r + N\_inf + 95 \\ 0 & N\_r + N\_inf + 96 \le n \le N\_r + N\_b - 1 \end{cases} \tag{202–13}$$

$$Tr_n[0] = \begin{cases} S\_t_{(n)} & 0 \le n \le N\_r + N\_b - 1 \end{cases} \tag{202–14}$$

$Tr_n[0]$ is the same as $S\_t_{(n)}$ and it is scrambled by the PRBS11 scrambler during the refresh header and scrambled by the PRBS33 scrambler during the training payload.

202.3.5.2.1 Refresh header encoding

The refresh_hdr is all zeros until eight bytes before the end of refresh_hdr. The next eight bytes header shall consist of 4 bytes of 0x01, followed by 4 bytes of 0xF0. The refresh_hdr bits are scrambled with the PRBS11 scrambler defined in (see 202.3.4.1). The PRBS11 scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

202.3.5.3 PMA training symbol generation

For training payload, $Tr_n[0]$ shall be scrambled with the $DS_n[0]$ which is equal to $Scr_n[0]$ defined in 202.3.4. The output scrambled bit A_n shall be input to PAM2 mapper. The refresh header is scrambled with the PBRS11 scrambler per 202.3.5.2.1.

Editor's Note (to be removed prior to Working Group Ballot):

Since training is never PAM4, the following can be deleted or moved to a section on the 10G data payload. Perhaps along with Equation (202–15).

The generation of scrambled bits $\{A_n,B_n\}$ can be found at Figure 202–4, with Equation 202.3.2.2.18. The $\{A_n,B_n\}$ shall be input to the Gray mapping for PAM4 encoding specified by 202.3.2.2.18. The output G_n can be input to precoder and then to the PAM4 mapper defined by 202.3.2.2.19.

$$G_n = \text{Gray mapping}(\{A_n, B_n\}) \tag{202–15}$$

Editor's Note (to be removed prior to Working Group Ballot):

These equations need to be amended and put in the correct section probably next section works. T(n) is not just training symbols, it's the whole burst, so it is PAM2 all the time except when tx_speed = 10G AND tx_mode = SEND_N AND (N_r<=n<=N_p-1).

$$T_{(n)} = \begin{cases} PAM2\_Mapper(A_n) & \sim(\text{tx\_speed} = 10\ \text{Gb/s} \times (\text{tx\_mode} = \text{SEND\_N} + \\ & \quad \text{tx\_mode} = \text{SEND\_TA\_EXT})) + (0 \le n \le N\_r - 1) \\ PAM4\_Mapper(G_n) & \text{tx\_speed} = 10\ \text{Gb/s} \times (\text{tx\_mode} = \text{SEND\_N} + \\ & \quad \text{tx\_mode} = \text{SEND\_TA\_EXT}) \times (N\_r \le n \le N\_r + N\_p - 1) \end{cases} \quad (202\text{–}16)$$

202.3.5.4 Generation of symbol O_n

Editor's Note (to be removed prior to Working Group Ballot):

From 202.3.2.2, On denotes the training sequence for SEND_TS and SEND_TA. (Note that Tn is used in 802.3ch.). May need linkage to T_n.

The transmit symbol O_n is selected by TDD control logic. For each TDD cycle (specified in 202.3.6), the transmitter will send out T_n and 0, based on symbol time index n.

n will be continuous symbol count modulo N_tdd. The 33-bit scrambler shall be stopped during refresh headers and QUIET period.

PAM2_Mapper is specified in 202.3.2.2.20.

PAM4_Mapper is specified in 202.3.2.2.19.

Gray mapping is specified in 202.3.2.2.18.

N_tdd is the number of symbols equivalent to a nominal 9.6 μs TDD cycle time.

$$O_n = \begin{cases} T_{(n)} & 0 \le n \le N\_r + N\_p - 1 \\ 0 & N\_r + N\_p \le n \le N\_tdd - 1 \end{cases} \quad (202\text{–}17)$$

202.3.5.5 PMA training mode descrambler polynomials

Editor's Note (to be removed prior to Working Group Ballot):

Needs to be acquired from PAM2, and then just continues on with PAM4.

The PCS shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status. The FOLLOWER PCS employs the receiver descrambler generator polynomial per Equation (202–9) and the LEADER PCS employs the receiver descrambler generator polynomial per Equation (202–10).

202.3.6 PCS TDD signaling

The timing diagram in Figure 202–15 shows the TDD cycle signaling and TDD frame structures assuming the LS_TX is configured as the LEADER and the HS_TX is configured as the FOLLOWER. Table 202–8 specifies the LS_TX and HS_TX transmit times in each TDD cycle.

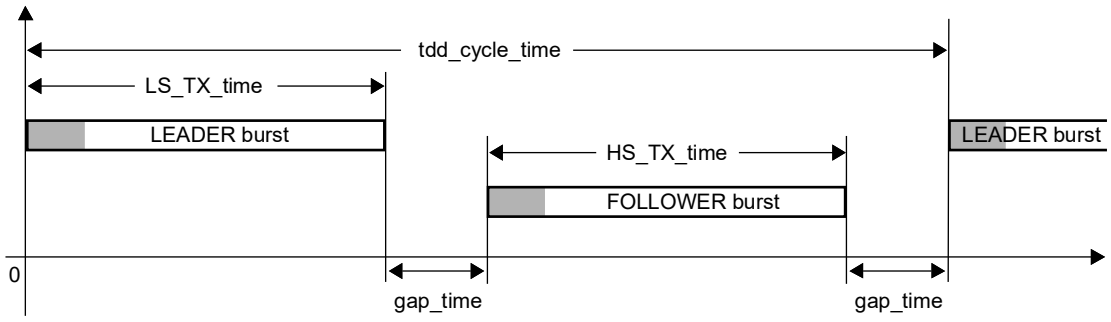


Figure 202–15—FOLLOWER/LEADER TDD cycle illustration

Table 202–8—LS_TX_time and HS_TX_time

tx_mode	LS_TX_time (ns)	HS_TX_time (ns)
SEND_TS	4480	4480
SEND_TA	560	8826.67
SEND_N		

The symmetric training burst timing and structure are illustrated in Figure 202–16.

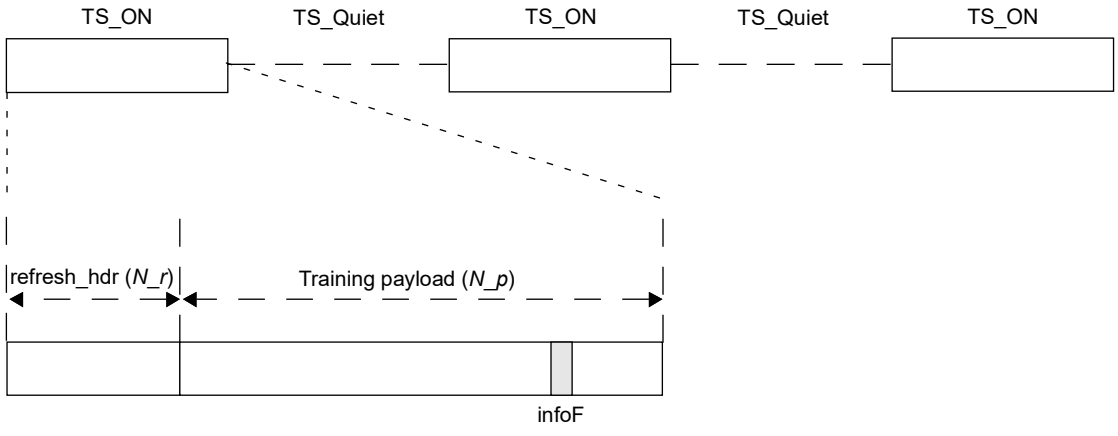


Figure 202–16—Symmetric training timing and frame structure

Figure 202–17 illustrates the LS_TX timing and frame structure for both the data mode and the asymmetric training modes. The refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 202.3.5. Note that FEC is not used with the training payload.

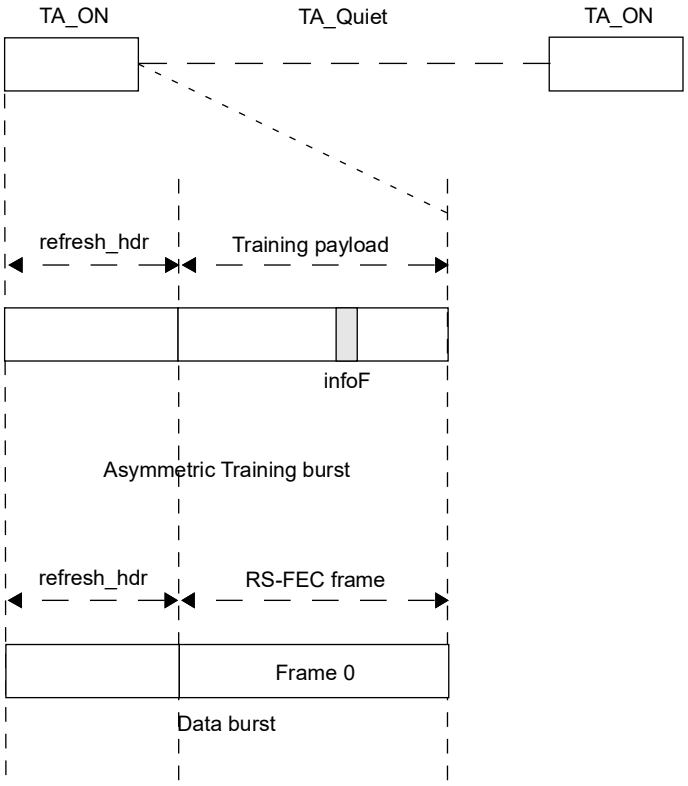


Figure 202–17—Asymmetric training/Data Mode timing and frame structure—LS_TX

Figure 202–18 illustrates the HS_TX timing and frame structure for both the data mode and the asymmetric training modes. As with the LS_TX direction, the refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 202.3.5 and FEC is not used with the training payload.

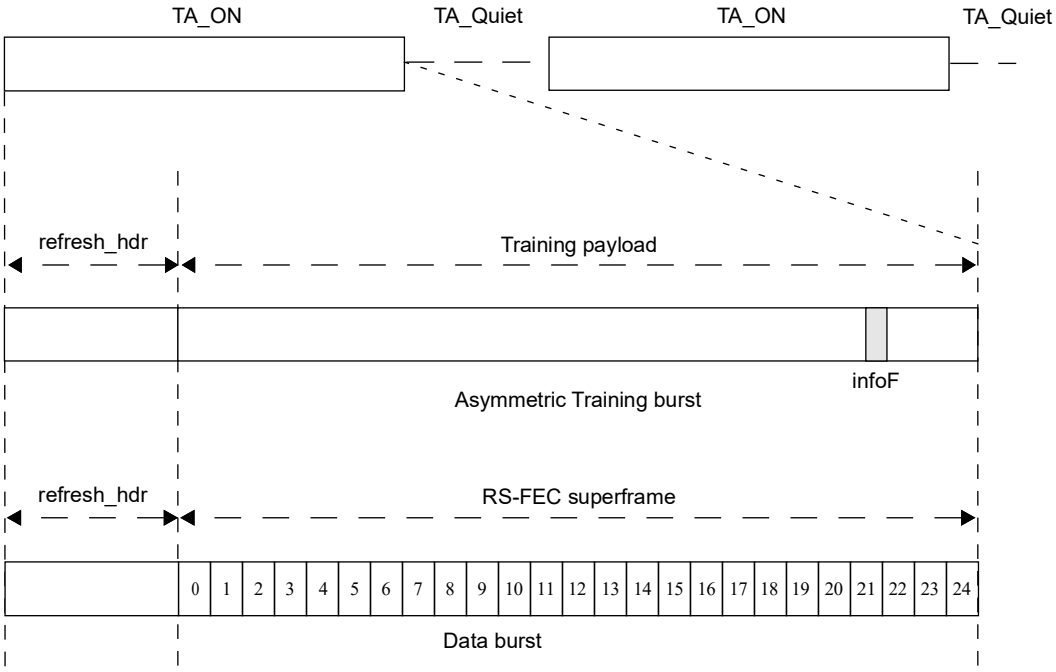


Figure 202–18—Asymmetric training/Data Mode timing and frame structure—HS_TX

202.3.7 PCS Detailed functions and state diagrams

202.3.7.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

202.3.7.2 State diagram parameters

202.3.7.2.1 Constants

EBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
: 65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
: 72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

IBLOCK_R<71:0>
72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.

RFER_CNT_LIMIT
TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: Integer
VALUE: 88
Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>
72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.
The Link Interruption ordered set is defined in 46.3.4.

202.3.7.2.2 Variables

block_lock
Boolean variable that is set TRUE when receiver acquires block delineation.

hi_rfer
Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one rfer_timer interval.

pcs_data_mode
Variable set by the PMA PHY Control function. See 202.4.4.1.

pcs_reset
Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rf_valid
Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

rs_fec_frame_done
A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. It is set FALSE otherwise.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 202–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_data_active

A Boolean variable that is set TRUE when the PHY PCS Receive function is operating in the data frame receive mode and set FALSE otherwise. This can be controlled by pre-defined timer after timing and frame synchronization is achieved.

rx_raw<71:0>

Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

tdd_detect

Set TRUE when the receiver has reliably detected TDD signaling. It is set FALSE otherwise.

tx_coded<64:0>

Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 202–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_data_active

A Boolean variable that is set TRUE during the TDD transmit mode, when PHY PCS is transmitting RS-FEC data frames. It is set FALSE otherwise.

tx_raw<71:0>

Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

tx_qt_active

A Boolean variable that is set TRUE during the TDD transmit mode, when the PHY is transmitting quiet signaling. It is set FALSE otherwise.

202.3.7.2.3 Timers

TDD_on_a_timer

A timer used to control the duration for the Transmission of asymmetric training sequence during TRAINING1 and COUNTDOWN1 state of PHY Control state. A value of 560 ns for the LEADER PHY and a value of 8826.67 ns for the FOLLOWER PHY.

TDD_on_d_timer

A timer used to control the duration for the Transmission of asymmetric data sequence during PCS_TEST and PCS_DATA state of PHY Control state. A value of 560 ns for the LEADER PHY and a value of 8826.67 ns for the FOLLOWER PHY.

TDD_on_s_timer

A timer used to control the duration for the Transmission of symmetric PAM2 training sequence during TRAINING0 and COUNTDOWN0 state of PHY Control state. A value of 4480 ns is defined.

TDD_qt_a_timer

A timer used to control the duration for the QUIET period of asymmetric training during TRAINING1 and COUNTDOWN1 state of PHY Control state. A value of 9040 ns for the LEADER PHY and a value of 773.33 ns for the FOLLOWER PHY.

TDD_qt_d_timer

A timer used to control the duration for the QUIET period during PCS_TEST and PCS_DATA state of PHY Control state. A value of 9040 ns for the LEADER PHY and a value of 773.33 ns for the FOLLOWER PHY.

TDD_qt_s_timer

A timer used to control the duration for the QUIET period of symmetric PAM2 training during TRAINING0 and COUNTDOWN0 state of PHY Control state. A value of 5120 ns is defined.

202.3.7.2.4 Functions

DECODE(rx_coded<64:0>)

In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 202.3.2.2.2

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 202.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and seven valid control characters other than /E/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a control code specified in Table 202–3. A valid O code is one containing an O code specified in Table 202–3.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) Eight valid control characters other than /O/, /S/, /T/, /E/;

b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;

c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 202–3. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 202–3.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

202.3.7.2.5 Counters

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt

Count number Reed-Solomon frames received during current period.

202.3.7.2.6 Messages

RX_FRAME

A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

202.3.7.3 State diagrams

The RFER monitor state diagram shown in Figure 202–19 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 202–20 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

The PCS 64B/65B Receive state diagram shown in Figure 202–21 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams.

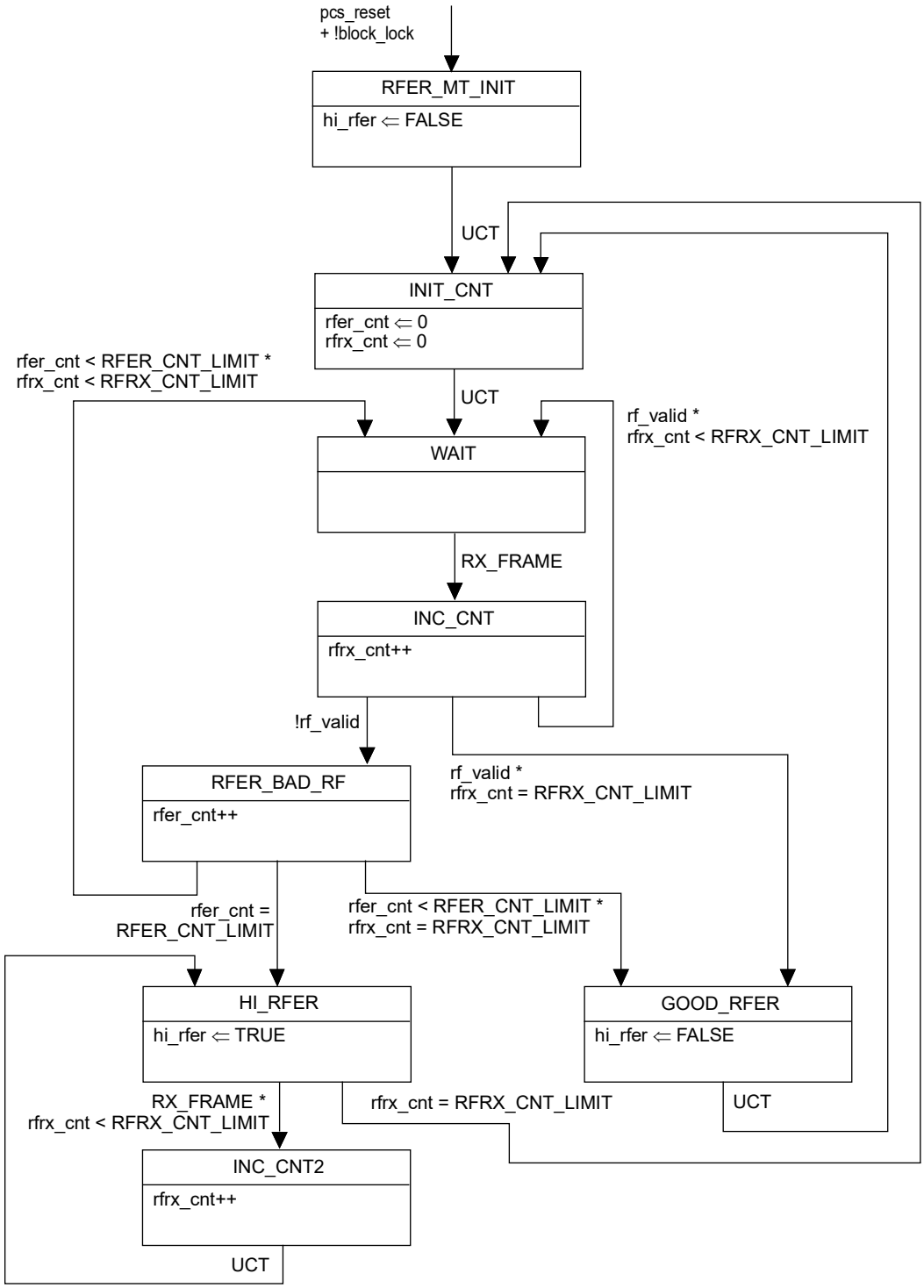


Figure 202–19—RFER monitor block state diagram

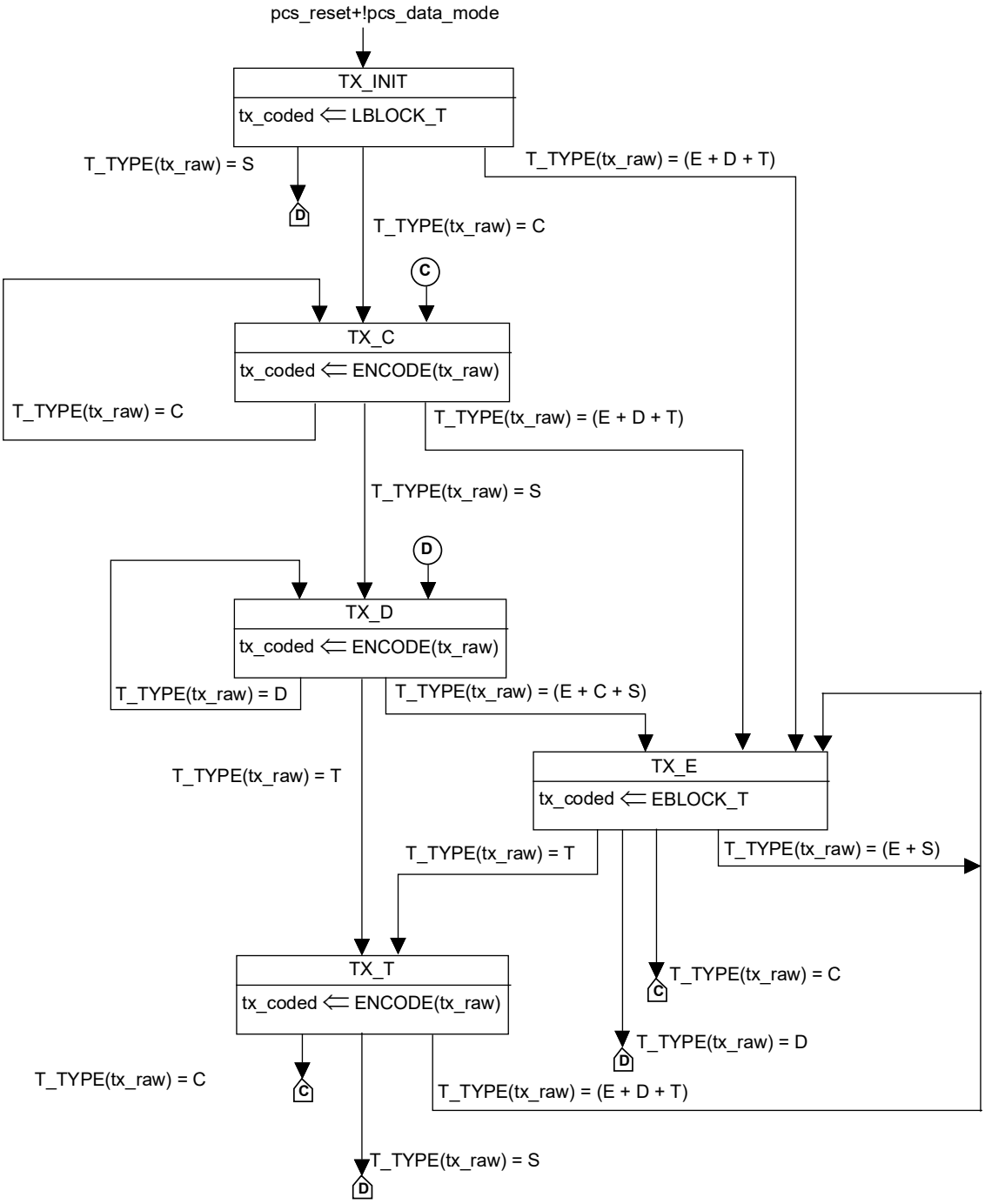


Figure 202–20—PCS 64B/65B Transmit state diagram

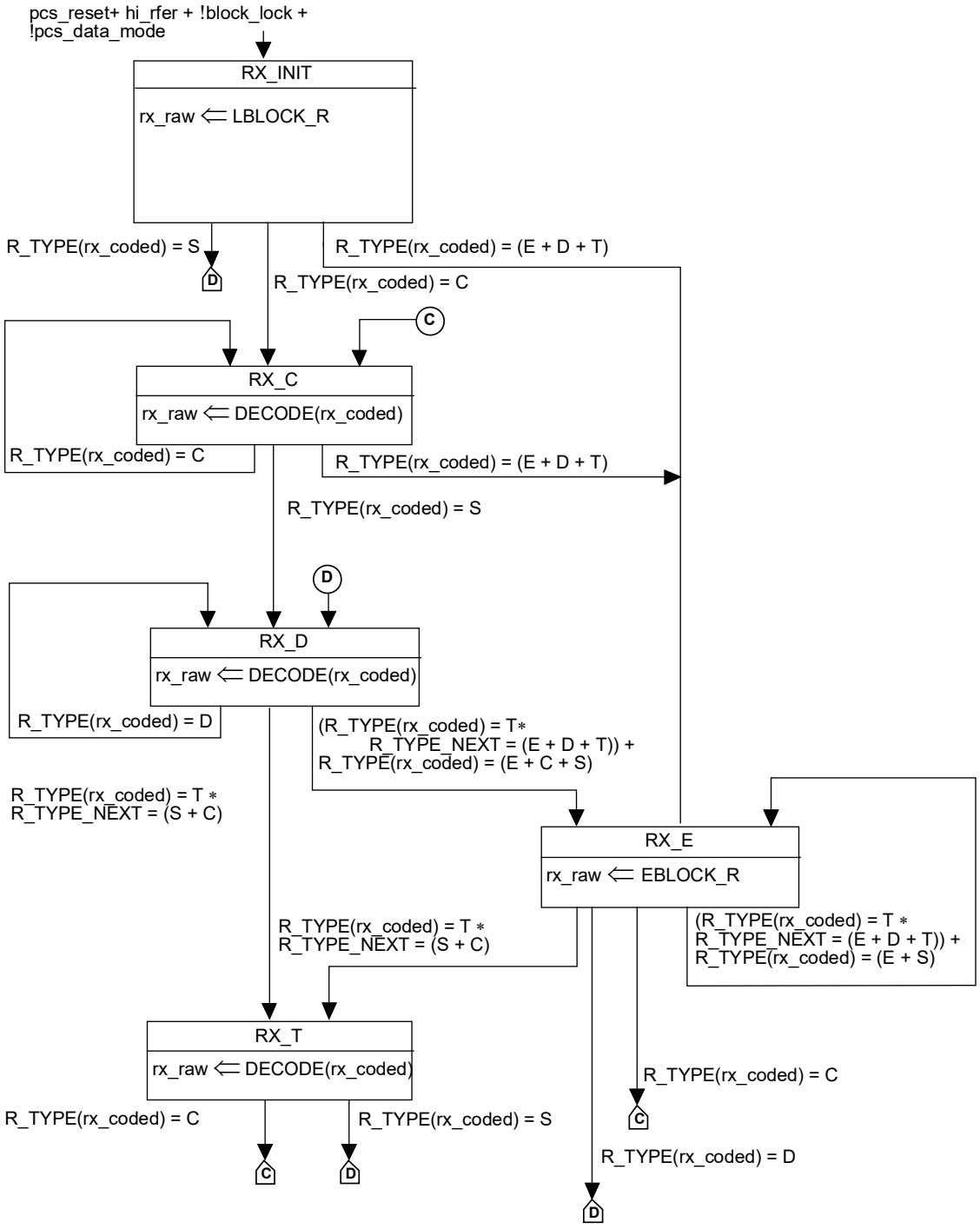


Figure 202–21—PCS 64B/65B Receive state diagram

202.3.8 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

202.3.8.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10 (TBD). A latch low view of this status is reflected in MDIO 3.2323.2 (TBD) and the inverse of this status is reflected in MDIO 3.2323.7 (TBD).

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8 (TBD). A latching low version of this status is reflected in MDIO bit 3.2324.6 (TBD).

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9 (TBD). A latching high version of this status is reflected in MDIO bit 3.2324.7 (TBD).

202.3.8.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

Editor's Note (to be removed prior to Working Group Ballot):

The descriptions in MDIO register 3.2324 need to be updated to align with Clause 202 as the current descriptions only point to Clause 149.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 202–19 is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

202.3.9 Operations, administration, and maintenance (OAM)

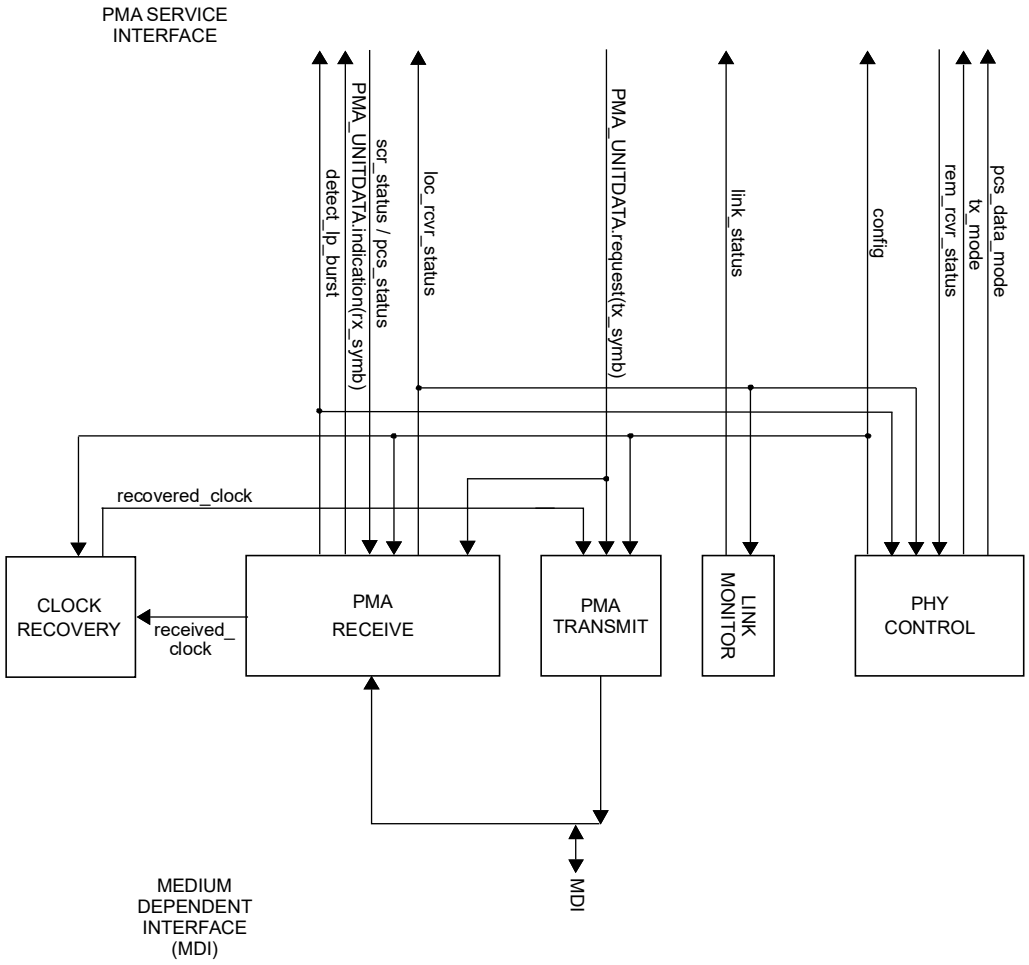
MultiGBASE-A operations, administration, and maintenance (OAM) is as specified for MultiGBASE-T1 PHYs in 149.3.9. OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one per TDD burst into the OAM fields in the HS_PATH and LS_PATH. OAM bits after the first ten per burst are reserved.

202.4 Physical Medium Attachment (PMA) sublayer

202.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 202.2.1 to the baseband medium specified in 202.7 or 202.8.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 202.9 or 202.10.



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

Figure 202–22—PMA reference diagram

202.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 202–22, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 202–22.

202.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 202–26), if link partner has already exited DISABLE_TRANSMITTER state.

202.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a two-level or four-level modulated signal on a single balanced pair of conductors or a single ended coaxial cable. When the PHY Control state diagram (see Figure 202–26) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI, followed by a quiet period to complete a TDD cycle. The PMA shall repeat such TDD cycles with the predefined timing parameters specified in 202.3.6. The signals generated by PMA Transmit shall comply with the electrical specifications given in 202.5.2.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source the transmit symbol clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of 202.5.2.3. The LEADER-FOLLOWER relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the recovered clock of 202.4.2.6 while meeting the jitter requirements of 202.5.2.3.

Editor's Note (to be removed prior to Working Group Ballot):

Need to add text to address transmit fault detection.

202.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

202.4.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM2 or PAM4 signals on the balanced pair or the single ended coaxial cable. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a -T1 link segment meeting the requirements of 202.7 or a -V1 link segment meeting the requirements of 202.8.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization. No echo cancellation is needed due to the TDD nature of the duplexing method.

The PMA Receive function uses the parameters pcs_status and scr_status, as well as the state of the equalization and estimation functions, to determine the quality of the receiver performance and generates the

loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see Figure 202–26). Failing to receive link partner's consecutive TDD bursts could trigger deassertion of loc_rcvr_status. The SEND_Z signal during the TDD QUIET period alone shall not trigger the DUT to de-assert its loc_rcvr_status. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for signal inversions.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.193.7 (TBD).

202.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 202–26.

During PMA training (TRAINING and COUNTDOWN states in Figure 202–26), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the 96 bits starting after the *N_inf* th bit of the training payload specified in 202.3.5.3. The link partner is not required to decode every Infofield transmitted but is required to decode Infofields at a rate that enables the correct actions prior to the training phase transition.

The 12-octet Infofield shall include the fields in 202.4.2.4.2 through 202.4.2.4.8, also shown in Figure 202–23 and Figure 202–24. When PMA_state = 00, Infofield shall be transmitted at least 16 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octet 8	octets 9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	delay counter	PHY capability bits	CRC16

Figure 202–23—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	PhaseSwBC24	CRC16

Figure 202–24—Infofield COUNTDOWN format

202.4.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved ‹bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (i.e., the LSB of octet 1 is sent first).

202.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<T:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0 > and so forth.

202.4.2.4.3 PHY burst count (BC24)

The PHY burst count consists of 3 octets [Oct4<7:0>,Oct5<7:0>,Oct6,7:0>] and indicates the running count of PHY bursts sent LSB first. The BC24 continues to run uninterrupted for the duration of the link.

BC24 is defined to rollover to 0 after it reaches 16776959. BC24 could roll over in the case the LEADER has started long before the FOLLOWER sends the first responding burst.

202.4.2.4.4 Message Field

The Message Field is one octet. For both the LEADER and FOLLOWER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, training_phase<4:3>, reserved<2:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.

The two training_phase-indicator bits training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> =00 indicates SYMMETRIC TRAINING and training_phase<4:3>=01 indicates ASYMMETRIC TRAINING.

All possible Message Field settings are listed in Table 202–9 for the LEADER or FOLLOWER. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 202–9 for the LEADER, and the first or second row of Table 202–9 for the FOLLOWER. Moreover, for a given Message Fields setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

Table 202–9—Infofield message field valid LEADER or FOLLOWER settings

PMA_state<7:6>	loc_rcvr_status	training_phase<4:3>	reserved	reserved	reserved
00	0	00	0	0	0
00	1	00	0	0	0
01	1	00	0	0	0
00[a]	0	01	0	0	0
00	1	01	0	0	0
01	1	01	0	0	0

[a]This row can be skipped if not applicable.

202.4.2.4.5 PHY capability bits

This multi-rate PHY supports bidirectional data transfer with 2.5 Gb/s, 5 Gb/s, or 10 Gb/s point-to-point transmission or reception in one direction and 100 Mb/s point-to-point reception or transmission in the other direction. The direction of asymmetry and high speed rate are determined at link startup. The management control configures the LEADER to negotiate with the FOLLOWER to configure it for the desired high speed data rate that the FOLLOWER is expected to use. The PHY capability and negotiated speed bits of the Infofield are used to establish the FOLLOWER rate and check for misconfiguration

When PMA_state<7:6>= 00, then [Oct9<7:0>,Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 202–10 for the details.

Table 202–10—PHY capability bits

octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData								PrecodeSel		OAMEn	Negotiated speed		Speed Capability 2.5 Gb/s	Speed Capability 5 Gb/s	Speed Capability 10 Gb/s

Speed Capability (PHY_S sets its TX capability and PHY_D set its RX capability): Oct10<5> 2.5 Gb/s capable, Oct10<6> 5 Gb/s capable, Oct10<7> 10 Gb/s capable.

Negotiated speed: 00 - 2.5 Gb/s, 01 - 5 Gb/s, 10 - 10 Gb/s

OAMEn: The optional OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1.

PrecodeSel indicates the requested precoder and is available for 10 Gb/s Speed Capability only (see 202.3.2.2.19).

The capability bit values shall be considered as valid only when loc_rcvr_status bit is 1.

The criteria to set Negotiated Speed is TBD.

202.4.2.4.6 TDD delay counter

When PMA_state<7:6>=00, then Oct8<7:0> contains TDD delay counter sent LSB first. The format of TDD delay counter is Oct8<0> = Reserved, Oct8<1:6> = delay_count<5:0>, and Oct8<7> = delay_count_valid. See Table 202–11 for the details.

Table 202–11—TDD delay counter

octet 8							
0	1	2	3	4	5	6	7
Reserved	delay_count						delay_count_valid

Editor's Note (to be removed prior to Working Group Ballot):

The text in the following 4 paragraphs is repeated in 202.4.2.4.11. Need to identify what information is needed here.

After the LEADER detects the FOLLOWER TDD burst position, it should estimate the link segment delay, then set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to 1. Each LSB unit represents 5.333 ns delay (16 symbols at 3 GBd).

The FOLLOWER shall accept the received remote delay_count only when received remote delay_count_valid bit is set to 1. The FOLLOWER shall store this delay_count number.

As acknowledgment of the reception of this delay_count, the FOLLOWER shall send back its received delay count in its own delay_count field and set its delay_count_valid to 1, so the LEADER can confirm the exchange of this information is completed. When the LEADER or the FOLLOWER finishes the exchange of delay count, the negotiated speed, and the PrecodeSel, it shall set Negotiation_done signal to 1. The PHY Control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.

Starting from Asymmetric training and continuing through to the data mode, the FOLLOWER shall adjust its transmit burst position according to the stored delay_count.

202.4.2.4.7 Phase switch PHY burst count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>] contains the phase switch burst count (PhaseSwBC24) sent LSB first. PhaseSwBC24 indicates the burst count when the LEADER transmitter switches from current training phase to the next training phase or Data mode. PhaseSwBC24 shall be a minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state.

Since phase switch is always initiated from the LEADER, the PhaseSwBC24 value of FOLLOWER Infofield will be ignored. The LEADER will exit a COUNTDOWN state after sending the last burst (BC24=PhaseSwBC24-1), and receiving the last burst from the FOLLOWER. The FOLLOWER will exit a COUNTDOWN state after receiving the last burst (BC24=PhaseSwBC24-1) from the LEADER and finishing sending the last burst of its own.

202.4.2.4.8 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>)] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

202.4.2.4.9 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 202–25. In Figure 202–25 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 202–25, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

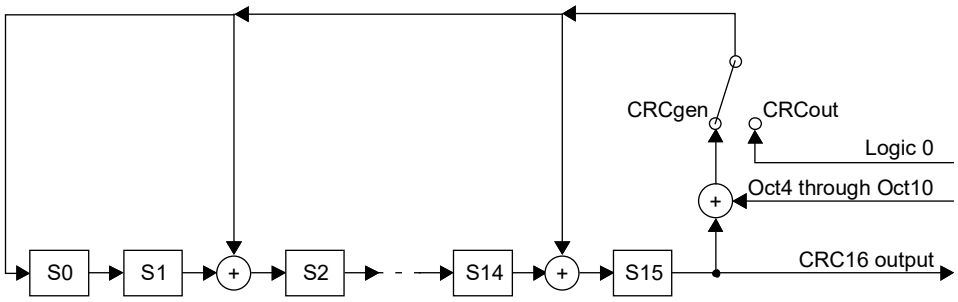


Figure 202–25—CRC16

202.4.2.4.10 PMA MDIO function mapping

Editor's Note (to be removed prior to Working Group Ballot):

Possible modifications to 149.4.2.4.9 may be required. Recommend adding text to describe references to register usage and naming.

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 202–12. Mapping of MDIO status variables to PMA status variables is shown in Table 202–13.

Table 202–12—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1 PMA control register	1.2309.14	PMA_transmit_disable

Table 202–13—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1 PMA status register	1.2310.1	PMA_receive_fault

202.4.2.4.11 Startup sequence

Editor's Note (to be removed prior to Working Group Ballot):

Table 149-15 provides some time limits on state transitions. It may be useful to apply here. TBD.

The startup sequence shall comply with the state diagram description given in Figure 202–26. PMA_CONFIG is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

When entering the TRAINING0 state, the FOLLOWER shall align the first symbol of the transmit PMA training frame to be on the transmit MDI 133.33 ns after the last PMA training payload symbol from the LEADER appears on the FOLLOWER input MDI. The FOLLOWER shall maintain this alignment while in the TRAINING0 state. The FOLLOWER Infofield burst count shall match the LEADER Infofield burst count from the previous PMA training frame.

In the TRAINING0 state, PAM2 transmission is used and PHY capabilities, PrecoderSel, and delay_count are exchanged with Infofields as specified in 202.4.2.4.5. The final negotiated speed mode will be determined by the LEADER. The FOLLOWER shall continue to maintain this alignment until it enters the TRAINING0 state.

At any COUNTDOWN or PCS_TEST state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT state and attempts a retrain.

When entering the TRAINING1 state, the FOLLOWER shall use the LEADER transmitted delay_count to align its transmit PMA training frame to be 176 ns - delay_count × 5.33 ns, after the last PMA training payload symbol from the LEADER appears on the FOLLOWER input MDI.

The LEADER link_fail_inhibit_timer is started when it detects the first FOLLOWER transmitted PMA training frame. The FOLLOWER link_fail_inhibit_timer is started when it sends first PMA training frame to the LEADER. The link_fail_inhibit_timer value is defined to be 97.5 ms, it is used to force a restart if the link up cannot be achieved within maximum allowed time.

The LEADER and FOLLOWER will move from TRAINING0 state to COUNTDOWN0 state, if local_rcvr_status and rem_rcvr_status are both asserted, and negotiation_done bit is OK.

202.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive link and communicates it via the variable link_status. Failure of the underlying receive link causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the link.

The Link Monitor function shall comply with the state diagram of Figure 202–28.

Upon power on reset, or release from power down, the PHY sets link_control = DISABLE. During this period, link_status = FAIL is asserted. When the PHY link_control is set to ENABLE, the Link Monitor state diagram begins monitoring the PMA. As soon as reliable transmission is achieved, with pcs_data_mode=TRUE, the variable link_ status = OK is asserted, upon which further PHY operations can take place.

202.4.2.6 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 202.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock for use when configured as the FOLLOWER.

202.4.3 MDI

Communication through the MDI is summarized in 202.4.3.1 and 202.4.3.2.

202.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. During RS-FEC frame transmission, 10 Gb/s transmit path uses PAM4 while all other symbols transmitted within a burst use PAM2. PMA Transmit generates a pulse-amplitude modulated signal in the form shown in Equation (202–18).

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \quad (202–18)$$

In Equation (202–18), a_n is the PAM4 modulation symbol from the set {–1, –1/3, +1/3, +1} or the PAM2 modulation symbol from the set {–1, +1} to be transmitted at time nT, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 202.5.2.

202.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as shown in Equation (202–19).

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \quad (202–19)$$

In Equation (202–19) $hR(t)$ denotes the symbol response of the overall impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

202.4.4 State variables

202.4.4.1 State diagram variables

config
The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.
Values: LEADER or FOLLOWER.

link_control
This variable is generated by management or set by default.
Values: ENABLE or DISABLE.

link_status
The link_status parameter set by PMA Link Monitor state diagram.
Values: OK or FAIL.

loc_countdown_done
This variable is only used by the LEADER. It is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state, or after entering the new TRAINING state, and is set to TRUE once the LEADER finishes sending the last LEADER countdown Infofield and receiving the responding (last) Infofield from the FOLLOWER at the current TRAINING stage.

loc_rcvr_status
Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY at the current TRAINING stage. This variable is transmitted in the loc_rcvr_status bit of the Infofield by the local PHY.
Values:
OK: The receive link for the local PHY is operating reliably.
NOT_OK: Operation of the receive link for the local PHY is unreliable.

negotiation_done
During symmetric training phase, after loc_rcvr_status=1, the LEADER and FOLLOWER shall exchange capabilities, delay_count and negotiated speed, and then set negotiation_done bit.
Values:
OK: Negotiation is done, can move to COUNTDOWN0 state.
NOT_OK: Negotiation is not done, stay in TRAINING0 state.

pcs_data_mode
Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

pma_reset
Allows reset of all PMA functions. It is set by PMA Reset.
Values: ON or OFF.

PMA_state
Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.
Values:
00: TRAINING state.
01: COUNTDOWN state.

rem_countdown_done

This variable is only used by the FOLLOWER. It is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SLIENT state, or after entering the new TRAINING state, and is set to TRUE once the FOLLOWER receives the last countdown Infofield from the LEADER and finishes sending one Infofield from the FOLLOWER at the current TRAINING stage.

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. This variable is received in the loc_rcvr_status bit in the Infofield from the remote PHY. This variable is set to NOT_OK if the PCS has not decoded valid Infofields from the remote PHY.

Values:

OK: The receive link for the remote PHY is operating reliably.

NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.

tdd_watchdog_status

Variable indicating the status of the TDD monitor. During normal operation, NOT_OK is assigned when a TDD signal is not reliably detected within a moving time window equivalent to 10 complete TDD cycles.

Values:

OK: TDD burst is detected reliably.

NOT_OK: TDD burst is not detected reliably.

tx_mode

The PMA generates this variable continuously and passes it to the PCS via the PMA_TXMODE.indication primitive (see 202.2.1).

Values:

SEND_N: This value is continuously asserted when transmission of sequences of symbols representing a XGMII data stream take place.

SEND_TS: This value is continuously asserted when transmission of sequences of symbols representing the symmetric training sequences of symbols is to take place.

SEND_TA: This value is continuously asserted when transmission of sequences of symbols representing the asymmetric training sequences of symbols is to take place.

SEND_Z: This value is asserted when transmission of zero symbols is to take place.

202.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

link_fail_inhibit_timer

A timer used to determine the maximum amount of time the PHY Control stays in the TRAINING, COUNTDOWN, and PCS_TEST states. The timer shall expire 97.5 ms ± 0.5 ms after being started.

LEADER: This timer will be started when the LEADER PHY receives the first burst from the FOLLOWER.

FOLLOWER: This timer will be started when the FOLLOWER PHY sends the first burst to the LEADER.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT and PCS_TEST states. The timer shall expire 975 μs ± 50 μs after being started.

202.4.5 State diagrams

The PHY Control state diagram is shown in Figure 202–26 and Figure 202–27.

The Link Monitor state diagram is shown in Figure 202–28.

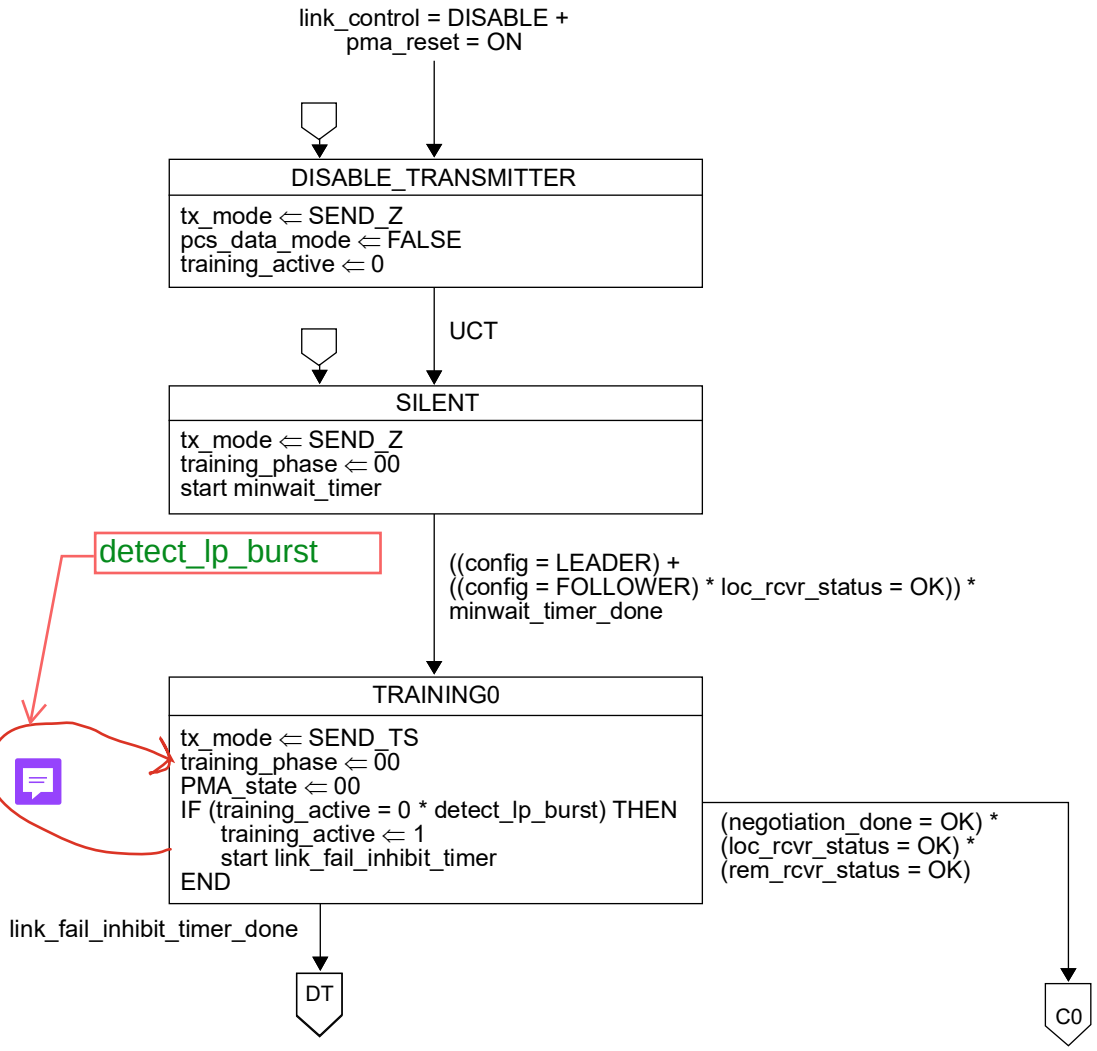


Figure 202–26—PHY Control state diagram, part a

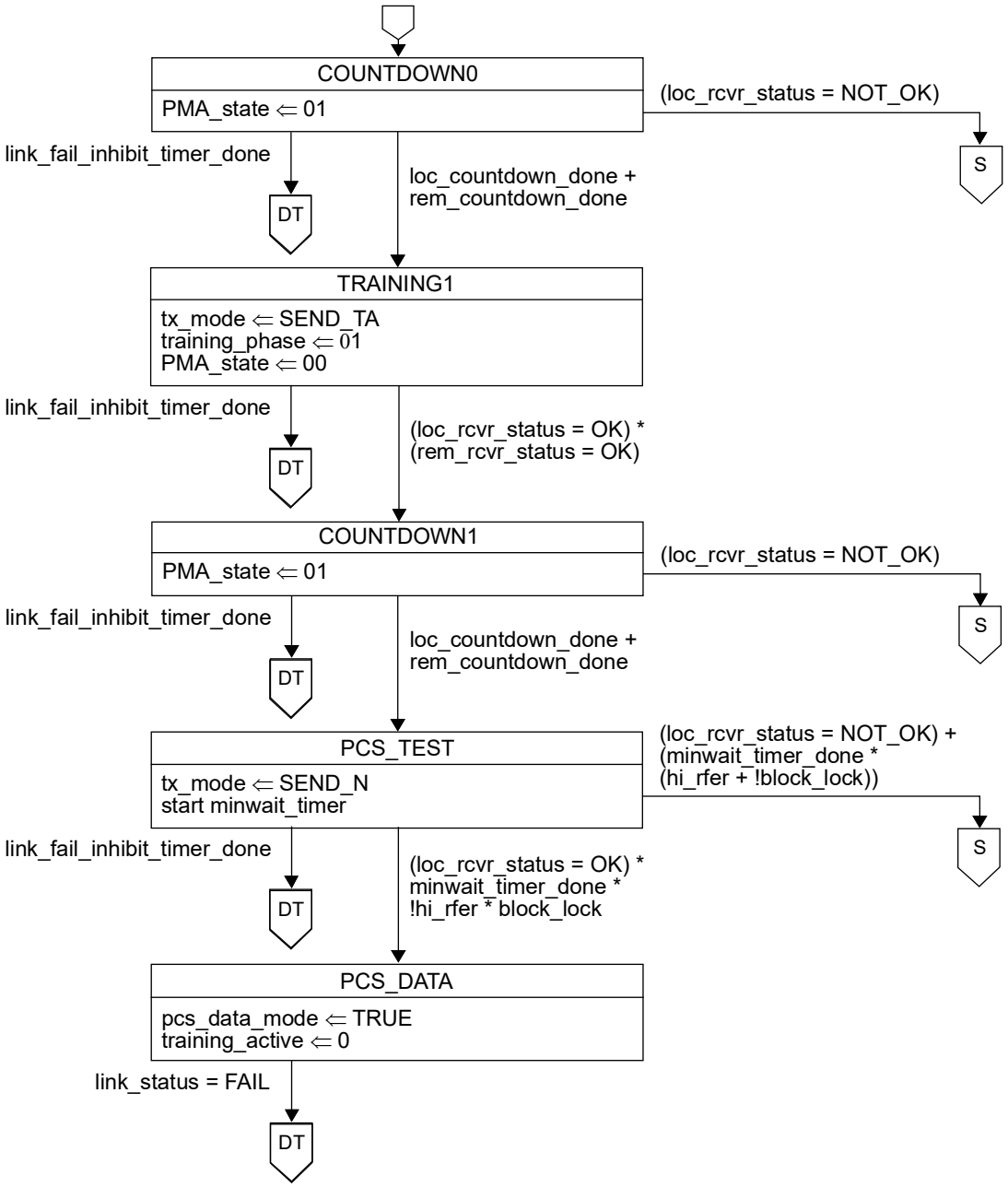


Figure 202–27—PHY Control state diagram, part b

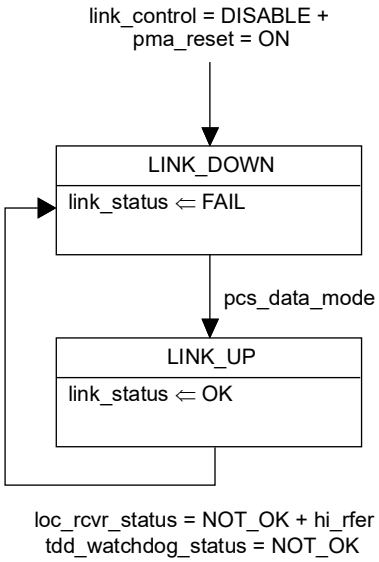


Figure 202–28—Link Monitor state diagram

202.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

202.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 202–14. If MDIO is not implemented, then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Test mode 1 enables testing of timing jitter on the LEADER and FOLLOWER transmitters. The LEADER and FOLLOWER PHYs are connected over a link segment defined in 202.7 or 202.8. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5. TX_TCLK_187.5 is equal to 187.5 MHz and is a divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous repeating pattern of {+1, -1} symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference.

Table 202–14—MDIO management registers settings for test modes

Register value	Register description
000	Normal (non-test mode) operation
001	Test mode 1—Setting LEADER and FOLLOWER PHYs for transmit clock jitter test in linked mode
010	Test mode 2—Transmit MDI jitter test in LEADER mode
011	Test mode 3—Precoder test mode
100	Test mode 4—Transmitter distortion test
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test
110	Test mode 6—Transmitter droop test mode
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring

Test mode 3 is for testing the precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the transmit precoder specified in 202.3.2.2.19, to be precoded according to the transmit precoder settings as determined by the value set in register 1.2313:10:9, or equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.

Test mode 4 is for transmitter distortion testing. When test mode 4 is enabled in PAM2 mode, the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (202–20) such that $A_n = Scr_n[0]$ (see Figure 202–4). All PHYs shall support transmission of this signal at 3 GBd. PHYs that support 5 Gb/s and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM4 mode, the PHY shall transmit the PCS scrambler generator polynomial per Equation (202–20) such that $A_n = Scr_n[0]$ and $B_n = Scr_n[3] \oplus Scr_n[8]$ (see Figure 202–4). PHYs that support 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

$$g(x) = 1 + x^9 + x^{11} \tag{202–20}$$

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit continuously with no quiet gap or refresh header and with transmit signal level corresponding to the normal mode of operation. The PCS Transmit will encode data as when tx_mode = SEND_N, and as if continuously receiving idle control characters from the XGMII. The test applies to both the LEADER and FOLLOWER. The clock is sourced from a stable clock with 100 ppm accuracy for this test.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, the input to the RS-FEC is all-zero message symbols and the continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors.

Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

202.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 202–29, Figure 202–30, and Figure 202–31, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

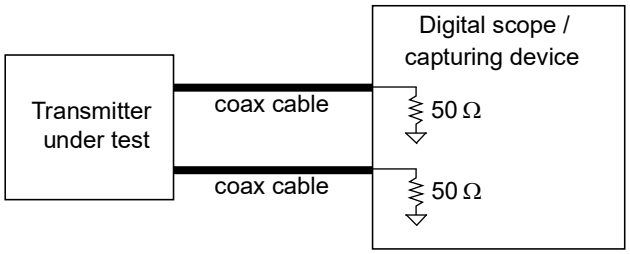


Figure 202–29—Transmitter test fixture 1 for -T1 transmitter droop, transmitter linearity, power spectral density, transmit power level, and MDI jitter measurements

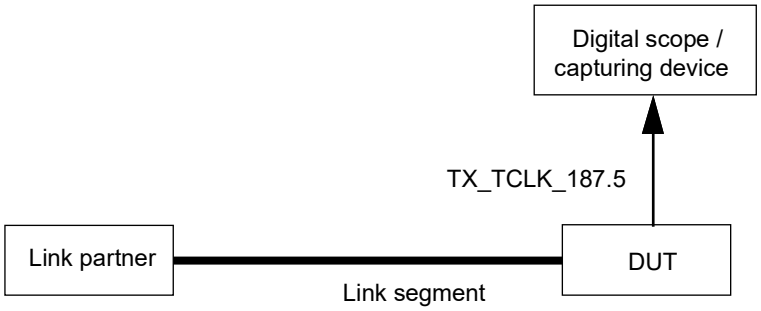


Figure 202–30—Transmitter test fixture 2 for -T1 and -V1 LEADER and FOLLOWER clock jitter measurement

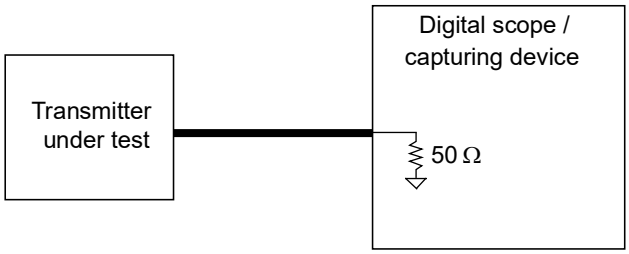


Figure 202–31—Transmitter test fixture 3 for -V1 transmitter droop, transmitter linearity, power spectral density, transmit power level, and MDI jitter measurements

202.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 202.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be ac-coupled (i.e., it presents a high dc common-mode impedance at the MDI). There may be various methods for ac-coupling in actual implementations.

When a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

202.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using transmitter test fixture 1 (see Figure 202–29) or test fixture 3 (see Figure 202–31), the magnitude of both the positive and negative droop shall be less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing.

202.5.2.2 Transmitter distortion

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 1 (see Figure 202–29) or transmitter test fixture 3 (see Figure 202–31) as appropriate to the MDI.

The peak distortion is determined by sampling the signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signal shall be at least 4000 transmitted symbols long and be sampled with the minimum 10x oversampling. The transmit baud rate may be reduced to 1 Gs/s by repeating the symbols using the same clock edge as in normal mode of operation.

The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM4 transmitters.

```
% Post processing pseudo-code for transmitter distortion
clear
Ns=2^11-1; % Scrambler length
Nc=70; % Canceller length
```

```
Modulation=2; % Choices are 2 or 4 for PAM2 and PAM4

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
   scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% Generate tm4 (test mode 4) for a given modulation
if Modulation==2
   tm4=2*scr-1;
else if Modulation==4
   tm4=ones(Ns,1);
   map=[-1;-1/3;1;1/3];
   DS=[scr,mod(circshift(scr,3) + circshift(scr,8),2)];
   data = 2*DS(:,1)+DS(:,2);
   for n=1:length(DS)
   tm4(n) =map(data(n)+1);
   end
else
   disp('Error: The code supports either PAM2 or PAM4')
   return
end

% Test mode4 matrix
for i=1:Nc
X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file

% Minimum of 4K TX symbols, 10X oversampling, high resolution capture
fid=fopen('TestMode4.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF at Nyquist
[A,B]=butter(1,1/10,'low');
tx=filter(A,B,tx);

% HPF (with this HPF, the 70-tap canceller residual linear error is 0.00
tx = filter([1,-1],[1,-0.98],tx);

% Select one period, 10x oversampling, a row vector
tx=tx((1:Ns*10)+2e3)'; % removes HPF transients

% Level normalization
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10
tx1=tx(n:10:end);
temp=xcorr(tx1,tm4); % Align data and test pattern
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);
coef=tx1/X; % Compute coefficients that minimize squared error in a cyclic
   block
err=tx1-coef*X; % Linear canceller
dist(n) = max(abs(err)); % Peak distortion
```

```
SNR(n)=std(tx)/std(err); % SNR
End

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist
```

202.5.2.3 Transmitter timing jitter and jitter at the MDI

The following measurements are performed for a PHY in LEADER mode:

1) The RMS jitter for jitter frequencies greater than 100 kHz measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1 shall be less than 1 ps when supporting 10 Gb/s, 2 ps when supporting 5 Gb/s/, and 4 ps when supporting 2.5 Gb/s.
2) Peak-to-peak of Time Interval Error measured in test mode 1 using test fixture 2 over a period of 100 μs shall be less than 10 ps when supporting 10 Gb/s, 20 ps when supporting 5 Gb/s, and 40 ps when supporting 2.5 Gb/s.

The following measurements are performed using test fixture 2 (see Figure 202–30) for a PHY in FOLLOWER mode:

1) The RMS jitter for jitter frequencies greater than 1 MHz measured in test mode 1 shall be less than 1 ps when supporting 10 Gb/s, 2 ps when supporting 5 Gb/s, and 4 ps when supporting 2.5 Gb/s.
2) Peak-to-peak of Time Interval Error over any period of 10 μs measured in test mode 1 over 50 overlapping periods of 10 μs each shall be less than 15 ps for 10 Gb/s, 30 ps for 5 Gb/s, and 60 ps for 2.5 Gb/s. The overlapping period of 5 μs is assumed.

202.5.2.4 Transmitter power spectral density (PSD) and power level

Transmitter power spectral density (PSD) and power level measurements are performed in test mode 5. The measured transmit power shall be in the range specified in Table 202–15 when using the same test fixture as used for PSD measurement.

Table 202–15—Power levels

Transmit MAC data rate	Differential (balanced)		Single-ended (unbalanced)	
	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
100 Mb/s	0	2	-3	-1
2.5 Gb/s	0	2	-3	-1
5 Gb/s	2	4	-1	1
10 Gb/s	0	2	-3	-1

The power spectral density of the transmitter of -T1, measured into a 100 Ω differential load using test fixture 1 (see Figure 202–29), shall be between the upper and lower masks specified in Equation (202–21) and Equation (202–22).

The upper and lower masks for each MAC data rate are shown in Figure 202–32, Figure 202–33, and Figure 202–34. See Table 202–2 for the definition of *S*. See Table 202–16 for the definition of PSD mask *K* factor.

Table 202–16—PSD mask *K* factor

Transmit MAC data rate	*K*
100 Mb/s	0
2.5 Gb/s	0
5 Gb/s	0
10 Gb/s	2

$$UPSD(f) = \begin{cases} -89 - K & \text{dBm/Hz} \quad 40 < f \le 1200 \times S \\ -87 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 1200 \times S < f \le 3000 \times S \\ -80 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 3000 \times S < f \le 5000 \times S \end{cases} \tag{202–21}$$

$$LPSD(f) = \begin{cases} -93 - K & \text{dBm/Hz} \quad 40 < f \le 600 \times S \\ -92 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 600 \times S < f \le 2400 \times S \\ -86.4 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 2400 \times S < f \le 3500 \times S \end{cases} \tag{202–22}$$

where

f is the frequency in MHz

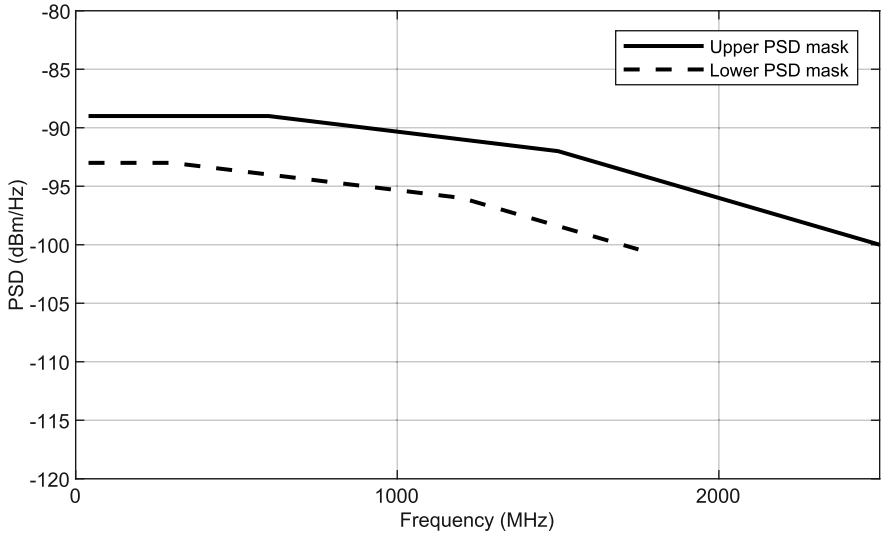


Figure 202–32—Transmitter Power Spectral Density for 100 Mb/s and 2.5 Gb/s MAC data rates, upper and lower masks

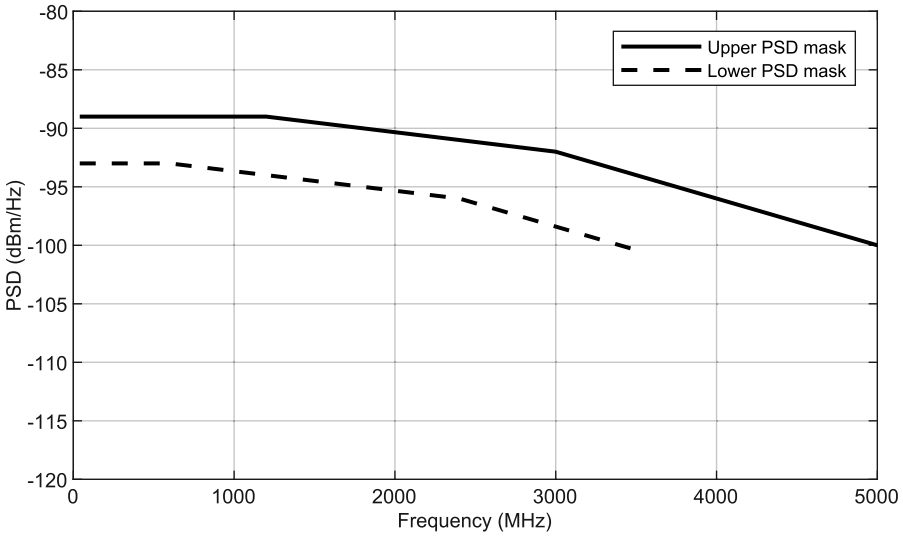


Figure 202–33—Transmitter Power Spectral Density for 5 Gb/s MAC data rate, upper and lower masks (TBD)

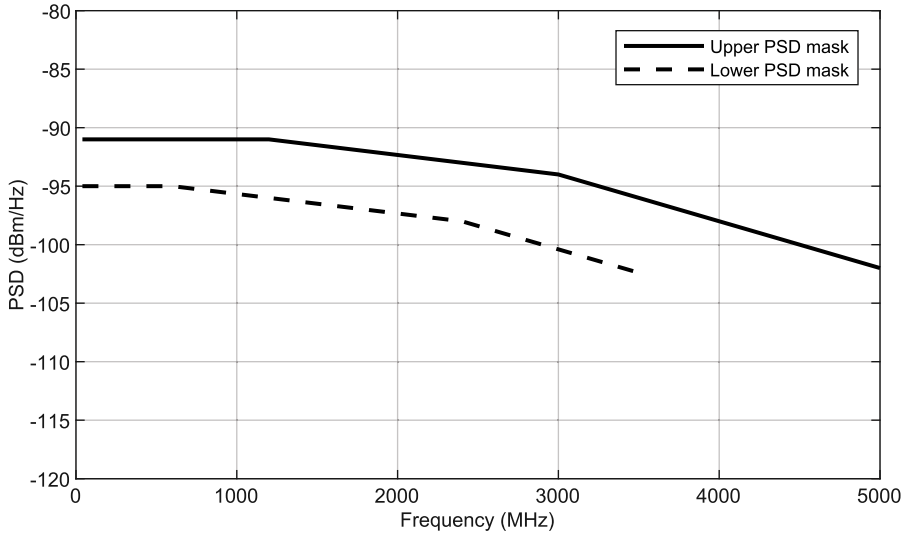


Figure 202–34—Transmitter Power Spectral Density for 10 Gb/s MAC data rate, upper and lower masks

For the power spectral density of -V1, with single ended termination of 50 Ω load and test fixture 3 (see Figure 202–31), both upper and lower PSD Masks are lower by 3 dB from Equation (202–21), Equation (202–22), Figure 202–32, Figure 202–33, and Figure 202–33.

202.5.2.5 Transmitter peak output

The transmit differential signal at the -T1 MDI should be less than the peak-to-peak values specified in Table 202–17 when measured with a 100 Ω termination. The transmit signal at the -V1 MDI should be less than the peak-to-peak values specified in Table 202–17 when measured with a 50 Ω termination. The limits in this clause apply to all transmitted symbol sequences, including SEND_N, SEND_TS, and SEND_TA.

Table 202–17—Transmitter peak-to-peak output

Transmit MAC data rate	-T1 MDI peak-to-peak output (V)	-V1 MDI peak-to-peak output (V)
100 Mb/s	1.3	0.65
2.5 Gb/s	1.3	0.65
5 Gb/s	1.5	0.75
10 Gb/s	1.7	0.85

202.5.2.6 Transmitter clock frequency

When using a local timing reference, the symbol transmission rate shall be within the range $6 \times S$ GBd ± 100 ppm with drift less than 1 ppm/sec).

When the FOLLOWER is using a recovered timing reference, the symbol transmission rate shall be within ± 10ppm of the recovered clock scaled by *S*.

202.5.3 Receiver electrical specifications

Editor's Note (to be removed prior to Working Group Ballot):

Coax signals are not differential at the MDI, so this clause may need to be reworded to include coax.

The PMA provides the Receive function specified in 202.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 202.7 or 202.8.

202.5.3.1 Receiver input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 202.5.2 and have passed through a link specified in 202.7 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion.

Single-ended signals received at the MDI that were transmitted from a remote transmitter within the specifications of 202.5.2 and have passed through a link specified in 202.8 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion.

This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

202.5.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver's tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 202–18. The minimum noise frequency is 10 MHz. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 202–35, with a link segment as defined in 202.7 for -T1 and shown in Figure 202–36, with a link segment as defined in 202.8 for -V1. The BER is expected to be less than 10^{-12}, and to satisfy this specification, the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

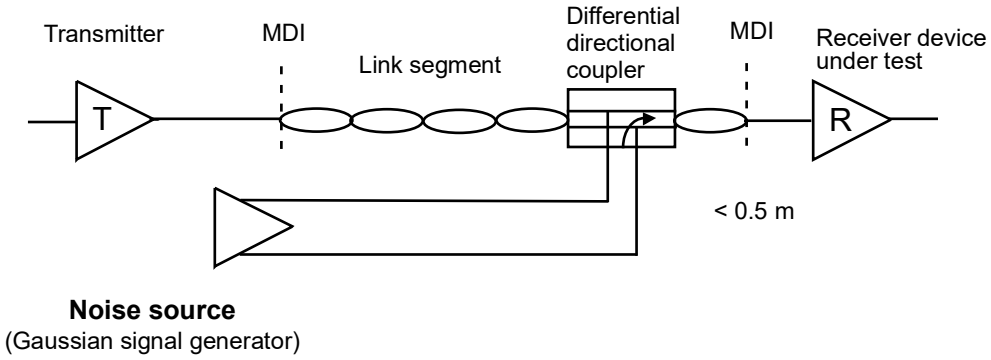


Figure 202–35—Broadband stationary noise rejection test setup, -T1

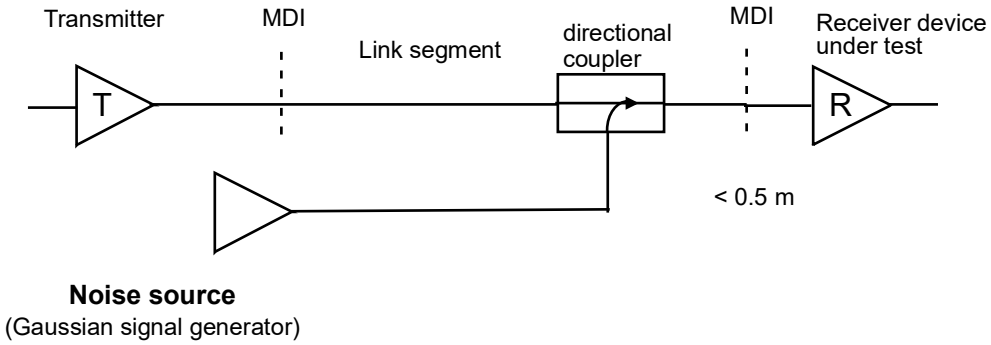


Figure 202–36—Broadband stationary noise rejection test setup, -V1

Table 202–18—Broadband stationary noise source, high speed

		Added noise at MDI (dBm/Hz)	
Transmit MAC data rate	**Noise bandwidth (MHz)**	**-T1**	**-V1**
2.5 Gb/s	1750	–140	-143
5 Gb/s	3500	–144	-147
10 Gb/s	3500	–148	-151

202.6 Management interface

MultiGBASE-A makes extensive use of the management functions that may be provided by the optional MDIO (see Clause 45).

202.7 Link segment characteristics, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. -T1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

202.7.1 Link transmission parameters

The transmission characteristics for a -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

202.7.1.1 Insertion loss

The insertion loss of a -T1 link segment shall meet the values determined using Equation (202–23).

$$\text{Insertion loss}(f) \le 0.322\sqrt{f} + 0.0019f + \frac{1}{\sqrt{f}} \quad \text{(dB)} \qquad (202–23)$$

where

f is the frequency in MHz; $10 \le f \le 5000$

Equation (202–23) is plotted in Figure 202–37, which is provided for information only.

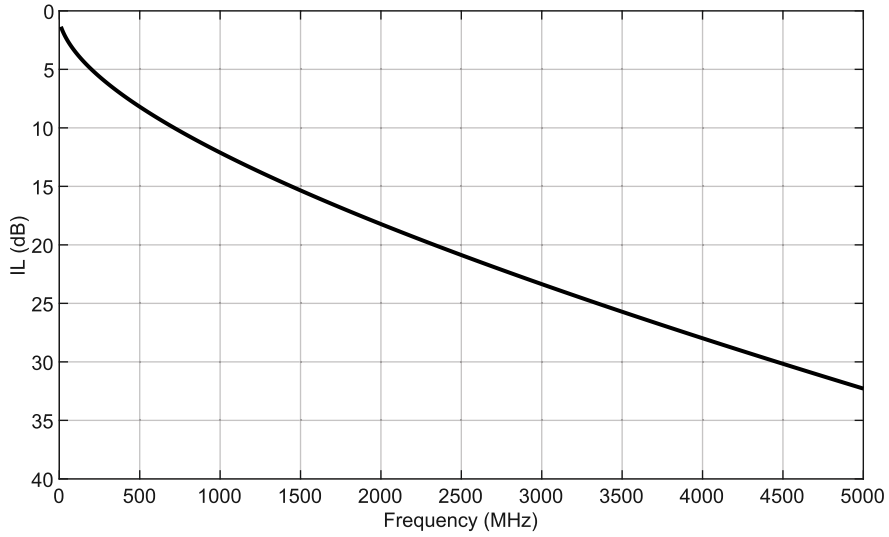


Figure 202–37—-T1 link segment insertion loss

202.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of a -T1 link segment is 100 Ω.

202.7.1.3 Return loss

The return loss of a -T1 link segment shall meet the values determined using Equation (202–24).

$$RL(f) \geq \begin{cases} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\langle\frac{f-500}{1500}\rangle & 500 \leq f < 2000 \\ 9.5 - 3\langle\frac{f-2000}{2500}\rangle & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{cases} \text{ (dB)} \qquad \text{(202–24)}$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–24) is plotted in Figure 202–38, which is provided for information only.

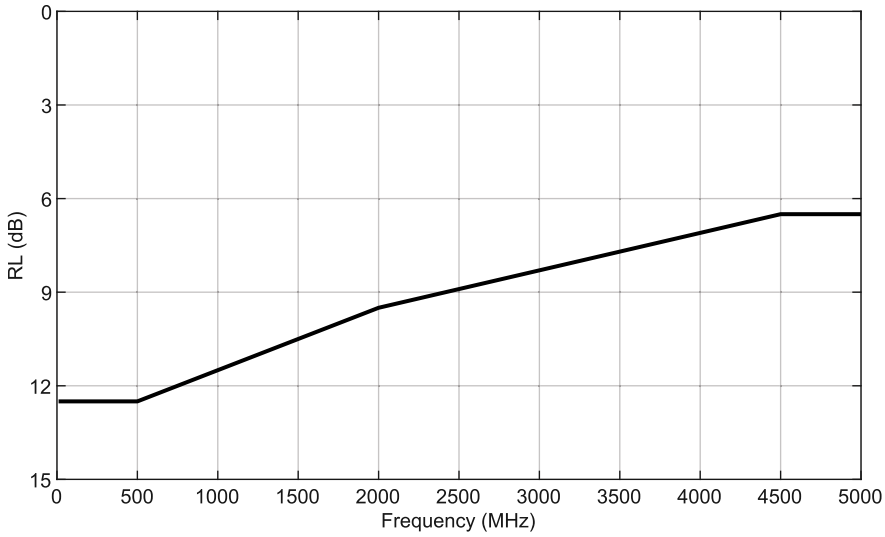


Figure 202–38—-T1 link segment return loss

202.7.1.4 Coupling attenuation

The coupling attenuation of a -T1 link segment shall be as specified in 149.7.1.4.

202.7.1.5 Screening attenuation

The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5.

202.7.1.6 Maximum link delay

The maximum link delay of a -T1 link segment shall be 160 ns.

202.7.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

202.7.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -T1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -T1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–32).

$$\mathrm{PSANEXT(f)} = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN(f)_j}}{10}} \ \mathrm{dB} \qquad (202\text{–}25)$$

where the function $\mathrm{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -T1 link segment j (1 to m) for the disturbed -T1 link segment.

The PSANEXT loss between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (202–33).

$$\mathrm{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad \text{(dB)} \qquad (202\text{–}26)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (202–33) is plotted in Figure 202–44, which is provided for information only.

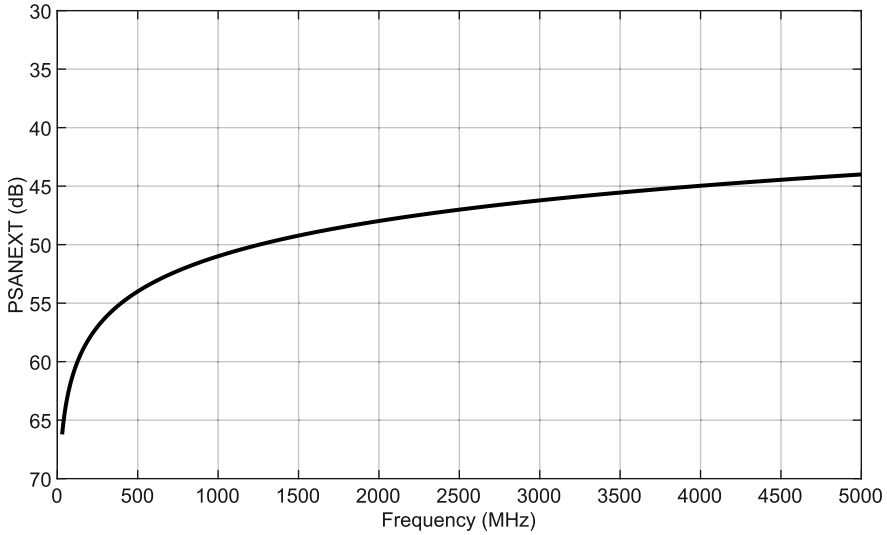


Figure 202–39—-T1 link segment PSANEXT loss

202.7.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -T1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -T1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–34).

$$\mathrm{PSAACRF(f)} = \left(-10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AFEXT(f)}_j}{10}}\right) - \mathrm{IL_d(f)} \quad \mathrm{dB} \qquad (202\text{–}27)$$

where

f	is the frequency in MHz; $30 \le f \le 5000$
$\mathrm{AFEXT}(f)_j$	is the magnitude of the alien FEXT loss at frequency f from a disturbing -T1 link segment j (1 to m) to the disturbed -T1 link segment in dB
$\mathrm{IL_d}(f)$	is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (202–35).

$$\text{PSAACRF}(f) \geq 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad \text{(dB)} \qquad (202\text{–}28)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (202–35) is plotted in Figure 202–45, which is provided for information only.

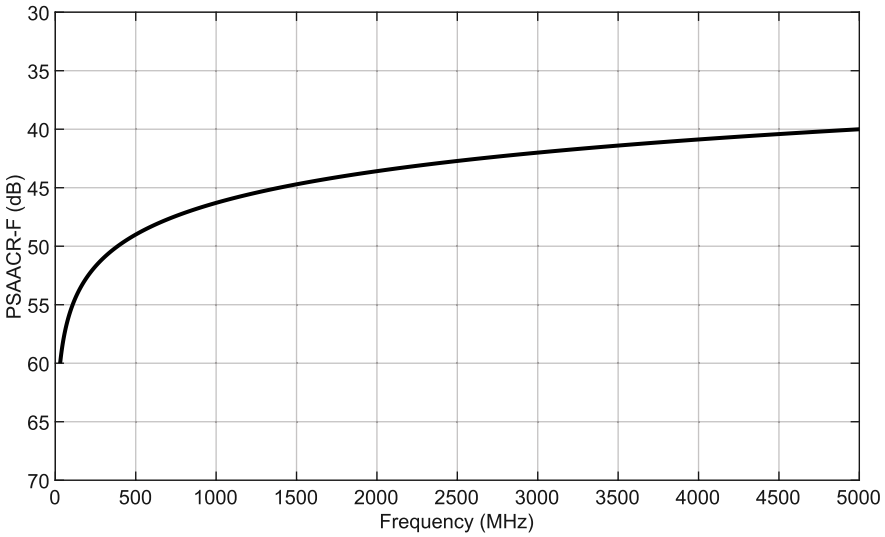


Figure 202–40—-T1 link segment PSAACRF

202.8 Link segment characteristics, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial cable (-V1) that meet the requirements specified in this subclause. -V1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

202.8.1 Link transmission parameters

The transmission characteristics for a -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

202.8.1.1 Insertion loss

The insertion loss of a -V1 link segment shall meet the values determined using Equation (202–29).

$$\text{Insertion loss}(f) \leq \ 0.3 + 0.345\sqrt{f} + 0.000825f + \frac{0.48}{\sqrt{f}} \quad \text{(dB)} \qquad \text{(202–29)}$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–29) is plotted in Figure 202–41, which is provided for information only.

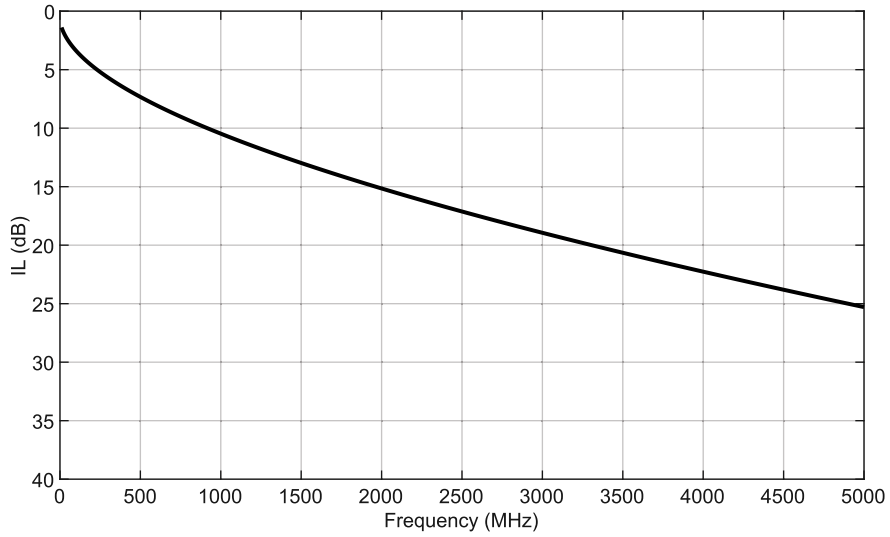


Figure 202–41—-V1 link segment insertion loss

202.8.1.2 Single ended characteristic impedance

The nominal characteristic impedance of a -V1 link segment is 50 Ω.

202.8.1.3 Return loss

The return loss of a -V1 link segment shall meet the values determined using Equation (202–30).

$$RL(f) \geq \begin{cases} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\langle\frac{f-500}{1500}\rangle & 500 \leq f < 2000 \\ 9.5 - 3\langle\frac{f-2000}{2500}\rangle & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{cases} \text{ (dB)} \qquad (202–30)$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–30) is plotted in Figure 202–42, which is provided for information only.

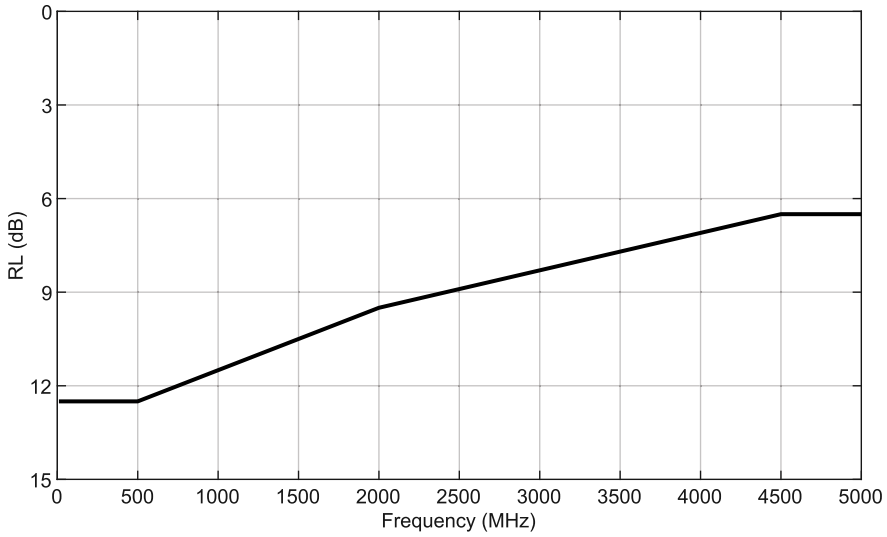


Figure 202–42—-V1 link segment return loss

202.8.1.4 Coupling attenuation

Coupling attenuation is not defined for -V1 link segments.

202.8.1.5 Screening attenuation

The screening attenuation of a -V1 link segment, measured in accordance with ISO 19642-11, shall meet the values determined using Equation (202–31). Additional screening attenuation test methodologies are defined in Annex 149A.

$$Screening\ attenuation(f) \geq \left\{ \begin{array}{ll} 64 & 10 \leq f < 3000 \\ 54 & 3000 \leq f \leq 5000 \end{array} \right\} \text{ (dB)} \qquad (202–31)$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (202–31) is plotted in Figure 202–43, which is provided for information only.

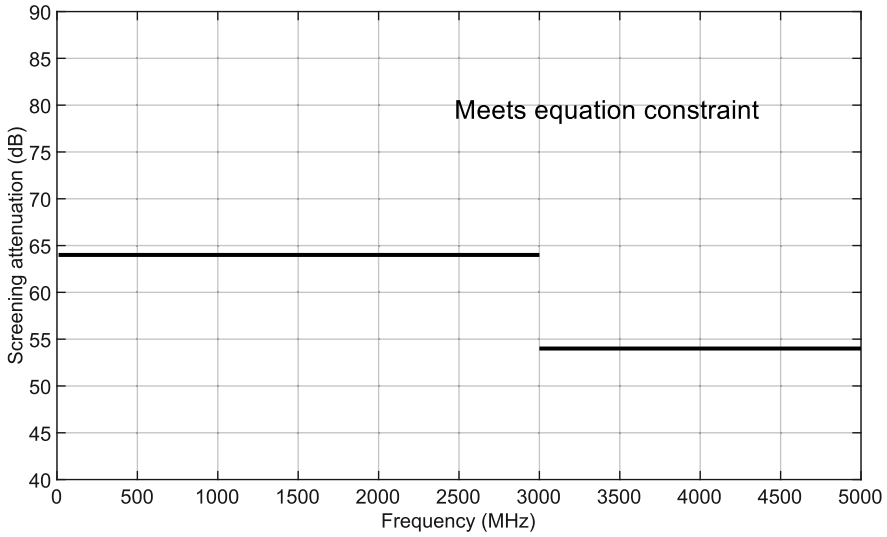


Figure 202–43—-V1 link segment screening attenuation

202.8.1.6 Maximum link delay

The maximum link delay of a -V1 link segment shall be 160 ns.

202.8.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

202.8.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -V1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -V1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–32).

$$\mathrm{PSANEXT(f)} = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN(f)_j}}{10}} \ \mathrm{dB} \qquad (202\text{–}32)$$

where the function AN(f)$_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -V1 link segment j (1 to m) for the disturbed -V1 link segment.

The PSANEXT loss between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (202–33).

$$\mathrm{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad \text{(dB)} \qquad (202\text{–}33)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (202–33) is plotted in Figure 202–44, which is provided for information only.

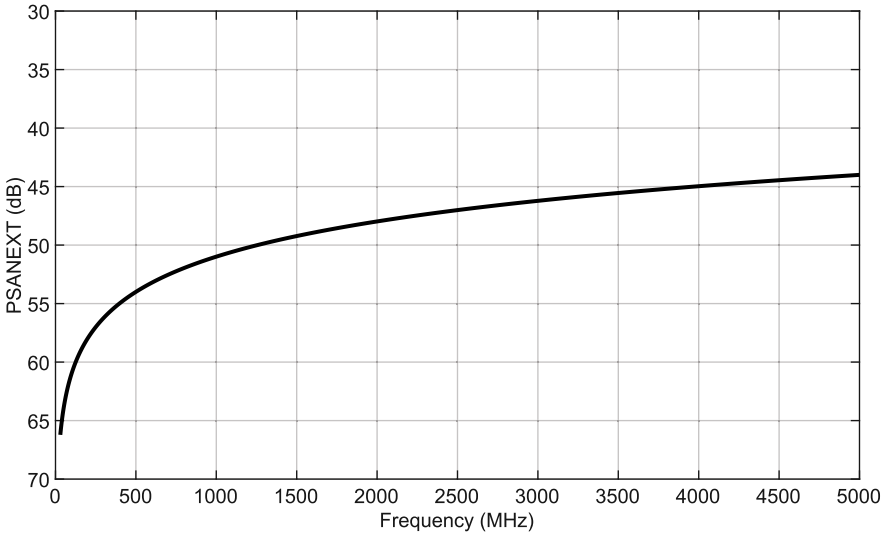


Figure 202–44—-V1 link segment PSANEXT loss

202.8.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -V1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -V1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (202–34).

$$\mathrm{PSAACRF(f)} = \left(-10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AFEXT(f)}_j}{10}}\right) - \mathrm{IL_d(f)} \quad \mathrm{dB} \qquad (202\text{–}34)$$

where

f is the frequency in MHz; $30 \le f \le 5000$

$\mathrm{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -V1 link segment j (1 to m) to the disturbed -V1 link segment in dB

$\mathrm{IL_d}(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (202–35).

$$\mathrm{PSAACRF}(f) \ge 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad \mathrm{(dB)} \qquad (202\text{–}35)$$

where

f is the frequency in MHz; $30 \le f \le 5000$

Equation (202–35) is plotted in Figure 202–45, which is provided for information only.

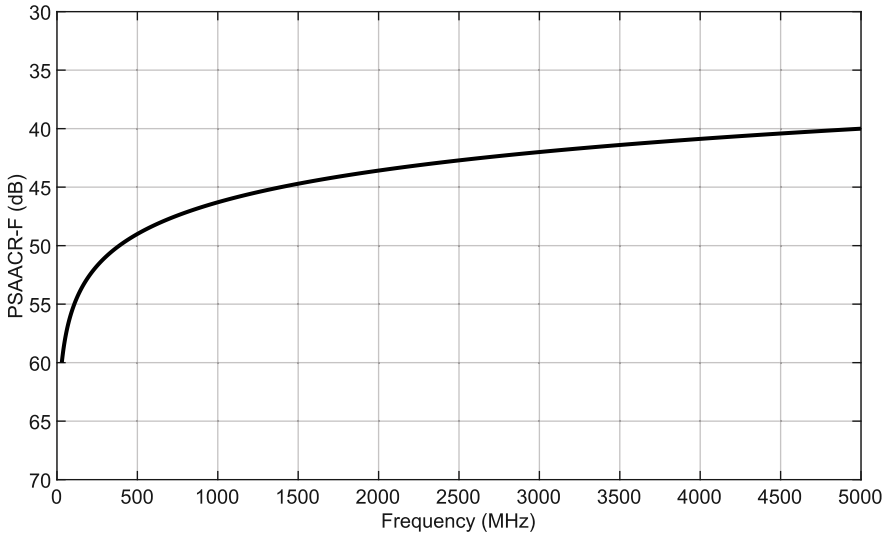


Figure 202–45—-V1 link segment PSAACRF

202.9 MDI specification, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

202.9.1 MDI connectors

The -T1 MDI connectors are as specified in 149.8.1.

202.9.2 MDI electrical specification

The electrical requirements specified in 202.5.2 and 202.5.3 shall be met when the PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors.

202.9.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -T1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (202–36). For the -T1 PMD, a nominal differential characteristic is impedance of 100 Ω is used.

$$MDI\_Return\_Loss(f) \geq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)} \qquad \text{(202–36)}$$

where

f is the frequency in MHz; $10 \leq f \leq Fmax$
$Fmax$ = TBD MHz for 100 Mb/s and 2.5 Gb/s data rate
= 4000 MHz for 5 Gb/s data rate
= 4000 MHz for 10 Gb/s data rate

Equation (202–36) is plotted in Figure 202–46, which is provided for information only.

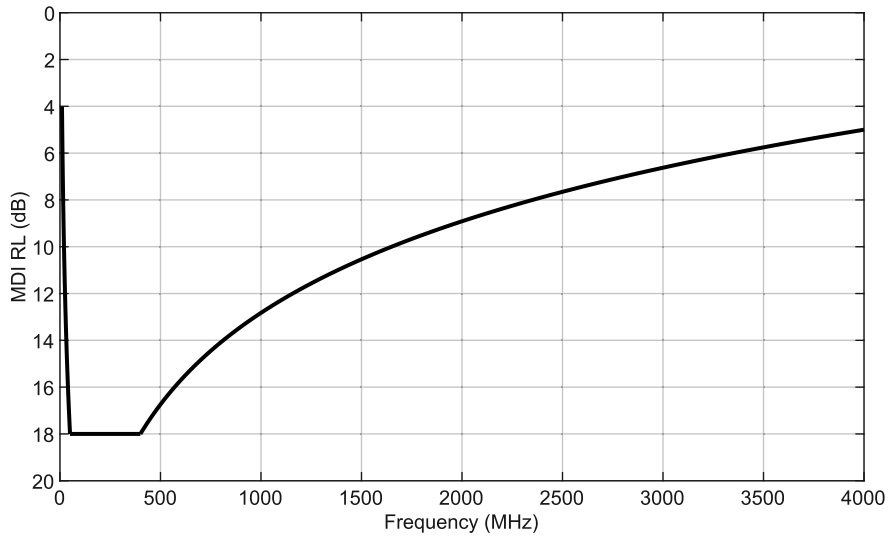


Figure 202–46—-T1 MDI return loss using Equation (202–36)

202.9.3 MDI fault tolerance

The -T1 MDI fault tolerance shall comply with 96.8.3.

202.10 MDI specification, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial MDI (-V1) that meets the requirements specified in this subclause.

202.10.1 MDI connectors

The -V1 mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the -V1 mechanical interface is beyond the scope of this standard.

202.10.2 MDI electrical specifications

The electrical requirements specified in 202.5.2 and 202.5.3 shall be met when the PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable.

202.10.2.1 MDI return loss

The differential impedance at the -V1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -V1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (202–37). For the -V1 PMD, a nominal differential characteristic is impedance of 50 Ω is used.

$$MDI\_Return\_Loss(f) \geq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)} \qquad (202\text{–}37)$$

where

f is the frequency in MHz; $10 \leq f \leq Fmax$
$Fmax$ = TBD MHz for 100 Mb/s and 2.5 Gb/s data rate
= 4000 MHz for 5 Gb/s data rate
= 4000 MHz for 10 Gb/s data rate

Equation (202–37) is plotted in Figure 202–47, which is provided for information only.

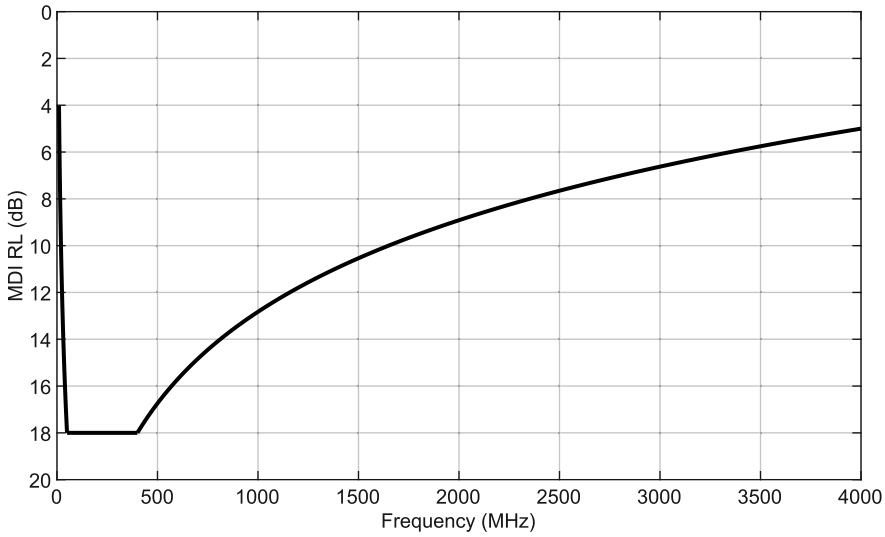


Figure 202–47—-V1 MDI return loss using Equation (202–37)

202.10.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 202–19, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

Table 202–19—Connection fault

Center conductor	Shield
No fault	Ground
MDI +	Ground
Ground	Ground
+50 V dc	Ground

202.11 Environmental specifications

202.11.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

202.11.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

202.11.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750–1
b) Electrical loads: ISO 16750–2, ISO 7637–2:2008, and ISO 8820–1
c) Mechanical loads: ISO 16750–3, ASTM D4728, and ISO 12103–1
d) Climatic loads: ISO 16750–4, IEC 60068–2–1, IEC 60068–2–27, IEC 60068–2–30, IEC 60068–2–38, IEC 60068–2–52, IEC 60068–2–64, and IEC 60068–2–78
e) Chemical loads: ISO 16750–5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

202.11.3 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21
b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21
c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3
d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

202.12 Delay constraints

Editor's Note (to be removed prior to Working Group Ballot):

Exceptions and modifications TBD.

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 202–20. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

Table 202–20—Delay Limits

Transmit MAC data rate	Bit times	Pause Quanta	Delay (ns)
100 Mb/s	1536	3	15 360
2.5 Gb/s	10 240	20	4096
5 Gb/s	13 824	27	2764.8
10 Gb/s	20 480	40	2048

202.13 Protocol implementation conformance statement (PICS) proforma for Clause 202, TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1[6]

202.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 202, TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

202.13.2 Identification

202.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

202.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3xx-202x, Clause 202, TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

[6]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

202.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] No [ ]
					Yes [ ]

202.13.4 PICS proforma tables for TDD proposal, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

202.13.4.1 PMD functional specifications

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ]
					Yes [ ] No [ ]
					Yes [ ] No [ ] N/A [ ]

202.13.4.2 Management functions

Item	Feature	Subclause	Value/Comment	Status	Support
					Yes [ ] N/A [ ]
					Yes [ ] No [ ] N/A [ ]

Annex 98B

(normative)

IEEE 802.3 Selector Base Page definition

98B.3 Technology Ability Field bit assignments

Change the reserved row for bits "A11 through A20" (as modified by IEEE Std 802.3dg-202x) and insert new rows before this row in Table 98B-1b as follows (unchanged rows not shown)

Replace Table 98B-1 as follows:

Table 98B–1b—Category-specific technology bit assignments for NULL category

bit	Selector description
…	
A11	100M+2.5GBASE-T1/V1 ability
A12	2.5G+100MBASE-T1/V1 ability
A13	100M+5GBASE-T1/V1 ability
A14	5G+100MBASE-T1/V1 ability
A15	100M+10GBASE-T1/V1 ability
A16	10G+100MBASE-T1/V1 ability
A17~~11~~ through A20	Reserved
…	

98B.4 Priority Resolution

Replace the 2nd sentence in the 1st paragraph of 98B.4 (as modified by IEEE Std 802.3dg-202x) as follows:

Table 98B–2 shall indicate the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value. The lowest numbered capability is the resolved ability.

Replace the dashed list in 98B.4 with the following table:

Table 98B–2—Priority Resolution[a]

		Link Partner																							
		25GBASE-T1	10GBASE-T1	100M+10GBASE-T1/V1(L)	100M+10GBASE-T1/V1(F)	10G+100MBASE-T1/V1(L)	10G+100MBASE-T1/V1(F)	5GBASE-T1	100M+5GBASE-T1/V1(L)	100M+5GBASE-T1/V1(F)	5G+100MBASE-T1/V1(L)	5G+100MBASE-T1/V1(F)	2.5GBASE-T1	100M+2.5GBASE-T1/V1(L)	100M+2.5GBASE-T1/V1(F)	2.5G+100MBASE-T1/V1(L)	2.5G+100MBASE-T1/V1(F)	1000BASE-T1	100BASE-T1L increased tx/rx	100BASE-T1L standard tx/rx	100BASE-T1	10BASE-T1S full duplex	10BASE-T1S half duplex	10BASE-T1L
PHY	25GBASE-T1	1																							
	10GBASE-T1		2																						
	100M+10GBASE-T1/V1(L)						3																		
	100M+10GBASE-T1/V1(F)					4																			
	10G+100MBASE-T1/V1(L)				4																				
	10G+100MBASE-T1/V1(F)			3																					
	5GBASE-T1							5																	
	100M+5GBASE-T1/V1(L)											6													
	100M+5GBASE-T1/V1(F)										7														
	5G+100MBASE-T1/V1(L)									7															
	5G+100MBASE-T1/V1(F)								6																
	2.5GBASE-T1												8												
	100M+2.5GBASE-T1/V1(L)																9								
	100M+2.5GBASE-T1/V1(F)															10									
	2.5G+100MBASE-T1/V1(L)														10										
	2.5G+100MBASE-T1/V1(F)													9											
	1000BASE-T1																	11							
	100BASE-T1L increased tx/rx																		12						
	100BASE-T1L standard tx/rx																			13					
	100BASE-T1																				14				
	10BASE-T1S full duplex																					15			
	10BASE-T1S half duplex																						16		
	10BASE-T1L																								17

[a] NOTE—"L" stands for "Leader" and "F" stands for "Follower"

Annex 201A

(informative)

Allocation of Delay Limit Budget

In 201.14, the Delay Limits are set for the HS_PATH and LS_PATH, not including the delays introduced by the physical medium interconnecting the two PHYs. In asymmetrical operation, the delay limits between the HS_PATH and LS_PATH are quite different.

To increase the chance of interoperability between different implementations it is recommended the transmit and receive portions of the PHY delay limits in 201.14 be allocated as follows:

a) The HS_TX TX_Delay is allocated 10% of the delay budget.
b) The HS_RX RX_Delay is allocated 90% of the delay budget.
c) The LS_TX TX_Delay is allocated 25% of the delay budget.
d) The LS_RX RX_Delay is allocated 75% of the delay budget.

In Figure 201A–1, XGMII transfers are shown as X(#) where # is sequentially incrementing. Let the first 64B/65B block of a RS-FEC frame or superframe contain the X(*n*) and X(*n*+1) XGMII transfers. To insure a consistent methodology on measuring the delays is used by all implementations, the following points in the data stream are used.

The TX_Delay is measured from the start of the X(*n*) transfer on the TX XGMII to the start of the first symbol of the frame or superframe at the MDI.

The RX_Delay is measured from the start of the first symbol of the frame or superframe at the MDI to the start of the X(*n*) transfer on the RX XGMII.

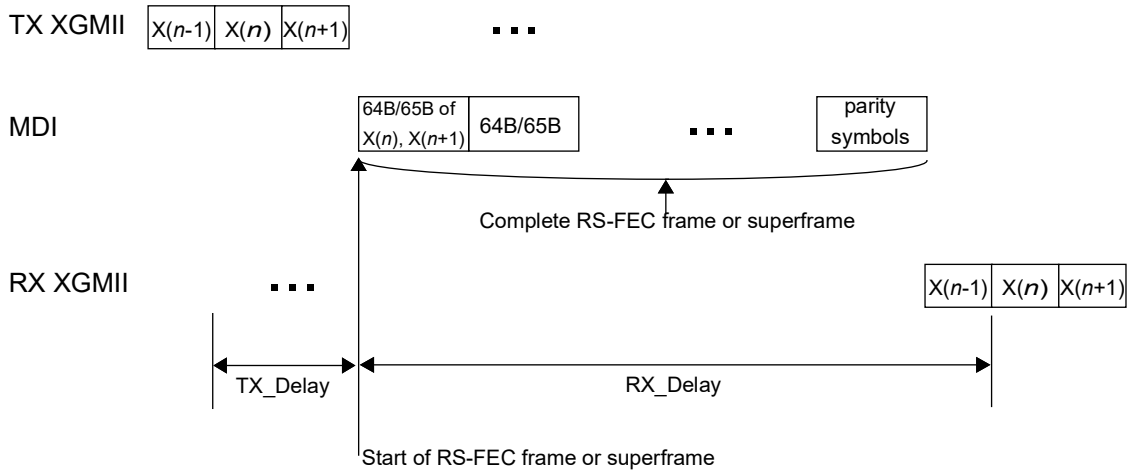


Figure 201A–1—XGMII to MDI to XGMII timing diagram

Since the start of the first symbol of the frame or superframe may not be measurable directly on the MDI, it is recommended that the PHY implementors specify TX_Delay and RX_Delay in the product documentation.