Evolution of 802.3dm: From GMSLE to ACT and Beyond

Contribution to 802.3dm Task Force

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Relative Complexity Analysis, Camera PHY Revisited

	ACT+GMSLE	TDD
Camera Downstream highspeed TX Complexity	**Least complex** **Low PAPR (NRZ)** ▪ **2.5Gbps, 5Gbps NRZ**	More complex ▪ TDD > 1.5% Digital
Camera Upstream lowspeed RX Complexity	▪ Less Complex	Much more complex ▪ TDD ▪ Equalization } >250% Analog ▪ LMS ▪ FEC } > 24.5% Digital
Camera Power Consumption	▪ **Lowest**	In same geometry, higher power consumption Higher
Camera LS RX FEC	n=50, k=46, m=6, t=2	n=130, k=122, m=8, t=4
Camera LS RX FEC decoder area complexity^	1.0x Least Complex^	**3.75x** Much more complex^ With 1/5 the burst protection
Upstream burst protection	51.2ns	10.6ns much less than GMSLE
Crystal-less Camera Serializer	Simple. GMSL in mass production	Possible, but more complex
Upstream latency (including FEC)	~8µs	~9.6µs (est., based on TDD presentation)
Summary	Lowest Complexity for 3MP 2.5Gbps and 8Mp 5Gbps cameras	Highest complexity. Raises cost, power for 3MP 2.5Gbps and 8MP 5Gbps cameras. XTAL-less more complex. Lower burst protection margin with > 2x the complexity

^equivalent area of num 2 input NAND gates + 2-port memory in same geometry ^^(floor((n-k)/2)*m)/Baud

Relative Complexity Analysis, HS RX, LS TX PHY

	ACT+GMSLE	TDD
POC – (Power over Coax)	Single inductor	Single inductor
Downstream HS Receiver Complexity	▪ NRZ for 2.5Gbps and 5Gbps modes ▪ Analog or Digital EQ OK	More complex ▪ TDD
Downstream HS FEC	n=360,k=326, m=10, t=17	n=130,k=122, m=8, t=4
Downstream HS RX FEC Correctable burst length ^^	60.4ns (L=1,2,4 in 2.5/5/10Gbps)	10.6ns (L=1,2,4) Significantly less burst protection
Downstream HS RX FEC Decoder Area Complexity^	2.4x^ High speed RX in smaller process than US RX	1x^
Downstream Latency (including FEC)	2.048µs^^^	Claimed 1µs from TDD presentation
Downstream Summary	Analog or digital EQ OK	High Complexity, TDD Lower burst noise protection
Extensible to higher speeds?	Yes	TDD overhead major consideration at 25Gbps

^equivalent 2 input NAND gates area + two port memory area in same geometry. 750MHz clock in all designs
^^^ from 802.3 clause 149 table 149-20

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	TDD – Proposal #1	TDD – Proposal #2	ASA 2.0 (MLE)	ASA 2.1 (MLE)
Released	Nov 2024	Jan 2025	May 2024	Feb 2025
Baud Rate	3.125Gsps/6.25Gsps	3.0Gsps/6.0Gsps	SG1- SG5 2/4/6/8Gsps	SG1- SG5 2/4/6/8Gsps
Cycle timing and Encoding	Fixed – 8.96usec – 896ns 64b65 and 80b/81b	Fixed – 9.6usec – 933ns 64b65b	2.5us – 26.832us (SG driven) 64b65b	2.5us – 26.832us (SG driven) 64b65b
FEC	8bit – RS – 3 FEC types 9bit – RS – 3 FEC types	1 FEC for all speeds 8bit – RS – 130,122	240,214	240,214
Link Start up procedure	Fixed time slot w/ predefined burst	Fixed time slot w/ predefined burst	Multi-phase dynamic training with OAM message exchanges and PTB clock alignment	Multi-phase dynamic training with OAM message exchanges and PTB clock alignment
Burst Timing & Switch Logic	Fixed – PTB?	Fixed – PTB?	Deterministic – PTB based 6844 – PTB tics Fixed Quiet gap Anchored to StartTDD	More robust startup Variable w/ (628-6708) PTB tics Refined for shorter Upstream Same – better startup phases
OAM	Not Defined	Not Defined	Occurs during startup and dynamical for updates	Occurs during startup and dynamical for updates
Clock Leader and PTB	Not Defined	Not Defined	Foundation for synchronization and timing accuracy	Foundation for synchronization and timing accuracy
ASEP	Needs DLL extensions, config. space, and stream sync procedures	Needs DLL extensions, config. space, and stream sync procedures	Supports	Supports

Relation of ASA with 802.3dm TDD proposal

- The current TDD baseline Chini_3dm_01a_0125.pdf is different from ASA 2.0/2.1
- The following is different:
  - **OAM protocol** (Clause 5.5)
    - Used for fault management, link configuration, power mode control, and enumeration
      - ASA uses Clause 5.5 which defines a block message for - DelayRequest, Write, ReadError, StartEum, etc.
      - This is essential for – Remote diagnostics, Wake/sleep transition, Field configurability (reconfigure streams dynamically), trigger recovery events (soft reset, downgrade modes)
  - **Training states** – Clause 4.2.7 ASA Link Training Phases this clause defines four-phase training state machine:
    - Phase 1G – Basic OAM frame exchange – confirms physical connectivity
    - Phase SGA – Short bursts, initial FEC and PTB sync attempt
    - Phase SGB – Medium bursts – improved PTB sync and diagnostics
    - Phase SGC – Full-rate data bursts with validated PTB, FEC, and stream alignment
    - Important: During training phase OAM messages are embedded in bursts and interpreted as part of the link FSM – not separate protocols.

Relation of ASA with 802.3dm TDD proposal (continued)

- **PTB (Precision Time Base)** used for time synchronization framework – Clause 4.2.8
  - TDD proposal is using a fixed slot burst scheduling – no timing message exchange – no delay request/reply mechanism, no timestamp propagation
  - TDD proposal – Assumes a pre-aligned w/o PTB incorporated
- **Diagnostics** – ASA has implemented a robust diagnostic stack using OAM-based status reporting
  - LinkQuality, ExtendedLinkTrainingStatus, SQI, MSE, FECstat, real time link margin, State-base fault recovery, soft reset, and degraded mode fallback – (Clause 3.2.x and 4.2.4-4.2.5)
  - No details are mentioned – on if this will be included
- **ASEP (Application Stream Encapsulation Protocol)**
  - Clause 3.5 is used for RAW video, I2C, GPIO signaling, and latency guarantees
  - Is this apart of the 802.3 proposal for ethernet framing?
- How this interops with **deployed ASA silicon** and deployed ASA infrastructure.

Relation of ASA with 802.3dm TDD proposal Conclusion

- How can you add all these features to Chini_3dm_01a_0125.pdf ?
  - How does the training and alignment with a TDD PHY work without startup state machines, PTB, or dynamic negotiation?
- ASA PHYs assume:
  - Every PHY must go through controlled start up phases, OAM negotiation, clock sync (PTB), and link testing before data moves
- Key differences
  - TDD 802.3dm = timing driven
  - ASA = protocol driven