Impact of High Pass Filtering on ACT Testmode 4 SNDR measurements

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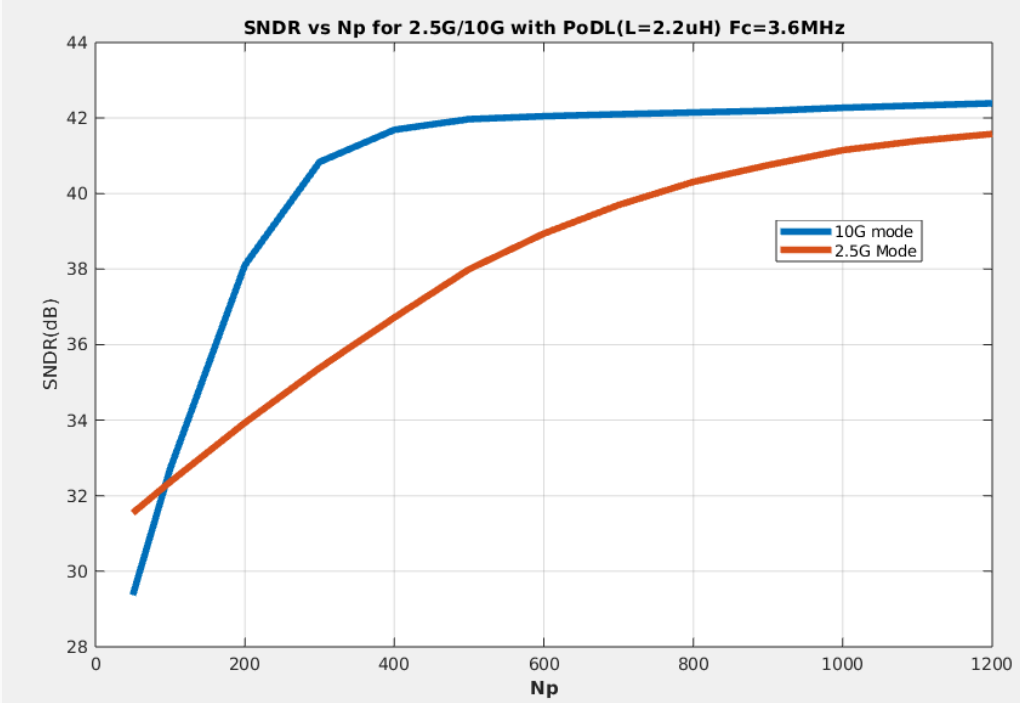
How TM4 SNDR is measured (802.3ch / 802.3dm)

1. DUT PHY transmits a known **PRBS13Q** pattern
2. Scope captures the **MDI waveform** and computes a **linear-fit pulse response**; peak `Pmax` = linear, distortion-free signal within an `Np`-long window
3. **Nonlinearity power** `σe²` = residual between captured MDI and linear-fit reconstruction
4. **Random-noise power** `σn²` = variance across repeated captures of the same pattern
5. **SNDR** = `10·log10( Pmax² / (σe² + σn²) )` — higher is better

- The window `Np` bounds how long an impulse response the linear fit can model
- **Anything longer than `Np` lands in the residual** — it cannot be captured
- Higher `Np` is used to compensate refelction



SNDR vs `Np` — Higher Np compensates for BLW

What PoDL/PoC adds to the channel

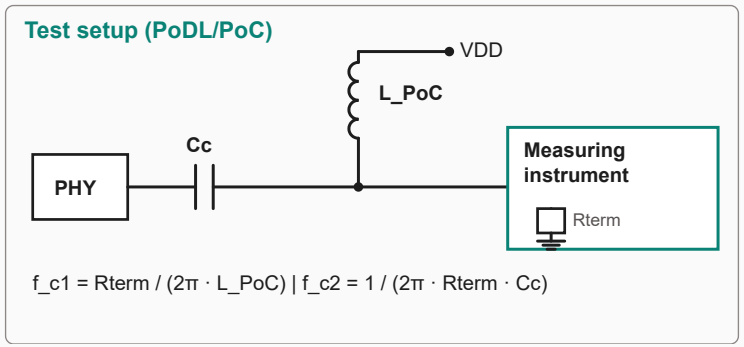
PoDL/PoC feeds DC supply onto the same conductors as the signal. The test signal path is:

- Series **AC coupling cap** `Cc` — blocks DC from the PHY
- Shunt **PoC inductor** `L_PoC` to VDD — passes DC supply, blocks AC

This network is a **low-frequency high-pass** with two real poles:

- `f_c1 = Rterm / (2π · L_PoC)` ← inductor + termination
- `f_c2 = 1 / (2π · Rterm · Cc)` ← coupling cap + termination

PRBS13Q still excites significant LF content ⇒ shaped by this HPF ⇒ **baseline wander (BLW)**



PoDL/PoC network and its high-pass response

Why the standard method inaccurately estimates the SNDR

- BLW time constants are **orders of magnitude longer than a UI** and typically **exceed** `Np`
- The linear fit **cannot capture the slow baseline** — it falls outside the window
- That energy lands in the **residual** ⇒ counted as **nonlinearity** (`σe²`)
- The repeat-variance step **misclassifies** slowly varying BLW as **random noise** (`σn²`), because the baseline is not stationary across pattern repetitions

Net effect: the SNDR estimator interprets a **linear, deterministic, network-induced** artifact as both distortion and noise — and reports a depressed number for a perfectly compliant device.

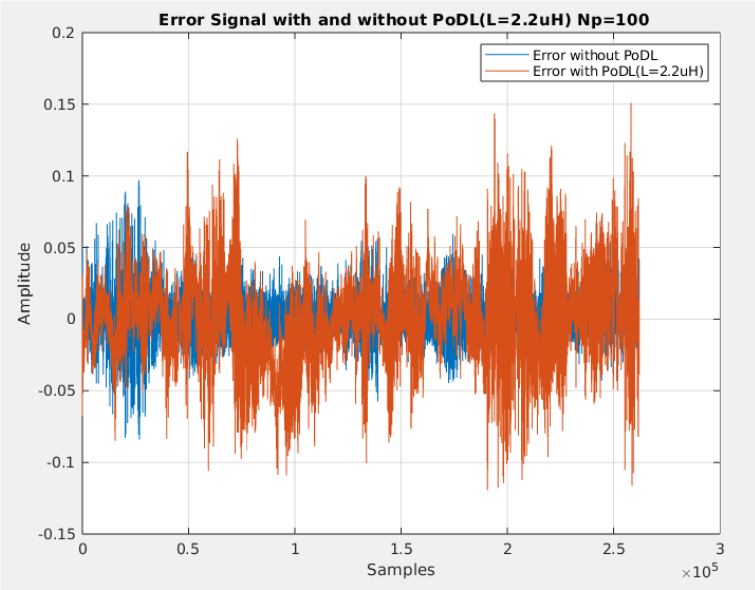
Measured evidence (TM4, 10G)

Configuration	SNDR
Without PoDL (reference)	**40.9 dB**
With PoDL (uncompensated)	32.8 dB

- **~8 dB drop** contributed entirely by passive, linear components
- Inductors and capacitors do not generate distortion or noise
- Yet the test attributes the deficit to the PHY

The error-signal trace tells the story:

- **Without PoDL**: residual `e[n]` is white-like, no slow trend
- **With PoDL**: residual carries a clear **LF tail** that tracks pattern run-length — signature of a 2nd-order high-pass step response



Error signal (10G, `Np = 100`) — without PoDL (top) vs. with PoDL (bottom)

Why this matters

- **False failures on compliant silicon**: PoDL/PoC baseline wander alone can push a fully compliant transmitter below the SNDR limit, even though the PHY itself meets the spec
- **Result depends on the fixture, not the DUT**: the same PHY can swing several dB simply by inserting or bypassing the PoDL/PoC network — making cross-lab and cross-fixture comparisons unreliable

Bottom line — today' TM4 SNDR procedure does not separate **PHY performance** from **fixture response** when PoDL/PoC is present, so it **miscalculates the true SNDR** of the device under test.