# PCS Function Verification Using Deterministic Test Modes

Extending the Test Mode 3 principle to other PCS functions

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# Motivation: Test Mode 3 Shows a Useful Pattern

### Not a normal link test

Test Mode 3 applies to the high-speed data path and checks a PCS function through the PMA electrical test interface.

### Why it is valuable

It isolates the fault to one side of the link, does not require link-partner cooperation, and produces a deterministic waveform.

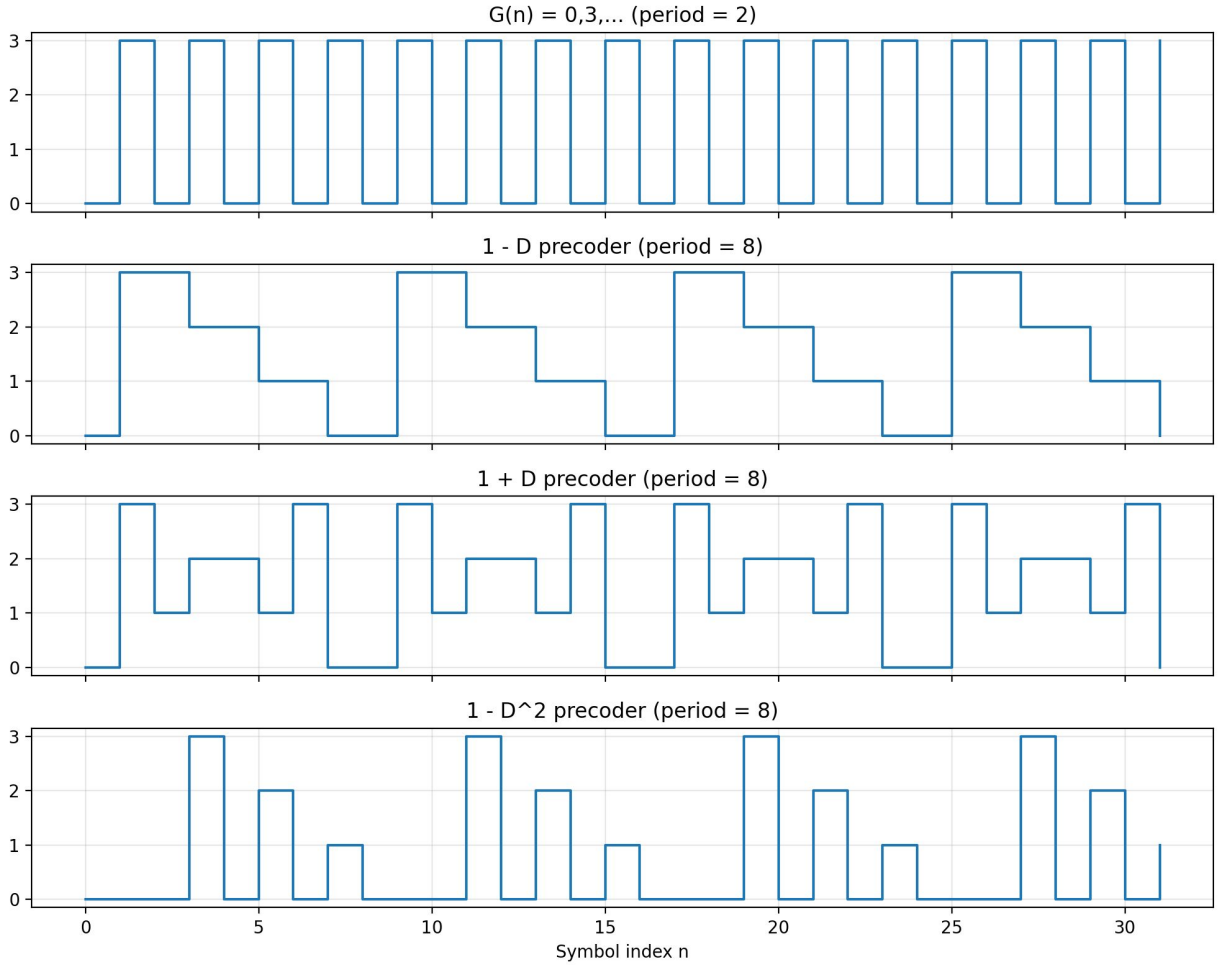
## Main idea

- Use simple, deterministic PCS input patterns.
- Define the expected output or internal encoder input clearly.
- Make the result easy to verify with a scope or a simple pattern checker.
- Apply the same principle beyond the precoder/decoder path.

**Test Mode 3 is the example; the principle can be extended to interleaver and RS-FEC verification.**

# Test Mode 3: Precoder/Decoder Verification

Deterministic stimulus → deterministic electrical waveform




**Verification value**

Recognizable waveform; no full BER setup required.

# Interleaver Verification

## Test setup

- Input pattern: repeating {0, 1, 2, 3} with period 4 for 10G, and {1,3} with period of 2 for 5G
- Full superframe: 326 × L message symbols.
- Expected encoder input depends on L.

## Expected encoder inputs

- For 10G
  - L = 1: one encoder sees {0,1,2,3,…}.
  - L = 2: Enc#1 sees {1,3,…}; Enc#2 sees {0,2,…}.
  - L = 4: each encoder sees one constant value
- For 5G
  - L = 1: one encoder sees {1,3}
  - L = 2: each encoder sees one constant value

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istributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message ymbols from the superframe; otherwise, the RS-FEC encoder operates exactly the same as specified in 49.3.2.2.17.

**49.3.2.2.16 RS-FEC recombine**

he L encoded RS-FEC frames are recombined into an interleaved RS-FEC superframe. The output ymbols are as follows:

$m_{326 \times L-1}, m_{326 \times L-2}, \ldots, m_1, m_0, p_{1,33}, \ldots, p_{L,33}, \ldots, p_{1,0}, \ldots, p_{L,0}$, where $p_{i,r}$ is the $r^{th}$ parity symbol of the $i^{th}$ encoder.

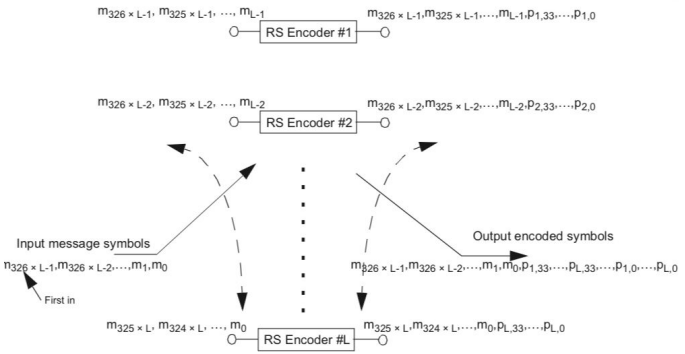


**Figure 149–9—Interleaving block diagram with interleaving depth L**

### Pass/fail concept

Pass when each RS-FEC encoder receives the predicted symbol stream for the selected L value.

# Conclusion: Extend the Test Mode 3 Approach

## Proposed principle

- Start from a simple, deterministic PCS input.
- Choose a pattern that creates a unique and predictable output.
- Make the expected result observable at the electrical interface or at a clearly defined PCS boundary.
- Use the result to isolate implementation issues without requiring link-partner cooperation.

## Candidate extensions

### Interleaver

Repeating {0,1,2,3} produces predictable encoder-input streams for L = 1, 2, and 4.

### RS-FEC encoder

Use an all-zero message frame with one known non-zero symbol at a specified position, then check the parity response.

### Future PCS tests

Define additional low-complexity patterns for functions where deterministic observability improves debug and compliance confidence.

## Requested group feedback

- Which PCS functions are most valuable to cover?
- Where should the expected observation point be defined?
- Should these tests be added as dedicated test modes or as informative verification guidance?