# ACT and TDD Comparison

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Contribution to 802.3dm Task Force
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# Introduction

This is a contribution to address the comparisons done by TJ Houck and Jay Cordaro in the May interim and July plenary.

**Objective #1**: Summarize presentations that have been given thus far and major areas of difference between TDD and ACT that impact relative cost and future system development

**Objective #2**: Group past presentations into appropriate section and provide information on each topic of importance

Previous Comparison Presentations by TJ Houck and Jay Cordaro:
May interim
Comparative_Analysis

July Interim
ACT and TDD Comparison

# Supporters

- Abdelkadar Hessainia, Ampere
- Amrit Gopal, Ford
- Dongok Kim, Hyundai
- Gumersindo Cauce Veloso, BMW
- Hideki Goto, Toyota
- Hoai Hoang Bengtsson, Volvo Cars
- Jianyong Pei, LiAUTO
- Jiwu Yang, Nio
- John Leslie, JLR
- Jose Villanueva, Ampere
- Jun Sun, Geely/Zeekr
- Kirsten Matheus, BMW
- LingWu Zeng, BYD
- Mohandas Laourou, Stellantis
- Nicolas Morand, Stellantis
- Qin Shuai, BYD
- Sami Akin, CARIAD
- Tony Schedl, BMW
- Yonggang Zhu, Xpeng
- Christoph Arndt, Aumovio (Conti)
- Daniel Hopf, Aumovio (Conti)
- Marc Schreiner, ZF
- Masayuki Hoshino, Aumovio (Conti)
- Stefan Brunner, Harman
- Yasuhiro Kotani, DENSO

# Supporters (Cont'd)

- Ahmad Chini, Broadcom
- Charles Wu, Omnivision
- Ching-Yen Lee, Realtek
- Christian Martens, Fraunhofer
- Conrad Zerna, Aviva Links
- Debajyoti Pal, Onsemi
- Korhan Tanc, NXP
- Jorg Kock, NXP
- Mehmet Tazebay, Broadcom
- Murugavel Ganesan, SiliconAuto
- Neven Pischl, Broadcom
- Piergiorgio Beruto, Onsemi
- Prasad Chalasani, AnalogPort
- Scott Muma, Microchip
- Shivesh Dubey, NXP
- Stan He, JLSemi
- Ramanjit Ahuja, Onsemi
- Tiaq Ng, Aviva Links
- YJ Won, Microchip

# Supporters (Cont’d)

- Bert Bergner, TE Connectivity
- David Bollati, C&S
- Jae-Yong Chan, Keysight
- Junichi Takeuchi, JAE Connectors
- Johannes Nachtrab, Leoni
- Jonathan Silvano de Sousa, GG Group
- Mathias Kleinwaechter, In-tech
- Stefan Gianordoli, GG Group
- Sven Bergdolt, Leoni
- Thomas Stueber, Teledyne LeCroy

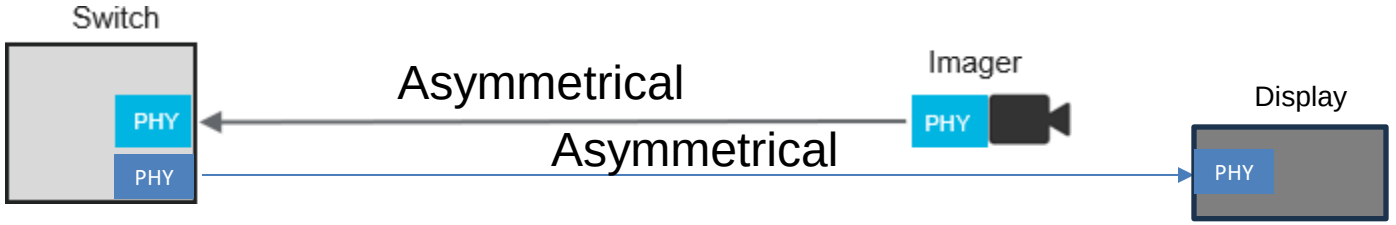
# Comparison Table

| | TDD – Proposal | ACT – Proposal |
|---|---|---|
| **Number of discreet ICs to provide complete set of Ser and DeSer combinations** | **Smallest number of implementations**<br>**Lowest development costs**<br>**Easy change of HS direction**<br>matheus_dm_01e_comparison_20250727.pdf | **Very high number of implementations**<br>(as evidenced by proprietary SerDes) |
| **Imager and Switch Integration** | **TDD is supported by imager vendors**<br>Switch side needs **Reversible** Asymmetrical PHYs | **No evidence** of ACT support **by imager vendors**<br>**Much more complex** to **reverse** high-speed direction<br>matheus_dm_01e_comparison_20250727.pdf |
| **Interoperability** | PHY vendors can **leverage ASA-ML**<br>(interop between 5 vendors) | **Interop** between ACT and 802.3ch **is not possible**<br>Autoneg, Link Sync, Modulation, FEC are different (see slide 14) |
| **PHY-level Sync** | **Low complexity** sensor **sync** without engaging higher protocols<br>**Higher precision**<br>see slide 19 | **High complexity sync** – requires higher layer protocols<br>**Lower precision**<br>see slide 19 |
| **Power, Performance, Area (PPA)** | **Optimum for Ser and DeSer. Better SNR.**<br>Dalmia_3dm_01_03102025.pdf \| Chini_3dm_02b_0325.pdf \| Chini_3dm_02a_0525.pdf Chini_3dm_02_07272025.pdf | **DeSerializer** side is **complicated. Performance: Lower SNR.**<br>**Power:** mode like EEE is **not available.**<br>Lo_3dm_02a_0125.pdf |
| **Crystal-less** | **Proven working solution for TDD**<br>Ng_3dm_01_05122025.pdf | **DME has high jitter w/o equalization.**<br>Proprietary SerDes are not DME based and use equalization |
| **Duplexing in Startup** | Starts in **TDD**<br>(remains in TDD for higher SNR) | Starts in **TDD !**<br>(**switches** from TDD to ACT after startup) |
| **Latency** | **No issue** in both DL and UL<br>matheus_dm_01e_comparison_20250727.pdf | **ACT fails** its own requirements in DL<br>houck_fuller_3dm_01_0724.pdf |

| | TDD – Proposal | ACT – Proposal |
|---|---|---|
| **Link Length** | **Capable of longer lengths with standard coax**<br>Enough SNR margin.<br>Prop delay can be increased if use case requires | **Longer link length with standard coax not possible due to lack of margin** (see EMC implementation)<br>Echo cancellation grows exponentially with longer length |
| **PoC Complexity** | **1 small inductor**<br>jingcong_dm_2024Sep_v2.pdf \| Chini_Tazebay_3dm_01a_0924.pdf<br>Zerna_802.3dm_01_250307_PoC_complexity_system.pdf \|<br>Chini_3dm_01c_07272025.pdf | **1 larger inductor claimed** – **Larger** footprint, **Lower** current rating, **Higher** power loss, and **Higher** cost<br>Inductor presented at IEEE is not valid!<br>Houck_3dm_02_0121_5.pdf \| Chini_3dm_01c_07272025.pdf |
| **Future for Higher Rates** | **Lowest complexity** for 1 Gbps Uplink.<br>**Linear scaling** to higher Downlink speeds<br>matheus_dm_01e_comparison_20250727.pdf | **1 Gbps UL is non-linearly complex.** Complete PHY redesign is necessary for each DL/UL speed combination.<br>matheus_dm_01e_comparison_20250727.pdf |
| **EMC** | **BEST Available Technology**<br>Zerna_3dm_01_250729.pdf \| Dalmia_Ng_EMI_COAX_3dm_01_04172025.pdf | **Inferior performance** compared to TDD.<br>High number of **missing tests** for Coax.<br>**STP not shown.** |

# PHY integration in the Switch

*A dual mode ch/dm PHY is not competitive




Implementation considerations: To ensure flexibility and maximize utilization of all switch ports, it is highly desirable that **each Multi-Gig PHY port** supports **asymmetrical** 802.3dm (camera link) with high-speed ***to the switch*** as well as ***asymmetrical 802.3dm from the switch***. Examples: display link or camera forwarding link) *)

Multi-mode port: Reversible HS 802.3dm **based on TDD**

**Ethernet Switch**

Updates to make multi-mode dm:

- None

802.3dm PHY

Multi-mode port: Reversible HS 802.3dm based on **ACT**

**Ethernet Switch**

Updates to make multi-mode dm:

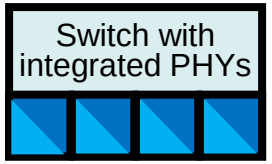
- Add high-speed TX PCS
- Add high-speed TX PMA
- Add low-speed RX PCS
- Add low-speed RX PMA

100M+MG BASE-T1

MG+100M BASE-T1

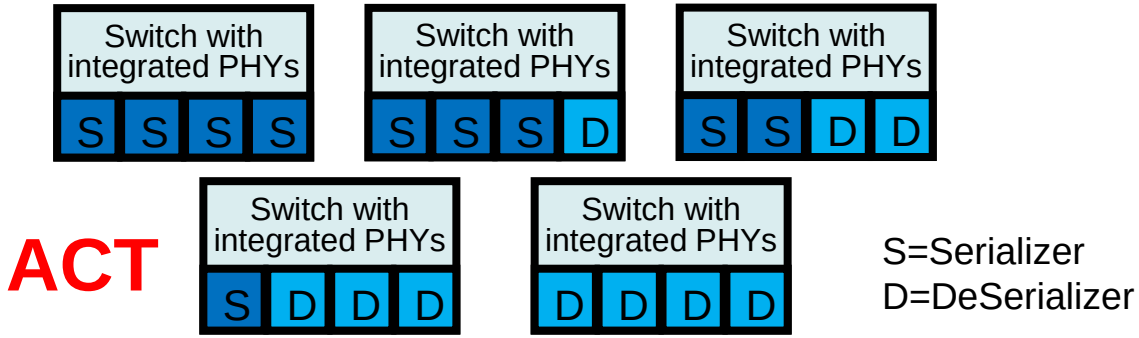
# Number of Implementations

**TDD**




One efficient product when change of high-speed direction is easy to realize

**ACT**




S=Serializer
D=DeSerializer

Five products when the change of high-speed direction is costly to realize

Implementation considerations:

Every implementation causes significant **development effort.**

The more needed, **the more the time and the relative cost**. Unlikely to have **multi-vendor**for each.

| **# parts to cover all options** | | **ACT** |
|---|---|---|
| Single port | 1 (3) | 2 (6) |
| Dual port | 1 (6) | 3 (21) |
| Quad port | 1 (15) | 5 (126) |
| Overall | **3 (24)** | **10 (153)** |

These number increase over proportionally when additionally optimizing for the three different speeds (in brackets)

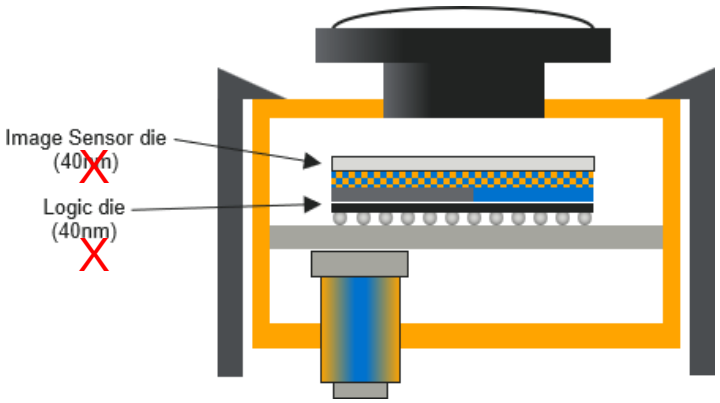
**ACT** will lead to **significantly more development** effort.

# Eco-System Summary

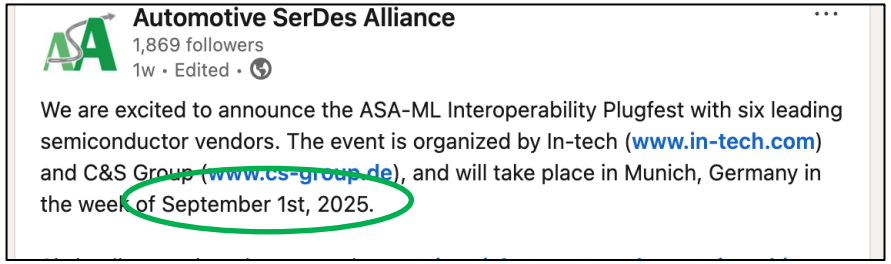
- Conformance & interoperability PHY specification are only the first step for wide market adoption. A fully established eco-system is required to successfully deploy a particular technology in automotive market.
- This eco-system comprises (among other)
  - a physical layer specification,
  - silicon availability (multi-vendor solution),
  - test houses (conformance, interoperability, and EMC testing),
  - testability (multiple test equipment vendors),
  - channel & components (cable, connector, magnetic vendors) and EMC test specification

- **ACT Limitations**
  - **No** available eco-system to leverage from
  - **New** channel and component specifications required
  - **Few communalities** between proprietary SerDes and ACT (different Baud rate, different US modulation)
- **TDD Advantages**
  - Eco-system **available**
  - **Re-use** of channel & component as well as EMC specification
  - **6+ vendors with extensive experience**

# PHY Integration in the Imager




- ASA-ML Interop plug-fest took place week of Sep 1st
- **2 of TOP 3 automotive imager vendors participated!**
- Imagers are available in 28nm & 22nm nodes also. Not just 40nm

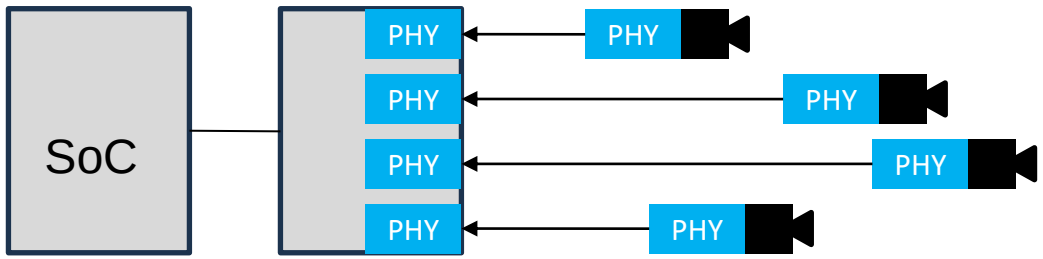



https://www.ieee802.org/3/ISAAC/public/091423/2023-09-06_Automotive%20camera%20PHY%20requirements%20study_V2.1.pdf

This link contains the original source of the picture in 802.3!
- This link is not cited by Houck et al
- The picture in the original link does not state 40nm

**TDD PHYs are being actively demonstrated by Imager silicon vendors, paving the path to integration of TDD serializers in imager ICs.**
**There is NO evidence of ACT PHY support for imager integration!**

# PHY-level Sync




It is desirable to **synchronize camera shutters** in certain use cases (e.g. 360° images)
Legacy implementations use GPIOs from the SoC to sent vsynch signals using hardware.
Unsynchronized videos cause the need for a larger video buffer.
802.3 PHYs do not incorporate a special side channel for GPIOs

## ACT Limitations

ACT **higher layer protocol support is needed** for synchronization
**Requires IEEE 802.1AS TSN** (about 80ns accuracy) to be adapted for asymmetric communication
Requires **changes from known** implementations (both hardware and software)

## TDD Advantages

**Inherent** precision time base in the PHY layer
**+/- 5.3 ns accuracy** for delay compensated GPIO for shutter synchronization
**Leverages** from known TDD implementations

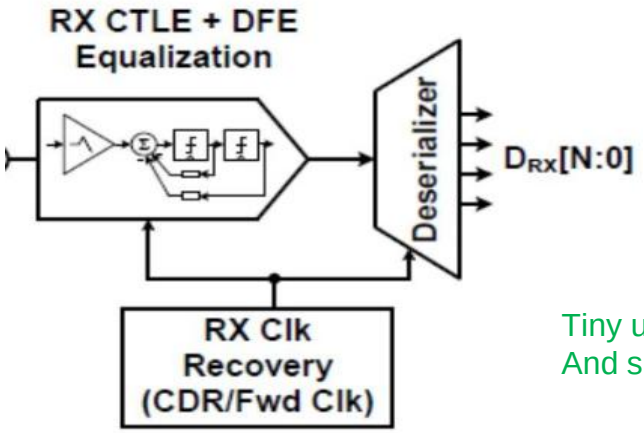
# 802.3dm OVERALL PPA Analysis: TDD vs ACT

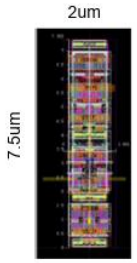
| | TDD | ACT |
|---|---|---|
| **Camera DS highspeed TX Complexity** | Not complex | Not complex |
| **Camera US lowspeed RX Complexity** | **Proven**. 10 vendors have announced TDD implementations.<br>If complicated as claimed by ACT proponents, how is this possible? | Higher processing rate drives higher power, despite the counterintuitive expectation otherwise. |
| **Camera Power Consumption** | **Best reported** | Excluded parts of the design (missing blocks) to score a draw w/ TDD |
| **ECU US lowspeed TX Complexity** | Not complex | Not complex |
| **ECU DS highspeed RX Complexity** | **Low complexity 8b FEC** | **Higher complexity 10b FEC, ADC/DFE/Filtering** |
| **ECU RX Power Consumption** | **Similar to camera-side (<3mW)** | **Not yet provided, likely much higher due to FEC increase** |
| **Crystal-less Camera Serializer** | **Proven working solution for TDD demonstrated** | **DME has high jitter w/o equalization.**<br>Proprietary SerDes are not DME based and use equalization |
| **Latency (including FEC)** | **~50% better in DS** | **2x Higher DS latency** |
| **Energy efficiency modes** | **Enables predetermined EEE to save power if Camera capability and line rate aren't aligned to 2.5/5/10** | **Requires continuous transmission, no practical EEE** |
| **ESD** | **Baseline** | **More complicated design than baseline** (superposition of simultaneous US/DS signals) |

**Summary: PPA (Power – Performance – Area) is the industry norm to compare technologies.**
**Complexity is captured in one or more of these three aspects.**
**TDD outshines ACT when properly analyzed under PPA methodology.**

# Camera Side Complexity and Power Summary

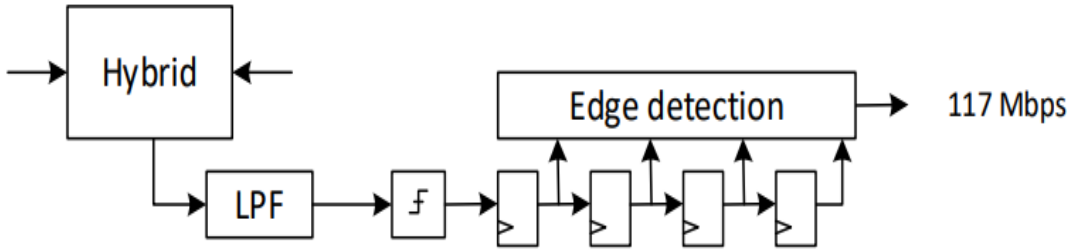
- **TDD Camera Receiver <0.012mm2, <3mW**
- **Processing rate 175MS/s**
- **Proven Architecture in Automotive Serdes**




Tiny upstream Slicer
And smaller Filters

- **ACT Camera Receiver – 0.012mm2, 3mW (Missing Blocks)**
- **Processing rate 468MS/s**
- **DME typically used in HDX Burst Communication, not FDX**




**Missing blocks: HPF, RX Clk Recovery (CDR/Fwd Clk). Link sync and auto-negotiation circuits. 4X sampling clock and decimation circuit. Slicer calibration circuit.**

*ACT Reference: https://www.ieee802.org/3/dm/public/0125/Lo_3dm_02a_0125.pdf

*TDD Reference: https://www.ieee802.org/3/dm/public/0725/Chini_3dm_02_07272025.pdf

- **The receiver blocks are a very small portion of total PHY (i.e. consider ESD!) and the PHY itself is a small portion of a camera solution. TDD receiver supports link sync, speed negotiation and clock recovery, the filters are smaller by a large factor and slicer is tiny, leading to a smaller overall relative cost.**

# ECU Side Complexity and Power Summary

- No echo canceller, No high order filter.
- TDD ECU Receiver- Similar architecture as in the camera at 2.5Gbps 0.012mm2, <3mW
- Similar architecture for 5Gbps, potentially with more DFE taps.
- Low complexity 8-bit FEC
- No additional circuit for link synchronization and speed negotiation

- ACT ECU Receiver – Area is not provided- Multiple architectures suggested or simulated.
- For Camera DS highspeed TX Complexity, the ACT version is more complex and needs higher supply to accommodate superposition of US/DS TX signals
- For ECU US lowspeed TX Complexity, similarly more complex than TDD and needs higher supply for same reason
- ADC+FFE+DFE receiver + High order TX filtering
- Digital or analog echo cancellation, optimized for asymmetric signaling
- 10bit-FEC, very large increase in complexity and power compared o incumbent 8-bit FEC and TDD.
- Additional circuits needed for link synchronization and speed negotiation.

- TDD uses similar low complexity SerDes receiver architecture on the ECU side, making it several times more cost efficient than ACT and incumbent solutions. ACT complexity on the ECU side is a concern as the complex FEC requirement makes it difficult to compete even with the incumbent solutions.

# Energy Efficiency Modes

Qa

| Resolution | Fps | Res | Blanking | Data rate |
|---|---|---|---|---|
| 2048 x 1080 | 30 | 12 | +10% | **0.88 Gbps** |
| 4096 x 2160 | 30 | 12 | +10% | **3.5 Gbps** |
| 5840 x 2160 | 30 | 12 | +15% | **5.2 Gbps** |
| 7200 x 2160 | 30 | 12 | +20% | **6.7 Gbps** |

## ACT Limitations

ACT **requires continuous transmission** for staying synchronized

**Not practical** to initiate low power mode in case the link capacity is not fully utilize

## TDD Advantages

**Inherent gaps** in the transmission

**System synchronized** automatically

Additional energy saving via EEE **possible with adjustments**

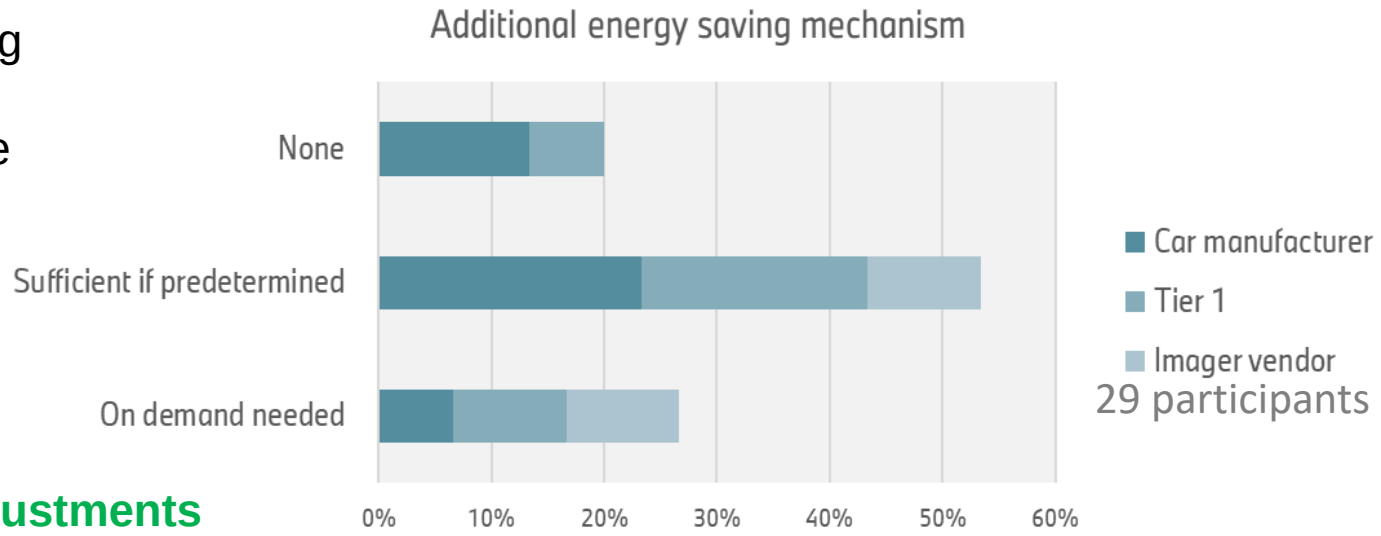
Many camera video streams have rates which **do not fill the 2.5, 5, or 10 Gbps**

Mainstream use cases will result in highly in-efficient utilization

Power saving is highly desirable

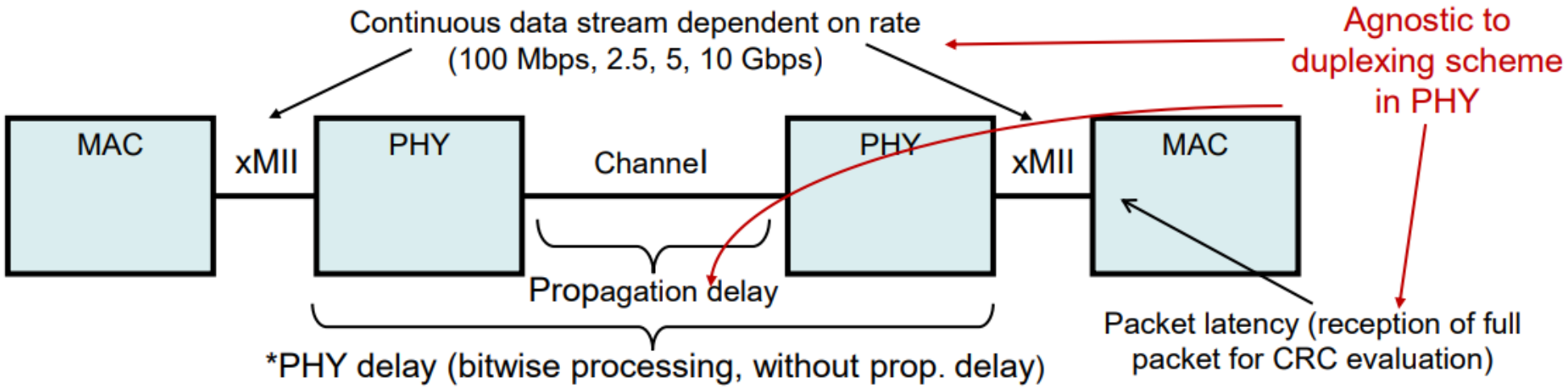
On-demand EEE may be difficult for such scenario (to small idle times), but **prescheduled EEE is of interest**

(see chart from matheus_ISAAC_02_01092024.pdf)



# Latency Summary

- Early on, latency was framed as a major and deciding factor, until the problem was carefully studied:




| PHY delay* | TDD | ACT |
|---|---|---|
| Upstream delay (including FEC) | 9.6µs for all speed grades[1] | ~8µs[2] |
| Downstream delay (including FEC) | ~1.1us[3] | 2.048µs[2] |

1 Chini_3dm_01a_0125.pdf
2 Houck_Cordero_ComparativeAnalysis_
3 Dalmia_Goel_3dm_01a_11112024.pdf

- It is proposed to limit the latency to 10us worst case in the switch to camera direction and 1us worst case in the camera to switch direction.
https://www.ieee802.org/3/dm/public/0724/houck_fuller_3dm_01_0724.pdf

# Interoperability between ACT and 802.3ch

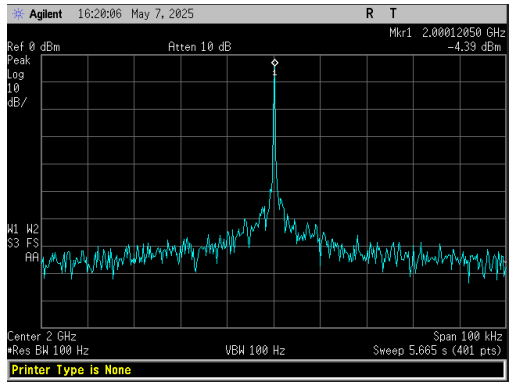
Differences shown in Red

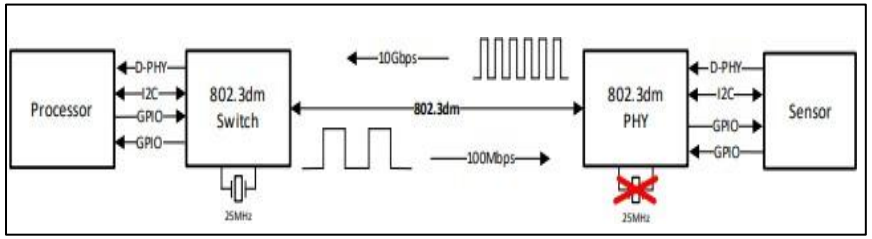
| | ACT – Proposal #1 | ACT – Proposal #2 | ACT – Proposal #3 | ACT – Proposal #4 | ACT – Proposal #5 | 802.3ch |
|---|---|---|---|---|---|---|
| Released | Sept 2024 | Nov 2024 | Jan 2025 | May 2025 | July 2025 | June 2020 |
| Baud rate and modulation | DL: 5625*S M, PAM4<br>UL: 104.625 M PAM2,234.375/281.25M DME | DL: 5625*S Mbps, PAM4<br>UL: 234.375 Mbps DME | DL: 5625*S Mbps, PAM4<br>UL: 234.375 Mbps DME | DL 10Gbps: 5625 Mbps, PAM4<br>DL 5Gbps: 5625 Mbps, PAM2<br>DL 2.5Gbps: 2812.5Mbps, PAM2<br>UL: 234.375 Mbps DME | DL 10Gbps: 5625 Mbps, PAM4<br>DL 5Gbps: 5625 Mbps, PAM2<br>DL 2.5Gbps: 2812.5Mbps, PAM2<br>UL: 234.375 Mbps DME | DL: 5625*S Mbps, PAM4<br>UL: 5625*S Mbps, PAM4 |
| STP Transmit power | DL: 0dBm<br>UL: -6dBm | DL: 0dBm<br>UL: -6dBm | DL: 0dBm<br>UL: 0dBm | 10Gbps = -1 ~ 2 (dBm)<br>5Gbps = -1 ~ 2 (dBm)<br>2.5Gbps = -4 ~ -1 (dBm)<br>100Mbps = -3 ~ 0 (dBm) | 10Gbps = -1 ~ 2 (dBm)<br>5Gbps = -1 ~ 2 (dBm)<br>2.5Gbps = -4 ~ -1 (dBm)<br>100Mbps = -3 ~ 0 (dBm) | 0dBm |
| FEC | DL: 10bit RS – 360,326<br>UL: 5bit –RS – 2 FECs | DL: 10bit – RS – 360,326<br>UL: 6bit – RS – 50,46 | DL: 10bit RS 360,326<br>UL: 6bit – RS – 50,46 | DL: 10bit – RS – 360,326<br>UL: 6bit – RS – 50,46 | DL: 10bit – RS – 360,326<br>UL: 6bit – RS – 50,46 | DL: 10bit – RS – 360,326<br>UL: 10bit – RS – 360,326 |
| Line coding | DL: 64b/65b<br>UL: 2 types | DL: 64b/65b<br>UL: 16b/17b | 64b/65b | 64b/65b | 64b/65b | 64b/65b |
| OAM bits | DL: 10<br>UL: none/2 | DL: 10<br>UL: 4 | DL: 10<br>UL: ? (16 reserved bits) | DL: 10<br>UL: 10 (+ 6 reserved bits) | DL: 10<br>UL: 10 (+ 6 reserved bits) | DL:10<br>UL:10 |
| synchronize start of training | Not defined | Not defined | Not defined | Not defined | Link Sync (changing)<br>No Auto-Negotiation | Link Synchronization/ Auto-Negotiation |
| EEE capability | No | No | No | No | No | Yes |

ACT and 802.3ch have fundamental differences in startup, modulation and FEC.

# Crystal-less Summary

- Clock recovery was passed by a motion to be an 802.3dm **objective**
- Crystal-less operation for TDD is **demonstrated** in [Ng_3dm_01_05122025.pdf]



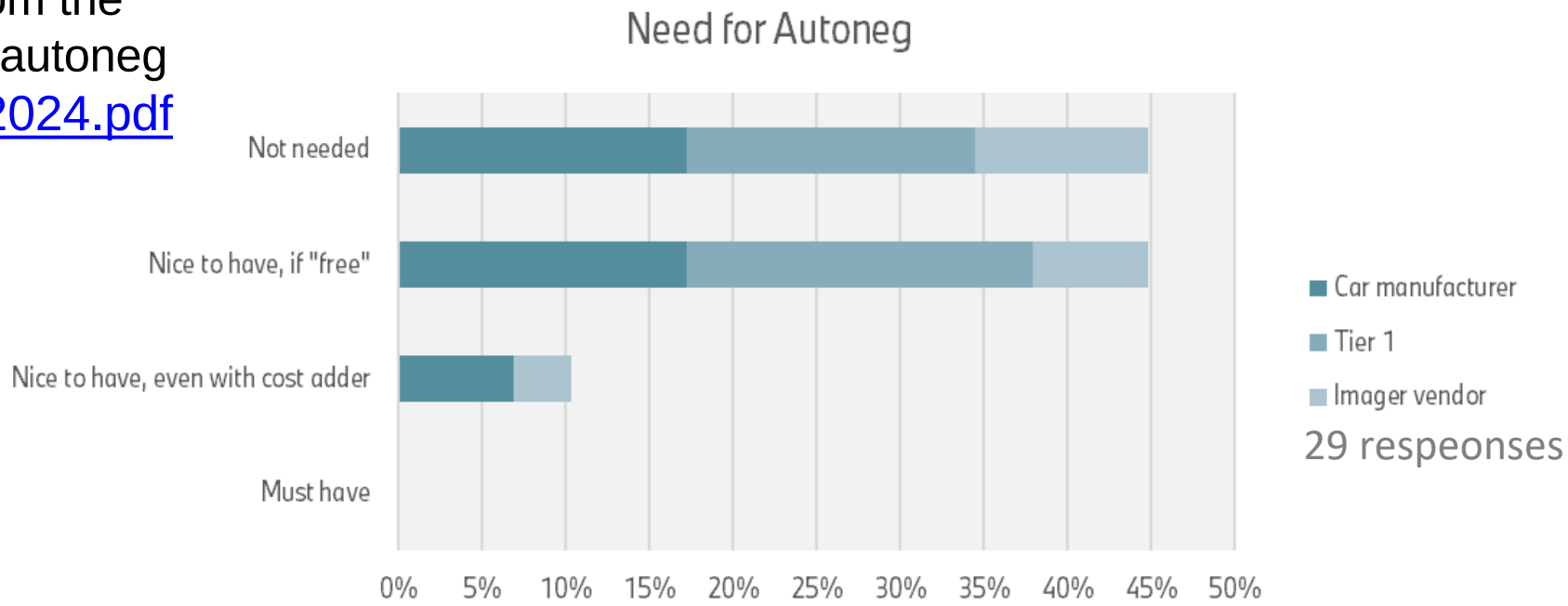

Houck_Ragnar_Fuller_3dm_01_0917.pdf

- **ACT Limitations**
  - It has been demonstrated that **DME signal accumulates data-dependent jitter**
  - Without equalization, the **jitter is excessive** for proper clock recovery
  - **Clause 98 Autoneg is not shown to work for ACT crystal-less operation**

- **TDD Advantages**
  - During upstream burst, **3Gbps signal** available for clock recovery circuit. This is **>10x better** than ACT signal.
  - During quiet gaps, modern **digital PLLs easily hold** the learned frequency
  - Incoming signal that is used for clock recovery has **better jitter properties** than ACT signal
  - TDD startup is **inherently ok** for crystal-less operation

# Crystal-less and Autoneg

- 55% of survey participants from the automotive industry may use autoneg [matheus_ISAAC_02_01092024.pdf]



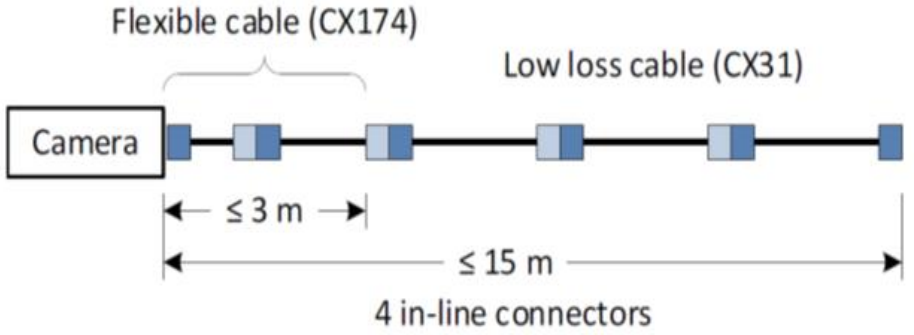

- **ACT Limitations**
  - Clause 98 Autoneg **is not shown to work** for crystal-less operation

- **TDD Advantages**
  - Has **inherent** (“free”) autoneg for high-speed during startup (via capability exchange to negotiate speed 2.5/5/10).
  - Crystalless operation is not affected by autoneg or startup

# Cable Length

P802.3dm adopted a 15m length objective

- Shown to be adequate for all passenger cars, utility vans, and city/regional buses (matheus_jonsson_dalmia_ISAAC_01_1411202327_v1.0.pdf, matheus_ISAAC_03_1411202327_v1.0b.pdf)
- The need for longer cable not substantiated
- Potential volume in other markets (industrial automation, aerospace) small with no impact into automotive market




Per the velocity factor assumptions of the previous slide , the worst case is:

- Total Delay = (5.05 × 3) + (5.05 × 12) + (connector delay) ≈ 76 ns

With slowest version of coax cable

- >20m easily achievable with e.g. 90 ns delay limit

→ Length is IL limited and not delay limited

- **ACT Limitations**
  - **Cable length limitations known** with incumbents https://www.analog.com/media/en/technical-documentation/user-guides/gmsl3-channel-specification-user-guide.pdf
  - **Smaller SNR margin** than TDD limits the reach
- **TDD Advantages**
  - **Sufficient SNR margin** to cover longer cable reach with standard cables
  - **>20m** achievable with common cable, more if needed
  - **Re-use** of channel and component specification possible

# Future for Higher Rates

Higher rates might be of interest for downstream and upstream

1. Higher DS data rates (esp. 15 Gbps, 25 Gbps), e.g. zimmerman_3ISAAC_01b_012224.pdf
2. Higher US data rates (esp. 1 Gbps), e.g., matheus_ISAAC_01c_10042023.pdf

## ACT Limitations

- Upstream rates such as 1Gbps and 2.5Gbps are **non-linearly difficult** to achieve for ACT scheme
- As the ratio of downstream to upstream frequencies that overlap, **the echo problem gets harder**
- Claims of upstream receiver not needing equalization do not hold any merit at these rates

## TDD Advantages

- Upstream rates such as 1Gbps and 2.5Gbps are **easy to achieve** for TDD scheme
- **TDD** PHY scales LINEARLY to higher speeds as shown in the table below! It shows how TDD scales to **25G** and **50G**
- In an example below, only DS line rate and the number of RS frames are **changed linearly**
- **No other change** is made for the purpose of demonstrating feasibility!

| | | | | Dn | | | | | | | Up | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Per RS frame | | | | Burst | | | Per RS frame | | | | | | | | | | | | |
| Dn Line Rate [Gbps] | Up Line Rate [Gbps] | Resync Header [ns] | IBG [ns] | 64/65 blocks | OAM bits | Payload bytes | Parity bytes | RS frames | Length [bits] | Length [ns] | 64/65 blocks | OAM bits | Payload bytes | Parity bytes | RS frames | Length [bits] | Length [ns] | Target [ns] | Dn [ns] | Up [ns] | Total [ns] | Dn Payload per burst [bits] | **Dn Data Rate [Gbps]** | Up Payload per burst [bits] | **Up Data Rate [Mbps]** |
| 3 | 3 | 186.67 | 106.7 | 15 | 1 | 122 | 8 | 25 | 26000 | 8666.67 | 15 | 17 | 124 | 6 | 1 | 1040 | 346.67 | 9600 | 8853.3 | 533.3 | 9600.0 | 24000 | **2.500** | 960 | **100.0** |
| 6 | 3 | 186.67 | 106.7 | 15 | 1 | 122 | 8 | 50 | 52000 | 8666.67 | 15 | 17 | 124 | 6 | 1 | 1040 | 346.67 | 9600 | 8853.3 | 533.3 | 9600.0 | 48000 | **5.000** | 960 | **100.0** |
| 12 | 3 | 186.67 | 106.7 | 15 | 1 | 122 | 8 | 100 | 104000 | 8666.67 | 15 | 17 | 124 | 6 | 1 | 1040 | 346.67 | 9600 | 8853.3 | 533.3 | 9600.0 | 96000 | **10.000** | 960 | **100.0** |
| **30** | 3 | 186.67 | 106.7 | 15 | 1 | 122 | 8 | **250** | 260000 | 8666.67 | 15 | 17 | 124 | 6 | 1 | 1040 | 346.67 | 9600 | 8853.3 | 533.3 | 9600.0 | 240000 | **25.000** | 960 | **100.0** |
| **60** | 3 | 186.67 | 106.7 | 15 | 1 | 122 | 8 | **500** | 520000 | 8666.67 | 15 | 17 | 124 | 6 | 1 | 1040 | 346.67 | 9600 | 8853.3 | 533.3 | 9600.0 | 480000 | **50.000** | 960 | **100.0** |

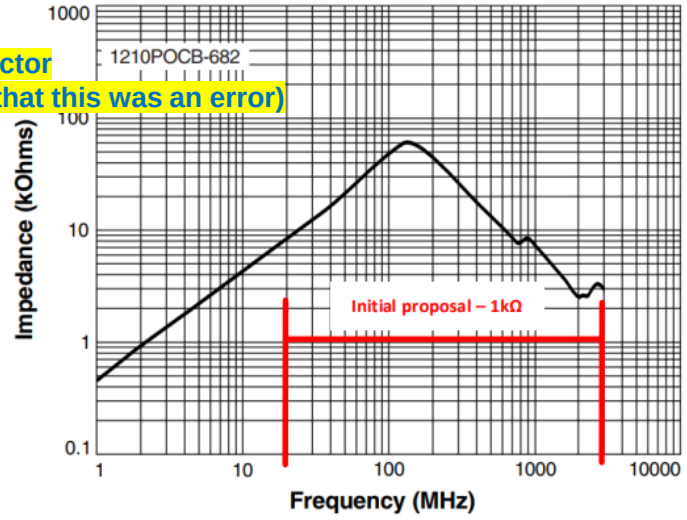
# PoC Complexity

- **TDD does not have** a low-speed backward channel occupying low frequency range and thus **1 inductor solution** can be achieved.
  - jingcong_dm_2024Sep_v2.pdf
- **1μH** inductor is suggested for TDD under 802.3dm MDI Return Loss and there are **many good candidates** available in the market.
  - Chini_3dm_01c_07272025.pdf
- **TDD's 1 inductor solution** has **LOWER** footprint, **HIGHER** current rating, **LOWER** power loss, and **LOWER** relative cost.

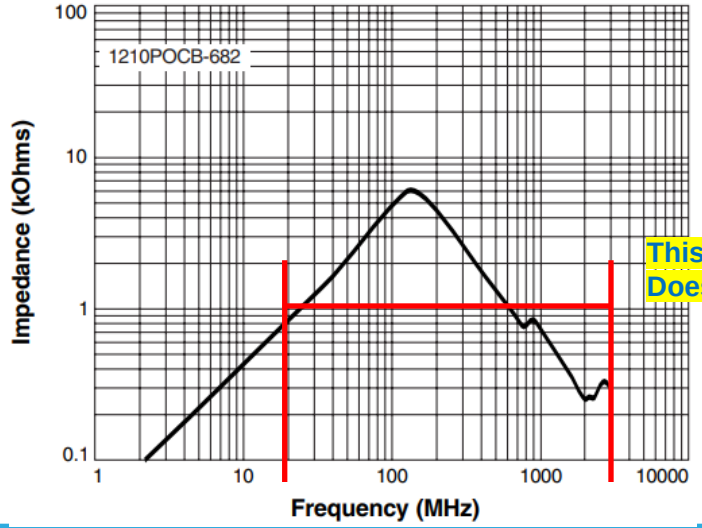
**ACT Questions:**

- Houck_3dm_02_0121_5.pdf claimed that the inductor impedance for ACT should be larger than 1k ohm across 20MHz – 3000MHz and then 1 inductor solution with **6.8μH**, e.g., 1210POCB-682, was introduced as shown in the left figure.
  - However, the impedance for 1210POCB-682 has been updated and **NO alternative** is provided for ACT.
- A mystery PoC inductor that has inductance **> 10μH** may be applicable for ACT – **no specific information has been presented.**

**Presented 6.8uH inductor**
**(later verbally stated that this was an error)**




updated



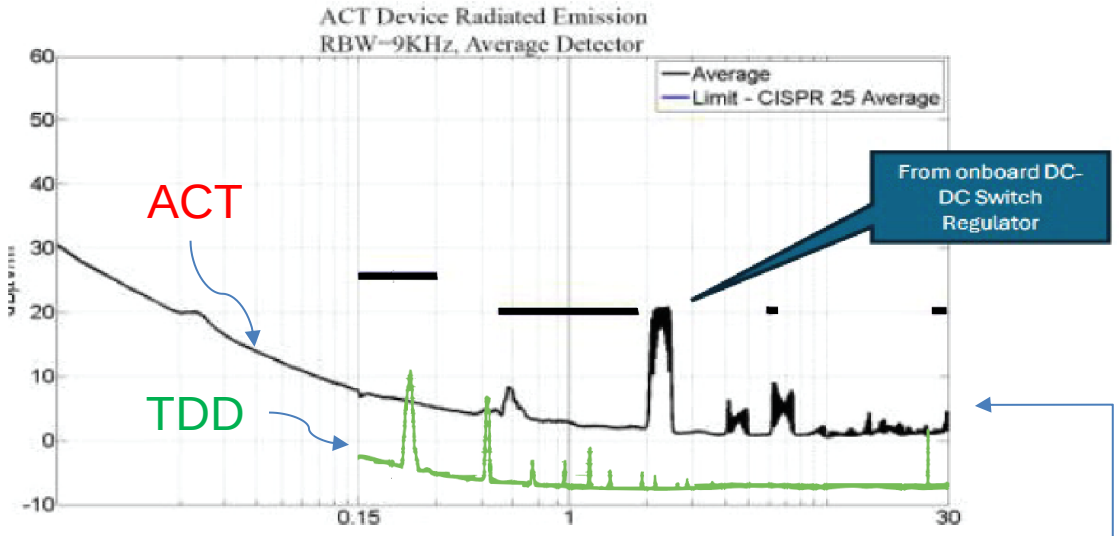

**This is the actual 6.8uH inductor.**
**Does not meet ACT targets!**

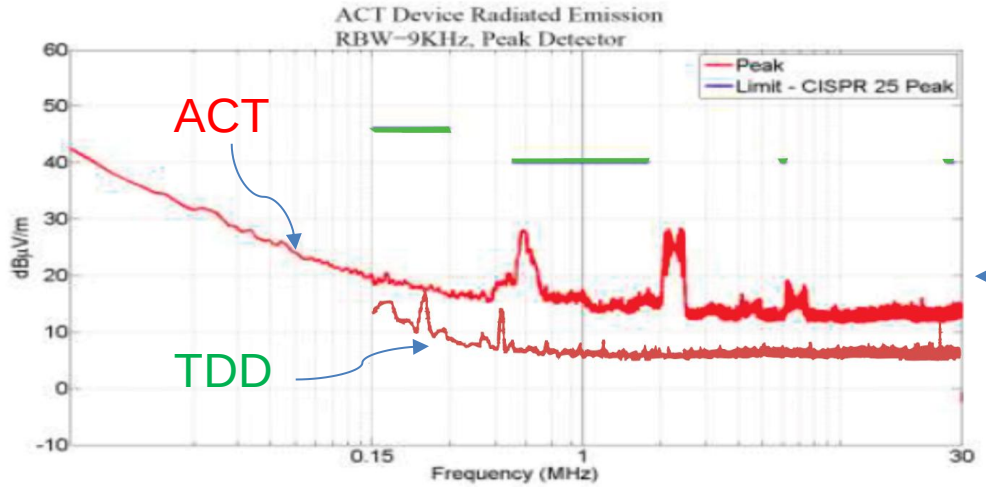
# EMC CISPR Results – BIG PICTURE

| | TDD | ACT |
|---|---|---|
| Coax Emissions | **Complete set**<br>**Published** | **>Half of results not published**<br>**(Most plots show less margin than TDD)** |
| Coax<br>Radiated<br>Immunity | • 2 meter cable – Yes<br>• **7 meter cable – Yes**<br>• **12 meter cable – Yes**<br>• **Complete frequency range** | • 2 meter cable – Yes<br>• **7 meter cable – NO**<br>• **12 meter cable – NO**<br>• **Starting near 400MHz, end at 3.4GHz (critical frequencies missing)** |
| Coax BCI | **15cm – Yes**<br>45cm – Yes<br>**75cm – Yes** | **15cm – Not shown in the setup**<br>45cm – Yes<br>**75cm – ?** |
| STP Emissions | **Complete set**<br>**published** | **NO results published** |
| STP Radiated immunity | **Yes** | **NO results published** |
| STP BCI | **Yes** | **NO results published** |

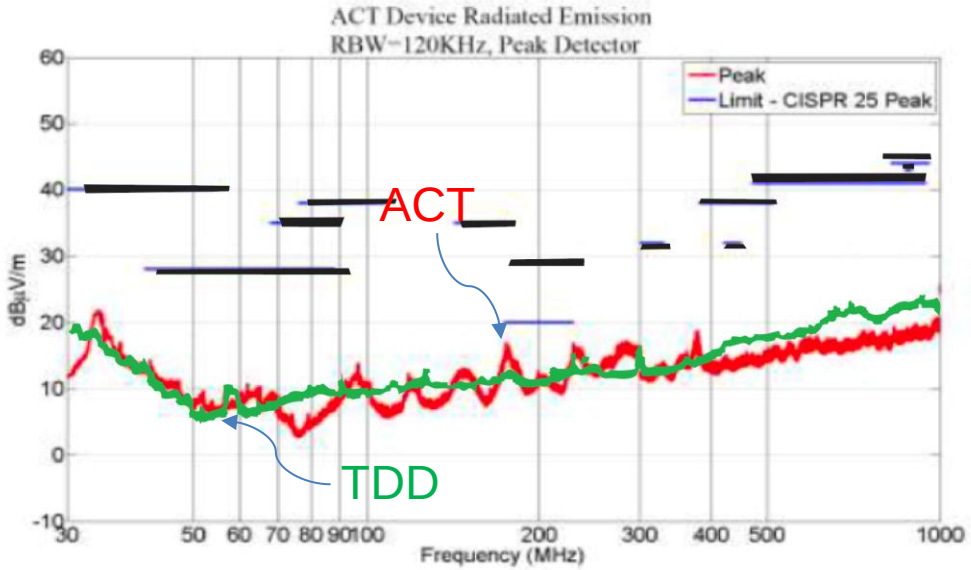
Summary of results published till July 2025. Non CISPR tests are addressed elsewhere.

# Overlay Comparison of EMC Results Presented at IEEE




0.15MHz to 30 MHz



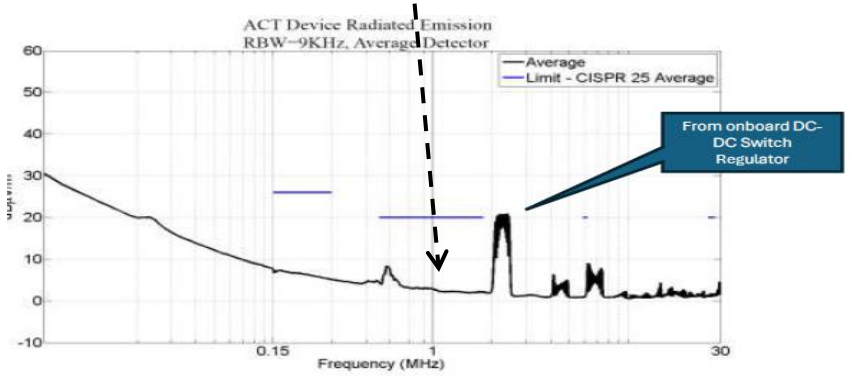

30MHz to 1GHz

**TDD has superior EMC performance**

# EMC Summary

**Discontinuity at 1 MHz, where the axis changes, from logarithmical based on 0.15 to 1**

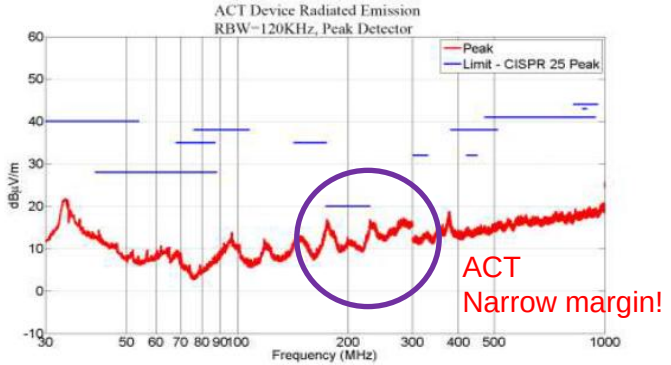
Coax emission evaluation 0.15-30MHz




wu_3dm_01a_072925.pdf

Zerna_3dm_01b_250729.pdf

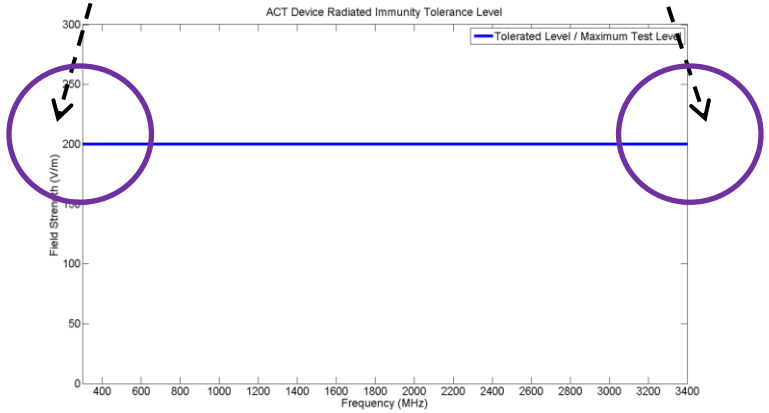
Coax emission evaluation 30MHz – 1GHz




wu_3dm_01a_072925.pdf

**Missing ACT results in relevant ranges <350 MHz and >3400MHz**

Radiated immunity evaluation




wu_3dm_01a_072925.pdf

- **ACT Limitations**
  - **Missing results for relevant** frequencies, STP, and meaningful link lengths
  - **Significantly smaller** margin in presented results
  - **No confirmation** from independent test house
- **TDD Advantages**
  - **Complete** CISPR EMC results published
  - All tests are a **pass**
  - Tests performed by **independent test house**

# Summary

| | TDD | ACT |
|---|---|---|
| **Crystal-less** | Demonstrated | Breaks auto-negotiation |
| **EMC** | Proven robust | Incomplete disclosure suggests real issues |
| **Power, Size, Complexity** | Suited to the application | Higher DS latency, no on-demand EEE possible |
| **Higher speed** | Lowest complexity (simple scaling) | Requires complete overhaul |
| **Cable Length** | Supports objective of >15meters with higher SNR margin | Lower SNR margin |
| **Interoperability** | Proven interop between 5 vendors for TDD-based ASA-ML | No |
| **Integration** | Proven support from imager vendors, reversable pins | No evidence of support, incapable of reversing |
| **PHY-level SYNC** | Inherently built into TDD | Not Defined |
| **Ecosystem** | Exists to leverage from | Years behind |
| **Number of Implementations** | Optimal for creating variants of chips needed to serve the market | Unreasonably large number of chips needed to serve applications |

THANK YOU

Questions?