ACT vs TDD Comparison: Evidence Based Results

Contribution to 802.3dm Task Force
September 15, 2025

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Introduction

This presentation points out some of the errors in the presentation “ACT and TDD Comparison”, by Claude Gauthier and Frank Wang

https://www.ieee802.org/3/dm/public/0925/Gauthier_Wang_3dm_01_09152025.pdf

We believe these errors should be corrected by the authors

Comparison Table

	TDD – Proposal	ACT – Proposal
Crystal-less	Proven working solution for TDD Ng_3dm_01_05122025.pdf	Not demonstrated. DME has high jitter w/o equalization. Proprietary SerDes are not DME based and use equalization
Duplexing in Startup	Starts in TDD (remains in TDD for higher SNR)	Starts in TDD ! (switches from TDD to ACT after startup)
EMC	BEST Available Technology Zerna_3dm_01_250729.pdf | Dalmia_Ng_EMI_COAX_3dm_01_04172025.pdf	Inferior performance compared to TDD. High number of missing tests for Coax. STP not shown.
Power, Performance, Area (PPA)	Optimum for Ser and DeSer. Better SNR. Dalmia_3dm_01_03102025.pdf | Chini_3dm_02b_0325.pdf | Chini_3dm_02a_0525.pdf Chini_3dm_02_07272025.pdf	DeSerializer side is complicated. Performance: Lower SNR. Power: mode like EEE is not available. Lo_3dm_02a_0125.pdf
Imager and Switch Integration	TDD is supported by imager vendors Switch side needs Reversible Asymmetrical PHYs	No evidence of ACT support by imager vendors Much more complex to reverse high-speed direction matheus_dm_01e_comparison_20250727.pdf
Interoperability	PHY vendors can leverage ASA-ML (proven interop between 5 vendors) ASA Press Releases and announcements	Interop between ACT and 802.3ch is not possible Autoneg, Link Sync, Modulation, FEC are different (see slide 14)
Future for Higher Rates	Lowest complexity for 1 Gbps Uplink. Linear scaling to higher Downlink speeds matheus_dm_01e_comparison_20250727.pdf	1 Gbps UL is non-linearly complex. Complete PHY redesign is necessary for each DL/UL speed combination. matheus_dm_01e_comparison_20250727.pdf
Latency	No issue in both DL and UL matheus_dm_01e_comparison_20250727.pdf	ACT fails its own requirements in DL houck_fuller_3dm_01_0724.pdf

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Incorrect, corrections needed

Incorrect: Crystal-less operation has been demonstrated, see slide 3 wu_3dm_01a_072925.pdf

Incorrect: ACT uses half duplex in training, not TDD

Incorrect: EMC test results for ACT show excellent performance, passing all EMC tests with coax (see wu_3dm_01a_072925.pdf). No test results have been shared for the new TDD, only ASA-ML.

Incorrect: There is no evidence that SerDes has a higher SNR than ACT. Theoretically, TDD upstream operates at a higher baud rate than ACT so that ACT will have better SNR than TDD.

Incorrect: EEE is not needed to achieve low power with ACT.

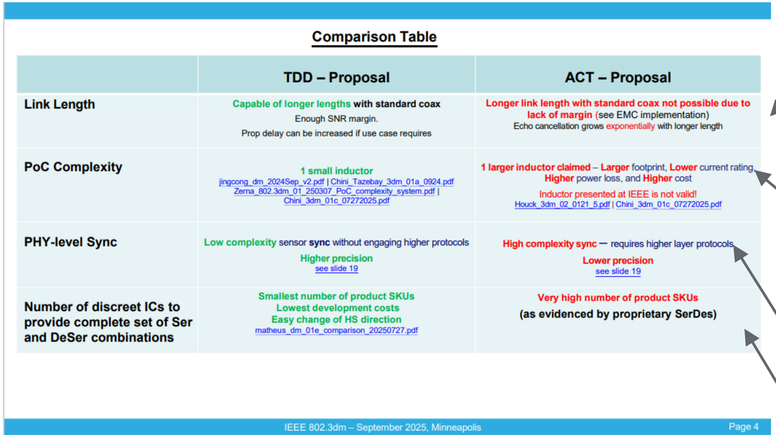
Incorrect: The complexity of the ACT architecture is lower than TDD

Incorrect: This is ASA not TDD – 802.3dm is TDD
Incorrect and Misleading: Reversibility is not part of PAR or Objectives. The PHY can be reversible is a strong indication that it's not fully optimized for the target application

Misleading: Versions of ASA and TDD are not interoperable. See p15 of https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf for ASA/TDD interoperability issues.

Incorrect: See slide for more information – slide 20

Incorrect: TDD does not include uplink – calculations are not correct for latency
ACT meets requirements – see below calculations on slide



Comparison Table

	TDD – Proposal	ACT – Proposal
Link Length	**Capable of longer lengths with standard coax** Enough SNR margin. Prop delay can be increased if use case requires	**Longer link length with standard coax not possible due to lack of margin** (see EMC implementation) Echo cancellation grows exponentially with longer length
PoC Complexity	**1 small inductor** jingcong_dm_2024Sep_v2.pdf | Chini_Tazebay_3dm_01a_0924.pdf Zerna_802.3dm_01_250307_PoC_complexity_system.pdf | Chini_3dm_01c_07272025.pdf	**1 larger inductor claimed** – **Larger** footprint, **Lower** current rating, **Higher** power loss, and **Higher** cost Inductor presented at IEEE is not valid! Houck_3dm_02_0121_5.pdf | Chini_3dm_01c_07272025.pdf
PHY-level Sync	**Low complexity** sensor **sync** without engaging higher protocols **Higher precision** see slide 19	**High complexity sync** — requires higher layer protocols **Lower precision** see slide 19
Number of discreet ICs to provide complete set of Ser and DeSer combinations	**Smallest number of product SKUs** **Lowest development costs** **Easy change of HS direction** matheus_dm_01e_comparison_20250727.pdf	**Very high number of product SKUs** **(as evidenced by proprietary SerDes)**

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Incorrect, corrections needed

Incorrect: The TDD proposal resist to adopt the tougher limit line proposed for insertion loss proposed in ACT. This fact, by itself, is a sign that TDD cannot operate on longer cables.

Incorrect: TDD has larger bandwidth, more ISI, and is sensitivity to longer propagation delay as shown in collision presentation below

https://ieee802.org/3/dm/public/adhoc/062625/jonsson_3dm_01_06_26_25.pdf

Incorrect: No discussion of **Slide 19** on TDD, higher bandwidth than ACT and low frequency baseline wander issues
https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

Slide 5 – 2 inductors – no 1 inductor solutions with 15m w/ 4inlines
https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

Incorrect: This is not synchronization. GPIO Delay Compensation is jitter control and is not TSN

Misleading: This is a implementation decision

Proprietary SerDes SKUs is not provided for comparison

802.3dm OVERALL PPA Analysis: TDD vs ACT

	TDD	ACT
Camera DS highspeed TX Complexity	Not complex	Not complex
Camera US lowspeed RX Complexity	Proven. 10 vendors have announced TDD products. If complicated as claimed by ACT proponents, how is this possible?	Higher processing rate drives higher power, despite the counterintuitive expectation otherwise.
Camera Power Consumption	Best reported	Excluded parts of the design (missing blocks) to score a draw w/ TDD
ECU US lowspeed TX Complexity	Not complex	Not complex
ECU DS highspeed RX Complexity	Low complexity 8b FEC	Higher complexity 10b FEC, ADC/DFE/Filtering
ECU RX Power Consumption	Similar to camera-side (<3mW)	Not yet provided, likely much higher due to FEC increase
Crystal-less Camera Serializer	Proven working solution for TDD demonstrated	Not demonstrated. DME has high jitter w/o equalization. Proprietary SerDes are not DME based and use equalization
Latency (including FEC)	~50% better in DS	2x Higher DS latency
Energy efficiency modes	Enables predetermined EEE to save power if Camera capability and line rate aren't aligned to 2.5/5/10	Requires continuous transmission, no practical EEE
ESD	Baseline	More complicated design than baseline (superposition of simultaneous US/DS signals)

Summary: PPA (Power – Performance – Area) is the industry norm to compare technologies.
Complexity is captured in one or more of these three aspects.
TDD outshines ACT when properly analyzed under PPA methodology.

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Incorrect, corrections needed

Incorrect: TDD downstream transmit power is higher than ACT, burning more power, and requiring more circuit complexity/area to maintain linearity

Incorrect and Misleading: This is ASA not 802.3dm TDD proposed PHY. Information on how ASA MLE is not TDD: Evolution of 802.3dm: From GMSLE to ACT and Beyond

Incorrect and Misleading: This is not possible. Even if we assume that power consumption scales linearly with symbol rate (which is not true) and account for the off time of a TDD receiver, it would still burn more power because TDD needs equalization.

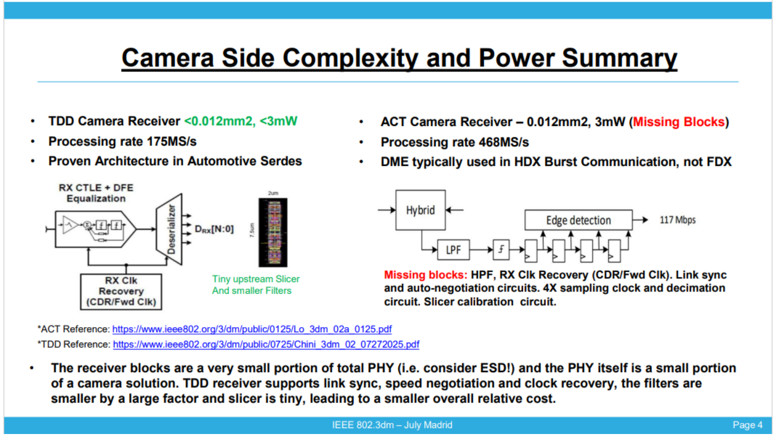
Misleading: FEC complexity is a tradeoff between burst protection and complexity. Simpler TDD FEC has less robustness to burst errors.

Incorrect: It is not possible that the power consumption of the DS and US receivers be similar, when DS receiver is ON much longer time than US

Incorrect: ACT will be better FEC does not determine latency

Incorrect: Power savings does not require EEE on ACT – please remove.

Incorrect: ESD design does not depend on whether simultaneous signaling occurs. Both TDD and ACT require Tx and Rx to be connected to the same pins for single pair wire support.



Incorrect, corrections needed

Misleading and Incorrect: 3Gbps PHY can never be smaller than 100Mbps especially with low power modes described. This is constraint by Physics of high speed design

See **slide 12** – size comparison
https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

Incorrect and Misleading: Size comparison – this presentation does not include the low power complexity
https://www.ieee802.org/3/dm/public/0125/Houck_3dm_01_0121_5.pdf

Misleading: TDD includes low power circuitry for turning off PHY and other states and don't see that included

See **page 9** discussing die size increase for low power states
https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

ECU Side Complexity and Power Summary

- No echo canceller, No high order filter.
- TDD ECU Receiver- Similar architecture as in the camera at 2.5Gbps 0.012mm2, <3mW
- Similar architecture for 5Gbps, potentially with more DFE taps.
- Low complexity 8-bit FEC
- No additional circuit for link synchronization and speed negotiation

- ACT ECU Receiver – Area is not provided- Multiple architectures suggested or simulated.
- For Camera DS highspeed TX Complexity, the ACT version is more complex and needs higher supply to accommodate superposition of US/DS TX signals
- For ECU US lowspeed TX Complexity, similarly more complex than TDD and needs higher supply for same reason
- ADC+FFE+DFE receiver + High order TX filtering
- Digital or analog echo cancellation, optimized for asymmetric signaling
- 10bit-FEC, very large increase in complexity and power compared o incumbent 8-bit FEC and TDD.
- Additional circuits needed for link synchronization and speed negotiation.

- TDD uses similar low complexity SerDes receiver architecture on the ECU side, making it several times more cost efficient than ACT and incumbent solutions. ACT complexity on the ECU side is a concern as the complex FEC requirement makes it difficult to compete even with the incumbent solutions.

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Incorrect, corrections needed

Incorrect: Not a significant factor in power or complexity of design. Supply voltage, process node, transmitter design is an implementer's decision

Incorrect and Misleading: No higher order Tx filtering needed. ADC based architecture is not required for high-speed receiver.

It is implementation choice.

Incorrect: FEC size at ECU-side is only 200% greater, 469% longer burst protection FEC size is very small and power insignificant, should not be determining factor.

Slide 10: https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

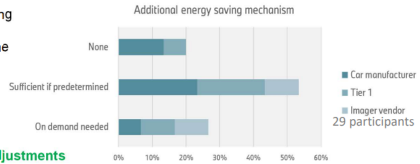
Energy Efficiency Modes

Oa

Resolution	Fps	Res	Blanking	Data rate
2048 x 1080	30	12	+10%	0.88 Gbps
4096 x 2160	30	12	+10%	3.5 Gbps
5840 x 2160	30	12	+15%	5.2 Gbps
7200 x 2160	30	12	+20%	6.7 Gbps

Many camera video streams have rates which **do not fill the 2.5, 5, or 10 Gbps**
Mainstream use cases will result in highly in-efficient utilization
Power saving is highly desirable
On-demand EEE may be difficult for such scenario (to small idle times), but **prescheduled EEE is of interest**

(see chart from matheus_ISAAC_02_01092024.pdf)



ACT Limitations

ACT **requires continuous transmission** for staying synchronized
Not practical to initiate low power mode in case the link capacity is not fully utilize

TDD Advantages

Inherent gaps in the transmission
System synchronized automatically
Additional energy saving via EEE **possible with adjustments**

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Incorrect, corrections needed

Incorrect: Imagers continuously transmit having low power minimal circuitry is lower risk

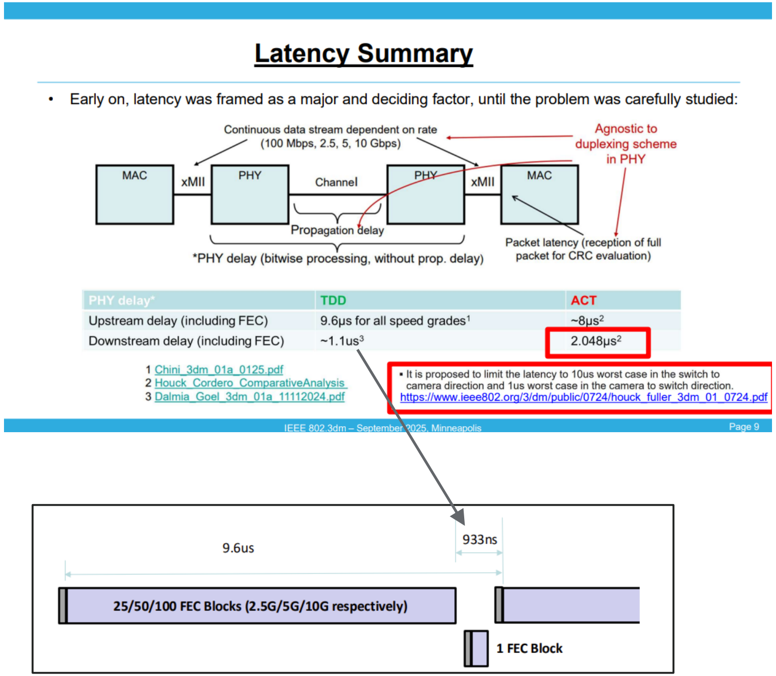
Incorrect: System does not automatically synchronize because of TDD. This requires processing

Incorrect: TDD requires continuous updates to stay synchronized

Misleading: Link is optimized per speed – the links are not dynamically changing speed

Incorrect: TDD low power modes require power – the circuitry is not a light switch it can't be shut off without consequences

Slide 9
https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf



Incorrect, corrections needed

Incorrect: 933nsec buffer not included – TDD 1.1usec is for downstream not the entire link.

Misleading: Not calling out all speed grade delays – this is for 10Gbps

ACT latency with interleaving + FEC:
2.5Gbp = 1.28usec
5.0Gbps = 640ns/1.28usec | interleave = 1/2
10Gbps = 320ns/640ns/1.28us | interleave = 1/2/4

Missing: Links are not included in slide

EMC CISPR Results – BIG PICTURE

	TDD	ACT
Coax Emissions	Complete set Published	>Half of results not published (Most plots show less margin than TDD)
Coax Radiated Immunity	• 2 meter cable – Yes • 7 meter cable – Yes • 12 meter cable – Yes • Complete frequency range	• 2 meter cable – Yes • 7 meter cable – NO • 12 meter cable – NO • Starting near 400MHz, end at 3.4GHz (critical frequencies missing)
Coax BCI	15cm – Yes 45cm – Yes 75cm – Yes	15cm – Not shown in the setup 45cm – Yes 75cm – ?
STP Emissions	Complete set published	NO results published
STP Radiated immunity	Yes	NO results published
STP BCI	Yes	NO results published

Summary of results published till July 2025. Non CISPR tests are addressed elsewhere.

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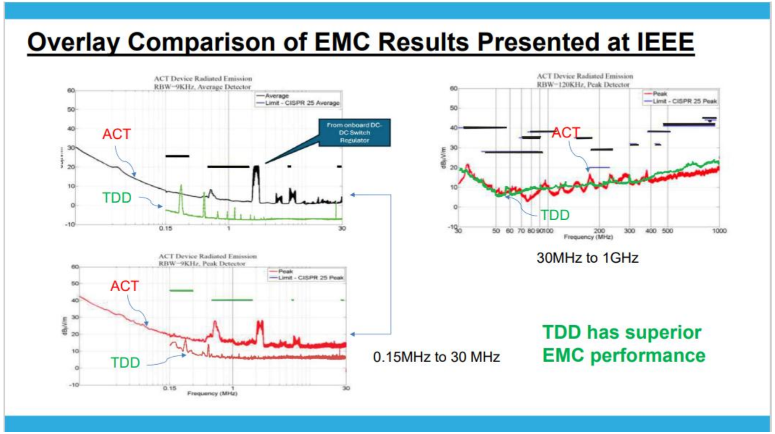
Corrections and Clarification needed

Misleading: What was timing, bandwidth, and frequencies for DL/UL tested?

Is this TDD or ASA?

If the above differs ASA is not TDD as specified [Evolution of 802.3dm: From GMSLE to ACT and Beyond]

Review **Slide 9 –** TDD is Time driven ASA is Protocol driven



Incorrect, corrections needed

Misleading: Is this TDD or ASA? Please specify exact timing

Misleading: ACT tested Crystal-less and PoC – TDD did not

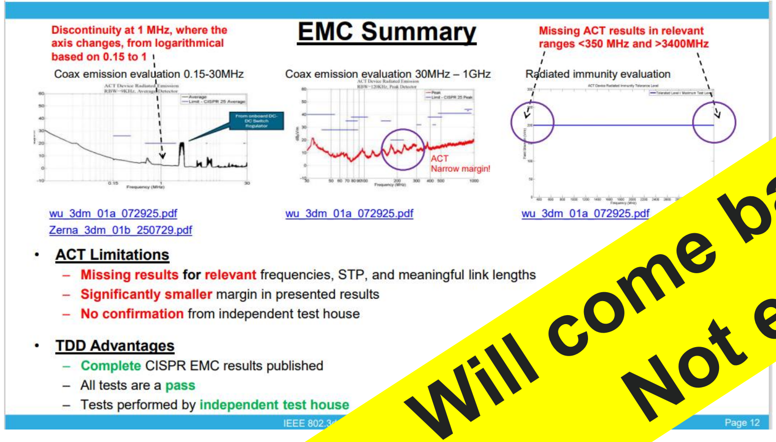
Review **Slide 3**
https://www.ieee802.org/3/dm/public/0725/wu_3dm_01a_072925.pdf

Incorrect: to compare the noise floor (where there are no peaks) between different CISPR25 measurements.

The noise floor depends on the equipment used in the test (LNA noise figure, spectrum analyzer type), independent of the modulation type.

Misleading: Radiated emissions is very dependent on board and cable type.

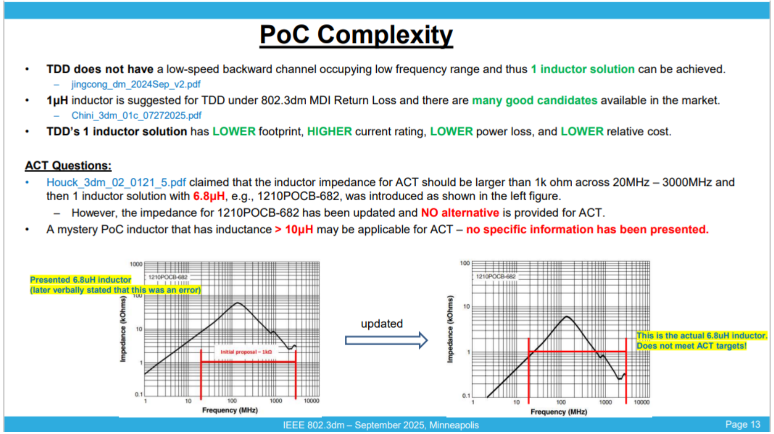
It is not valid to compare different test setups for relative performance.



Additional co
Same comp

Will come back to in Future

Not enough time



Incorrect, corrections needed

Misleading: Does the 1uH TDD 1 inductor solution work with EMC and 15 meters with 4 in-line cables?

Incorrect: Return Loss does not prove a valid solution

Incorrect: TDD requires impedance – no discussion – review impedance presentation again and comparison presentation on why this is critical

No discussion of **slide 19** on TDD, higher bandwidth than ACT and low frequency baseline wander issues
https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

Baseline wander issues for TDD (Low frequency)
https://ieee802.org/3/dm/public/adhoc/062625/jonsson_3dm_02_06_26_25.pdf

Why Impedance Matters – review full presentation and explain why TDD does not require impedance when Low frequency content is present
https://www.ieee802.org/3/dm/public/0125/Houck_3dm_01_0121_5.pdf

Incorrect, cor[illegible]eded

Interoperability between ACT and 802.3ch

Differences shown in Red

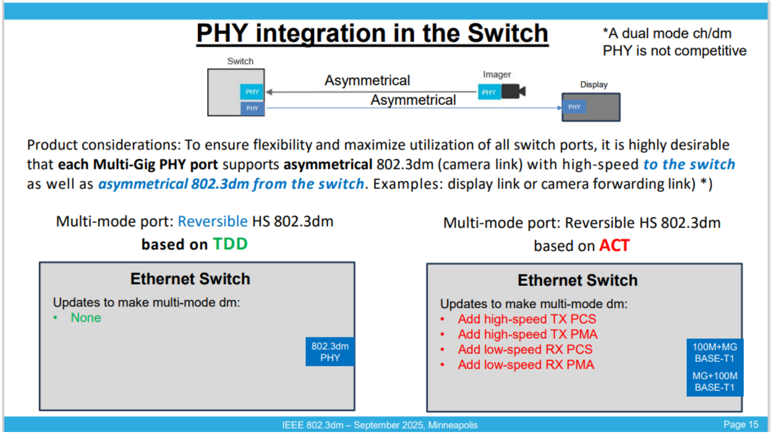
	ACT – Proposal #1	ACT – Proposal #2	ACT – Proposal #3	ACT – Proposal #4	ACT – Proposal #5	802.3ch
Released	Sept 2024	Nov 2024	Jan 2025	May 2025	July 2025	June 2020
Baud rate and modulation	DL: 5625*S M, PAM4 UL: 104.625 M PAM2,234.375/281.25M DME	DL: 5625*S Mbps, PAM4 UL: 234.375 Mbps DME	DL: 5625*S Mbps, PAM4 UL: 234.375 Mbps DME	DL 10Gbps: 5625 Mbps, PAM4 DL 5Gbps: 5625 Mbps, PAM2 DL 2.5Gbps: 2812.5Mbps, PAM2 UL: 234.375 Mbps DME	DL 10Gbps: 5625 Mbps, PAM4 DL 5Gbps: 5625 Mbps, PAM2 DL 2.5Gbps: 2812.5Mbps, PAM2 UL: 234.375 Mbps DME	DL: 5625*S Mbps, PAM4 UL: 5625*S Mbps, PAM4
STP Transmit power	DL: 0dBm UL: -6dBm	DL: 0dBm UL: -6dBm	DL: 0dBm UL: 0dBm	10Gbps = -1 ~ 2 (dBm) 5Gbps = -1 ~ 2 (dBm) 2.5Gbps = -4 ~ -1 (dBm) 100Mbps = -3 ~ 0 (dBm)	10Gbps = -1 ~ 2 (dBm) 5Gbps = -1 ~ 2 (dBm) 2.5Gbps = -4 ~ -1 (dBm) 100Mbps = -3 ~ 0 (dBm)	0dBm
FEC	DL: 10bit RS – 360,326 UL: 5bit –RS – 2 FECs	DL: 10bit – RS – 360,326 UL: 6bit – RS – 50,46	DL: 10bit RS 360,326 UL: 6bit – RS – 50,46	DL: 10bit – RS – 360,326 UL: 6bit – RS – 50,46	DL: 10bit – RS – 360,326 UL: 6bit – RS – 50,46	DL: 10bit – RS – 360,326 UL: 10bit – RS – 360,326
Line coding	DL: 64b/65b UL: 2 types	DL: 64b/65b UL: 16b/17b	64b/65b	64b/65b	64b/65b	64b/[illegible]
OAM bits	DL: 10 UL: none/2	DL: 10 UL: 4	DL: 10 UL: ? (16 reserved bits)	DL: 10 UL: 10 (+ 6 reserved bits)	DL: 10 UL: 10 (+ 6 reserved bits)	[illegible]
synchronize start of training	Not defined	Not defined	Not defined	Not defined	Link Sync (changi[illegible] No Auto-Ne[illegible]	[illegible]
EEE capability	No	No	No	No	[illegible]	[illegible]

ACT and 802.3ch have fundamental differences in startup [illegible]

IEEE 802.3dm – September 2025, Minneapolis [illegible]

Will come back to in Future

Not enough time



Comments

Misleading: This is a implementation decision and not a part of PAR

PHYs are fixed during production

Why would display and camera ports be changing in production? This is a physical link and PHY would be optimized per customer application

This is the whole advantage of 802.3dm over 802.3ch

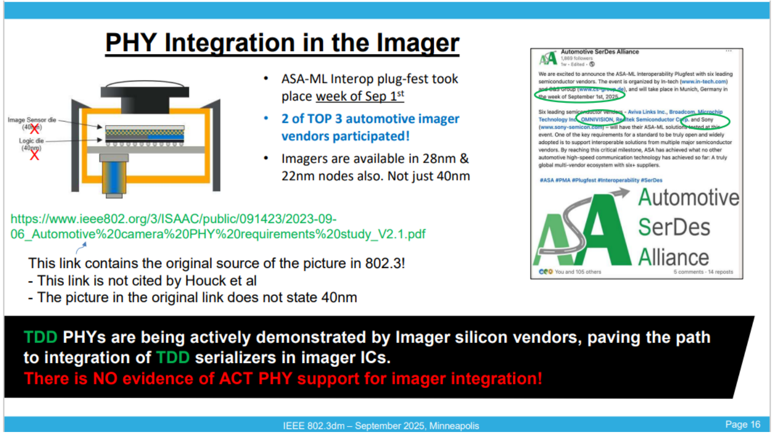
Incorrect: This is a disadvantage for TDD when comparing optimized ACT product

TDD – 2 x FAST TX/RX PHYs capable of 12Gbps – More die size compared to ACT not cost competitive to ACT now

ACT 1 x FAST RX and 1 x FAST TX

Misleading: TDD has 1 additional FAST TX and FAST RX per PHY with this application

This is a large increase in die size will double the die size of an ACT optimized PHY



Incorrect, corrections needed

Misleading: TDD is not ASA – why is information of another standard's plugfest shown in 802.3dm is this appropriate for IEEE?

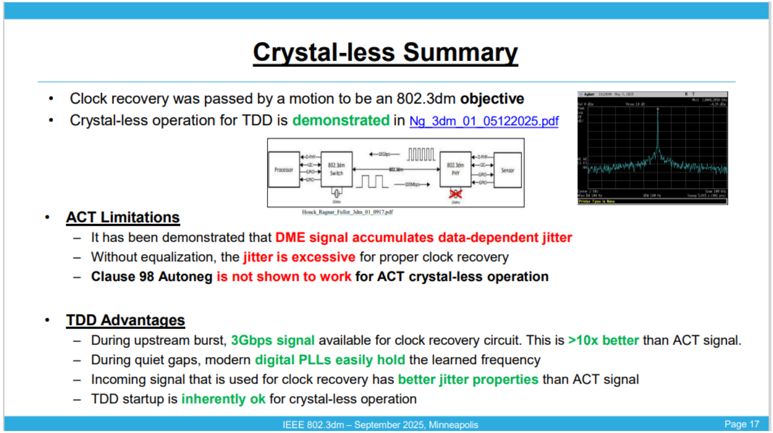
Information on how ASA MLE is not TDD:
Evolution of 802.3dm: From GMSLE to ACT and Beyond

TDD = Timing Driven
ASA = Protocol Driven

Incorrect: ASA-ML has not been proposed to 802.3dm only ASA MLE

Incorrect: ASA ML/ASA MLE and TDD are not interoperable
Does TDD PHY proposed in 802.3dm operate with ASA-ML parts?

Slides 4, 5, 6, and 7 describe this relationship
Evolution of 802.3dm: From GMSLE to ACT and Beyond

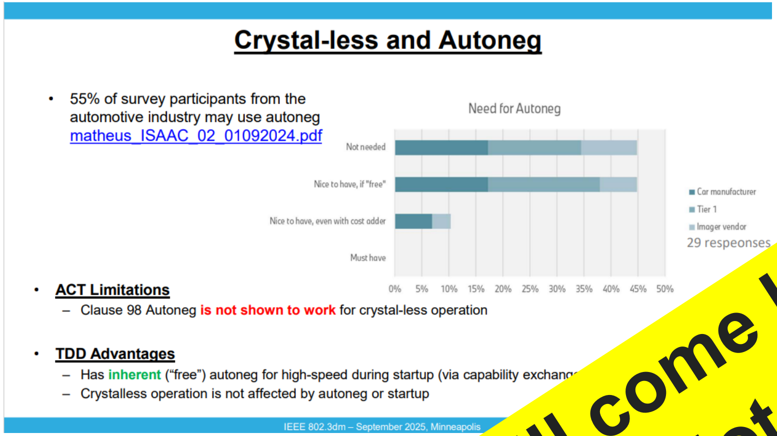


Incorrect, corrections needed

Incorrect: Differential Manchester Encoded (DME) modulation is a mature and robust method which has been used for decades in communications

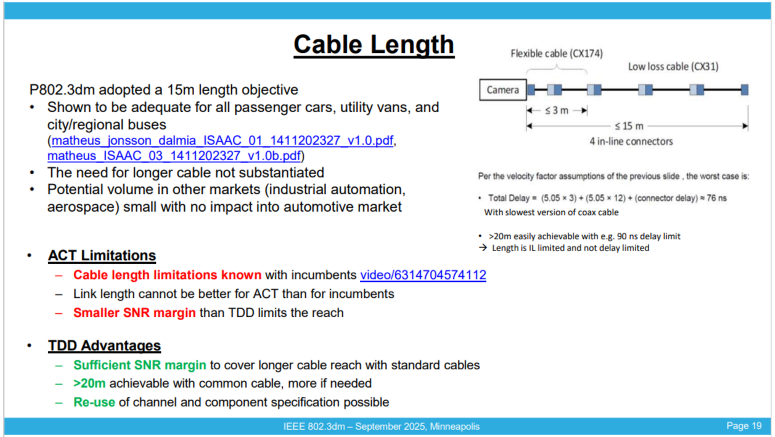
Incorrect: Clause 98 is an optional part of the ACT proposal and has nothing to do with ACT crystal-less operation

Incorrect: Incoming signal does not have better jitter properties than a DME ACT signal with proper timing recovery.



Incorrect, correction needed

Will come back to in Future
Not enough time



Incorrect, corrections needed

Incorrect: SNR does not cover the Link Delay issues as described in the comparison presentation.

Incorrect: Collisions will occur – **Slide 5** comparison table under Long Cable Length

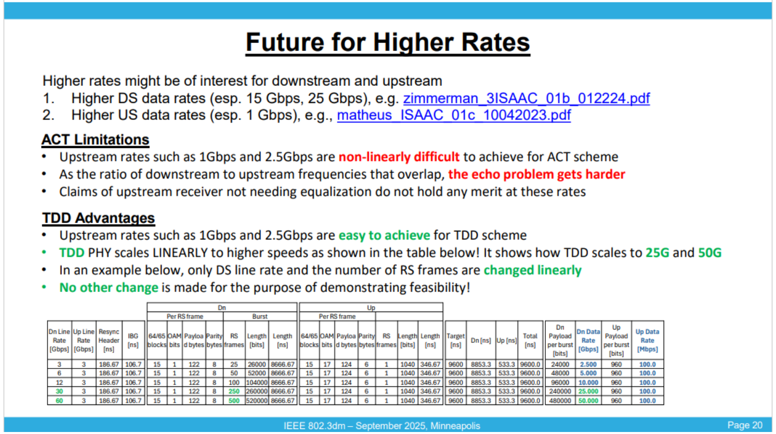
https://ieee802.org/3/dm/public/adhoc/062625/jonsson_3dm_01_06_26_25.pdf

Incorrect: Both references do not provide data disagreeing with 15meters

Only referenced for BMW X5, X6, X7 – Where is the market data for other vehicles? This only shows 11m's

Misleading: hogenmuller_01_0512.pdf requests 40 meters for commercial vehicles – which is reference on **slide 4**

https://www.ieee802.org/3/ISAAC/public/1123/matheus_jonsson_dalmia_ISAAC_01_1411202327_v1.0.pdf



Future for Higher Rates

Higher rates might be of interest for downstream and upstream
1. Higher DS data rates (esp. 15 Gbps, 25 Gbps), e.g. zimmerman_3ISAAC_01b_012224.pdf
2. Higher US data rates (esp. 1 Gbps), e.g., matheus_ISAAC_01c_10042023.pdf

ACT Limitations
- Upstream rates such as 1Gbps and 2.5Gbps are **non-linearly difficult** to achieve for ACT scheme
- As the ratio of downstream to upstream frequencies that overlap, **the echo problem gets harder**
- Claims of upstream receiver not needing equalization do not hold any merit at these rates

TDD Advantages
- Upstream rates such as 1Gbps and 2.5Gbps are **easy to achieve** for TDD scheme
- **TDD** PHY scales LINEARLY to higher speeds as shown in the table below! It shows how TDD scales to **25G** and **50G**
- In an example below, only DS line rate and the number of RS frames are **changed linearly**
- **No other change** is made for the purpose of demonstrating feasibility!

				Dn							Up														
				Per RS frame				Burst			Per RS frame														
Dn Line Rate [Gbps]	Up Line Rate [Gbps]	Resync Header [ns]	IBG [ns]	64/65 blocks	OAM bits	Payload bytes	Parity bytes	RS frames	Length [bits]	Length [ns]	64/65 blocks	OAM bits	Payload bytes	Parity bytes	RS frames	Length [bits]	Length [ns]	Target [ns]	Dn [ns]	Up [ns]	Total [ns]	Dn Payload per burst [bits]	Dn Data Rate [Gbps]	Up Payload per burst [bits]	Up Data Rate [Mbps]
3	3	186.67	106.7	15	1	122	8	25	26000	8666.67	15	17	124	6	1	1040	346.67	9600	8853.3	533.3	9600.0	24000	2.500	960	100.0
6	3	186.67	106.7	15	1	122	8	50	52000	8666.67	15	17	124	6	1	1040	346.67	9600	8853.3	533.3	9600.0	48000	5.000	960	100.0
12	3	186.67	106.7	15	1	122	8	100	104000	8666.67	15	17	124	6	1	1040	346.67	9600	8853.3	533.3	9600.0	96000	10.000	960	100.0
30	3	186.67	106.7	15	1	122	8	250	260000	8666.67	15	17	124	6	1	1040	346.67	9600	8853.3	533.3	9600.0	240000	25.000	960	100.0
60	3	186.67	106.7	15	1	122	8	500	520000	8666.67	15	17	124	6	1	1040	346.67	9600	8853.3	533.3	9600.0	480000	50.000	960	100.0

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Incorrect, corrections needed

Incorrect: Ignored the IBGs

See presentation breakdown that describes this behavior **Page 16** https://www.ieee802.org/3/dm/public/0725/Houck_Cordaro_3dm_01b_07292025.pdf

Incorrect: 30Gbps Downlink = 23.89Gbps payload
8.6667/9.6 = 0.90278

0.90278 x 64/65 x 122/130 = 0.83231 x 30Gbps = 25.03Gbps

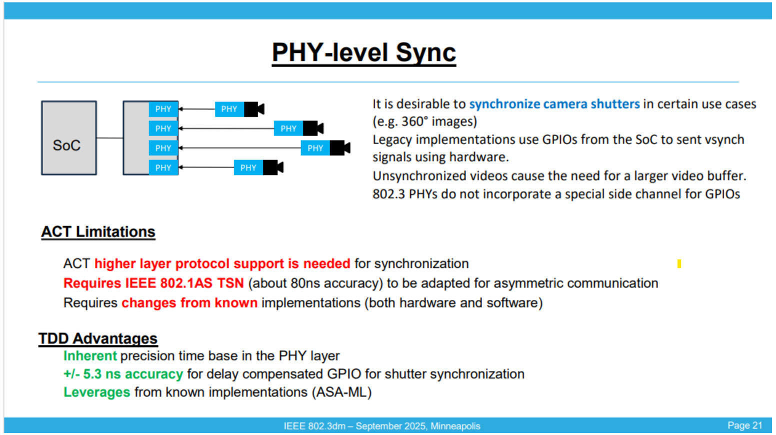
Now with Overhead included = 30Gbps x 0.79644 = 23.89Gbps

25Gbps/0.79644 = 31.38Gbps total bandwidth

Incorrect: 1Gbps is currently not apart of the PAR

Misleading: Echo is hard for both TDD and ACT at 25Gbps

TDD will likely have to change IBG to allow more frequency content to settle – Meaning not compatible with 2.5/5.0/10Gbps timing



Incorrect, corrections needed

Delay compensation is a feature that can be implemented in ACT. SERDES accomplishes delay compensation without TSN

This is a implementation decision and not a part of the 802.3dm PAR

This is not unique to TDD – this is copied from SERDES which invented this feature

ACT does not require hardware and software changes it has built in low latency behavior

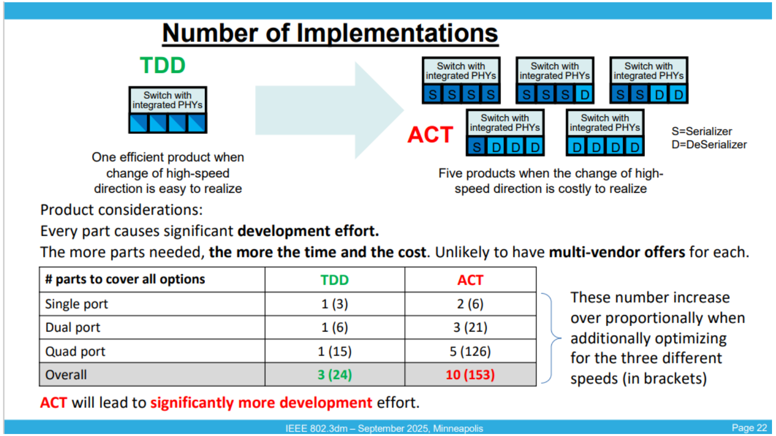
Incorrect: TSN is not required for ACT

Incorrect: ACT GPIOs are fast acting stated last September (Hamburg) and was the reason ASA-MLE did not move forward and TDD is now proposed, due to latency issues.

Review entire presentation for history on latency in 802.3dm: https://www.ieee802.org/3/dm/public/0924/Houck_Fuller_3dm_03_0917.pdf

Where did the 5.3ns accuracy come from? No link or calculation or method explaining.

No reasoning behind why this is needed for customers and more importantly why the standard needs this



Incorrect, corrections needed

Misleading: This is a implementation decision

Misleading: All the ACT dies are far more competitive in price than the TDD PHY as mentioned in previous slide

Misleading: This is an implementation decision not an advantage

Incorrect: This is a disadvantage when comparing optimized product

TDD – 2 x FAST TX/RX PHYs capable of 12Gbps – More die size compared to ACT not cost competitive to ACT now

ACT 1 x FAST RX and 1 x FAST TX

Eco-System Summary

- Conformance & interoperability PHY specification are only the first step for wide market adoption. A fully established eco-system is required to successfully deploy a particular technology in automotive market.
- This eco-system comprises (among other)
  - a physical layer specification,
  - silicon availability (multi-vendor solution),
  - test houses (conformance, interoperability, and EMC testing),
  - testability (multiple test equipment vendors),
  - channel & components (cable, connector, magnetic vendors) and EMC test specification
- **ACT Limitations**
  - **No** available eco-system to leverage from
  - **New** channel and component specifications required
  - **Few communalities** between proprietary SerDes and ACT (different Baud rate, different US modulation)
- **TDD Advantages**
  - Eco-system **available**
  - **Re-use** of channel & component as well as EMC specification
  - **6+ vendors with extensive experience**

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Incorrect, corrections needed

Incorrect: ASA has not been proposed to 802.3dm - no 802.3dm proposed TDD has a working PHY

Misleading: ASA and TDD are not interoperable – there has been no proposal on this

Does TDD PHY proposed in 802.3dm operate with ASA parts?

Slides 4, 5, 6, and 7 describe this relationship
Evolution of 802.3dm: From GMSLE to ACT and Beyond

Summary

	TDD	ACT
Crystal-less	Demonstrated	Breaks auto-negotiation
EMC	Proven robust	Incomplete disclosure suggests real issues
Power, Size, Complexity	Suited to the application	Higher DS latency, no on-demand EEE possible
Higher speed	Lowest complexity (simple scaling)	Requires complete overhaul
Cable Length	Supports objective of >15meters with higher SNR margin	Lower SNR margin
Interoperability	Proven interop between 5 vendors for TDD-based ASA-ML	No
Integration	Proven support from imager vendors	No evidence of support
PHY-level SYNC	Inherently built into TDD	Not Defined
Ecosystem	Exists to leverage from	Years behind
Number of Implementations	Optimal for creating variants of chips needed to serve the market	Unreasonably large number of chips needed to serve applications

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Incorrect, corrections needed

Incorrect and Misleading: Requires update to table with corrections discussed above

Thank You