192.13 Protocol implementation conformance statement (PICS) proforma for Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1[1]

192.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

192.13.2 Identification

192.13.2.1 Implementation identification

Supplier[1]	
Contact point for inquiries about the PICS[1]	
Implementation Name(s) and Version(s)[1,3]	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2]	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

[1]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

192.13.2.1

192.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3dm-202x, Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [ ] Yes [ ] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

192.13.2.2

192.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*OAM	MultiGBASE-A OAM capability	192.3.7	Supports MultiGBASE-A OAM frame exchange function	O	Yes [ ] No [ ]
*MDIO	Support of MDIO capability	45.1	Register and interface support	O	Yes [ ] No [ ]
*PHY-T1	MultiGBASE-AT1 capability	192.1.1	Supports MultiGBASE-AT1 operation	O/1a	Yes [ ] No [ ]
*PHY-V1	MultiGBASE-AV1 capability	192.1.1	Supports MultiGBASE-AV1 operation	O/1a	Yes [ ] No [ ]
~~*7.5GTX~~	~~7.5 Gb/s transmit MAC data rate~~	~~192.1.1~~	~~Supports 7.5 Gb/s mode of operation, PHY_S~~	~~O~~	~~Yes [ ] No [ ]~~
~~*10GTX~~	~~10 Gb/s transmit MAC data rate~~	~~192.1.1~~	~~Supports 10 Gb/s mode of operation, PHY_S~~	~~O~~	~~Yes [ ] No [ ]~~
~~*10GRX~~	~~10 Gb/s receive MAC data rate~~	~~192.1.1~~	~~Supports 10 Gb/s mode of operation, PHY_D~~	~~O~~	~~Yes [ ] No [ ]~~

*INS-LS, T1	Installation/link segment, -T1	192.7	Items marked with INS-LS, T1 include installation and cabling specifications for link segments and are not applicable to a PHY manufacturer	~~O~~PHY-T1:M	Yes [ ] No [ ]
*INS-LS, V1	Installation/link segment, -V1	192.8	Items marked with INS-LS, V1 include installation and cabling specifications for link segments and are not applicable to a PHY manufacturer	~~O~~PHY-V1:M	Yes [ ] No [ ]
*MGAL	MultiGBASE-A Leader capability	192.1	Supports MultiGBASE-A Leader operation	O.1b	Yes [ ] No [ ]
*MGAF	MultiGBASE-A Follower capability	192.1	Supports MultiGBASE-A Follower operation	O.1b	Yes [ ] No [ ]
*PHY_D	PHY_D capability	192.1.1	Supports PHY_D mode of operation	O.1c	Yes [ ] No [ ]
*PHY_S	PHY_S capability	192.1.1	Supports PHY_S mode of operation	O.1c	Yes [ ] No [ ]
*TX100M	100 Mb/s transmit MAC data rate	192.1.1	Supports transmit MAC data rate of 100 Mb/s	PHY_D:M	Yes [ ] No [ ]
*RX100M	100 Mb/s receive MAC data rate	192.1.1	Supports receive MAC data rate of 100 Mb/s	PHY_S:M	Yes [ ] No [ ]

*TX2.5G	2.5 Gb/s transmit MAC data rate	192.1.1	Supports transmit MAC data rate of 2.5 Gb/s	PHY_S: O.1d	Yes [ ] No [ ]
*TX5G	5 Gb/s transmit MAC data rate	192.1.1	Supports transmit MAC data rate of 5 Gb/s	PHY_S: O.1d	Yes [ ] No [ ]
*TX7.5G	7.5 Gb/s transmit MAC data rate	192.1.1	Supports transmit MAC data rate of 7.5 Gb/s	PHY_S: O.1d	Yes [ ] No [ ]
*TX10G	10 Gb/s transmit MAC data rate	192.1.1	Supports transmit MAC data rate of 10 Gb/s	PHY_S: O.1d	Yes [ ] No [ ]
*RX2.5G	2.5 Gb/s receive MAC data rate	192.1.1	Supports receive MAC data rate of 2.5 Gb/s	PHY_D: O.1e	Yes [ ] No [ ]
*RX5G	5 Gb/s receive MAC data rate	192.1.1	Supports receive MAC data rate of 5 Gb/s	PHY_D: O.1e	Yes [ ] No [ ]
*RX7.5G	7.5 Gb/s receive MAC data rate	192.1.1	Supports receive MAC data rate of 7.5 Gb/s	PHY_D: O.1e	Yes [ ] No [ ]
*RX10G	10 Gb/s receive MAC data rate	192.1.1	Supports receive MAC data rate of 10 Gb/s	PHY_D: O.1e	Yes [ ] No [ ]

192.13.3

192.13.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

192.13.4.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS Reset	192.3.2.1	Meets requirements 192.3.2.1	M	Yes [ ]
PCST2	Control and management interface restoration	192.3.2.1	Restored to operation within 10 ms from the setting of bit 3.2322.15	M	Yes [ ]
PCST3	LS_TX PCS Transmit compliance	192.3.2.2	Conforms to the PCS 64B/65B Transmit state diagram in Figure 192–22 and to the PCS Transmit bit ordering in Figure 192–5 ~~and Figure 192–6~~	PHY_D:M	Yes [ ]
PCST3a	HS_TX PCS Transmit compliance	192.3.2.2	Conforms to the PCS 64B/65B Transmit state diagram in Figure 192–22 and to the PCS Transmit bit ordering in Figure 192–6	PHY_S:M	Yes [ ]
PCST4	PMA_TXMODE.indication message SEND_Z value	192.3.2.2	PCS Transmit passes Z symbols at each symbol period to the PMA via the PMA_UNITDATA.request primitive	M	Yes [ ]
PCST5	PMA_TXMODE.indication message SEND_TS or SEND_TA value	192.3.2.2	PCS Transmit generates the O_n sequence defined in 192.3.4 to the PMA via the PMA_UNITDATA.request primitive	M	Yes [ ]
PCST6	PMA_TXMODE.indication message SEND_N value	192.3.2.2	The PCS is in the data mode of operation and the PCS Transmit function uses a 65B coding technique to generate code-groups that represent data or control	M	Yes [ ]

PCST7	Idle /I/ insertion and deletion	192.3.2.2.7	Occurs in groups of four. /I/s may not be added while data is being received. The first four characters after a /T/ are not be deleted when deleting /I/s.	M	Yes [ ]
PCST8	RS-FEC (LS) encoding	192.3.2.2.13	Takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and generates the six 8-bit parity symbols (48 bits total)	PHY_D:M	Yes [ ]
PCST9	RS-FEC (HS) encoding	192.3.2.2.13	Takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and generates the six 8-bit parity symbols (48 bits total)	PHY_S:M	Yes [ ]
PCST10	Transmitter interleaving depth, L	192.3.2.2.14	Round-robin interleaving scheme shown in Figure 192–8 is applied	PHY_S:M	Yes [ ]
PCST11	Transmitter interleaving depth, L > 1	192.3.2.2.14	Predefined for each data rate and complies with Table 192–4	M	Yes [ ]
PCST12	Superframe aggregation	192.3.2.2.14	HS_TX PCS Transmit aggregates L RS-FEC input frames into an interleaved RS-FEC input	PHY_S:M	Yes [ ]
PCST13	Scrambled refresh header data bit	192.3.2.2.17	See Equation (192–4)	M	Yes [ ]
PCST14	PRBS11 scrambler polynomial	192.3.2.2.18	The PRBS11 pattern generator produces the same result as the implementation shown in Figure 192–10	M	Yes [ ]
PCST15	PRBS11 scrambler state rule	192.3.2.2.18	Scrambler state is never initialized to all zeros	M	Yes [ ]
PCST16	PRBS11 scrambler continuity	192.3.2.2.18	Once started, during PMA training, the scrambler continues to run uninterrupted during the refresh headers of each frame	M	Yes [ ]

PCST17	PRBS11 scrambler stop rule	192.3.2.2.18	Once started, during PMA training, the scrambler stops during the burst payload field and QUIET	M	Yes [ ]
PCST18	PRBS33 scrambler polynomial, Leader	192.3.2.2.19	PCS Transmit uses Equation (192–9) as the transmitter scrambler generator polynomial superframe	MGAL:M	Yes [ ]
PCST19	PRBS33 scrambler polynomial, Follower	192.3.2.2.19	PCS Transmit uses Equation (192–10) as the transmitter scrambler generator polynomial superframe	MGAF:M	Yes [ ]
PCST20	PRBS33 scrambler state rule	192.3.2.2.19	Scrambler state is never initialized to all zeros	M	Yes [ ]
PCST21	PRBS33 scrambler continuity	192.3.2.2.19	Once started, during PMA training, the scrambler continues to run uninterrupted during the payload of PMA training frames and data mode frames	M	Yes [ ]
PCST22	PRBS33 scrambler stop rule	192.3.2.2.19	Once started, during PMA training, the scrambler stops during QUIET and refresh headers	M	Yes [ ]
PCST23	Gray mapping (Tx) for PAM4	192.3.2.2.20	See 192.3.2.2.20	TX10G~~TX~~:M	Yes [ ] N/A [ ]
PCST24	Gray mapping (Rx) for PAM4	192.3.2.2.20	See 192.3.2.2.20	RX10G~~R X~~:M	Yes [ ]
PCST25	PAM4 (Tx)	192.3.2.2.21	See 192.3.2.2.21	TX10G~~TX~~:M	Yes [ ]
PCST26	PAM3 (Tx)	192.3.2.2.22	See 192.3.2.2.22	TX7.5G~~T X~~:M	Yes [ ]

192.13.4.1

192.13.4.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support

PCSR1	LS_RX PCS Receive compliance	192.3.2.3	Conforms to the PCS 64B/65B Receive state diagram in Figure 192–23 and the PCS Receive bit ordering in Figure 192–12~~ for the LS_RX and Figure 192–13 for the HS_RX,~~ including compliance with the associated state variable as specified in 192.3.5.1.2	PHY_S: M	Yes [ ]
PCSR1a	HS_RX PCS Receive compliance	192.3.2.3	Conforms to the PCS 64B/65B Receive state diagram in Figure 192–23 and the PCS Receive bit ordering in Figure 192–13 including compliance with the associated state variable as specified in 192.3.5.1.2	PHY_D: M	Yes [ ]
PCST2	Frame and block synchronization	192.3.2.3.1	The receiving PCS concatenates rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload according to its data mode (see 192.3.2.3.1)	M	Yes [ ]
PCST3	Descrambler, Leader	192.3.2.3.2	The Leader PHY uses the receiver descrambler generator polynomial in Equation (192–10)	MGAL: M	Yes [ ]
PCST4	Descrambler, Follower	192.3.2.3.2	The Follower PHY shall uses the receiver descrambler generator polynomial in Equation (192–9)	MGAF: M	Yes [ ]
PCST5	RS-FEC parity bit integrity check	192.3.2.3.3	The PCS Receive function checks the integrity of the RS-FEC parity bits defined in 192.3.2.2.13	M	Yes [ ]

192.13.4.2

192.13.4.3 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	SEND_TS frequency	192.3.4	Uses a symmetric frame format and transmits at 3 GBd	M	Yes [ ]

PCS2	33-bit scrambler operation	192.3.4	Once started at the beginning of the training payload of the first training burst, continues to run uninterrupted for each symbol during all subsequent payloads and maintains its last state during the QUIET period and refresh headers	M	Yes [ ]
PCS3	Refresh header content	192.3.4.2	Composed of a leading sequence of zeros followed by four bytes of 0x01, followed by four bytes of 0xF0	M	Yes [ ]
PCS4	Scrambler synchronization acquisition and reporting	192.3.4.4	The PCS acquires descrambler state synchronization to the PAM2 training sequence and reports success through scr_status, and continues to use the synchronized state in all subsequent bursts in both data and training modes	M	Yes [ ]
PCS5	DECODE function rule	192.3.5.1.3	Decodes the block as specified in 192.3.2.2.4	M	Yes [ ]
PCS6	ENCODE function rule	192.3.5.1.3	Encodes the block as specified in 192.3.2.2.4	M	Yes [ ]
PCS7	PCS functions	192.3.5.2	Performs the functions of RFER monitor, Transmit, and Receive as shown in Figure 192–21, Figure 192–22, and Figure 192–23	M	Yes [ ]

192.13.4.3

192.13.4.4 OAM

Item	Feature	Subclause	Value/Comment	Status	Support
OAM1	State diagram behavior	192.3.7.4	Conforms to Figure 192–25 and Figure 192–26	OAM:M	Yes [ ] N/A [ ]
OAM2	HS_TX mode OAM frame structure, first bit	192.3.7.2.1	The first bit of the first OAM symbol (OAM<0>) is inserted in the first RS frame in the first superframe of the TDD burst	OAM:M	Yes [ ] N/A [ ]

OAM3	HS_TX mode OAM frame structure, subsequent bits	192.3.7.2.1	One subsequent bit of OAM<0> is inserted into each of second through tenth RS FEC frames	OAM:M	Yes [ ] N/A [ ]
OAM4	LS_TX mode OAM frame structure	192.3.7.2.1	The first symbol (OAM<0>) is inserted in the first ten bits of the OAM field of the RS frame so that one OAM symbols is carried in each TDD burst	OAM:M	Yes [ ] N/A [ ]
OAM5	When OAM is not implemented	192.3.7.2.1	10-bit OAM field is set to all zeros	OAM:M	Yes [ ] N/A [ ]
OAM6	OAM frame data	192.3.7.2.1	Reserved fields are set to zero	OAM:M	Yes [ ] N/A [ ]
OAM7	MultiGBASE-A OAM Frame acceptance criteria	192.3.7.2.13	See 192.3.7.2.13	OAM:M	Yes [ ] N/A [ ]
OAM8	mr_tx_received	192.3.7.4.3	Clear on read	OAM:M	Yes [ ] N/A [ ]

192.13.4.4

192.13.4.5 Physical Medium Attachment (PMA)

192.13.4.5.1 PMA Reset

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	PMA Reset function	192.4.2.1	See 192.4.2.1	M	Yes [ ]

192.13.4.5.1

192.13.4.5.2 PMA Transmit

Item	Feature	Subclause	Value/Comment	Status	Support

PMAT1	PMA Transmit operation	192.4.2.2	Continuously transmits pulses modulated by the symbols given by tx_symb onto the MDI, followed by a QUIET period to complete a TDD cycle, when the PHY Control state diagram (see Figure 192–31) is not in the DISABLE_TRANSMITTER state	M	Yes [ ]
PMAT2	PMA Transmit signal compliance	192.4.2.2	Complies with the electrical specifications given in 192.5.2	M	Yes [ ]
PMAT3	Clock source, Leader	192.4.2.2	The transmit symbol clock TX_TCLK is sourced from a local clock source, while meeting the transmit jitter requirements of 192.5.2.3, when the management parameter config is LEADER	MGAL: M	Yes [ ]
PMAT4	Loop timing	192.4.2.2	The Leader-Follower relationship include loops timing	MGAF: M	Yes [ ]
PMAT5	Clock source, Follower	192.4.2.2	The transmit symbol clock TX_TCLK is sourced from the recovered clock of 192.4.2.6, while meeting the jitter requirements of 192.5.2.3, when the management parameter config is FOLLOWER	MGAF: M	Yes [ ]
PMAT6	Transmit fault function mapping	192.4.2.2	Mapped to the transmit fault bit, as specified in 45.2.1.7.4, if the MDIO interface is implemented	MDIO: M	Yes [ ]
PMAT7	Launch power disable	192.3.2.2.1	The average launch power of the transmitter is as specified in 192.5.2.4 when the PMA_transmit_disable variable is set to TRUE and the value of tx_symb is Z	M	Yes [ ]

192.13.4.5.2

192.13.4.5.3 PMA Receive

Item	Feature	Subclause	Value/Comment	Status	Support

PMAR1	PMA Receive FEC error rate	192.4.2.3	RFER of less than 2×10^{-10} after RS-FEC decoding~~See 192.4.2.3~~	M	Yes [ ]
PMAR2	Status constraint	192.4.2.3	The reception of Z symbols during the TDD QUIET period alone does not trigger setting loc_rcvr_status to NOT_OK	M	Yes [ ]
PMAR3	Receive fault function mapping	192.4.2.3	Contributed to the receive fault bit specified in 45.2.1.7.5, if the MDIO interface is implemented	MDIO: M	Yes [ ]

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192.13.4.5.3

192.13.4.5.4 PHY Control

Item	Feature	Subclause	Value/Comment	Status	Support
CNTRL	PHY control compliance	192.4.2.4	Complies with the state diagram in Figure 192–31	M	Yes [ ]

192.13.4.5.4

192.13.4.5.5 Infofield

Item	Feature	Subclause	Value/Comment	Status	Support
IF1	12-octet Infofield fields	192.4.2.4	Include the fields in 192.4.2.4.2 through 192.4.2.4.8 as shown in Figure 192–28 and Figure 192–29	M	Yes [ ]
IF2	Infofield transmission	192.4.2.4	Transmit Infofield at least 16 times with each change to octets 7 to 10 when PMA_state = 00	M	Yes [ ]
IF3	Infofield reserved bits	192.4.2.4.1	Unused values are set to zero on transmit and ignored when received by the link partner	M	Yes [ ]
IF4	Infofield start of frame delimiter	192.4.2.4.2	Uses the hexadecimal value 0xBBA700	M	Yes [ ]

192.13.4.5.5

192.13.4.5.6 Message Field

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	PMA state communication	192.4.2.4.4	Bits PMA_state<7:6> communicate the state of the transmitting transceiver to the link partner	M	Yes [ ]
MF2	Training phase signal	192.4.2.4.4	Bits training_phase<4:3> communicate the training phase of the transmitting transceiver to the link partner	M	Yes [ ]
MF3	Invalid value transmission	192.4.2.4.4	Values not listed in Table 192–13 for the Leader or Follower are not transmitted and ignored at the receiver	M	Yes [ ]
MF4	Initial Message Field setting	192.4.2.4.4	The Message Field setting for the first transmitted PMA burst is the first row of Table 192–13 for the Leader, and the first or second row of Table 192–10 for the Follower	M	Yes [ ]
MF5	Next Message Field	192.4.2.4.4	Is the same Message Field setting or the Message Field setting corresponding to a row below the current setting in Table 192–13	M	Yes [ ]

192.13.4.5.6

192.13.4.5.7 PHY capability

Item	Feature	Subclause	Value/Comment	Status	Support
CAP1	OAM capability enable	192.4.2.4.5	Enabled only if both PHYs set the capability bit OAMen=1	~~O~~M	Yes [ ]
CAP2	OAM capability validity	192.4.2.4.5	Valid only when loc_rcvr_status<5> bit is one	~~O~~M	Yes [ ]

192.13.4.5.7

192.13.4.5.8 TDD delay counter

Item	Feature	Subclause	Value/Comment	Status	Support
DLY1	Delay counter rule	192.4.2.4.6	delay_count set to a value between 0 to 63 and the delay_count_valid bit set to one after the Leader detects the Follower TDD burst position and estimates the link segment delay	MGAL: M	Yes [ ]
DLY2	Delay count acceptance	192.4.2.4.6	The Follower accepts the received remote delay_count only when received remote delay_count_valid bit is set to one	MGAF: M	Yes [ ]
DLY3	Delay count storage	192.4.2.4.6	The Follower stores delay_count number	MGAF: M	Yes [ ]
DLY4	Delay acknowledgment	192.4.2.4.6	The Follower sends back its own delay_count field as acknowledgment of delay_count reception, and set its delay_count_valid to one	MGAF: M	Yes [ ]
DLY5	Negotiation success rule	192.4.2.4.6	The Leader or the Follower sets negotiation_done to OK when it finishes the exchange of delay count and the negotiated data rates	M	Yes [ ]
DLY6	Follower burst adjustment	192.4.2.4.6	The Follower adjusts its transmit burst position according to the stored delay_count, starting from Asymmetric training and continuing through to the data mode	MGAF: M	Yes [ ]

192.13.4.5.8

192.13.4.5.9 Phase switch

Item	Feature	Subclause	Value/Comment	Status	Support

PS1	PhaseSwBC24 burst count	192.4.2.4.7	A minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state	M	Yes [ ]

192.13.4.5.9

192.13.4.5.10 CRC16

Item	Feature	Subclause	Value/Comment	Status	Support
CRC1	CRC16 Infofield	192.4.2.4.9	Implements the CRC16 polynomial (x + 1)(x15 + x + 1) of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>	M	Yes [ ]
CRC2	CRC16 verification	192.4.2.4.9	Produces the same result as the implementation shown in Figure 192–30	M	Yes [ ]
CRC3	CRC16 initialization	192.4.2.4.9	The 16 delay elements in Figure 192–30 are initialized to zero	M	Yes [ ]

192.13.4.5.10

192.13.4.5.11 Startup

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	Startup sequence compliance	192.4.2.4.11	Complies with the state diagram description given in Figure 192–31	M	Yes [ ]
ST2	TRAINING0 alignment	192.4.2.4.11	The first symbol of the Follower's transmit PMA training frame at the transmit MDI is aligned at 400 ± 1 transmit symbols after arrival of the last PMA training payload symbol from the Leader at the Follower input MDI	MGAF: M	Yes [ ]

ST3	Alignment maintenance	192.4.2.4.11	The Follower maintains alignment while in the TRAINING0 and COUNTDOWN0 (i.e., while tx_mode = SEND_TS) states	MGAF: M	Yes [ ]
ST4	TRAINING1 alignment	192.4.2.4.11	The Follower uses the Leader transmitted delay_count to align its transmit PMA training frame to be 17 ns – delay_count × 5.333 ns (± 5.333 ns) after the last PMA training payload symbol from the Leader appears on the Follower input MDI	MGAF: M	Yes [ ]
ST5	Alignment maintenance	192.4.2.4.11	The Follower maintains its alignment while tx_mode is SEND_TA or SEND_N	MGAF: M	Yes [ ]

192.13.4.5.11

192.13.4.5.12 Link monitor

Item	Feature	Subclause	Value/Comment	Status	Support
LM1	Link Monitor function compliance	192.4.2.5	Complies with the state diagram of Figure 192–33	M	Yes [ ]

192.13.4.5.12

192.13.4.5.13 Clock recovery

Item	Feature	Subclause	Value/Comment	Status	Support
CR1	Clock Recovery function	192.4.2.6	Provides a clock suitable for signal sampling so that the RFER indicated in 192.4.2.3 is achieved	M	Yes [ ]

192.13.4.5.13

192.13.4.6 MDI signals

Item	Feature	Subclause	Value/Comment	Status	Support
MDIS1	MDI symbol response compliance	192.4.3.1	Complies with the electrical specifications given in 192.5.2	M	Yes [ ]

192.13.4.6

192.13.4.7 Timers

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	link_fail_timer expiration	192.4.4.2	Expires 97.5 ms ± 5 ms after being started	M	Yes [ ]
TIM2	minwait_timer expiration	192.4.4.2	Expires 975 µs ± 50 µs after being started	M	Yes [ ]
TIM3	tdd_watchdog_timer expiration	192.4.4.2	Expires 96 µs ± 5 µs after being started	M	Yes [ ]

192.13.4.7

192.13.4.8 PMA electrical specifications

192.13.4.8.1 Test modes

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Test modes	192.5.1	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes [ ]
TM2	Enable test modes	192.5.1	Enable by setting control register, 1.2313.15:13 as described in 192.5.1 when MDIO implemented; enabling of test modes is provided otherwise when MDIO is not implemented	MDIO: M	Yes [ ]

TM3	Test mode operation	192.5.1	Test modes only change data symbols provided to the transmitter circuitry	M	Yes [ ]
TM4	Test mode 1	192.5.1	When enabled, PHY provides access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5	M	Yes [ ]
TM5	Test mode 2	192.5.1	When enabled, PHY transmits a continuous repeating pattern of {+1, –1} symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference	M	Yes [ ]
TM6	Test mode 4, PAM2 mode at 3 GBd	192.5.1	When enabled, PHY transmits the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16). All PHYs support transmission of this signal at 3 GBd. ~~PHYs that support 5 Gb/s, and 7.5 Gb/s, and 10 Gb/s transmit rates support transmission of this signal at 6 GBd.~~	M	Yes [ ]
TM6a	Test mode 4, PAM2 mode at 6 GBd	192.5.1	When enabled, PHY transmits the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 5 Gb/s, and 7.5 Gb/s, and 10 Gb/s transmit rates support transmission of this signal at 6 GBd.	TX5G:M TX7.5G: M TX10G: M	Yes [ ]
TM7	Test mode 4, PAM3 mode	192.5.1	When enabled, PHY transmits the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 7.5 Gb/s transmit rates support transmission of this signal at 6 GBd.	TX7.5G: M	Yes [ ]
TM8	Test mode 4, PAM4 mode	192.5.1	When enabled, PHY transmits the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 10 Gb/s transmit rates support transmission of this signal at 6 GBd.	TX10G: M	Yes [ ]

TM9	Test mode 5	192.5.1	When enabled, PHY transmits continuously with no QUIET period or refresh header and with transmit signal level corresponding to the data mode of operation	M	Yes [ ]
TM10	Test mode 6	192.5.1	When enabled, PHY transmits a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source	M	Yes [ ]

192.13.4.8.1

192.13.4.8.2 Transmitter Electrical Specifications

Item	Feature	Subclause	Value/Comment	Status	Support
~~PMAT1~~ TES1	Coupling	192.5.2	Electrical input is ac-coupled	M	Yes [ ]
~~PMAT2~~ TES2	Transmitter electrical specifications	192.5.2	Meets requirements of 192.5.2	M	Yes [ ]
~~PMAT3~~ TES3	Transmitter output droop	192.5.2.1	Less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing, when measured in test mode 6 using transmitter test fixture 1 or test fixture 3	M	Yes [ ]
~~PMAT4~~ TES4	Captured block length and sampling	192.5.2.2	At least 4000 transmitted symbols long and sampled with a minimum of 10x oversampling	M	Yes [ ]
~~PMAT5~~ TES5	Transmitter peak distortion	192.5.2.2	Less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM4 transmitters, measured at a minimum of ten equally spaced phases of a single symbol period	M	Yes [ ]

~~PMAT6~~ TES6	RMS jitter, Leader mode	192.5.2.3	Less than 1 ps when supporting 10 Gb/s, less than 1.5 ps when supporting 7.5 Gb/s, less than 2 ps when supporting 5 Gb/s, and less than 4 ps when supporting 2.5 Gb/s for jitter frequencies greater than 100 kHz, measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1	MGAL: M	Yes [ ]
~~PMAT7~~ TES7	Time Interval Error, Leader mode	192.5.2.3	Less than 10 ps when supporting 10 Gb/s, less than 15 ps when supporting 7.5 Gb/s, less than 20 ps when supporting 5 Gb/s, and less than 40 ps when supporting 2.5 Gb/s, measured in test mode 1 using test fixture 2 over a period of 100 ms	MGAL: M	Yes [ ]
~~PMAT8~~ TES8	RMS jitter, Follower mode	192.5.2.3	Less than 1 ps when supporting 10 Gb/s, less than 1.5 ps when supporting 7.5 Gb/s, less than 2 ps when supporting 5 Gb/s, and less than 4 ps when supporting 2.5 Gb/s for jitter frequencies greater than 1 MHz, measured in test mode 1	MGAF: M	Yes [ ]
~~PMAT9~~ TES9	Time Interval Error, Follower mode	192.5.2.3	Less than 15 ps when supporting 10 Gb/s, less than 22.5 ps when supporting 7.5 Gb/s, less than 30 ps when supporting 5 Gb/s, and less than 60 ps when supporting 2.5 Gb/s, measured in test mode 1 over 50 overlapping periods of 10 ms	MGAF: M	Yes [ ]
~~PMAT10~~ TES10	Transmitter power levels	192.5.2.4	In the range of values specified in Table 192–22 when using the PSD measurement test fixture	M	Yes [ ]
~~PMAT11~~ TES11	MDI transmit signal	192.5.2.4	Nominally zero and less than -36 dBm for frequencies greater 10 MHz	M	Yes [ ]
~~PMAT12~~ TES12	Transmitter power spectral density, -T1	192.5.2.4	Between the upper mask specified in Equation (192–17) and the lower mask specified in Equation (192–18), measured into a 100 Ω differential load using test fixture 1	*PHY-T1:M	Yes [ ] N/A [ ]

TES13	Transmitter power spectral density, -V1	192.5.2.4	Between the upper mask specified in Equation (192–17) lowered by 3dB and the lower mask specified in Equation (192–18) lowered by 3dB, measured into a 50 Ω load using test fixture 3	*PHY-V1:M	Yes [ ] N/A [ ]
~~PMAT13~~ TES14	Symbol transmission rate	192.5.2.6	Within the range of $6 \times S$ GBd ± 100 ppm with drift less than 1 ppm/sec	M	Yes [ ]
~~PMAT14~~ TES15	Recovered symbol rate	192.5.2.6	Within ± 10 ppm of the recovered clock used by the Follower	MGAF: M	Yes [ ]

192.13.4.8.2

192.13.4.8.3 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	Bit error rate, -T1	192.5.3.1	Less than 10^{-12} after RS-FEC decoding	*PHY-T1:M	Yes [ ] N/A [ ]
PMAR2	Bit error rate, -V1	192.5.3.1	Less than 10^{-12} after RS-FEC decoding	*PHY-V1:M	Yes [ ] N/A [ ]

192.13.4.8.3

192.13.4.9 Link segment

192.13.4.9.1 Link segment characteristics, -T1

Item	Feature	Subclause	Value/Comment	Status	Support
LST1	Insertion loss, -T1	192.7.1.1	Meets requirements of 192.7.1.1	INS-LS, T1:M	Yes [ ] N/A [ ]
LST2	Return loss, -T1	192.7.1.3	Meets requirements of 192.7.1.3	INS-LS, T1:M	Yes [ ] N/A [ ]
LST3	Coupling attenuation, -T1	192.7.1.4	Meets requirements of 192.7.1.4	INS-LS, T1:M	Yes [ ] N/A [ ]
LST4	Screening attenuation, -T1	192.7.1.5	Meets requirements of 192.7.1.5	INS-LS, T1:M	Yes [ ] N/A [ ]
LST5	Propagation delay, -T1	192.7.1.6	Not more than 160 ns for all frequencies between 10 MHz and 5 GHz	INS-LS, T1:M	Yes [ ] N/A [ ]
LST6	PSANEXT loss, -T1	192.7.2.1	Meets requirements of 192.7.2.1	INS-LS, T1:M	Yes [ ] N/A [ ]
LST7	PSAACRF, -T1	192.7.2.2	Meets requirements of 192.7.2.2	INS-LS, T1:M	Yes [ ] N/A [ ]

192.13.4.9.1

192.13.4.9.2 Link segment characteristics, -V1

Item	Feature	Subclause	Value/Comment	Status	Support
LSV1	Insertion loss, -V1	192.8.1.1	Meets requirements of 192.8.1.1	INS-LS, V1:M	Yes [ ] N/A [ ]
LSV2	Return loss, -V1	192.8.1.3	Meets requirements of 192.8.1.3	INS-LS, V1:M	Yes [ ] N/A [ ]
LST3	Screening attenuation, -V1	192.8.1.5	Measured in accordance with ISO 19642–11 and meets requirements of 192.8.1.5	INS-LS, V1:M	Yes [ ] N/A [ ]
LST4	Propagation delay, -V1	192.8.1.6	Not more than 160 ns for all frequencies between 10 MHz and 5 GHz	INS-LS, V1:M	Yes [ ] N/A [ ]

LST5	Coupling parameter test methodologies, -V1	192.8.2	Applied with adaptation to unbalanced coaxial cabling and using a 50 Ω termination to ground	INS-LS, V1:M	Yes [ ] N/A [ ]
LST6	PSANEXT loss, -V1	192.8.2.1	Meets requirements of 192.8.2.1	INS-LS, V1:M	Yes [ ] N/A [ ]
LST7	PSAACRF, -V1	192.8.2.2	Meets requirements of 192.8.2.2	INS-LS, V1:M	Yes [ ] N/A [ ]

192.13.4.9.2

192.13.4.10 MDI

192.13.4.10.1 MDI specification, -T1

Item	Feature	Subclause	Value/Comment	Status	Support
MDIT1	Electrical requirements, -T1	192.9.2	Electrical requirements are for when a PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors	*PHY-T1:M	Yes [ ] N/A [ ]
MDIT2	Return loss, -T1	192.9.2.1	For each transmitter/receiver, measured with a nominal impedance of 50 Ω	*PHY-T1:M	Yes [ ] N/A [ ]
MDIT3	Fault tolerance, -T1	192.9.3	Meets requirements of 96.8.3	*PHY-T1:M	Yes [ ] N/A [ ]

192.13.4.10.1

192.13.4.10.2 MDI specification, -V1

Item	Feature	Subclause	Value/Comment	Status	Support
MDIV1	Electrical requirements, -V1	192.10.2	Electrical requirement are for when a PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable	*PHY-V1:M	Yes [ ] N/A [ ]

MDIV2	Return loss, -V1	192.10.2.1	For each transmitter/receiver, measured with a nominal impedance of 50 Ω	*PHY-V1:M	Yes [ ] N/A [ ]
MDIT3	Fault tolerance, -V1	192.10.3	MDI coaxial cable interface withstands, without damage, 50 V dc with the source current limited to 150 mA. Normal operation resumes after all short circuits are removed. Single MDI conductor withstands, without damage, high-voltage transient noises and ESD per application requirements.	*PHY-V1:M	Yes [ ] N/A [ ]

192.13.4.10.2

192.13.4.11 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Delay constraints	192.12	Complies with Table 192–27	M	Yes [ ]

192.13.4.11