

IEEE P802.3dm™/D2.1, 30th July 2026
(Amendment of IEEE Std 802.3™-2022 as amended by [list to be populated during publication process])

IEEE P802.3dm™/D2.1

Draft Standard for Ethernet Amendment 14: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet

Prepared by the
LAN/MAN Standards Committee
of the
IEEE Computer Society

This draft is an amendment of IEEE Std 802.3-2022 as amended by IEEE Std 802.3dd-2022, IEEE Std 802.3cs-2022, IEEE Std 802.3db-2022, IEEE Std 802.3ck-2022, IEEE Std 802.3de-2022, IEEE Std 802.3cx-2023, IEEE Std 802.3cz-2023, IEEE Std 802.3cy-2023, IEEE Std 802.3df-2024, IEEE Std 802.3da-2026, IEEE Std 802.3dk-2026, IEEE Std 802.3dg-2026, and IEEE Std 802.3dj-202x. This amendment adds Physical Layer (PHY) specifications and management parameters for 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation in one direction and 100 Gb/s operation in the other direction on automotive cabling in an automotive environment. Draft D2.1 is prepared for Working Group ballot recirculation. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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Abstract: This amendment to IEEE Std 802.3-2022 adds Physical Layer (PHY) specifications and management parameters for 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation in one direction and ~~100 Mb/s~~ operation in the other direction on automotive cabling in an automotive environment.

Keywords: 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1, automotive Ethernet, IEEE 802.3dm™, MultiGBASE-AT1, MultiGBASE-AV1

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Introduction

This introduction is not part of IEEE Std 802.3dm-20xx, IEEE Draft Standard for Ethernet. Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet.

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3dm-202x publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN)

through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

IEEE Std 802.3cy™-2023

Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and Annex 165A. This amendment adds Physical Layer specifications and management parameters for operation at 25 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3df™-2024

Amendment 9—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment includes Physical Layer specifications and management parameters for 400 Gb/s and 800 Gb/s operation.

IEEE Std 802.3-2022/Cor 1-2024

Corrigendum 1—This corrigendum includes changes to IEEE Std 802.3-2022 to correct the MDI return loss specifications in Clause 149 and Clause 165.

IEEE Std 802.3da™-2026

Amendment 10—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 188 through Clause 189. This amendment adds Physical Layer specifications and management parameters for enhancement of multidrop 10 Mb/s operation based on the 10BASE-T1S PHY specified in Clause 147 of IEEE Std 802.3-2022, and specifies optional provision of power over single balanced pair mixing segments. Additionally, this amendment includes additions and changes to Clause 148 to automatically allocate node IDs (Dynamic PLCA).

IEEE Std 802.3dk™-2026

Amendment 11—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 168. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s Ethernet optical interfaces for bidirectional operation over a single strand of single-mode fiber.

IEEE Std 802.3dg™-2026

Amendment 12—This amendment to IEEE Std 802.3-2022 specifies additions and appropriate modifications to add 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation, and associated optional provision of power, over a single balanced pair of conductors.

IEEE Std 802.3dj™-20xx

Amendment 13—This amendment includes changes to IEEE Std 802.3-2022, and adds Clause 174 through Clause 187 and Annex 174A through Annex 186A. This amendment includes Physical Layer specifications and management parameters for 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s operation.

IEEE Std 802.3-2022/Cor 2-20xx

Corrigendum 2—This corrigendum includes changes to IEEE Std 802.3-2022 to correct the normalization factors used for the Transmitter Distortion Figure Of Merit (TDFOM) calculation in Clause 166.

IEEE Std 802.3dm™-20xx

Amendment 13—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 191, Clause 192, Annex 191A, and Annex 191B. This amendment adds Physical Layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s (Clause 192 only) and 10 Gb/s operation in one direction and ~~100 Mb/s~~ operation in the other direction over a single balanced pair of conductors, or over a single coaxial cable.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

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Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet

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1. Introduction

1.1 Overview

1.1.3 Architectural perspectives

1.1.3.2 Compatibility interfaces

Change 1.1.3.2 list item f) as follows:

- f) *10 Gigabit Media Independent Interface (XGMII).* The XGMII is designed to connect a 2.5 Gb/s, 5 Gb/s, or 10 Gb/s capable MAC to a PHY of the same rate, or to an asymmetric PHY that supports 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s in the other. While conformance with implementation of this interface is not necessary to ensure communication, it allows maximum flexibility in intermixing PHYs and DTEs at 2.5 Gb/s, 5 Gb/s, and 10 Gb/s speeds. The XGMII is intended for use as a chip-to-chip interface. No mechanical connector is specified for use with the XGMII. The XGMII is optional.

1.3 Normative references

Insert the following references in alphanumeric order:

ISO 19642–11:2023, Road vehicles—Automotive cables—Part 11: Dimensions and requirements for coaxial RF cables with a specified analogue bandwidth up to 6 GHz (20 GHz).

1.4 Definitions

Insert the following new definitions after 1.4.46 100 Gb/s Parallel Physical Interface (CPPI):

1.4.46a 100M+10GBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 100 Mb/s and reception at 10 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191 and 191.9.)

1.4.46b 100M+10GBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 100 Mb/s and reception at 10 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191 and 191.10.)

1.4.46c 100M+2.5GBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 100 Mb/s and reception at 2.5 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191 and 191.9.)

1.4.46d 100M+2.5GBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 100 Mb/s and reception at 2.5 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191 and 191.10.)

1.4.46e 100M+5GBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 100 Mb/s and reception at 5 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191 and 191.9.)

1.4.46f 100M+5GBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 100 Mb/s and reception at 5 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191 and 191.10.)

1.4.46g 100M+MultiGBASE: PHYs that belong to the set of specific asymmetric PHYs that transmit at 100 Mb/s and receive at speeds in excess of 1000 Mb/s, with concurrent transmission in both directions, including 100M+2.5GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-T1, 100M+5GBASE-V1, 100M+10GBASE-T1, and 100M+10GBASE-V1. (See IEEE Std 802.3, Clause 191.)

Insert the following new definitions after 1.4.62 10BROAD36:

1.4.62a 10G+100MBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 10 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191 and 191.9.)

1.4.62b 10G+100MBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 10 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191 and 191.10.)

Change 1.4.88 as follows:

1.4.88 10 Gigabit Media Independent Interface (XGMII): The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the other direction). (See IEEE Std 802.3, Clause 46.)

Insert the following new definitions after 1.4.95 1G-EPON:

1.4.95a 2.5G+100MBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 2.5 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191 and 191.9.)

1.4.95b 2.5G+100MBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 2.5 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191 and 191.10.)

Insert the following new definitions after 1.4.178 50G-EPON:

1.4.178a 5G+100MBASE-T1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 5 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191 and 191.9.)

1.4.178b 5G+100MBASE-V1: IEEE 802.3 Physical Layer specification for an asymmetric full duplex Ethernet Physical Layer for point-to-point transmission at 5 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191 and 191.10.)

Change 1.4.249 as follows:

1.4.249 coaxial cable interface: The electrical and mechanical interface to the ~~shared~~ coaxial cable medium either contained within or connected to the Medium Attachment Unit (MAU). Also known as the Medium Dependent Interface (MDI).

Insert the following new definitions after 1.4.405c Multidrop Power Sourcing Equipment (MPSE) (as modified by IEEE Std 802.3da-2026):

1.4.405d MultiG+100MBASE: PHYs that belong to the set of specific asymmetric PHYs that transmit at speeds in excess of 1000 Mb/s and receive at 100 Mb/s, with concurrent transmission in both directions,

including 2.5G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-T1, 5G+100MBASE-V1, 10G+100MBASE-T1, and 10G+100MBASE-V1. (See IEEE Std 802.3, Clause 191.)

1.4.405e MultiG+100MBASE/100M+MultiGBASE: PHYs that belong to the set of specific asymmetric PHYs that transmit or received at speeds in excess of 1000 Mb/s and receive or transmit at 100 Mb/s, with concurrent transmission in both directions, including 2.5G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-T1, 5G+100MBASE-V1, 10G+100MBASE-T1, 10G+100MBASE-V1, 100M+2.5GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-T1, 100M+5GBASE-V1, 100M+10GBASE-T1, and 100M+10GBASE-V1. (See IEEE Std 802.3, Clause 191.)

1.4.405f MultiGBASE-A: PHYs that belong to the set of specific asymmetric PHYs that transmit at speeds in excess of 1000 Mb/s in one direction and less than or equal to 1000 Mb/s in the other direction, with the direction of asymmetry and high-speed rate determined at link startup for at least one transmission rate, including MultiGBASE-AT1 and MultiGBASE-AV1. (See IEEE Std 802.3, Clause 192.)

1.4.405g MultiGBASE-AT1: IEEE 802.3 Physical Layer specification for an asymmetric rate Ethernet full duplex point-to-point link operating at 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s in the other direction, with the direction of asymmetry and high-speed rate determined at link startup for at least one transmission rate, over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 192.)

1.4.405h MultiGBASE-AV1: IEEE 802.3 Physical Layer specification for an asymmetric rate Ethernet full duplex point-to-point link operating at 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s in the other direction, with the direction of asymmetry and high-speed rate determined at link startup for at least one transmission rate, over a single coaxial conductor. (See IEEE Std 802.3, Clause 192.)

1.5 Abbreviations

Insert the following new abbreviations into the list, in alphanumeric order:

TDD	time-division duplex
SNDR	signal-to-noise-and-distortion ratio

30. Management

30.3 Layer management for DTEs

30.3.2 PHY device managed object class

30.3.2.1 PHY device attributes

30.3.2.1.2 aPhyType

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “2.5GBASE-T1” as follows:

2.5G+100MBASE-T1/V1	Clause 191 2.5 Gb/s PAM2 transmit, 100 Mb/s DME receive
100M+2.5GBASE-T1/V1	Clause 191 100 Mb/s DME transmit, 2.5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “5GBASE-T1” as follows:

5G+100MBASE-T1/V1	Clause 191 5 Gb/s PAM2, 100 Mb/s DME receive
100M+5GBASE-T1/V1	Clause 191 100 Mb/s DME transmit, 5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “10GBASE-T1” as follows:

10G+100MBASE-T1/V1	Clause 191 10 Gb/s PAM4, 100 Mb/s DME receive
100M+10GBASE-T1/V1	Clause 191 100 Mb/s DME transmit, 10 Gb/s PAM4 receive

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for “400GBASE-R” as follows:

MultiGBASE-A	Clause 192 MultiG PAM2, PAM3, or PAM4 HS_PATH, ~~100 Mb/s~~ PAM2 LS_PATH

30.3.2.1.3 aPhyTypeList

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “2.5GBASE-T1” as follows:

2.5G+100MBASE-T1/V1	Clause 191 2.5 Gb/s PAM2 transmit, 100 Mb/s DME receive
100M+2.5GBASE-T1/V1	Clause 191 100 Mb/s DME transmit, 2.5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “5GBASE-T1” as follows:

5G+100MBASE-T1/V1	Clause 191 5 Gb/s PAM2, 100 Mb/s DME receive
100M+5GBASE-T1/V1	Clause 191 100 Mb/s DME transmit, 5 Gb/s PAM2 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “10GBASE-T1” as follows:

10G+100MBASE-T1/V1	Clause 191 10 Gb/s PAM4, 100 Mb/s DME receive
100M+10GBASE-T1/V1	Clause 191 100 Mb/s DME transmit, 10 Gb/s PAM4 receive

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for “400GBASE-R” as follows:

MultiGBASE-A PAM2 LS_PATH	Clause 192 MultiG PAM2, PAM3, or PAM4 HS_PATH, ~~100-Mb/s~~

30.5 Layer management for medium attachment units (MAUs)

30.5.1 MAU managed object class

30.5.1.1 MAU attributes

30.5.1.1.2 aMAUType

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “2.5GBASE-T1” as follows:

2.5G+100MBASE-T1	Single balanced pair of conductors PHY as specified in Clause 191
100M+2.5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 191
2.5G+100MBASE-V1	Coaxial Cable PHY as specified in Clause 191
100M+2.5GBASE-V1	Coaxial Cable PHY as specified in Clause 191

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “5GBASE-T1” as follows:

5G+100MBASE-T1	Single balanced pair of conductors PHY as specified in Clause 191
100M+5GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 191
5G+100MBASE-V1	Coaxial Cable PHY as specified in Clause 191
100M+5GBASE-V1	Coaxial Cable PHY as specified in Clause 191

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “10GBASE-T1” as follows:

10G+100MBASE-T1	Single balanced pair of conductors PHY as specified in Clause 191
100M+10GBASE-T1	Single balanced pair of conductors PHY as specified in Clause 191

10G+100MBASE-V1	Coaxial Cable PHY as specified in Clause 191
100M+10GBASE-V1	Coaxial Cable PHY as specified in Clause 191

Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for “802.9a” as follows:

MultiGBASE-AT1	Single balanced pair of conductors PHY as specified in Clause 192
MultiGBASE-AV1	Coaxial Cable PHY as specified in Clause 192

30.6 Management for link Auto-Negotiation

30.6.1 Auto-Negotiation managed object class

30.6.1.1 Auto-Negotiation attributes

30.6.1.1.5 aAutoNegLocalTechnologyAbility

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for “2.5GBASE-T1” as follows:

2.5G+100MBASE-T1	2.5G+100MBASE-T1 as specified in Clause 191
100M+2.5GBASE-T1	100M+2.5GBASE-T1 as specified in Clause 191
2.5G+100MBASE-V1	2.5G+100MBASE-V1 as specified in Clause 191
100M+2.5GBASE-V1	100M+2.5GBASE-V1 as specified in Clause 191

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for “5GBASE-T1” as follows:

5G+100MBASE-T1	5G+100MBASE-T1 as specified in Clause 191
100M+5GBASE-T1	100M+5GBASE-T1 as specified in Clause 191
5G+100MBASE-V1	5G+100MBASE-V1 as specified in Clause 191
100M+5GBASE-V1	100M+5GBASE-V1 as specified in Clause 191

Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for “10GBASE-T1” as follows:

10G+100MBASE-T1	10G+100MBASE-T1 as specified in Clause 191
100M+10GBASE-T1	100M+10GBASE-T1 as specified in Clause 191
10G+100MBASE-V1	10G+100MBASE-V1 as specified in Clause 191
100M+10GBASE-V1	100M+10GBASE-V1 as specified in Clause 191

45. Management Data Input/Output (MDIO) Interface

45.2 MDIO Interface Registers

45.2.1 PMA/PMD registers

Change the reserved row for 1.77 through 1.79 in Table 45-3 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, and IEEE Std 802.3dj-20xx); insert new row for 1.77; insert the superscript “b” for a footnote (shown as “a” as it can’t be changed), and associated footnote, to 1.2309 through 1.2317; insert new rows for 1.2318, 1.2319, and 1.2320; and change the reserved row for 1.2318 through 1.2400 (as modified by IEEE Std 802.3dj-20xx) as follows (unchanged rows not shown):

Table 45–3—PMA/PMD registers

Register address	Register name	Subclause
...		
<u>1.77</u>	<u>Asymmetrical BASE-T1/V1 PMA/PMD extended ability</u>	<u>45.2.1.60f</u>
~~1.77~~ <u>78</u> through 1.79	Reserved	
...		
1.2309	MultiGBASE-T1 PMA control ^a	45.2.1.242
1.2310	MultiGBASE-T1 PMA status ^a	45.2.1.243
1.2311	MultiGBASE-T1 training ^a	45.2.1.244
1.2312	MultiGBASE-T1 link partner training ^a	45.2.1.245
1.2313	MultiGBASE-T1 test mode control ^a	45.2.1.246
1.2314	MultiGBASE-T1 SNR operating margin ^a	45.2.1.247
1.2315	MultiGBASE-T1 minimum SNR margin ^a	45.2.1.248
1.2316	MultiGBASE-T1 user defined data ^a	45.2.1.249
1.2317	MultiGBASE-T1 link partner user defined data ^a	45.2.1.250
<u>1.2318</u>	<u>MultiGBASE-A PMA rate ability</u>	<u>45.2.1.250a</u>
<u>1.2319</u>	<u>MultiGBASE-A PMA rate negotiation</u>	<u>45.2.1.250b</u>
<u>1.2320</u>	<u>MultiGBASE-A PMA link partner rate negotiation</u>	<u>45.2.1.250c</u>
<u>1.2321 through 1.2400</u> ~~1.2318 through 1.2400~~		
...		

^aThis register also applies to MultiG type -V1 PHYs.

45.2.1.6 PMA/PMD control 2 register (Register 1.7)

Change Table 45-7 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, IEEE Std 802.3dk-2026, and IEEE Std 802.3dj-20xx) as follows (unchanged table rows and most unchanged bit description lines not shown):

Table 45-7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.7.7:0	PMA/PMD type selection	7 6 5 4 3 2 1 0 ... 0 0 1 1 1 1 0 1 = BASE-T1/ <u>V1</u> PMA/PMD ^b ...	R/W
...			

^aR/W = Read/Write, RO = Read only.

^bIf BASE-T1/V1 is selected, bits 1.2100.34:0 are used to differentiate which BASE-T1/V1 PMA/PMD is selected.

45.2.1.7 PMA/PMD status 2 register (Register 1.8)

45.2.1.7.4 Transmit fault (1.8.11)

Insert new rows in Table 45-9 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1, and insert a new row at the end of the table, as follows (unchanged rows not shown):

Table 45-9—Transmit fault description location

PMA/PMD	Description location
...	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	191.5.2.2
100M+2.5GBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-V1, 100M+10GBASE-V1	191.5.2.2
...	
MultiGBASE-AT1, MultiGBASE-AV1	192.4.2.2

45.2.1.7.5 Receive fault (1.8.10)

Insert new rows in Table 45-10 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as

follows and insert a new row at the end of the table (unchanged rows not shown):

Table 45–10—Receive fault description location

PMA/PMD	Description location
...	
2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1	191.5.2.3
100M+2.5GBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-V1, 100M+10GBASE-V1	191.5.2.3
...	
MultiGBASE-AT1, MultiGBASE-AV1	192.4.2.3

45.2.1.10 PMA/PMD extended ability register (Register 1.11)

Change the row for 1.11.11 in Table 45-19 as follows (unchanged rows not shown):

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.11.11	BASE-T1/ <u>V1</u> extended abilities	1 = PMA/PMD has BASE-T1/ <u>V1</u> extended abilities listed in register 1.18 0 = PMA/PMD does not have BASE-T1/ <u>V1</u> extended abilities	RO
...			

^aRO = Read only.

Change the title of 45.2.10.5 and the text as follows:

45.2.1.10.5 BASE-T1/V1 extended abilities (1.11.11)

When read as a one, bit 1.11.11 indicates that the PMA/PMD has BASE-T1/V1 extended abilities listed in register 1.18. When read as a zero, bit 1.11.11 indicates that the PMA/PMD does not have BASE-T1/V1 extended abilities.

Change the title of the following subsection as shown:

45.2.1.16 BASE-T1/V1 PMA/PMD extended ability register (1.18)

Change the title of the Table 45-19, change row 2 and insert new rows 3 and 4 (as modified by IEEE Std 802.3cy-2023, IEEE Std 802.3da-2026, and IEEE Std 802.3dg-2026) as follows (unchanged rows not shown)

Table 45-19—BASE-T1/V1 PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.18.15:12 40	Reserved	Value always 0	RO
1.18.11	MultiGBASE-AT1/AV1 ability	1 = PMA/PMD is able to perform MultiGBASE-AT1/AV1 0 = PMA/PMD is not able to perform MultiGBASE-AT1/AV1	RO
1.18.10	MultiG+100M/ 100M+MultiGBASE- T1/V1 ability	1 = PMA/PMD is able to perform MultiG+100M/100M+MultiGBASE-V1 ability 0 = PMA/PMD is able to perform MultiG+100M/100M+MultiGBASE-T1	RO
...			

^aRO = Read only.

Insert 45.2.1.16.aaaa and 45.1.16.aaab before 45.2.1.16.aaa (as inserted by IEEE Std 802.3dg-2026) as follows:

45.2.1.16.aaaa MultiGBASE-AT1/AV1 ability (1.18.11)

When read as a one, bit 1.18.11 indicates that the PMA/PMD is able to operate as a MultiGBASE-AT1/AV1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.11 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AT1/AV1 PMA/PMD type as indicated in register 1.77.

45.2.1.16.aaab MultiG+100M/100M+MultiGBASE-T1/V1 ability (1.18.10)

When read as a one, bit 1.18.10 indicates that the PMA/PMD is able to operate as a MultiG+100M/100M+MultiGBASE-V1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.10 indicates that the PMA/PMD is able to operate as a MultiG+100M/100M+MultiGBASE-T1 PMA/PMD type as indicated in register 1.77.

Insert 45.2.1.60f, 45.2.1.60f.x, and table 45-58f after 45.2.1.60e (as inserted by IEEE Std 802.3dj-202x) as follows:

45.2.1.60f Asymmetric PMA/PMD extended ability register (Register 1.77)

The assignment of bits in the Asymmetric PMA/PMD extended ability register is shown in Table 45-58f.

Table 45–58f—Asymmetric PMA/PMD extended ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.77.15:14	Reserved	Value always 0	RO
1.77.13	MultiGBASE-AV1 ability	1 = PMA/PMD is able to perform MultiGBASE-AV1 0 = PMA/PMD is not able to perform MultiGBASE-AV1	RO
1.77.12	MultiGBASE-AT1 ability	1 = PMA/PMD is able to perform MultiGBASE-AT1 0 = PMA/PMD is not able to perform MultiGBASE-AT1	RO
1.77.11	10G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-V1 0 = PMA/PMD is not able to perform 10G+100MBASE-V1	RO
1.77.10	100M+10GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-V1 0 = PMA/PMD is not able to perform 100M+10GBASE-V1	RO
1.77.9	10G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 10G+100MBASE-T1 0 = PMA/PMD is not able to perform 10G+100MBASE-T1	RO
1.77.8	100M+10GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+10GBASE-T1 0 = PMA/PMD is not able to perform 100M+10GBASE-T1	RO
1.77.7	5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-V1 0 = PMA/PMD is not able to perform 5G+100MBASE-V1	RO
1.77.6	100M+5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-V1 0 = PMA/PMD is not able to perform 100M+5GBASE-V1	RO
1.77.5	5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 5G+100MBASE-T1 0 = PMA/PMD is not able to perform 5G+100MBASE-T1	RO
1.77.4	100M+5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+5GBASE-T1 0 = PMA/PMD is not able to perform 100M+5GBASE-T1	RO
1.77.3	2.5G+100MBASE-V1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-V1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-V1	RO
1.77.2	100M+2.5GBASE-V1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-V1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-V1	RO
1.77.1	2.5G+100MBASE-T1 ability	1 = PMA/PMD is able to perform 2.5G+100MBASE-T1 0 = PMA/PMD is not able to perform 2.5G+100MBASE-T1	RO
1.77.0	100M+2.5GBASE-T1 ability	1 = PMA/PMD is able to perform 100M+2.5GBASE-T1 0 = PMA/PMD is not able to perform 100M+2.5GBASE-T1	RO

^aR/W = Read/Write, RO = Read only

45.2.1.60f.1 MultiGBASE-AV1 (1.77.13)

When read as a one, bit 1.77.13 indicates that the PMA/PMD is able to operate as a MultiGBASE-AV1 PMA/PMD type.

When read as a zero, bit 1.77.13 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AV1 PMA/PMD type.

45.2.1.60f.2 MultiGBASE-AT1 (1.77.12)

When read as a one, bit 1.77.12 indicates that the PMA/PMD is able to operate as a MultiGBASE-AT1 PMA/PMD type.

When read as a zero, bit 1.77.12 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AT1 PMA/PMD type.

45.2.1.60f.3 10G+100MBASE-V1 (1.77.11)

When read as a one, bit 1.77.11 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.11 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-V1 PMA/PMD type.

45.2.1.60f.4 100M+10GBASE-V1 (1.77.10)

When read as a one, bit 1.77.10 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.10 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-V1 PMA/PMD type.

45.2.1.60f.5 10G+100MBASE-T1 (1.77.9)

When read as a one, bit 1.77.9 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.9 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-T1 PMA/PMD type.

45.2.1.60f.6 100M+10GBASE-T1 (1.77.8)

When read as a one, bit 1.77.8 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.8 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-T1 PMA/PMD type.

45.2.1.60f.7 5G+100MBASE-V1 (1.77.7)

When read as a one, bit 1.77.7 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.7 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-V1 PMA/PMD type.

45.2.1.60f.8 100M+5GBASE-V1 (1.77.6)

When read as a one, bit 1.77.6 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.6 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-V1 PMA/PMD type.

45.2.1.60f.9 5G+100MBASE-T1 (1.77.5)

When read as a one, bit 1.77.5 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.5 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-T1 PMA/PMD type.

45.2.1.60f.10 100M+5GBASE-T1 (1.77.4)

When read as a one, bit 1.77.4 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.4 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-T1 PMA/PMD type.

45.2.1.60f.11 2.5G+100MBASE-V1 (1.77.3)

When read as a one, bit 1.77.3 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.3 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-V1 PMA/PMD type.

45.2.1.60f.12 100M+2.5GBASE-V1 (1.77.2)

When read as a one, bit 1.77.2 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.2 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-V1 PMA/PMD type.

45.2.1.60f.13 2.5G+100MBASE-T1 (1.77.1)

When read as a one, bit 1.77.1 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.1 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-T1 PMA/PMD type.

45.2.1.60f.14 100M+2.5GBASE-T1 (1.77.0)

When read as a one, bit 1.77.0 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.0 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-T1 PMA/PMD type.

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Change the title of the following subsection as shown:

45.2.1.214 BASE-T1/V1 PMA/PMD control register (Register 1.2100)

Change the title of the following table as shown. In Table 45–178, replace the rows for bits 1.2100.13:4 and 1.2100.3:0, with the rows for bits 1.2100.13:5 and 1.2100.4:0 (as modified by IEEE Std 802.3cy-2023 and IEEE Std 802.3da-2026) as follows (unchanged rows not shown):

Table 45–178—BASE-T1/V1 PMA/PMD control register bit definitions

Bit(s)	Name	Description	R/W ^a
...			
1.2100.13:5	Reserved	Value always 0	RO
1.2100.4:0	Type Selection	4 3 2 1 0 1 1 1 1 1 = MultiGBASE-AV1 1 1 1 1 0 = MultiGBASE-AT1 1 1 1 0 x = Reserved 1 1 0 1 1 = 10G+100MBASE-V1 1 1 0 1 0 = 100M+10GBASE-V1 1 1 0 0 1 = 10G+100MBASE-T1 1 1 0 0 0 = 100M+10GBASE-T1 1 0 1 1 1 = 5G+100MBASE-V1 1 0 1 1 0 = 100M+5GBASE-V1 1 0 1 0 1 = 5G+100MBASE-T1 1 0 1 0 0 = 100M+5GBASE-T1 1 0 0 1 1 = 2.5G+100MBASE-V1 1 0 0 1 0 = 100M+2.5GBASE-V1 1 0 0 0 1 = 2.5G+100MBASE-T1 1 0 0 0 0 = 100M+2.5GBASE-T1 0 1 1 x x = Reserved 0 1 0 1 x = Reserved 0 1 0 0 1 = Reserved 0 1 0 0 0 = 10BASE-T1M 0 0 1 1 1 = 25GBASE-T1 0 0 1 1 0 = 10GBASE-T1 0 0 1 0 1 = 5GBASE-T1 0 0 1 0 0 = 2.5GBASE-T1 0 0 0 1 1 = 10BASE-T1S 0 0 0 1 0 = 10BASE-T1L 0 0 0 0 1 = 1000BASE-T1 0 0 0 0 0 = 100BASE-T1	R/W

^aR/W = Read/Write, RO = Read only

Change the subclause title and first sentence of 45.2.1.214.2 (as modified by IEEE Std 802.3da-2026) as follows:

45.2.1.214.2 Type selection (1.2100.4:0) (~~1.2100.3:0~~)

Bits 1.2100.4:0 ~~1.2100.3:0~~ are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented.

45.2.1.244 MultiGBASE-T1 training register (1.2311)

45.2.1.244.1 Interleave request (1.2311.12:11)

Change the first paragraph of 45.2.1.244.1 (as modified by IEEE Std 802.3cy-2023) as follows:

Bits 1.2311.12:11 control the Reed-Solomon interleave setting of this PHY. Reed-Solomon interleaving is described in [149.3.2.2.15](#), ~~and 165.3.2.2.15~~, and [191.3.2.2.14](#). This is communicated to the link partner via Infofields as specified in [149.4.2.4.5](#), ~~and 165.4.2.4.5~~, [191.5.2.4.5](#), and [191.5.2.5.4](#).

45.2.1.244.2 Precoder selection (1.2311.5)

Change 45.2.1.244.2 as follows:

When bit 1.2311.5 is set to a one, the PHY shall use bits 1.2311.3:2 for the value of PrecodeSel, and when set to a zero the PHY controls the value of PrecodeSel. PrecodeSel is the desired precoder setting communicated to the link partner via the Infofield specified in [149.4.2.4.5](#) and [191.5.2.5.4](#).

45.2.1.244.4 User precoder selection (1.2311.3:2)

Change 45.2.1.244.4 as follows:

When bit 1.2311.5 is a one, bits 1.2311.3:2 are the requested precoder setting communicated by the PHY to the link partner via the PrecodeSel bits in the Infofield (see [149.4.2.4.5](#) and [191.5.2.5.4](#)).

45.2.1.245 MultiGBASE-T1 link partner training register (1.2312)

45.2.1.245.1 Link partner interleave request (1.2312.12:11)

Change the first paragraph of 45.2.1.245.1 (as modified by IEEE Std 802.3cy-2023) as follows:

Bits 1.2312.12:11 contain the Reed-Solomon interleave setting requested by the link partner. Reed-Solomon interleaving is described in [149.3.2.2.15](#), ~~and 165.3.2.2.15~~, and [191.3.2.2.14](#). This is communicated by the link partner via Infofields as specified in [149.4.2.4.5](#), ~~and 165.4.2.4.5~~, [191.5.2.4.5](#), and [191.5.2.5.4](#).

45.2.1.246 MultiGBASE-T1 test mode control register (1.2313)

45.2.1.246.1 Test mode control (1.2313.15:13)

Change the first paragraph of 45.2.1.246.1 (as modified by IEEE Std 802.3cy-2023) as follows:

Transmitter test mode operations defined by bits 1.2313.15:13, are described in [149.5.1](#), [Table 149–17](#), [165.5.1](#), ~~and Table 165–12~~, [191.6.1](#), [Table 191–13](#), [191.7.1](#), and [Table 191–19](#). The default value for bits 1.2313.15:13 is zero.

Insert the following new subclauses and tables after 45.2.1.250 and before 45.2.1.251 (as inserted by IEEE Std 802.3dj-202x) as follows:

45.2.1.250a MultiGBASE-A PMA rate ability (Register 1.2318)

The assignment of bits in the MultiGBASE-A PMA rate ability register is shown in Table 45–212aa.

Table 45–212aa—MultiGBASE-A PMA rate ability register bit definitions

Bit(s)	Name	Description	R/W ^a
1.2318.15	MultiGBASE-A PHY_D 10 Gb/s Rx ability	1 = PHY has MultiGBASE-A PHY_D 10 Gb/s Rx ability 0 = PHY does not have MultiGBASE-A PHY_D 10 Gb/s Rx ability	RO
1.2318.14	MultiGBASE-A PHY_D 7.5 Gb/s Rx ability	1 = PHY has MultiGBASE-A PHY_D 7.5 Gb/s Rx ability 0 = PHY does not have MultiGBASE-A PHY_D 7.5 Gb/s Rx ability	RO
1.2318.13	MultiGBASE-A PHY_D 5 Gb/s Rx ability	1 = PHY has MultiGBASE-A PHY_D 5 Gb/s Rx ability 0 = PHY does not have MultiGBASE-A PHY_D 5 Gb/s Rx ability	RO
1.2318.12	MultiGBASE-A PHY_D 2.5 Gb/s Rx ability	1 = PHY has MultiGBASE-A PHY_D 2.5 Gb/s Rx ability 0 = PHY does not have MultiGBASE-A PHY_D 2.5 Gb/s Rx ability	RO
1.2318.11:9	Reserved	Value always 0	RO
1.2318.8	MultiGBASE-A PHY_D 100 Mb/s Tx ability	1 = PHY has MultiGBASE-A PHY_D 100 Mb/s Tx ability 0 = PHY does not have MultiGBASE-A PHY_D 100 Mb/s Tx ability	RO
1.2318.7	MultiGBASE-A PHY_S 10 Gb/s Tx ability	1 = PHY has MultiGBASE-A PHY_S 10 Gb/s Tx ability 0 = PHY does not have MultiGBASE-A PHY_S 10 Gb/s Tx ability	RO
1.2318.6	MultiGBASE-A PHY_S 7.5 Gb/s Tx ability	1 = PHY has MultiGBASE-A PHY_S 7.5Gb/s Tx ability 0 = PHY does not have MultiGBASE-A PHY_S 7.5 Gb/s Tx ability	RO
1.2318.5	MultiGBASE-A PHY_S 5 Gb/s Tx ability	1 = PHY has MultiGBASE-A PHY_S 5Gb/s Tx ability 0 = PHY does not have MultiGBASE-A PHY_S 5 Gb/s Tx ability	RO
1.2318.4	MultiGBASE-A PHY_S 2.5 Gb/s Tx ability	1 = PHY has MultiGBASE-A PHY_S 2.5Gb/s Tx ability 0 = PHY does not have MultiGBASE-A PHY_S 2.5 Gb/s Tx ability	RO
1.2318.3:1	Reserved	Value always 0	RO
1.2318.0	MultiGBASE-A PHY_S 100 Mb/s Rx ability	1 = PHY has MultiGBASE-A PHY_S 100 Mb/s Rx ability 0 = PHY does not have MultiGBASE-A PHY_S 100 Mb/s Rx ability	RO

^aRO = Read only.

45.2.1.250a.1 MultiGBASE-A PHY_D 10 Gb/s Rx ability (1.2318.15)

When read as a one, bit 1.2318.15 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 10 Gb/s. When read as a zero, bit 1.2318.15 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 10 Gb/s.

45.2.1.250a.2 MultiGBASE-A PHY_D 7.5 Gb/s Rx ability (1.2318.14)

When read as a one, bit 1.2318.14 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 7.5 Gb/s. When read as a zero, bit 1.2318.14 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 7.5 Gb/s.

45.2.1.250a.3 MultiGBASE-A PHY_D 5 Gb/s Rx ability (1.2318.13)

When read as a one, bit 1.2318.13 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 5 Gb/s. When read as a zero, bit 1.2318.13 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 5 Gb/s.

45.2.1.250a.4 MultiGBASE-A PHY_D 2.5 Gb/s Rx ability (1.2318.12)

When read as a one, bit 1.2318.12 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.12 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 2.5 Gb/s.

45.2.1.250a.5 MultiGBASE-A PHY_D 100 Mb/s Tx ability (1.2318.8)

When read as a one, bit 1.2318.8 indicates that the PHY supports operating in PHY_D mode at a transmit data rate of 100 Mb/s. When read as a zero, bit 1.2318.8 indicates that the PHY does not support operating in PHY_D mode at a transmit data rate of 100 Mb/s.

45.2.1.250a.6 MultiGBASE-A PHY_S 10 Gb/s Tx ability (1.2318.7)

When read as a one, bit 1.2318.7 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 10 Gb/s. When read as a zero, bit 1.2318.7 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 10 Gb/s.

45.2.1.250a.7 MultiGBASE-A PHY_S 7.5 Gb/s Tx ability (1.2318.6)

When read as a one, bit 1.2318.6 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 7.5 Gb/s. When read as a zero, bit 1.2318.6 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 7.5 Gb/s.

45.2.1.250a.8 MultiGBASE-A PHY_S 5 Gb/s Tx ability (1.2318.5)

When read as a one, bit 1.2318.5 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 5 Gb/s. When read as a zero, bit 1.2318.5 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 5 Gb/s.

45.2.1.250a.9 MultiGBASE-A PHY_S 2.5 Gb/s Tx ability (1.2318.4)

When read as a one, bit 1.2318.4 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.4 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 2.5 Gb/s.

45.2.1.250a.10 MultiGBASE-A PHY_S 100 Mb/s Rx ability (1.2318.0)

When read as a one, bit 1.2318.0 indicates that the PHY supports operating in PHY_S mode at a receive data rate of 100 Mb/s. When read as a zero, bit 1.2318.0 indicates that the PHY does not support operating in PHY_S mode at a receive data rate of 100 Mb/s.

45.2.1.250b MultiGBASE-A PMA rate negotiation (Register 1.2319)

The assignment of bits in the MultiGBASE-A PMA supported rates register is shown in Table 45–212ab.

Table 45–212ab—MultiGBASE-A PMA rate negotiation register bit definitions

Bit(s)	Name	Description	R/W ^a
1.2319.15:6	Reserved	Value always 0	RO
1.2319.5:4	Negotiated PHY_D Transmit rate	5 4 0 0 = Negotiation in progress 0 1 = 100 Mb/s PHY_D Tx 1 x = Reserved	R/W
1.2319.3:1	Negotiated PHY_S Transmit rate	3 2 1 0 0 0 = Negotiation in progress 0 0 1 = 2.5 Gb/s PHY_S Tx 0 1 0 = 5 Gb/s PHY_S Tx 0 1 1 = 7.5 Gb/s PHY_S Tx 1 0 0 = 10 Gb/s PHY_S Tx 1 0 1 = Reserved 1 1 x = Reserved	R/W
1.2319.0	Negotiated Direction	1 = PHY_D requested of Follower 0 = PHY_S requested of Follower	R/W

^aRO = Read only, R/W = Read/Write.

45.2.1.250b.1 Negotiated PHY_D Transmit rate (1.2319.5:4)

When bits 1.2319:5:4 are 00, negotiation of the PHY_D transmit rate is in progress. When bits 1.2319:5:4 are 01, rate negotiation has selected a PHY_D transmit rate as described in Table 45–212ab and the Leader will request the Follower operate accordingly through Infocfield exchange. The same PHY_S receive rate is selected.

45.2.1.250b.2 Negotiated PHY_S Transmit rate (1.2319.3:1)

When bits 1.2319:3:1 are 000, negotiation of the PHY_S transmit rate is in progress. When bits 1.2319:5:4 are not 000, rate negotiation has selected a PHY_S transmit rate as described in Table 45–212ab and the Leader will request the Follower operate accordingly through Infocfield exchange. The same PHY_D receive rate is selected.

45.2.1.250b.3 Negotiated Direction (1.2319.0)

When bit 1.2319.0 is one, the Leader will operate in PHY_S mode and requests the Follower operate in PHY_D mode. When bit 1.2319.0 is zero, the Leader will operate in PHY_D mode and requests the Follower operate in PHY_S mode.

45.2.1.250c MultiGBASE-A PMA link partner rate negotiation (Register 1.2320)

The assignment of bits in the MultiGBASE-A PMA link partner rate negotiation register is shown in Table 45–212ac.

45.2.1.250c.1 Link partner PHY_D 10 Gb/s Rx ability (1.2320.15)

When read as a one, bit 1.2320.15 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 10 Gb/s. When read as a zero, bit 1.2320.15 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 10 Gb/s.

Table 45–212ac—MultiGBASE-A PMA link partner rate negotiation register bit definitions

Bit(s)	Name	Description	R/W ^a
1.2320.15	Link partner PHY_D 10 Gb/s Rx ability	1 = Link partner has MultiGBASE-A PHY_D 10 Gb/s Rx ability 0 = Link partner does not have MultiGBASE-A PHY_D 10 Gb/s Rx ability	RO
1.2320.14	Link partner PHY_D 7.5 Gb/s Rx ability	1 = Link partner has MultiGBASE-A PHY_D 7.5 Gb/s Rx ability 0 = Link partner does not have MultiGBASE-A PHY_D 7.5 Gb/s Rx ability	RO
1.2320.13	Link partner PHY_D 5 Gb/s Rx ability	1 = Link partner has MultiGBASE-A PHY_D 5 Gb/s Rx ability 0 = Link partner does not have MultiGBASE-A PHY_D 5 Gb/s Rx ability	RO
1.2320.12	Link partner PHY_D 2.5 Gb/s Rx ability	1 = Link partner has MultiGBASE-A PHY_D 2.5 Gb/s Rx ability 0 = Link partner does not have MultiGBASE-A PHY_D 2.5 Gb/s Rx ability	RO
1.2320.11:9	Reserved	Value always 0	RO
1.2320.8	Link partner PHY_D 100 Mb/s Tx ability	1 = Link partner has MultiGBASE-A PHY_D 100 Mb/s Tx ability 0 = Link partner does not have MultiGBASE-A PHY_D 100 Mb/s Tx ability	RO
1.2320.7	Link partner PHY_S 10 Gb/s Tx ability	1 = Link partner has MultiGBASE-A PHY_S 10 Gb/s Tx ability 0 = Link partner does not have MultiGBASE-A PHY_S 10 Gb/s Tx ability	RO
1.2320.6	Link partner PHY_S 7.5 Gb/s Tx ability	1 = Link partner has MultiGBASE-A PHY_S 7.5 Gb/s Tx ability 0 = Link partner does not have MultiGBASE-A PHY_S 7.5 Gb/s Tx ability	RO
1.2320.5	Link partner PHY_S 5 Gb/s Tx ability	1 = Link partner has MultiGBASE-A PHY_S 5 Gb/s Tx ability 0 = Link partner does not have MultiGBASE-A PHY_S 5 Gb/s Tx ability	RO
1.2320.4	Link partner PHY_S 2.5 Gb/s Tx ability	1 = Link partner has MultiGBASE-A PHY_S 2.5 Gb/s Tx ability 0 = Link partner does not have MultiGBASE-A PHY_S 2.5 Gb/s Tx ability	RO
1.2320.3:1	Reserved	Value always 0	RO
1.2320.0	Link partner PHY_S 100 Mb/s Rx ability	1 = Link partner has MultiGBASE-A PHY_S 100 Mb/s Rx ability 0 = Link partner does not have MultiGBASE-A PHY_S 100 Mb/s Rx ability	RO

^aRO = Read only.

45.2.1.250c.2 Link partner PHY_D 7.5 Gb/s Rx ability (1.2320.14)

When read as a one, bit 1.2318.14 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 7.5 Gb/s. When read as a zero, bit 1.2318.14 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 7.5 Gb/s.

45.2.1.250c.3 Link partner PHY_D 5 Gb/s Rx ability (1.2320.13)

When read as a one, bit 1.2318.13 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 5 Gb/s. When read as a zero, bit 1.2318.13 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 5 Gb/s.

45.2.1.250c.4 Link partner PHY_D 2.5 Gb/s Rx ability (1.2320.12)

When read as a one, bit 1.2318.12 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.12 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 2.5 Gb/s.

45.2.1.250c.5 Link partner PHY_D 100 Mb/s Tx ability (1.2320.8)

When read as a one, bit 1.2320.8 indicates that the link partner supports operating in PHY_D mode at a transmit data rate of 100 Mb/s. When read as a zero, bit 1.2320.8 indicates that the link partner does not support operating in PHY_D mode at a transmit data rate of 100 Mb/s.

45.2.1.250c.6 Link partner PHY_S 10 Gb/s Tx ability (1.2320.7)

When read as a one, bit 1.2320.7 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 10 Gb/s. When read as a zero, bit 1.2320.7 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 10 Gb/s.

45.2.1.250c.7 Link partner PHY_S 7.5 Gb/s Tx ability (1.2320.6)

When read as a one, bit 1.2320.6 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 7.5 Gb/s. When read as a zero, bit 1.2320.6 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 7.5 Gb/s.

45.2.1.250c.8 Link partner PHY_S 5 Gb/s Tx ability (1.2320.5)

When read as a one, bit 1.2320.5 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 5 Gb/s. When read as a zero, bit 1.2320.5 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 5 Gb/s.

45.2.1.250c.9 Link partner PHY_S 2.5 Gb/s Tx ability (1.2320.4)

When read as a one, bit 1.2320.4 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 2.5 Gb/s. When read as a zero, bit 1.2320.4 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 2.5 Gb/s.

45.2.1.250c.10 Link partner PHY_S 100 Mb/s Rx ability (1.2320.0)

When read as a one, bit 1.2320.0 indicates that the link partner supports operating in PHY_S mode at a receive data rate of 100 Mb/s. When read as a zero, bit 1.2320.0 indicates that the link partner does not support operating in PHY_S mode at a receive data rate of 100 Mb/s.

45.2.3 PCS registers

Change the rows for 3.2308, 3.2309 through 3.2312, 3.2313, 3.2314 through 3.2317, 3.2318 through 3.2319, 3.2320 through 3.2321, 3.2322, 3.2323, and 3.2324 in Table 45-233 by adding the superscripts “a” and “b” for footnotes, and associated footnotes, as follows (unchanged rows not shown):

Table 45–233—PCS registers

Register address	Register name	Subclause
...		
3.2308	BASE-T1 OAM transmit ^a	45.2.3.79
3.2309 through 3.2312	BASE-T1 OAM message ^a	45.2.3.80
3.2313	BASE-T1 OAM receive ^a	45.2.3.81
3.2314 through 3.2317	Link partner BASE-T1 OAM message ^{a,b}	45.2.3.82
3.2318 through 3.2319	MultiGBASE-T1 OAM status message ^{a,b}	45.2.3.83
3.2320 through 3.2321	Link partner MultiGBASE-T1 OAM status message ^{a,b}	45.2.3.84
3.2322	MultiGBASE-T1 PCS control ^b	45.2.3.85
3.2323	MultiGBASE-T1 PCS status 1 ^b	45.2.3.86
3.2324	MultiGBASE-T1 PCS status 2 ^b	45.2.3.87
...		

^aThis register also applies to MultiGBASE-A PHYs.

^bThis register also applies to MultiG type -V1 PHYs.

45.2.3.87 MultiGBASE-T1 PCS status 2 register (Register 3.2324)

45.2.3.87.1 Receive link status (3.2324.10)

Change the last sentence of 45.2.3.87.1 as follows:

When read as a one, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is not fully operational. Bit 3.2324.10 is a reflection of the pcs_status variable defined in 149.3.8.1, 191.3.6.1, and 192.3.6.1.

45.2.3.87.2 PCS high RFER (3.2324.9)

Change the last sentence of 45.2.3.87.2 as follows:

When read as a one, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS receiver is detecting 16 or more RS-FEC errored blocks within 88 RS-FEC frames. When read as a zero, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS is detecting fewer than 16 RS-FEC errored blocks within 88 RS-FEC frames. Bit 3.2324.9 is a reflection of the state of the hi_rfer variable defined in 149.3.7.2.2, 191.3.5.1.2, and 192.3.5.1.2.

45.2.3.87.3 PCS block lock (3.2324.8)

Change the last sentence of 45.2.3.87.3 as follows:

When read as a one, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has not achieved block lock. Bit 3.2324.8 is a reflection of the state of the block_lock variable defined in [149.3.8.1](#), [191.3.6.1](#), and [192.3.6.1](#).

45.2.3.87.6 BER count (3.2324.5:0)

Change the first sentence of 45.2.3.87.6 as follows:

The BER counter formed by bits 3.2324.5:0 is a six-bit counter as defined by RFER_count in [149.3.8.2](#), [191.3.6.2](#), and [192.3.6.2](#). These bits shall be reset to all zeros when the MultiGBASE-T1 PCS status 2 register is read by the management function or upon execution of the MultiGBASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)

46.1 Overview

Change the third paragraph of 46.1 as follows:

The RS adapts the bit serial protocols of the MAC to the parallel encodings of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s symmetrical PHYs or to the parallel encodings of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s asymmetrical PHYs in the transmit or receive path and 100 Mb/s in the other one. Though the XGMII is an optional interface, it is used extensively in this standard as a basis for specification. The 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s Physical Coding Sublayers (PCS), or the 100 Mb/s PCS in case of asymmetric PHYs, are specified to the XGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XGMII were implemented.

Change list item “a” in the fourth paragraph of 46.1 as follows:

- a) It is capable of supporting at least one of the following rates of operation: 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s (including asymmetric PHYs with one of these rates in the transmit or receive path and 100 Mb/s in the other path).

46.1.1 Summary of major concepts

Change list item “i” in 46.1.1 as follows:

- i) The XGMII is rate scalable and may support rates of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s (including asymmetric PHYs with one of these rates in the transmit or receive path and 100 Mb/s in the other one).

46.1.2 Application

Change the second paragraph of 46.1.2 as follows:

This interface is used to provide media independence so that an identical media access controller may be used with all 2.5GBASE, 5GBASE, and 10GBASE 100M+2.5GBASE, 2.5G+100MBASE, 5GBASE, 100M+5GBASE, 5G+100MBASE, 10GBASE, 100M+10GBASE, 10G+100MBASE, and MultiGBASE-A PHY types.

46.1.3 Rate of operation

Change the first paragraph of 46.1.3 as follows:

The XGMII supports MAC data rates of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s as defined within this clause. A compliant device may implement any subset of these rates. Symmetric Operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35. The XGMII supports symmetric operation with a MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s. The XGMII supports asymmetric operation with a MAC data rate of 100 Mb/s in the transmit or receive path and at least one of the specified multigigabit rates in the other one.

46.3 XGMII functional specifications

46.3.1 Transmit

46.3.1.1 TX_CLK (transmit clock)

Change the second paragraph of 46.3.1.1 as follows:

The TX_CLK frequency shall be $1/64 \times f_{\text{MAC}} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal MAC bit rate that the RS provides in the transmit direction (2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, 10 Gb/s, or 100 Mb/s). When interfacing to a PHY with a 7.5 Gbps transmit bit rate, the TX_CLK frequency calculation shall use 7.5 GHz in place of f_{MAC} , even though interfacing is to a MAC parameterized for 10 Gb/s as described in Table 4-2.

46.3.2 Receive

46.3.2.1 RX_CLK (receive clock)

Change the second paragraph of 46.3.2.1 as follows:

The frequency of RX_CLK may be derived from the received data or it may be that of a nominal clock (e.g., TX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be $1/64 \times f_{\text{MAC}} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal MAC bit rate that the RS provides in the receive direction (2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, 10 Gb/s, or 100 Mb/s). When interfacing to a PHY with a 7.5 Gbps receive bit rate, the RX_CLK frequency calculation shall use 7.5 GHz in place of f_{MAC} , even though interfacing is to a MAC parameterized for 10 Gb/s as described in Table 4-2.

46.6 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)³

46.6.2 Identification

46.6.2.3 Major capabilities/options

Insert new row at end of table (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
...					
ASM	Support of Asymmetric Multigigabit PHYs	46.1.2		O	Yes [] No []

46.6.3 PICS proforma tables for Reconciliation Sublayer and 10 Gigabit Media Independent Interface

46.6.3.1 General

³Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

Change PICs items G1, G2, and G3; insert new row G1a after row G1; insert new rows G3a, G3b, and G3c after row G3; and insert new row G6 after G5 as shown (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
G1	PHY support of 10 Gb/s MAC data rate <u>in at least one direction</u>	46.1.3	Support MAC data rate of 10 Gb/s	PHY:O.1	Yes [] N/A []
G1a	PHY support of 7.5 Gb/s MAC data rate <u>in at least one direction</u>	46.1.3	Support MAC data rate of 7.5 Gb/s	PHY:O.1	Yes [] N/A []
G2	PHY support of 5 Gb/s MAC data rate <u>in at least one direction</u>	46.1.3	Support MAC data rate of 5 Gb/s	PHY:O.1	Yes [] N/A []
G3	PHY support of 2.5 Gb/s MAC data rate <u>in at least one direction</u>	46.1.3	Support MAC data rate of 2.5 Gb/s	PHY:O.1	Yes [] N/A []
G3a	<u>Asymmetric support of 100 Mb/s in the transmit direction</u>	46.1.3	<u>Support MAC data rate of 100 Mb/s in the transmit direction when at least one of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s is supported in the receive direction</u>	ASM:M PHY:O.1	Yes [] N/A []
G3b	<u>Asymmetric support of 100 Mb/s in the receive direction</u>	46.1.3	<u>Support MAC data rate of 100 Mb/s in one direction when at least one of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s is supported in the transmit direction</u>	ASM:M PHY:O.1	Yes [] N/A []
G3c	<u>PHY does not support asymmetric operation</u>	46.1.3	<u>Only supports symmetric MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s</u>	!ASM:M PHY:O.1	Yes [] N/A []
...					
G6	<u>Functional Behavior</u>	46.1	<u>Behaves as if the RS and XGMII were implemented (even when not physically instantiated)</u>	M	Yes []

46.6.3.6 XGMII signal functional specifications

Change PICs items FS2 and FS9, and insert new rows FS2a, after FS2, and FS9a after row FS9 as shown (unchanged rows not shown):.

Item	Feature	Subclause	Value/Comment	Status	Support
...					
FS2	TX_CLK frequency	46.3.1.1	$1/64 \times f_{\text{MAC}} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal MAC bit rate <u>that the RS provides in the transmit direction</u>	XGE:M *!7.5G	Yes [] N/A []
FS2a	TX_CLK frequency for 7.5 Gb/s	46.3.1.1	<u>TX_CLK frequency calculation shall use 7.5 GHz in place of f_{MAC}</u>	XGE:M *!7.5G	Yes [] N/A []
...					
FS9	RX_CLK frequency	46.3.2.1	$1/64 \times f_{\text{MAC}} \pm 100$ ppm, where f_{MAC} is the frequency (in Hz) corresponding to the MAC's nominal MAC bit rate <u>that the RS provides in the receive direction</u>	XGE:M *!7.5G	Yes [] N/A []
FS9a	RX_CLK frequency for 7.5 Gb/s	46.3.2.1	<u>RX_CLK frequency calculation shall use 7.5 GHz in place of f_{MAC}</u>	XGE:M *!7.5G	Yes [] N/A []
...					

Change the title of Clause 98 as follows:

98. Auto-Negotiation for single differential-pair or single-ended (unbalanced) media

98.1 Overview

Change the text of 98.1 as follows:

98.1.1 Scope

Clause 98 describes the ~~single twisted-pair~~ Auto-Negotiation function ~~that allows used on single differential-pair media or single-ended unbalanced media to allow~~ a device to advertise enhanced modes of operation it possesses to a device at the remote end of a link segment and to detect corresponding enhanced operational modes that the other device may be advertising. [Annex 98A](#) describes the Selector Field that is used by Auto-Negotiation to identify the type of message being sent.

The objective of the ~~single twisted-pair~~ [Clause 98](#) Auto-Negotiation function is to provide the means to exchange information between two devices that share a link segment and to automatically configure both devices to take maximum advantage of their abilities. It has the additional objective of providing a common synchronization time between two devices prior to link training.

~~Single twisted-pair~~ [Clause 98](#) Auto-Negotiation is performed using differential Manchester encoding (DME) pages. DME provides a DC balanced signal. DME does not add packet or upper layer overhead to the network devices. DME is transferred in a half-duplex manner over the media ~~single twisted-pair copper cable~~.

~~Single twisted-pair~~ [Clause 98](#) Auto-Negotiation does not test the link segment characteristics.

[Clause 98](#) Auto-Negotiation may be used with either differential balanced-pair media or with single-ended unbalanced media.

The function allows the devices at both ends of a link segment to advertise abilities, acknowledge receipt and understanding of the common mode(s) of operation that both devices share, and to reject the use of operational modes that are not shared by both devices. Where more than one common mode exists between the two devices, a mechanism is provided to allow the devices to resolve to a single mode of operation using a predetermined priority resolution function. The ~~single twisted-pair~~ [Clause 98](#) Auto-Negotiation function allows the identification of the operational mode of the link partner. Should multiple modes be present, management may select between the various offered modes. How such selection is done is beyond the scope of this standard.

98.1.2 Relationship to the ISO/IEC Open Systems Interconnection (OSI) reference model

The ~~single twisted-pair~~ [Clause 98](#) Auto-Negotiation function is provided at the Physical Layer of the ISO/IEC OSI reference model as shown in Figure 98–2. A device that supports multiple modes of operation may advertise its capabilities using the ~~single twisted-pair~~ [Clause 98](#) Auto-Negotiation function. The actual transfer of information is observed only at the MDI.

98.2 Functional specifications

Change the text of 98.2 as follows (unchanged text and figures not shown):

The ~~single twisted-pair~~ Clause 98 Auto-Negotiation function provides a mechanism to control connection of a single MDI to a single PHY type, where more than one PHY type may exist. A management interface provides control and status of ~~single twisted-pair~~ Clause 98 Auto-Negotiation, but the presence of a management agent is not required.

Auto-Negotiation shall provide the following functions (as shown in Figure 98–1):

- a) Transmit
- b) Receive
- c) Half duplex
- d) Arbitration

If used with a single-ended unbalanced MDI and medium, when measured with 50 Ω termination, transmit signal at MDI shall be within range of 0.5 V $\pm$ 30% peak-to-peak.

98.2.1.2 Link codeword encoding

98.2.1.2.4 Technology Ability Field

Change the first paragraph of 98.2.1.2.4 as follows (unchanged text not shown):

Technology Ability Field (A[26:0]) is a 27-bit wide field containing information indicating supported technologies specific to the selector field value when used with the ~~single twisted-pair~~ Auto-Negotiation Ethernet. These bits are mapped to individual technologies such that abilities are advertised in parallel for a single selector field value. The Technology Ability Field encoding for the IEEE 802.3 selector with ~~single twisted-pair~~ Clause 98 Auto-Negotiation Ethernet is described in 98B.3.

98.2.4 Arbitration function requirements

98.2.4.2 Priority Resolution function

Change 98.2.4.2 as follows:

Since a local device and a link partner may have multiple ~~common-compatible~~ abilities, a mechanism to resolve which mode to configure is required. The mechanism used by Auto-Negotiation is a Priority Resolution function that predefines the hierarchy of supported technologies. The single PHY enabled to connect to the MDI by Auto-Negotiation shall be the technology ~~corresponding to the bit in the Technology Ability Field common to~~ of the local device that is compatible with the and-link partner Technology Ability Field that has the highest priority as defined in 98B.4 (~~listed-numbered~~ from highest priority (1) to lowest priority).

In order to avoid priority conflicts, Leader/Follower configuration is logically resolved before applying Table 98B-2.

The ~~common-highest priority compatible~~ technology is referred to as the *highest common denominator*, or HCD, technology. If the local device receives a Technology Ability Field with a bit set that is reserved, the local device shall ignore that bit for priority resolution. Determination of the HCD technology occurs on entrance to the AN GOOD CHECK state. In the event that there is no ~~common-compatible~~ technology, HCD shall have a value of “NULL,” indicating that no PHY receives link_control = ENABLE and link_status[HCD] = FAIL.

98.3 State diagram variable to Auto-Negotiation register mapping

Change the title of Table 98-7 as follows (unchanged rows not shown):

Table 98-7—State diagram variable to ~~Single-lane twisted-pair media~~ Auto-Negotiation MDIO register mapping

...

98.5 Detailed functions and state diagrams

98.5.1 State diagram variables

Insert new items at the end of the dashed list after the first paragraph of 98.5.1 as follows:

- 100M+2.5GigT1/V1; represents that the 100M+2.5GBASE-T1/V1 PMA is the signal source.
- 100M+5GigT1/V1; represents that the 100M+5GBASE-T1/V1 PMA is the signal source.
- 100M+10GigT1/V1; represents that the 100M+10GBASE-T1/V1 PMA is the signal source.
- 2.5GigT1+100MT1/V1; represents that the 2.5G+100MBASE-T1/V1 PMA is the signal source.
- 5GigT1+100MT1/V1; represents that the 5G+100MBASE-T1/V1 PMA is the signal source.
- 10GigT1+100MT1/V1; represents that the 10G+100MBASE-T1/V1 PMA is the signal source.

NOTE—If the priority resolution is an asymmetrical ability, the HCD values are complementary, e.g. if the HCD for a device is 100M+2.5GigT1, the HCD for its link partner would be 2.5Gig+100MT1.

Change the last sentence of the third paragraph of 98.5.1 as follows (unchanged text not shown):

The mapping between state diagram variables and ~~Single twisted-pair~~ Auto-Negotiation MDIO registers is shown in Table 98–7.

Change the title of 98.6 as follows:

98.6 Protocol implementation conformance statement (PICS) proforma for Clause 98, Auto-Negotiation for ~~S~~single ~~D~~ifferential-~~P~~pair or single-ended (unbalanced) ~~M~~media⁴

Change the first sentence of 98.6.1 as follows:

98.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 98, Auto-Negotiation for ~~S~~single ~~D~~ifferential-~~P~~pair or single-ended (unbalanced) ~~M~~media, shall complete the following protocol implementation conformance statement (PICS) proforma.

98.6.2 Identification

98.6.2.2 Protocol summary

Change the first row of the following table as follows (unchanged rows not shown):

Identification of protocol standard	IEEE Std 802.3-202x, Clause 98, Auto-Negotiation for ~~S~~ single ~~D~~ ifferential- ~~P~~ pair or single-ended (unbalanced) ~~M~~ media
...	

98.6.3 Major capabilities/options

Add two new rows at the end of the following table (unchanged rows not shown)

Item	Feature	Subclause	Value/Comment	Status	Support
...					
*DIFF	Differential balanced-pair media	98.1.1		O/2	Yes [] No []
*UNB	Unbalanced single-ended media	98.1.1		O/2	Yes [] No []

98.6.4 General

*Change the second row of the following table as follows (unchanged rows not shown):*¹

Item	Feature	Subclause	Value/Comment	Status	Support
G1	~~Single twisted-pair~~ Clause 98 Auto-Negotiation function	98.2	Provide Auto-Negotiation transmit, Auto-Negotiation receive, Auto-Negotiation half-duplex, and Auto-Negotiation arbitration	M	Yes []
...					

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98.6.5 DME transmission

Change DME10 and add DME11 at the end of the following table (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
...					
DME10	Transmit differential signal at the MDI	98.2.1.1.4	Within range of 1 V ± 30% peak-to-peak when measured in reference to a 100 Ω termination	<u>DIFF:</u> M	Yes []
<u>DME11</u>	<u>Transmit signal at the MDI</u>	<u>98.2.1.1.4</u>	<u>Within range of 0.5 V ± 30% peak-to-peak when measured in reference to a 50 Ω termination</u>	<u>UNB:</u> <u>M</u>	<u>Yes []</u>

Insert new clauses as follows:

191. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium for MultiG+100M/100M+MultiGBASE-T1/V1

191.1 Overview

This clause defines a set of twelve distinct PHY types, see 191.1.1, that share the same PCS and PMA specifications. To aid in readability, the following terms are used:

MultiG	one of 2.5G, 5G, 10G
T1	a single shielded balanced pair of conductors
V1	a single-ended coaxial cable
MultiG+100MBASE	PHY_S PCS
100M+MultiGBASE	PHY_D PCS
MultiG+100M/100M+MultiGBASE-T1/V1	the 12 PHYs
MultiG+100M/100M+MultiGBASE-T1	the subset of PHYs that communicate using a shielded, balanced, pair of conductors
MultiG+100M/100M+MultiGBASE-V1	the subset of PHYs that communicate using a coaxial cable

This clause defines the MultiG+100M/100M+MultiGBASE Physical Coding Sublayer (PCS) as well as the MultiG+100M/100M+MultiGBASE Physical Medium Attachment (PMA) sublayers. Together, the PCS and corresponding PMA sublayers comprise a MultiG+100M/100M+MultiGBASE-T1/V1 Physical Layer device (PHY). Provided in this clause are functional and electrical specifications for each of the 12 PHYs.

MultiG+100M/100M+MultiGBASE-T1 PHYs are intended to be operated over a single balanced pair of conductors. The link segment specifications defined in 191.9 were derived from automotive requirements, but may also be used for non-automotive applications. The link segments supporting the operation of these PHYs are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) (see 191.11) allowing implementers to provide their own link segments to operate these PHYs as long as the normative requirements included in 191.9 are met.

MultiG+100M/100M+MultiGBASE-V1 PHYs are intended to be operated over a single coaxial cable. The link segment specifications defined in 191.10 were derived from automotive requirements, but may also be used for non-automotive applications. The link segments supporting the operation of these PHYs are defined in terms of performance requirements between the Medium Dependent Interfaces (MDIs) (see 191.12) allowing implementers to provide their own link segments to operate these PHYs as long as the normative requirements included in 191.10 are met.

These PHYs continuously transmit in both directions concurrently, but at different baud rates. Unlike frequency division techniques, the PHYs have full spectral overlap in the two transmit directions, but utilize the relatively narrow bandwidth of the Low Data Rate (LDR) signal to enable separation of the remote signal from the echo signal.

This clause defines multiple PHY types named according to <maximum transmit data rate>+<maximum receive data rate>BASE-T1/V1, where -T1 is for single differential balanced-pair media, and -V1 is for single-ended unbalanced media. Clause 191 PHYs are defined to use the Clause 46 XGMII in a configuration where the RS supports an asymmetric data rate with the multigigabit transmit (or receive) rate on the TX (or RX) path, and the 100 Mb/s receive (or transmit) rate on the RX (or TX) path of the XGMII. The Clause 4 MAC parameters for the appropriate rate (multigigabit or 100 Mb/s) are used in conjunction with the PHYs described in this clause in conjunction with either the multigigabit (HS) path or the 100 Mb/s (LS) path.

191.1.1 Nomenclature

The PHYs included within MultiG+100M/100M+MultiGBASE-T1/V1 (see Table 191–2 for more detail) are:

100M+2.5GBASE-T1
2.5G+100MBASE-T1
100M+5GBASE-T1
5G+100MBASE-T1
100M+10GBASE-T1
10G+100MBASE-T1
100M+2.5GBASE-V1
2.5G+100MBASE-V1
100M+5GBASE-V1
5G+100MBASE-V1
100M+10GBASE-V1
10G+100MBASE-V1

In order to efficiently describe the 12 PHYs, the following nomenclature is used. See Figure 191–1 for a block diagram.

HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter
PHY_D	Device containing LS_TX and HS_RX (100M+MultiGBASE-T1/V1)
PHY_S	Device containing HS_TX and LS_RX (MultiG+100MBASE-T1/V1)

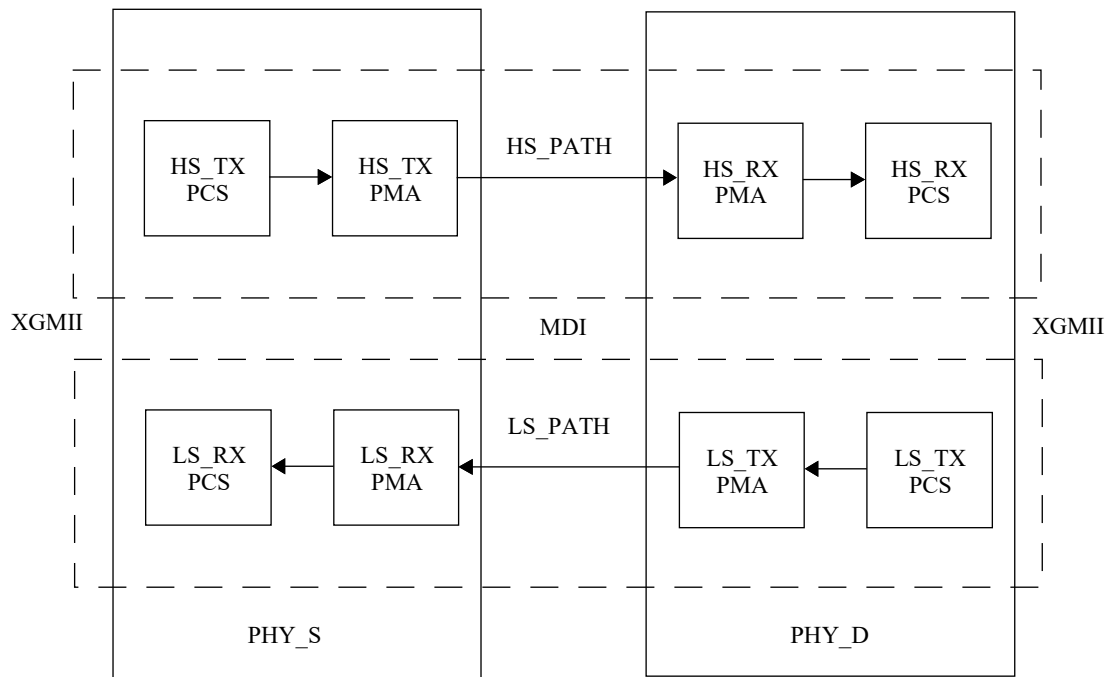


Figure 191-1—MultiG+100M/100M+MultiGBASE-T1/V1 block diagram

For all PHYs communicating on a shielded, balanced, pair of conductors, regardless of transmit bit rate, use:

MultiG+100M/100M+MultiGBASE-T1

For all PHYs communicating on a coaxial cable, regardless of transmit bit rate, use:

MultiG+100M/100M+MultiGBASE-V1

For all PHYs, regardless of transmit bit rate or cable type, use:

MultiG+100M/100M+MultiGBASE-T1/V1

Additionally, for parameters that scale with the transmit bit rate of the PHY, the parameter S is used for scaling, see Table 191-1. When incorporating Clause 149 requirements which use the scaling factor S by reference, refer to Table 191-1 rather than Table 149-1.

Table 191-1—Scaling parameter

PHY type	S
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	1
2.5G+100MBASE-T1/V1	0.5

The characteristics of each of the 12 PHY types are expanded in Table 191–2.

Table 191–2—PHY/PMD type definitions

PHY name	Transmit bit rate	Receive bit rate	Medium Interface
100M+2.5GBASE-T1	100 Mb/s	2.5 Gb/s	Differential (balanced)
2.5G+100MBASE-T1	2.5 Gb/s	100 Mb/s	Differential (balanced)
100M+5GBASE-T1	100 Mb/s	5 Gb/s	Differential (balanced)
5G+100MBASE-T1	5 Gb/s	100 Mb/s	Differential (balanced)
100M+10GBASE-T1	100 Mb/s	10 Gb/s	Differential (balanced)
10G+100MBASE-T1	10 Gb/s	100 Mb/s	Differential (balanced)
100M+2.5GBASE-V1	100 Mb/s	2.5 Gb/s	Single-ended (unbalanced)
2.5G+100MBASE-V1	2.5 Gb/s	100 Mb/s	Single-ended (unbalanced)
100M+5GBASE-V1	100 Mb/s	5 Gb/s	Single-ended (unbalanced)
5G+100MBASE-V1	5 Gb/s	100 Mb/s	Single-ended (unbalanced)
100M+10GBASE-V1	100 Mb/s	10 Gb/s	Single-ended (unbalanced)
10G+100MBASE-V1	10 Gb/s	100 Mb/s	Single-ended (unbalanced)

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

- T1 represents a single shielded balanced pair of conductors (i.e., differential)
- V1 represents a single-ended coaxial cable (i.e., unbalanced)

191.1.2 Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 to other standards

The relationship between a MultiG+100M/100M+MultiGBASE-T1/V1 PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 191–2. The PHY sublayers (shown shaded) in Figure 191–2 connect one [Clause 4](#) Media Access Control (MAC) layer to the medium. The XGMII is defined in Clause 46.

Auto-Negotiation for all MultiG+100M/100M+MultiGBASE-T1/V1 PHYs is defined in Clause 98.

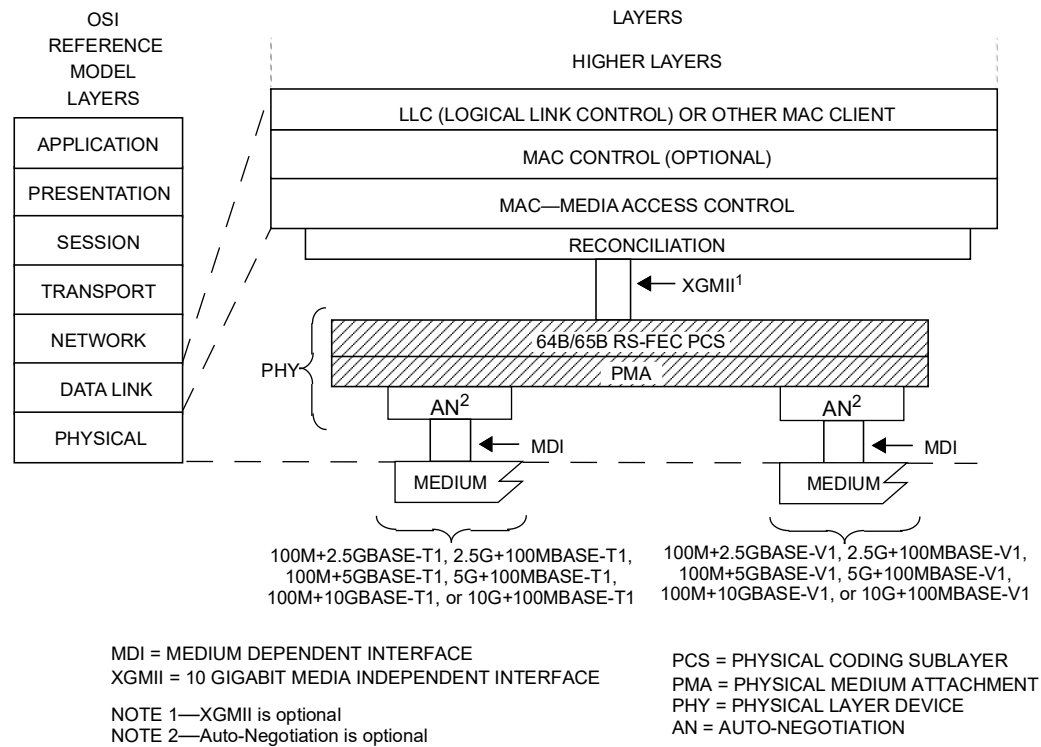


Figure 191-2—Relationship of MultiG+100M/100M+MultiGBASE-T1/V1 PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

191.1.3 Operation of MultiG+100M/100M+MultiGBASE-T1/V1

A MultiG+100MBASE-T1/V1 PHY is a PHY_S device which transmits at a bit rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s and receives at a bit rate of 100 Mb/s. A 100M+MultiGBASE-T1/V1 PHY is a PHY_D device which transmits at a bit rate of 100 Mb/s and receives at a bit rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s. Figure 191-3 shows a block diagram of the PHY_S device and Figure 191-4 shows a block diagram of the PHY_D device.

The PHY_S device includes the high speed transmit function and low speed receive function required for asymmetric operation over the link segment. The top-level arrangement of the PCS, PMA, synchronization, monitoring, and Tx Clock Generation blocks is shown in Figure 191-3. While the block diagram illustrates data, status, and control flow among these elements, the detailed functional definitions are provided in the remainder of Clause 191.

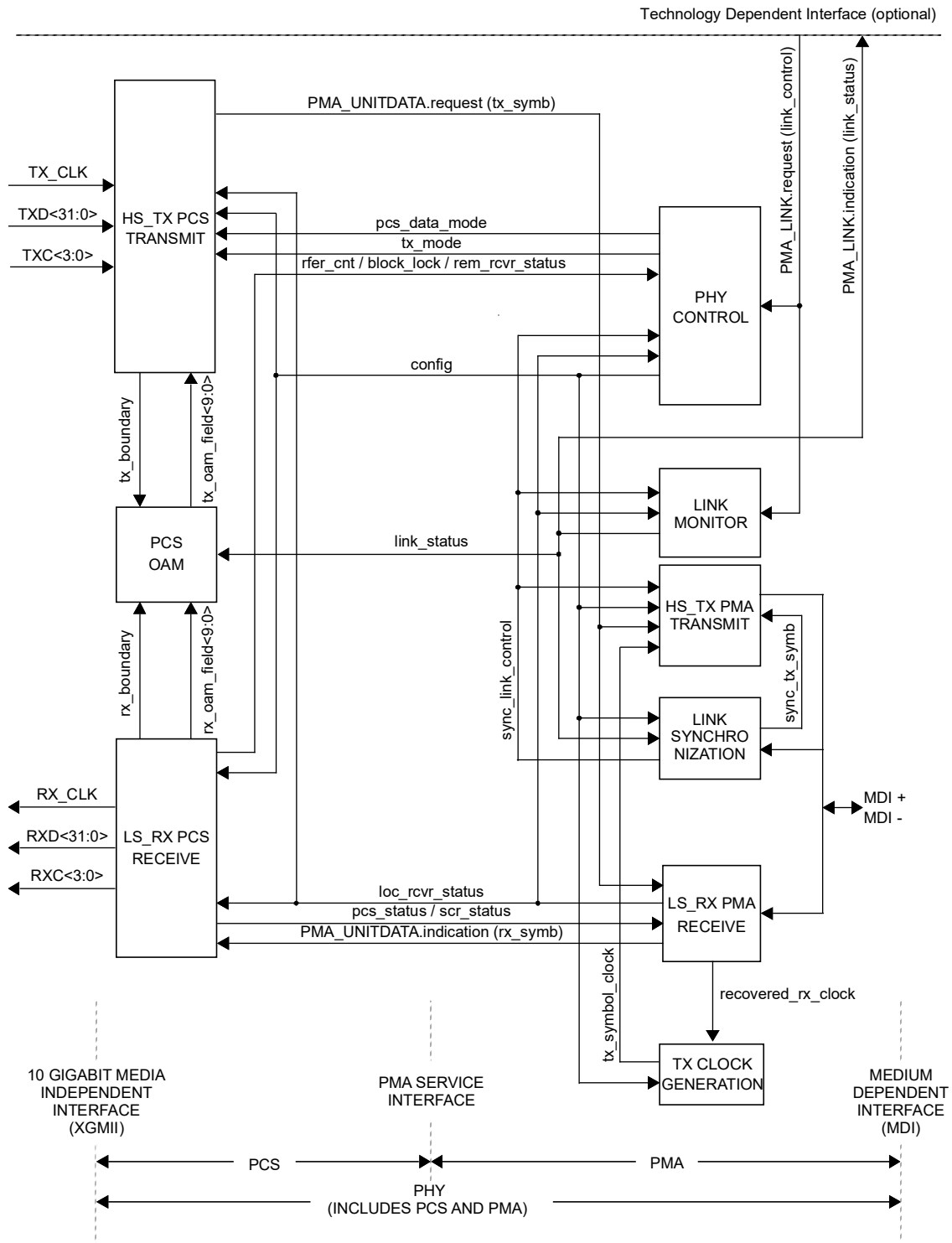
The PHY_D device includes the low speed transmit function and high speed receive function required for asymmetric operation over the link segment. The top-level arrangement of the PCS, PMA, synchronization, monitoring, and Tx Clock Generation blocks is shown in Figure 191-4. While the block diagram illustrates data, status, and control flow among these elements, the detailed functional definitions are provided in the remainder of Clause 191.

Auto-Negotiation (Clause 98) may optionally be used by MultiG+100M/100M+MultiGBASE-T1/V1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional.

A MultiG+100M/100M+MultiGBASE-T1/V1 PHY can operate as Leader or Follower, per runtime configuration. A Leader PHY uses a local clock to determine the timing of transmitter operations. A Follower PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. The Leader-Follower relationship is established by forced configuration in the Link Synchronization process (see 191.5.2.8), or by Auto-Negotiation if it is implemented and enabled.

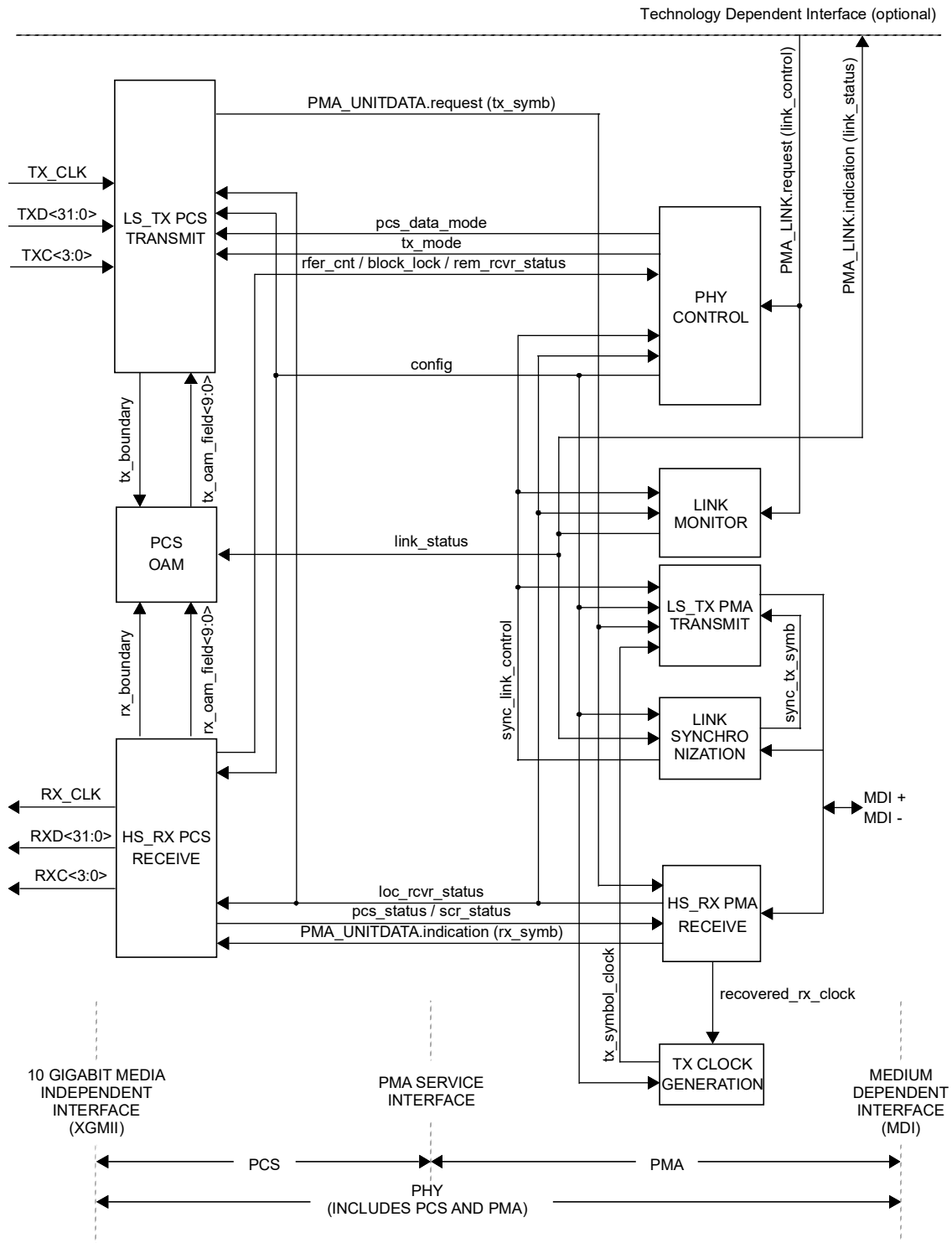
NOTE—[Annex K](#) describes the optional alternative terminology Leader and Follower which was formerly known as "master" and "slave".

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NOTE—The tx_symbol_clock is derived from the recovered_rx_clock when the PHY is loop timed, otherwise it is derived from a local clock source.

Figure 191-3—PHY_S functional block diagram



NOTE—The tx_symbol_clock is derived from the recovered_rx_clock when the PHY is loop timed, otherwise it is derived from a local clock source.

Figure 191–4—PHY_D functional block diagram

191.1.3.1 Physical Coding Sublayer (PCS), high speed path (HS_PATH)

For the high speed path, the HS_TX and HS_RX PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, to the 2.5G+100MBASE-T1/V1, 5G+100MBASE-T1/V1, or 10G+100MBASE-T1/V1 PMA sublayer. In addition to the pcs_data_mode (called data mode in this Clause) of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface. The HS_TX PCS is in the PHY_S and the HS_RX PCS is in the PHY_D.

The HS_PATH contains the PCS functions as specified in 149.3, except as modified by 191.3.

191.1.3.2 Physical Coding Sublayer (PCS), low speed path (LS_PATH)

For the low speed path, the LS_TX and LS_RX PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, to the 100M+2.5GBASE-T1/V1, 100M+5GBASE-T1/V1, or 100M+10GBASE-T1/V1 PMA sublayer. In addition to the data mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface. The LS_TX PCS is in the PHY_D and the LS_RX PCS is in the PHY_S.

For the low speed path, in data mode, the PCS LS_TX receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and TXC<3:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block.

These 65-bit blocks are then aggregated into groups of four blocks. The contents of each group are contained in a vector tx_group4x65B. Next, 10 OAM bits and a 6-bit CRC field are appended to form a 276-bit block. The 6-bit CRC is calculated over the four 65B blocks and the 10 OAM bits as specified in 191.4.2.2.15. Each of these 276-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(50,46,6). The RS-FEC output frame consists of 300 bits. The duration of the frame is 2560 ns. These bits are exclusive OR'd with a degree 33 scrambler to create the PHY_D payload. The LS_PATH contains the PCS functions as described in 191.4.2.2.

The tx_group4x65B <259:0> is defined as:

$$\text{tx\_group4x65B } \langle 65 \times i + j \rangle = \text{tx\_coded}_i \langle j \rangle$$

where $i = 0$ to 3, $j = 0$ to 64, and tx_coded_{*i*}<64:0> is the i^{th} 64B/65B block where tx_coded₀<64:0> is the first block transmitted.

The LS_RX PCS reverses the above process and presents eight XGMII data octets over two consecutive transfers on the XGMII service interface on RXD<31:0> and RXC<3:0>.

In the training mode (see 191.4.4), the LS_TX transmits and the LS_RX receives differential Manchester encoding (DME) training frames to synchronize to the PHY frame (and advertise capabilities such as OAM). See 191.5.2.2.1 for details on the DME symbols.

Details of the PCS functions and state diagrams are covered in 191.4. The interface to the PMA is an abstract message-passing interface specified in 191.5.

191.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto the MDI of a single balanced pair of conductors (-T1) or a single coaxial cable (-V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions.

For the HS_PATH, the PMA provides communications at $5625 \times S$ MBd. See Table 191–1 for the definition of S . For the LS_PATH, the PMA provides communications at 117.1875 MBd.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled following the completion of PHY Link Synchronization or optional Auto-Negotiation and provides the startup functions required for successful PHY operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link channel and communicates this status to other functional blocks. A failure of the receive channel causes the data mode operation to stop and Auto-Negotiation or Link Synchronization to restart.

PMA functions and state diagrams are specified in 191.5. The electrical parameters of the PMA, i.e., test modes and electrical specifications for the transmitter and receiver, are specified in 191.6 and 191.7.

191.1.3.4 Link Synchronization

The purposes of the Link Synchronization function are to: detect the presence of the link partner; act as the data source for the PHY Control state diagram; and control behavior on failure, including timeouts. The Link Synchronization function is used when Auto-Negotiation is disabled or not implemented. Link Synchronization operates in a half-duplex fashion. Link Synchronization is defined in 191.5.2.8.

191.1.4 Signaling, high speed path (HS_PATH)

HS_TX PCS generates continuous code-group sequences that the HS_TX PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The signaling scheme achieves a number of objectives including:

- a) Forward error correction (FEC) coded symbol mapping for data.
- b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
- c) Algorithmic mapping from the received signal to RXD<31:0> and RXC<3:0>.
- d) Uncorrelated symbols in the transmitted symbol stream.
- e) No correlation between the HS_PATH and LS_PATH symbol streams.
- f) Block framing and other control signals.
- g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
- h) Ability to automatically detect and correct for incorrect polarity in the connection for the single balanced pair of conductors (-T1).

The PHY may operate in two basic modes: the data mode or the training mode.

In data mode, the HS_TX PCS generates a continuous stream of PAM4 symbols that are transmitted via the HS_TX PMA at one of four voltage levels for 10 Gb/s and PAM2 symbols that are transmitted via the HS_TX PMA at one of two voltage levels for 2.5 Gb/s and 5 Gb/s. In training mode, PHY Control directs the PCS to generate only PAM2 symbols for the HS_TX PMA to transmit.

191.1.5 Signaling, low speed path (LS_PATH)

LS_PATH PCS generates continuous code-group sequences that the LS_TX PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The signaling scheme achieves a number of objectives including:

- a) Forward error correction (FEC) coded symbol mapping for data.
- b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to DME symbols in the transmit path. See 191.5.2.2.1 for details on the DME symbols.
- c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
- d) Uncorrelated symbols in the transmitted symbol stream.
- e) No correlation between the HS_PATH and LS_PATH symbol streams.
- f) Block framing and other control signals.
- g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

The PHY may operate in two basic modes: the data mode or the training mode.

The LS_TX PCS generates a continuous stream of bits that are transmitted via the LS_TX PMA in both training mode and data mode.

191.1.6 Interfaces

All MultiG+100M/100M+MultiGBASE-T1/V1 PHY implementations are compatible at the MDI and at the XGMII, if implemented. Implementation of the XGMII is optional. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not. The MDI for single balanced pair of conductors (-T1) and single coaxial cable (-V1) are different.

191.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

191.2 PHY_S and PHY_D service primitives and interfaces

PHY_S and PHY_D transfer data and control information across the following four service interfaces:

- a) 10 Gigabit Media Independent Interface (XGMII)
- b) Technology Dependent Interface
- c) PMA service interface
- d) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46; the Technology Dependent Interface is specified in 98.4. The PMA service interface is defined in 191.2.2 and the MDI is defined in 191.11 for -T1 and in 191.12 for -V1.

191.2.1 Technology Dependent Interface

The following service primitives are used to exchange status indications and control signals across the Technology Dependent Interface, required in PHYs that implement Auto-Negotiation, as specified in 98.4:

PMA_LINK.request(link_control)
PMA_LINK.indication(link_status)

191.2.1.1 PMA_LINK.request

This primitive allows the Auto-Negotiation to enable and disable operation of the PMA, as specified in 98.4.2.

191.2.1.1.1 Semantics of the primitive

PMA_LINK.request(link_control)

The link_control parameter can take on one of two values: DISABLE, or ENABLE.

DISABLE Used by the Auto-Negotiation function to disable the PHY.

ENABLE Used by the Auto-Negotiation function to enable the PHY.

191.2.1.1.2 When generated

Auto-Negotiation generates this primitive to indicate a change in link_control as described in 98.4.

191.2.1.1.3 Effect of receipt

This primitive affects the operation of the PMA Link Monitor function as defined in 191.5.2.7, the PMA PHY Control function as defined in 191.5.2.6, and the PMA Receive function defined in 191.5.2.3 for both the HS_RX PMA and the LS_RX PMA.

191.2.1.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 98.4.1. This primitive informs the PCS, PMA PHY Control function, and the Auto-Negotiation functions about the status of the underlying link.

191.2.1.2.1 Semantics of the primitive

PMA_LINK.indication(link_status)

The link_status parameter can take on one of two values: FAIL or OK.

FAIL No valid link established.

OK The Link Monitor function indicates that a valid MultiG+100M/100M+MultiGBASE-T1/V1 link is established. Reliable reception of signals transmitted from the remote PHY is possible.

191.2.1.2.2 When generated

The PMA generates this primitive to indicate a change in link_status in compliance with the state diagram given in Figure 191–35.

191.2.1.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 98.4.1.

191.2.2 PMA service interface

The following service primitives are used to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_PCSSYNC.request(block_lock, rfer_cnt)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication(pcs_data_mode)

The use of these primitives is illustrated in Figure 191–5 and Figure 191–6. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 191–5 and Figure 191–6.

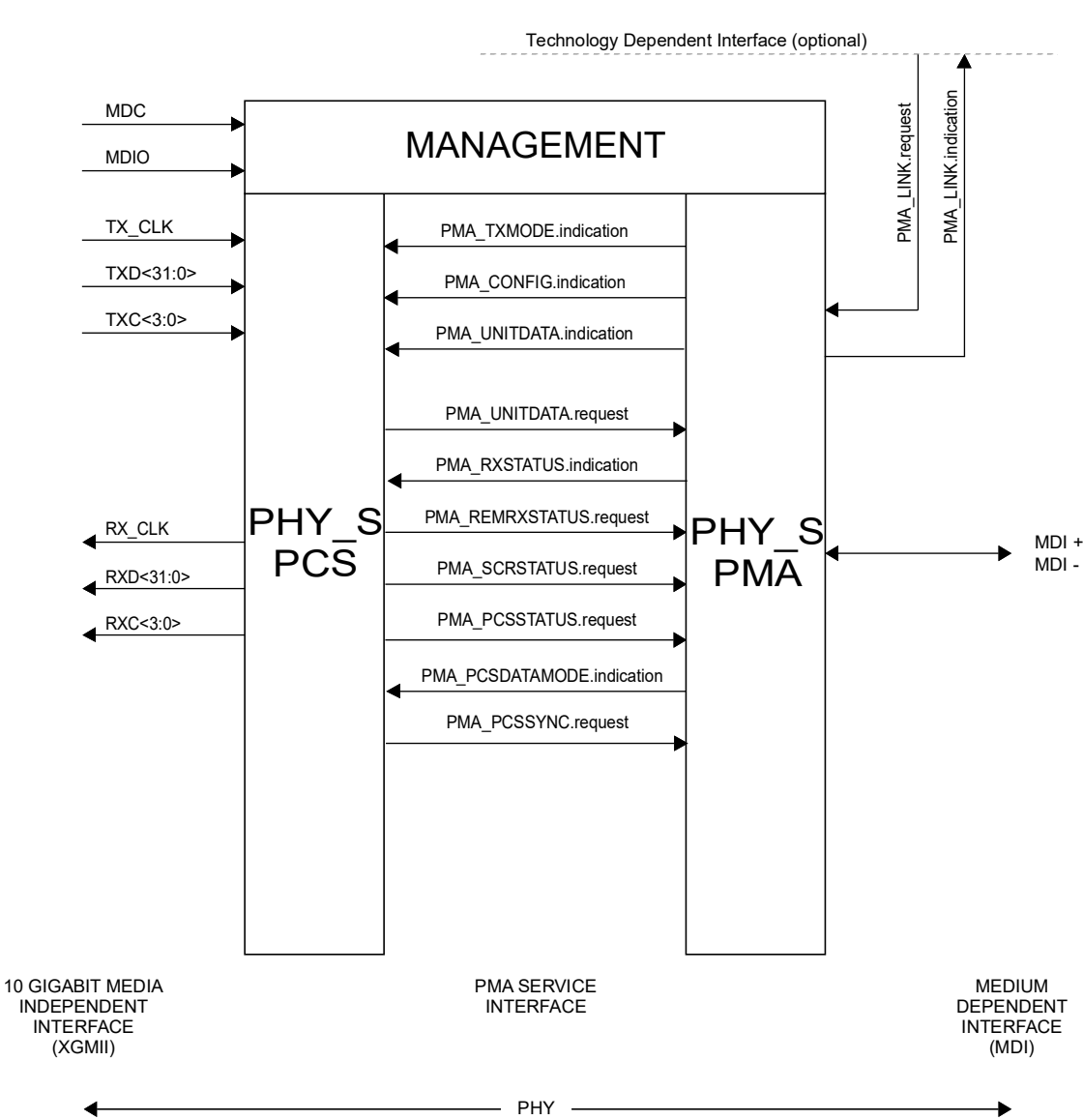


Figure 191-5—PHY_S service interfaces

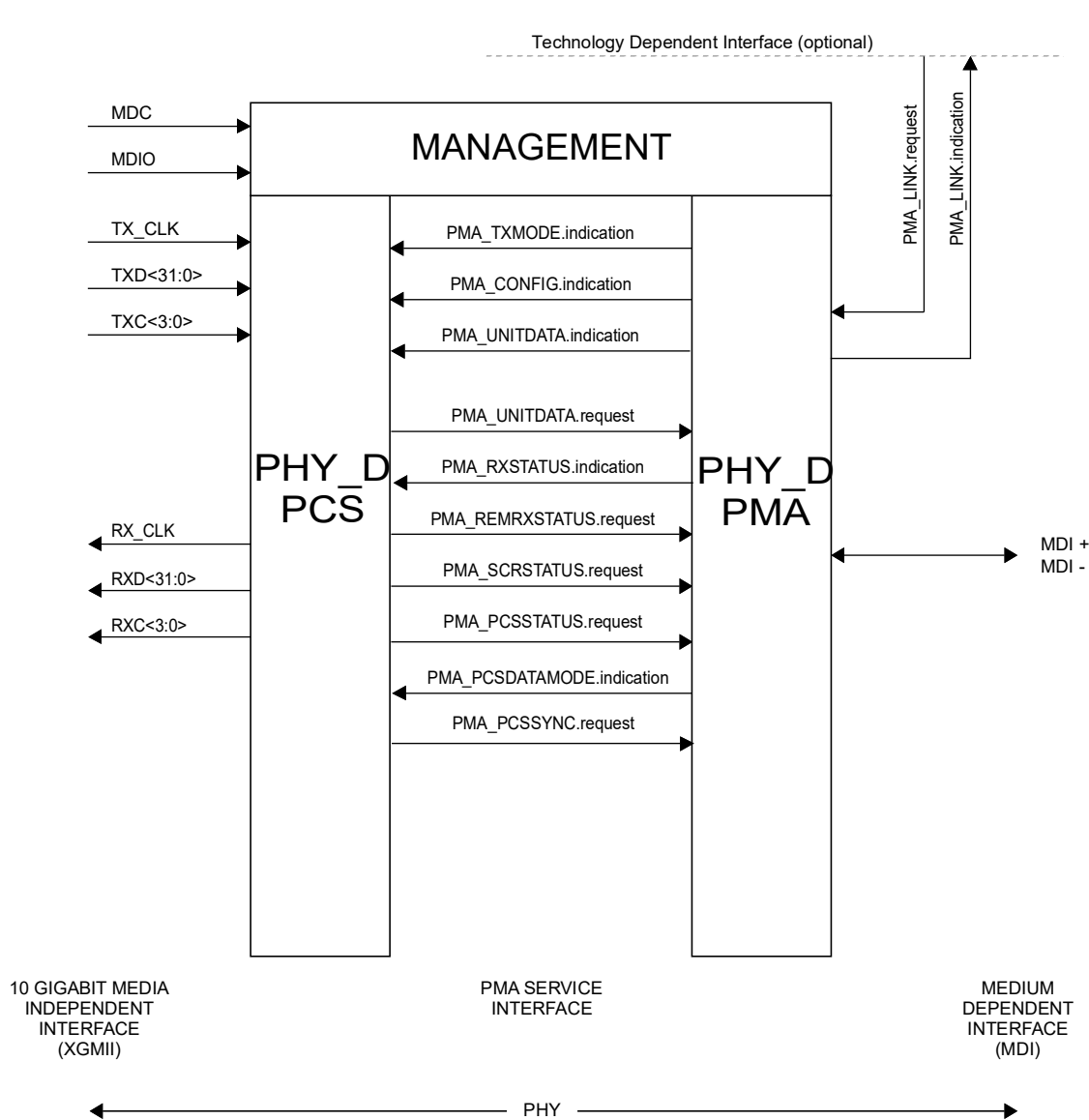


Figure 191-6—PHY_D service interfaces

191.2.2.1 PMA_TXMODE.indication

The transmitter normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

191.2.2.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values:

SEND_N	This value is continuously asserted during transmission of sequences of symbols representing an XGMII data stream in the data mode.
SEND_T	This value is continuously asserted when transmission of sequences of symbols representing the training mode is to take place.
SEND_Z	This value is continuously asserted when transmission of Z symbols is required.

191.2.2.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

191.2.2.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 191.3.2.2 for the HS_TX and in 191.4.2.2 for the LS_TX.

191.2.2.2 PMA_CONFIG.indication

If the Auto-Negotiation process is enabled, PMA_CONFIG LEADER-FOLLOWER configuration is determined during Auto-Negotiation (see Clause 98) and the result is provided to the PMA. If the Auto-Negotiation process is not implemented or not enabled, PMA_CONFIG LEADER-FOLLOWER configuration is predetermined to be LEADER or FOLLOWER via management control during initialization or via default hardware setup.

191.2.2.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PCS and PMA Transmit via the parameter config whether the PHY operates as a Leader PHY or as a Follower PHY. The parameter config can take on one of the following two values:

LEADER	This value is continuously asserted when the PHY operates as a Leader PHY.
FOLLOWER	This value is continuously asserted when the PHY operates as a Follower PHY.

191.2.2.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

191.2.2.2.3 Effect of receipt

PCS and PMA Tx Clock Generation perform their functions in LEADER or FOLLOWER configuration according to the value assumed by the parameter config.

191.2.2.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 191.3.2.2 for the HS_TX and in 191.4.2.2 for the LS_TX to represent XGMII data and control streams or other sequences.

191.2.2.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb the value of the symbols to be sent over the MDI.

The HS_TX tx_symb may take on one of the following values:

- {-1, -1/3, +1/3, +1} in normal operation for 10G+100MBASE-T1/V1.
- {-1, +1} in normal operation for 2.5G+100MBASE-T1/V1 and 5G+100MBASE-T1/V1, and HS_PATH training frames.

Z when Z symbols are to be transmitted in the following case:
when PMA_TXMODE.indication is SEND_Z during PMA training.

The LS_TX tx_symb may take on one of the following values:

- {0,1} in normal operation.

Z when Z symbols are to be transmitted in the following case:
when PMA_TXMODE.indication is SEND_Z during PMA training.

191.2.2.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

191.2.2.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 191.6.2 for the HS_TX and 191.7.2 for the LS_TX.

191.2.2.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

191.2.2.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the clock recovered from the received signal by the PMA Receive function (recovered_rx_clock).

191.2.2.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the HS_RX PMA_UNITDATA.indication primitive is 2812.5 MHz for 100M+2.5GBASE-T1/V1, and 5625 MHz for 100M+5GBASE-T1/V1 and 100M+10GBASE-T1/V1, as governed by recovered_rx_clock. The nominal rate of the LS_RX PMA_UNITDATA.indication primitive is 117.1875 MHz, as governed by recovered_rx_clock.

191.2.2.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

191.2.2.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the PCS descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the training mode PCS descrambler has achieved synchronization.

191.2.2.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values:

- OK The training mode PCS descrambler has achieved synchronization.
- NOT_OK The training mode PCS descrambler is not synchronized.

191.2.2.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

191.2.2.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 191.5.2.3 for HS_RX and in 191.5.2.3 for LS_RX.

191.2.2.6 PMA_PCSSTATUS.request

PMA_PCSSTATUS.request is as described in 149.2.2.6.

191.2.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementer. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

191.2.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The `loc_rcvr_status` parameter can take on one of two values:

OK This value is asserted and remains true during reliable operation of the receive link for the local PHY.

NOT_OK This value is asserted whenever operation of the link for the local PHY is unreliable.

191.2.2.7.2 When generated

PMA Receive generates `PMA_RXSTATUS.indication` messages to indicate a change in `loc_rcvr_status` on the basis of signals received at the MDI.

191.2.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 191–3, Figure 191–4, Figure 191–7, Figure 191–8, Figure 191–34, 191.3.2.3, 191.4.2.3, and 191.5.2.6.

191.2.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its `loc_rcvr_status` parameter. The parameter `rem_rcvr_status` conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter `rem_rcvr_status` is set to the value received in the `loc_rcvr_status` bit in the Infofield from the remote PHY. The `rem_rcvr_status` is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

191.2.2.8.1 Semantics of the primitive

`PMA_REMRXSTATUS.request(rem_rcvr_status)`

The `rem_rcvr_status` parameter can take on one of two values:

OK The receive link for the remote PHY is operating reliably.

NOT_OK Reliable operation of the receive link for the remote PHY is not detected.

191.2.2.8.2 When generated

The PCS generates `PMA_REMRXSTATUS.request` messages to indicate a change in `rem_rcvr_status` based on the PCS decoding the `loc_rcvr_status` bit in Infofield messages received from the remote PHY during training.

191.2.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 191–34.

191.2.2.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The PMA PHY Control function generates the `pcs_data_mode` variable. It is passed to the PCS Control function via the `PMA_PCSDATAMODE.indication` primitive.

191.2.2.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

The pcs_data_mode parameter can take on one of two values:

TRUE	The PHY Control is in the state PCS_DATA.
FALSE	The PHY Control is not in the state PCS_DATA.

191.2.2.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

191.2.2.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 191.3.2.2 for HS_TX and 191.4.2.2 for LS_TX.

191.2.2.10 PMA_PCSSYNC.request

191.2.2.10.1 Semantics of the primitive

PMA_PCSSYNC.request(block_lock, rfer_cnt)

The PMA_PCSSYNC.request primitive passes the block_lock and rfer_cnt parameters from the PCS to the PMA.

The parameter block_lock can take on one of the following two values:

TRUE	The PCS Synchronization process has acquired block delineation.
FALSE	The PCS Synchronization process has not acquired block delineation.

The parameter rfer_cnt can take on one of the following two values:

TRUE	The PCS Synchronization has detected 16 errors in one RFRX_CNT_LIMIT interval.
FALSE	The PCS Synchronization has not detected 16 errors in one RFRX_CNT_LIMIT interval.

191.2.2.10.2 When generated

The PCS generates PMA_PCSSYNC.request messages to indicate a change in block_lock or rfer_cnt.

191.2.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 191–34.

191.3 Physical Coding Sublayer (PCS) functions, high speed path (HS_PATH)

191.3.1 PCS service interface (XGMII)

The PCS service interface allows the PHY_S PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

191.3.2 PCS functions

The HS_PATH PCS comprises the following functions: PCS Reset, HS_TX PCS Transmit in the PHY_S device, HS_RX PCS Receive in the PHY_D device, and an optional PCS OAM. The PCS Transmit and PCS Receive functions execute simultaneously and asynchronously. All operating functions start immediately after the successful completion of the PCS Reset function.

The PHY_S PCS reference diagram, Figure 191–7 and the PHY_D PCS diagram, Figure 191–8, show how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 191–7 and Figure 191–8.

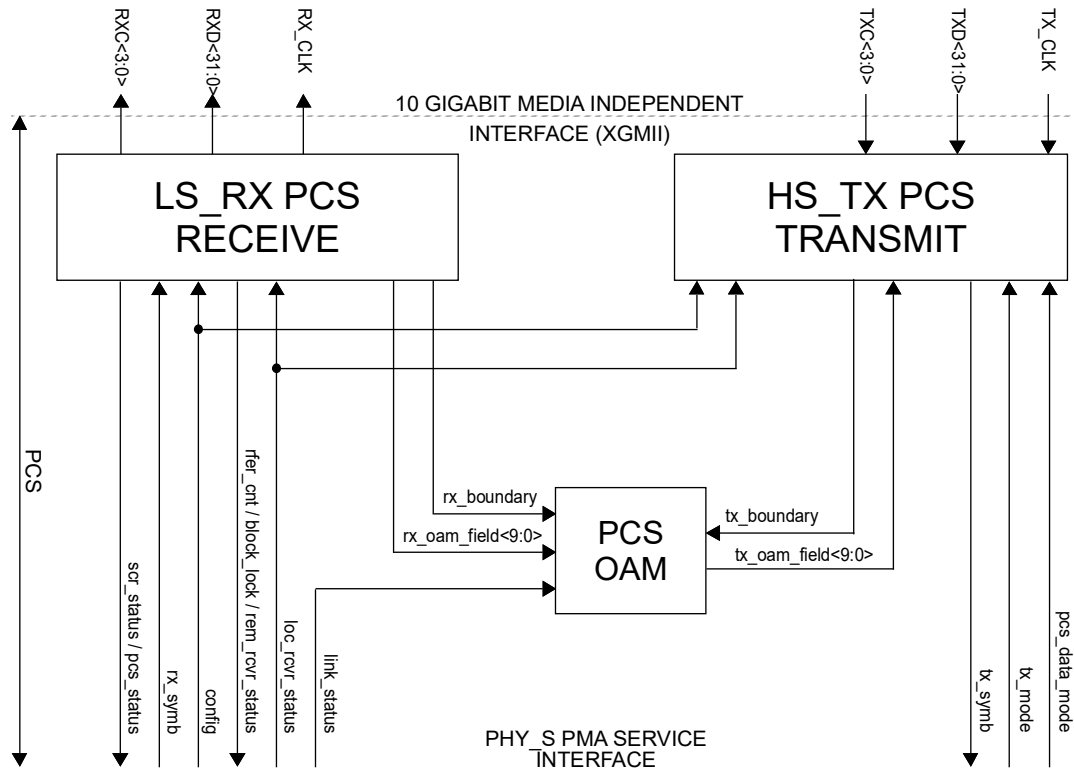


Figure 191-7—PHY_S PCS reference diagram

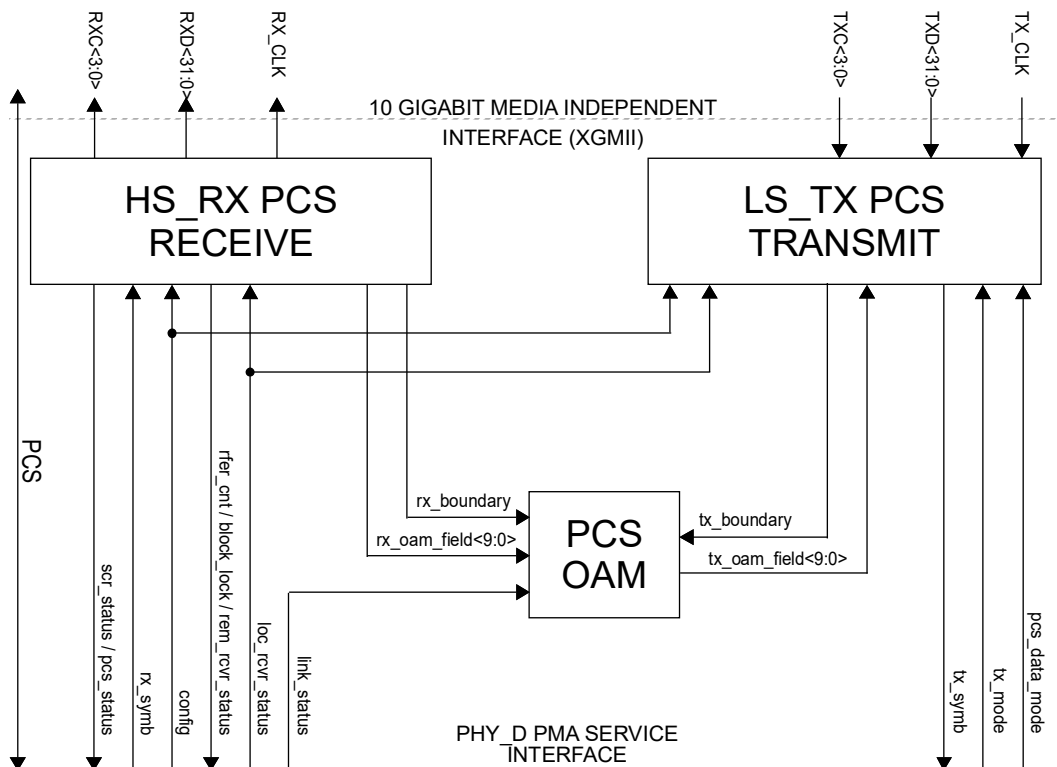


Figure 191–8—PHY_D PCS reference diagram

191.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. This means that there is only one PCS Reset, resetting both the low speed and high speed paths. The PCS Reset function shall be executed whenever one of the following conditions occur:

- a) Power on (see 191.3.5.1.2).
- b) The receipt of a request for reset from the management entity.

PCS Reset sets `pcs_reset = TRUE` while any of the above reset conditions hold true. All state diagrams take the open-ended `pcs_reset` branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

191.3.2.2 PCS Transmit function

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 191–19. The PCS Transmit bit ordering shall conform to Figure 191–11 for a 10G+100MBASE-T1/V1 PHY. For a 5G+100MBASE-T1/V1 or a 2.5GBASE-T1/V1 PHY, the PCS Transmit bit ordering shall conform to Figure 191–12.

When communicating with the XGMII, the PHY_S PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process takes L groups of 50 65B blocks, where L is the interleaving depth, and the possible choices of L are 1, 2, and 4. A 10-bit OAM field is appended to each group. This forms the input to an L -interleaved RS-FEC which adds $L \times 340$ parity bits. The resulting $L \times 3600$ bits are then scrambled. These bits are then mapped, two at a time, into a PAM4 symbol for 10G and one at a time into a PAM2 symbol for 2.5G and 5G. In each symbol period, transmit data-units are sent to the PMA service interface via the `PMA_UNITDATA.request` primitive. The symbol period, T_s , is $1000 / (5.625 \times S)$ ps. See Table 191–1 for the definition of S .

The `PMA_TXMODE.indication` message, received from the PMA PHY Control function, controls the operation of the PCS Transmit function.

If a `PMA_TXMODE.indication` message has the value `SEND_Z`, PCS Transmit shall pass a `Z` symbol at each symbol period to the PMA via the `PMA_UNITDATA.request` primitive.

If a `PMA_TXMODE.indication` message has the value `SEND_T`, PCS Transmit shall generate a sequence (T_n) defined in 191.3.4.1 to the PMA via the `PMA_UNITDATA.request` primitive. These code-groups are used for training mode and only transmit the values $\{-1, +1\}$.

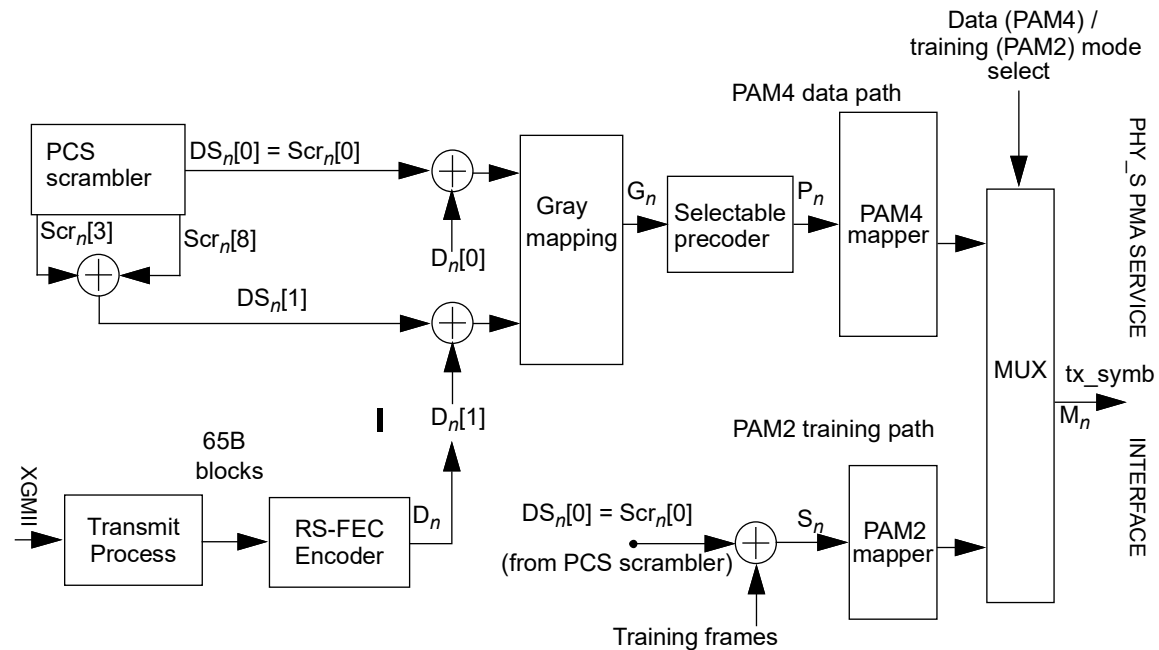
During training mode an Infocfield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 191.5.2.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation. In data mode, the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, the 50 blocks of 65B encoded bits are appended with a 10-bit OAM field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes L-interleaved ($L = 1, 2$, or 4) Reed-Solomon encoders to generate and append 340 parity check bits to form 3600-bit ($360,326$) RS-FEC frames. These frames are interleaved into an L-interleaved RS-FEC superframe.

Each RS-FEC input superframe consists of $3260 \times L$ bits, or $326 \times L$ Reed-Solomon message symbols. The interleaving function is integrated with the RS-FEC encoding, applying a round-robin interleaving scheme and distributing the 10-bit Reed-Solomon message symbols into L RS-FEC encoders. After encoding, the RS-FEC frames from each encoder are recombined into one single interleaved RS-FEC superframe, which consists of $360 \times L$ symbols, or $3600 \times L$ bits. The bits of the RS-FEC superframe are then scrambled by the PCS using an additive PCS scrambler, encoded in PAM4 symbols for 10G and PAM2 symbols for 2.5G and 5, and transferred to the PMA.

The value of L used by the transmitter is determined by the link partner and signaled during the PAM2 training mode Infocfield exchange.

The block diagram of HS_TX PCS Transmit functions is shown in Figure 191–9 and Figure 191–10.

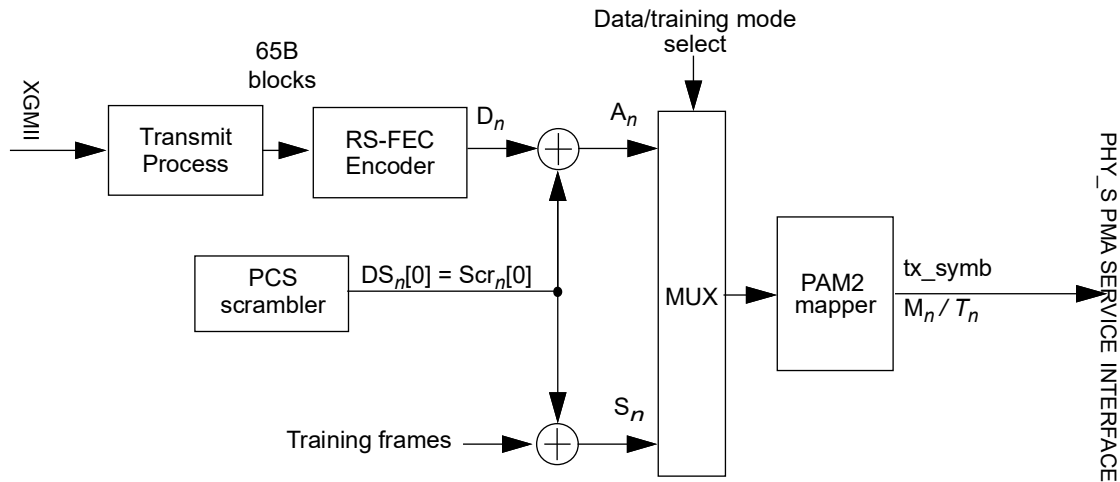


NOTE —The S_n are from the training frame, and the MUX selects the PAM2 path while in PAM2 training states.

Figure 191–9—10 Gb/s HS_TX PCS Transmit function block diagram

191.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2 PMA training frame synchronization allows establishment of RS-FEC



NOTE 1 — The S_n are from the training frame, and the A_n are for the 2.5 Gb/s and 5 Gb/s HS_PATH.
NOTE 2 — The output of the PAM2 mapper is M_n in data mode and T_n in training mode.

Figure 191-10—2.5 Gb/s and 5 Gb/s HS_TX PCS Transmit function block diagram

frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 191.3.2.2.4.

The use of blocks, notation, block structure, control codes, and encoding of ordered sets, idle, start, terminate, and error characters is identical for the high speed path and the low speed path.

191.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 191-11 for 10G transmit and Figure 191-12 for 2.5G and 5G transmit. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.

191.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7 . Control characters other than /O/, /S/, and /T/ are labeled C_0 to C_7 . The control character for ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7 .

For PHY_S, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

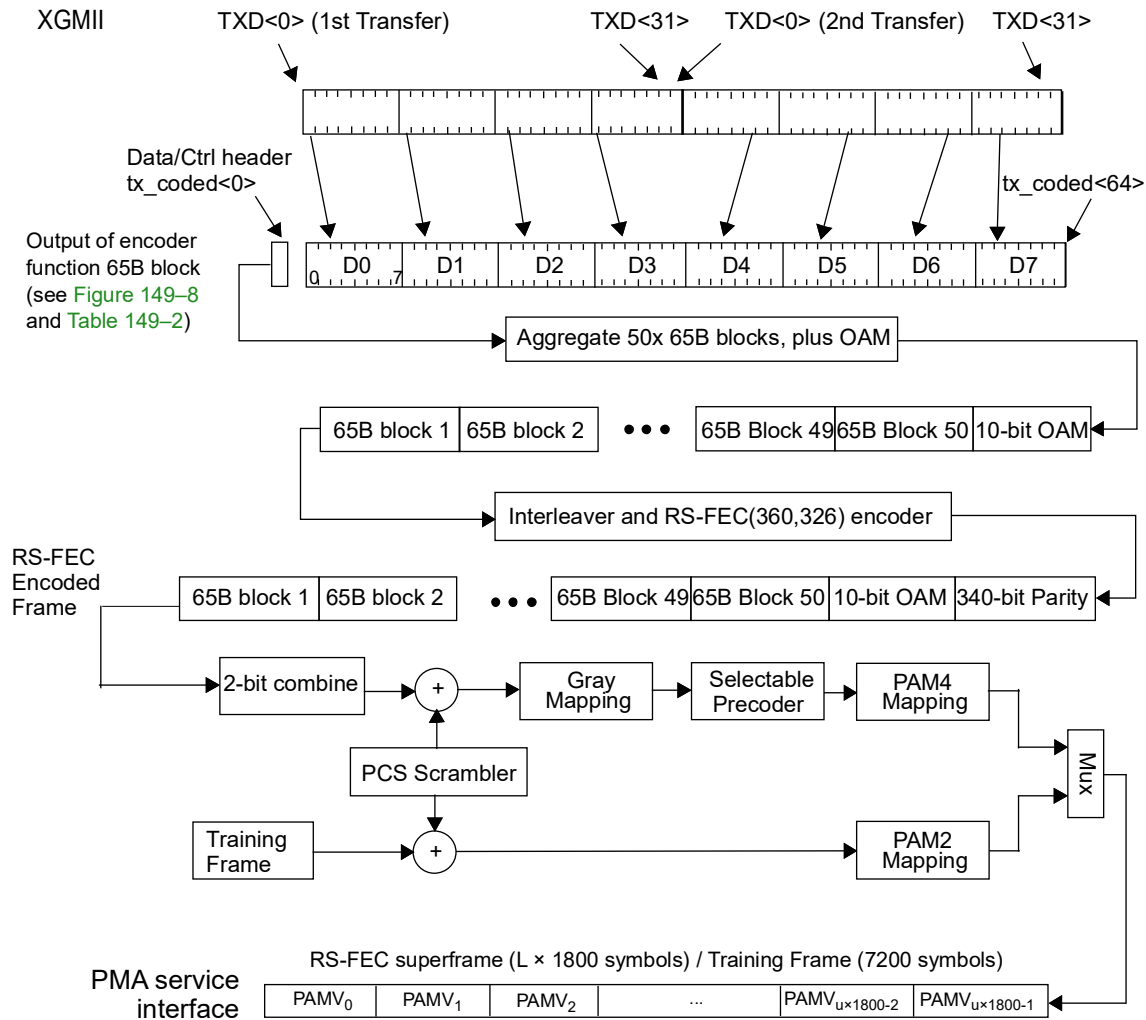


Figure 191-11—PCS 10 Gb/s Transmit bit ordering for data mode and training mode, HS_TX

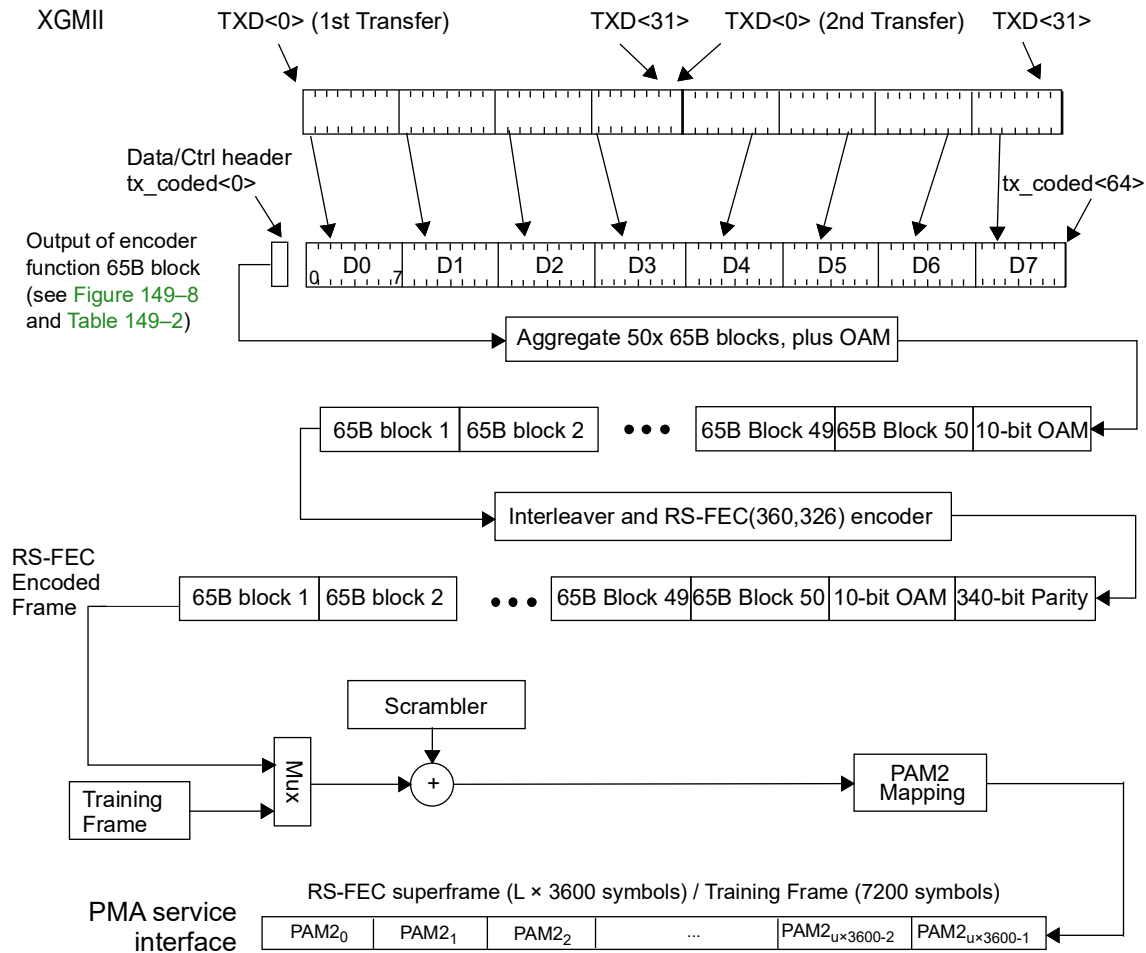
Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled $tx\_coded<31:0>$ and $rx\_coded<31:0>$ where $tx\_coded<0>$ and $rx\_coded<0>$ represent the first transmitted bit. The value of the data/control header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

191.3.2.2.4 Block structure

See 149.3.2.2.4 with MultiGBASE-T1 replaced with MultiG+100M/100M+MultiGBASE-T1/V1.

191.3.2.2.5 Control codes

Control codes shall be encoded as specified in 149.3.2.2.5.



NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.
NOTE 2—Figure shown for L = 1.
NOTE 3—For RS-FEC Frame u=1, For Training Frame u=2.

Figure 191-12—PCS 5 Gb/s and 2.5 Gb/s Transmit bit ordering for data mode and training mode, HS_TX

191.3.2.2.6 Ordered sets

Ordered sets are as specified in 149.3.2.2.6, except that LPI signaling and the /LI/ ordered set are not used by PHY_S PHYs. All other ordered sets defined in 149.3.2.2.6 apply unchanged.

191.3.2.2.7 Idle (/I/)

Idles shall be encoded as specified in 149.3.2.2.7.

191.3.2.2.8 Start (/S/)

See 149.3.2.2.9.

191.3.2.2.9 Terminate (/T/)

See 149.3.2.2.10.

191.3.2.2.10 Ordered set (/O/)

The ordered set control characters (/O/) shall be encoded as specified in 149.3.2.2.11.

191.3.2.2.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 191.3.5.1.3 for further information.

191.3.2.2.12 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 100 XGMII data transfers are encoded into an RS-FEC frame.

For PAM4 path HS_TX (10 Gb/s), it takes 1800 PMA_UNITDATA transfers to send an RS-FEC frame of data, and a XGMII to PMA transfer rate of exactly 1:18.

For PAM2 path HS_TX (5 Gb/s and 2.5 Gb/s), it takes 3600 PMA_UNITDATA transfers to send an RS-FEC frame of data, and a XGMII to PMA transfer rate of exactly 1:36.

Therefore, for PHY_S, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 1:18, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 191–19). The contents of each block are contained in a vector $\text{tx\_coded}_{\langle 64:0 \rangle}$, which is passed to the RS-FEC encoder and PCS scrambler. $\text{tx\_coded}_{\langle 0 \rangle}$ contains the data/ctrl header and the remainder of the bits contain the block payload.

191.3.2.2.13 RS-FEC framing and RS-FEC encoder

To form the RS-FEC frame, 50 65B blocks are grouped as follows:

$$\text{tx\_group}_{50 \times 65B}^{\langle 65 \times i + j \rangle} = \text{tx\_coded}_i^{\langle j \rangle}$$

where $i = 0$ to 49, $j = 0$ to 64, and $\text{tx\_coded}_i^{\langle 64:0 \rangle}$ is the i^{th} 64B/65B block and $\text{tx\_coded}_0^{\langle 64:0 \rangle}$ is the first block transmitted.

The resulting RS-FEC frame of 50 65B blocks, followed by the 10-bit OAM field and 340 parity bits is 3600 bits. See Figure 191–11 and Figure 191–12 for details on PCS bit ordering. See 191.3.2.2.16 for details on RS-FEC encoding.

The RS-FEC encoding takes the 3260-bit vector, consisting of $\text{tx\_group}_{50 \times 65B}$, and the 10-bit OAM field, and shall generate the 34 10-bit parity symbols (340 bits total).

191.3.2.2.14 RS-FEC superframe and round-robin interleaving

RS-FEC superframes shall be interleaved as specified in 149.3.2.2.15, with the exception that 2.5GBASE-T1 is replaced by 2.5G+100MBASE-T1/V1, 5GBASE-T1 is replaced by 5G+100MBASE-T1/V1, and 10GBASE-T1 is replaced by 10G+100MBASE-T1/V1.

191.3.2.2.15 RS-FEC recombine

As specified in 149.3.2.2.16.

191.3.2.2.16 Reed-Solomon encoder

As specified in 149.3.2.2.17.

191.3.2.2.17 PCS scrambler PAM4

As specified in 149.3.2.2.18, with the exception that the scrambler defined in 191.3.2.2.19 is used in place of the scrambler in 149.3.4.

191.3.2.2.18 PCS scrambler PAM2

The bits of the interleaved RS-FEC superframe are presented as D_n , where n is an index indicating the symbol number, and are scrambled using an additive PCS scrambler. The scrambling sequence DS_n is equal to $Scr_n[0]$ defined in 191.3.2.2.19.

All incoming PAM2 path HS_TX (5 Gb/s and 2.5 Gb/s) data bits are D_n , as shown in Figure 191–10. The DS_n are applied as an additive PCS scrambler sequence to each incoming data bit, D_n , to generate a single scrambled data bit, A_n , as shown in Equation (191–1).

$$A_n = DS_n \oplus D_n \quad (191-1)$$

191.3.2.2.19 PCS scrambler polynomial

The PHY_S HS_TX PCS Transmit process shall employ Equation (191–2) as PHY_S HS_TX transmitter side-stream scrambler generator polynomial. Equation (191–2) is applied regardless of whether PHY_S HS_TX is Leader or Follower.

$$g_S(x) = 1 + x^{20} + x^{33} \quad (191-2)$$

An implementation of side-stream scramblers by linear-feedback shift registers is shown in Figure 191–13. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA TRAINING STATE, shall continue to run uninterrupted during transition from SEND_T to SEND_N.

Side-stream scrambler employed by the PHY_S Transmit

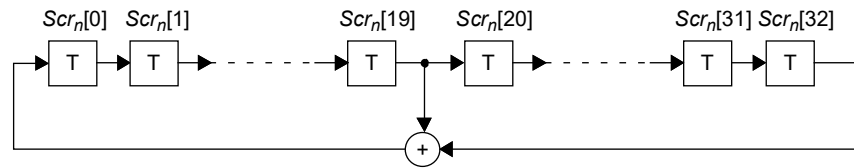


Figure 191–13—PHY_S realization of side-stream scramblers by linear feedback shift registers

191.3.2.2.20 Gray mapping for PAM4 encoding

For 10 Gb/s transmit rate, bit pairs shall be gray-mapped for PAM4 encoding as specified in 149.3.2.2.19.

191.3.2.2.21 Selectable precoder

For 10 Gb/s transmit rate, gray-coded PAM4 symbols shall be precoded as specified in 149.3.2.2.20.

191.3.2.2.22 PAM4 encoding

For 10 Gb/s transmit rate, precoded PAM4 symbols shall be encoded as specified in 149.3.2.2.21.

191.3.2.2.23 PAM2 encoding

The PCS Transmit process shall encode each output symbol to one of two PAM2 levels as specified in this subclause.

The PAM2 encoded symbols are denoted $M(n)$, where:

n is an index indicating the symbol number.

Each consecutive output symbol, A_n , is mapped to one of two PAM2 levels and assigned to the PAM2 encoder output $M(n)$.

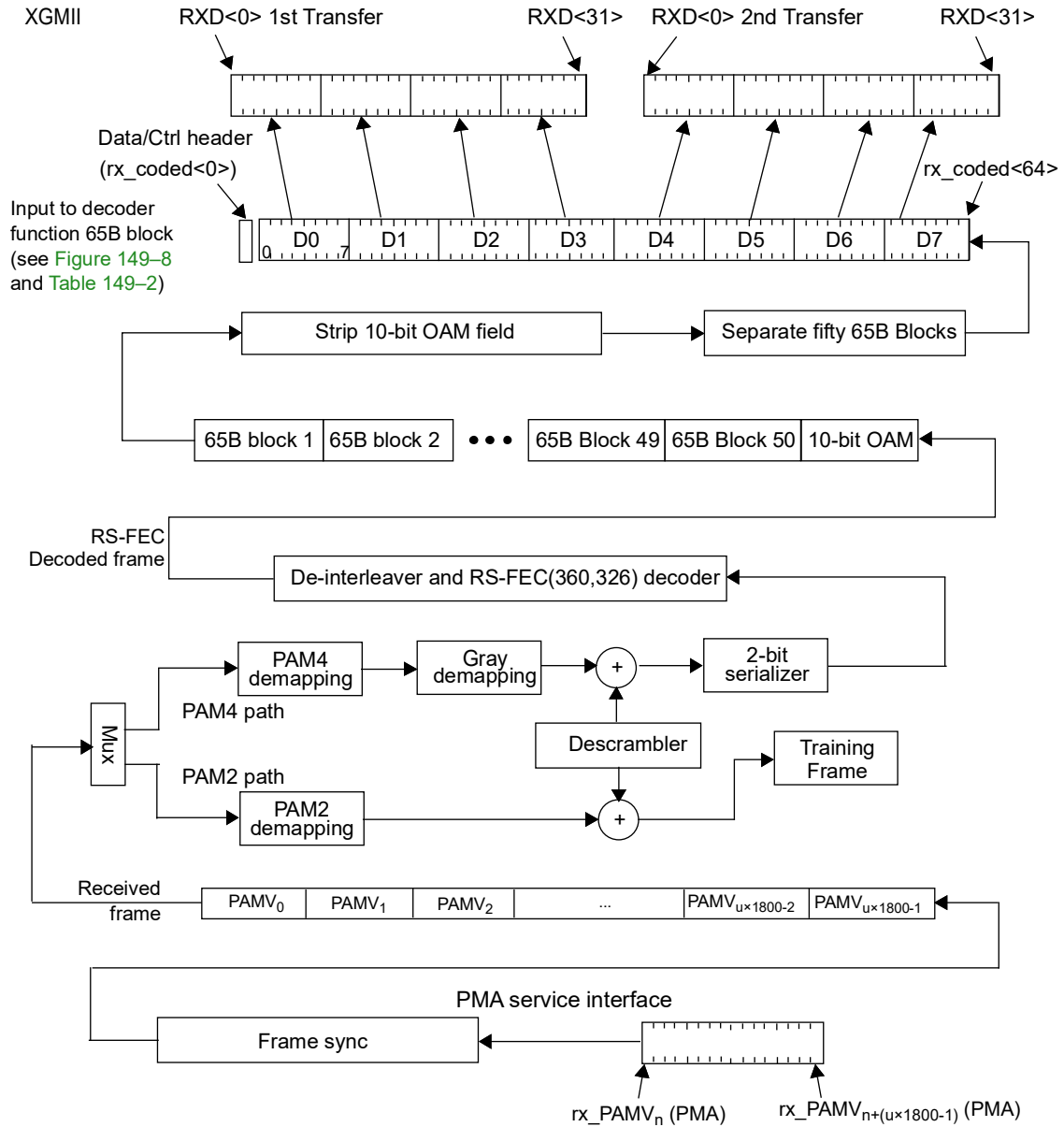
Mapping from the output symbol A_n to a PAM2 encoded symbol $M(n)$ is as follows:

- 0 maps to +1, and
- 1 maps to −1.

191.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 191–20 and the PCS Receive bit ordering in Figure 191–14 for 10 Gb/s and Figure 191–15 for 5 Gb/s and 2.5 Gb/s. Conformance includes compliance with the associated state variables as specified in 191.3.5.1.2.

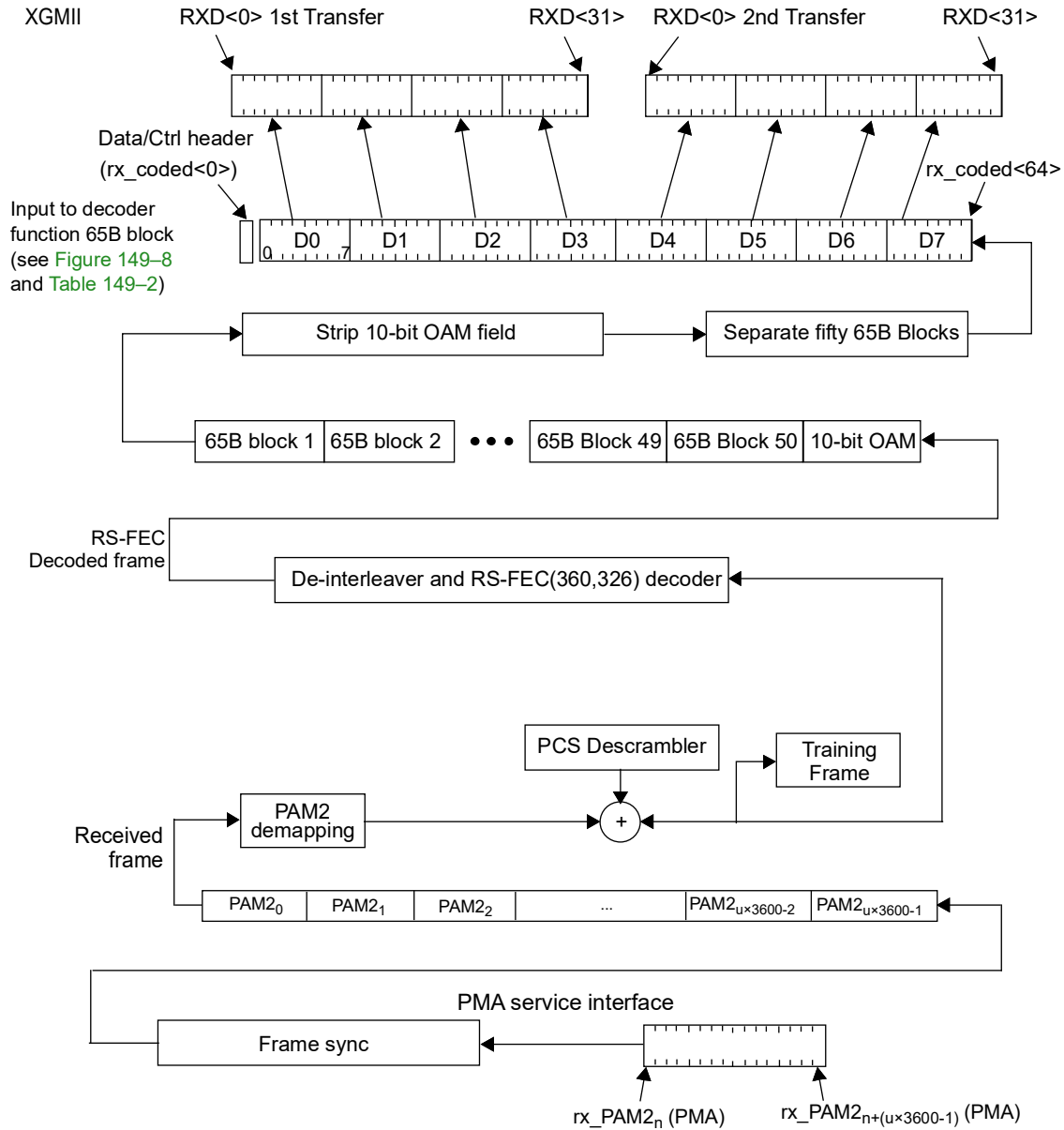
The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received symbols are demapped and descrambling is performed.



NOTE 1—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the XGMII.
NOTE 2—Figure shown for L = 1.
NOTE 3—For RS-FEC Frame, V=4 and u=1. For Training Frame, V=2 and u=4.

Figure 191-14—PCS 10 Gb/s Receive bit ordering for data mode and training mode, HS_RX

Following descrambling, the L-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. The decoder marks frames that cannot be corrected with error symbols. The RS-FEC decoded frame is then separated into a 10-bit OAM field and 50 64B/65B blocks. This process generates the 64B/65B block vector $rx\_coded<64:0>$, which is then decoded to form the XGMII signals $RXD<31:0>$ and $RXC<3:0>$ as specified in the PCS 64B/65B Receive state diagram (see Figure 191-20). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA



NOTE 1—This figure shows the mapping from a 64B/65B block a block containing eight data characters to the XGMII.
NOTE 2—Figure shown for $L = 1$.
NOTE 3—For RS-FEC Frame $u=1$. For Training Frame $u=2$.

Figure 191-15—PCS 5G and 2.5G Receive bit ordering for data mode and training mode, HS_RX

sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and indicates that the PCS descrambler state has been acquired by setting the `scr_status` parameter `PMA_SCRSTATUS.request` primitive to OK. Descrambler acquisition is a prerequisite to RS-FEC block lock and should be robust to bit errors without RS-FEC.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor state diagram shown in Figure 191–18 monitors the received signal for high RS-FEC frame error ratio. The monitor state diagram asserts `hi_rfer` to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, `block_lock` is de-asserted. `block_lock` is re-asserted upon detection of a valid RS-FEC frame. When `block_lock` is asserted and `hi_rfer` is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(`loc_rcvr_status`). When `loc_rcvr_status` indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets `block_lock` to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment bit every 450 PAM2 symbols, which is aligned with the PCS partial PHY frame boundary, as well as an Infofield, which is inserted in the 16th PCS partial PHY frame. When the PCS Synchronization process is synchronized to this pattern, `block_lock` is asserted.

191.3.2.3.1 Frame and block synchronization

When operating in the data mode, a 100M+10GBASE-T1/V1 PHY's HS_RX PCS shall form a PAM4 stream from the PMA_UNITDATA.indication primitive by concatenating indications in order from `rx_PAM4_0` to `rx_PAM4_1799` (see Figure 191–14). It obtains block lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

When operating in the data mode, a 100M+2.5GBASE-T1/V1 PHY and a 100M+5GBASE-T1/V1 PHY's HS_RX PCS shall form a PAM2 stream from the PMA_UNITDATA.indication primitive by concatenating indications in order from `rx_PAM2_0` to `rx_PAM2_3599` (see Figure 191–15). It obtains block lock to the PHY frames during PAM2 training using synchronization bits provided in the training frames.

191.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. PHY_D shall employ the receiver descrambler generator polynomial defined by Equation (191–2). Equation (191–2) is applied regardless of whether PHY_D is Leader or Follower.

191.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

- a) The block type field contains a reserved value.
- b) Any control character contains a value not in Table 149–2.
- c) Any O code contains a value not in Table 149–2.
- d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 191.3.2.2.13. If the check fails the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

191.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously according to the appropriate rate's transmit bit ordering diagram (Figure 191–11 or Figure 191–12), with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero.

When the receiver PCS is operating in test-pattern mode it shall receive continuously according to the appropriate rate's receive bit ordering diagram (Figure 191–14 or Figure 191–15). The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 in 191.6.1.

191.3.4 HS_PATH PMA training frame

During PMA training, the training frames are embedded with indicators to establish alignment to the RS-FEC superframe composed of 16 partial PHY frames that comprise the block. The last partial PHY frame is embedded with an information field used to exchange messages between link partners.

For 10 Gb/s, the timing relationship among training frame, partial frame, RS-FEC frame, superframe, and partial PHY frame count (PFC24) are shown in Figure 191–16.

For 2.5 Gb/s and 5 Gb/s, the timing relationship among training frame, partial frame, RS-FEC frame, superframe, and partial PHY frame count (PFC24) are shown in Figure 191–17.

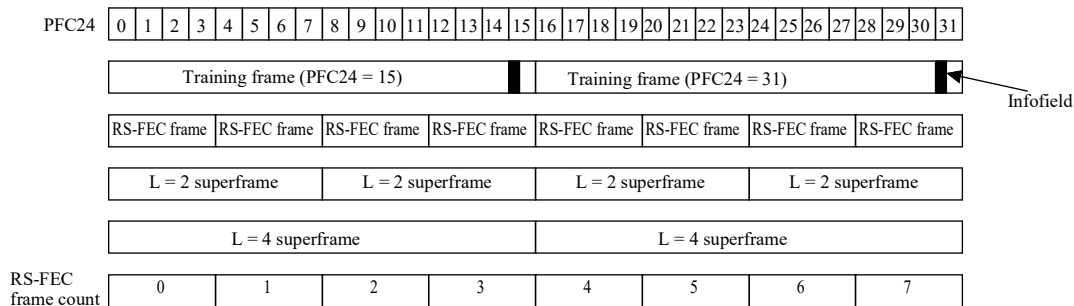


Figure 191–16—Timing relationship to PFC24 for 10G

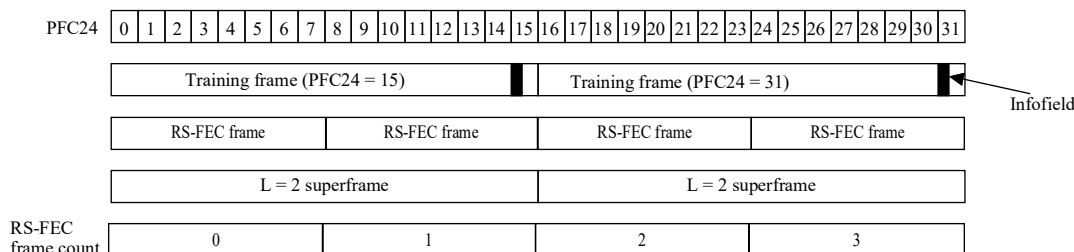


Figure 191–17—Timing relationship to PFC24 for 2.5G and 5G

PMA training frame encoding is based on the generation, at time n , of the bit S_n . The first bit is inverted in the first 15 partial PHY frames of each RS-FEC block. The first 96 bits of the 16th partial PHY frame are

XORed with the contents of the Infofield. Each partial PHY frame is 450 bits long, beginning at S_n where $(n \bmod 450) = 0$. See Equation (191-3).

$$S_n = \begin{cases} \text{Scr}_n[0] \oplus \text{Infofield}_{(n \bmod 450)} & 6750 \leq (n \bmod 7200) \leq 6845 \\ \text{Scr}_n[0] \oplus 1 & \text{else if } (n \bmod 450) = 0 \\ \text{Scr}_n[0] & \text{otherwise} \end{cases} \quad (191-3)$$

191.3.4.1 Generation of symbol T_n

The bit S_n is mapped to the transmit symbol T_n as follows, if $S_n = 0$ then $T_n = +1$, if $S_n = 1$ then $T_n = -1$.

191.3.4.2 PMA training mode PCS descrambler polynomials

The PHY shall acquire PCS descrambler state synchronization to the PAM2 training sequence and report success through `scr_status`. For PCS descrambling, the high speed receiver employs the receiver PCS descrambler generator polynomial per 191.3.2.3.2.

191.3.5 Detailed functions and state diagrams

191.3.5.1 State diagram parameters

191.3.5.1.1 Constants

EBLOCK_R<71:0>

72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>

65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>

72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>

65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

RFER_CNT_LIMIT

TYPE: Integer

VALUE: 16

Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT

TYPE: Integer

VALUE: 88

Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>

72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.

The Link Interruption ordered set is defined in 46.3.4.

191.3.5.1.2 Variables

block_lock

Boolean variable that is set TRUE by the PCS Synchronization process when it acquires block delineation. It is passed to the PMA via the block_lock parameter of the PMA_PCSSYNC.request primitive.

hi_rfer

Boolean variable that is set TRUE by the PCS Synchronization process when the rfer_cnt reaches 16 errors in one RFRX_CNT_LIMIT interval. It is passed to the PMA via the rfer_cnt parameter of the PMA_PCSSYNC.request primitive.

pcs_data_mode

Generated by the PMA PHY Control function and indicates whether or not the local PHY may transition its PCS state diagrams out of their initialization states. The current value of the pcs_data_mode is passed to the PCS via the PMA_PCSDATAMODE.indication primitive.

Values:

TRUE: The PCS is transmitting and receiving data from the XGMII.
FALSE: The PCS is in a training or test mode.

pcs_reset

Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rx_coded<64:0>

Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>

Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

rf_valid

Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

tx_coded<64:0>

Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 149–8. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>

Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

191.3.5.1.3 Functions

DECODE(rx_coded<64:0>)

In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the

RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector `rx_raw<71:0>`, which is sent to the XGMII. The DECODE function decodes the block based on code specified in 149.3.2.2.2.

ENCODE(`tx_raw<71:0>`)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector `tx_coded`. The ENCODE function encodes the block as specified in 191.3.2.2.2.

R_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 65-bit `rx_coded` vector as belonging to one of the five types {C, S, T, D, E} depending on its contents.

A vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

- a) A block type field of 0x1E and eight valid control characters other than /E/;
- b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
- c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

- a) A block type field of 0x33 and four valid control characters;
- b) A block type field of 0x66 and a valid O code;
- c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

E; The vector does not meet the criteria for any other value, or is part of an invalid RS-FEC frame, see 191.3.2.3.3.

A valid control character is one containing a MultiGBASE-T1 control code specified in Table 149–2. A valid O code is one containing an O code specified in Table 149–2.

R_TYPE(`rx_coded<64:0>`)

Returns the R_BLOCK_TYPE of the `rx_coded<64:0>` bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the `rx_coded` vector immediately following the current `rx_coded` vector.

T_BLOCK_TYPE = {C, S, T, D, E}

This function classifies each 72-bit `tx_raw` vector as belonging to one of the five types {C, S, T, D, E} depending on its contents. A vector belongs to only one type.

Values: C; The vector contains one of the following:

- a) Eight valid control characters other than /O/, /S/, /T/, and /E/;
- b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
- c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A `tx_raw` character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 149–2. A valid ordered set

consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 149–2.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

191.3.5.1.4 Counters

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt

Count number of Reed-Solomon frames received during current period.

191.3.5.1.5 Messages

RX_FRAME

A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

191.3.5.2 State diagrams

The RFER monitor state diagram shown in Figure 191–18 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 191–19 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

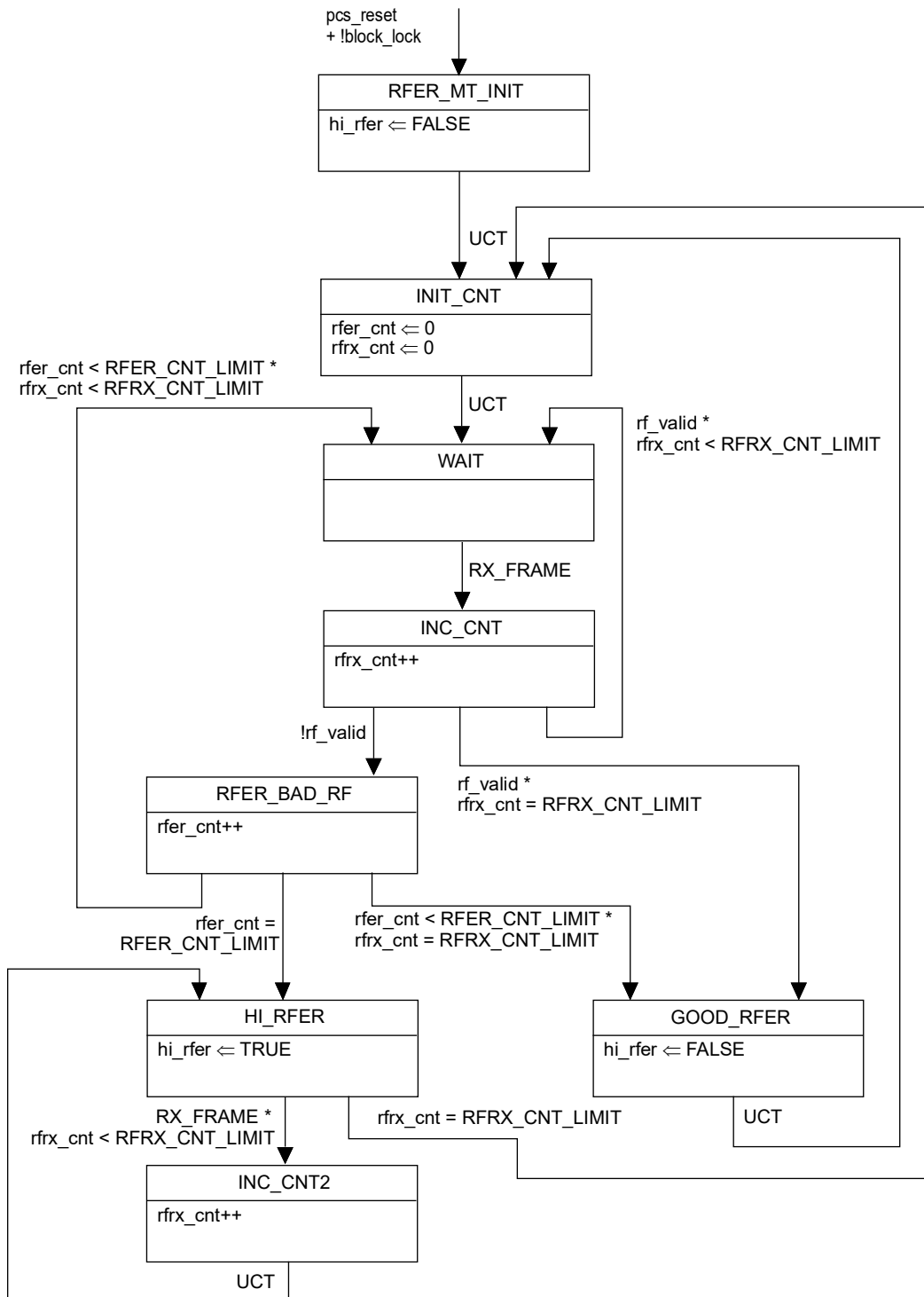


Figure 191–18—RFER monitor state diagram

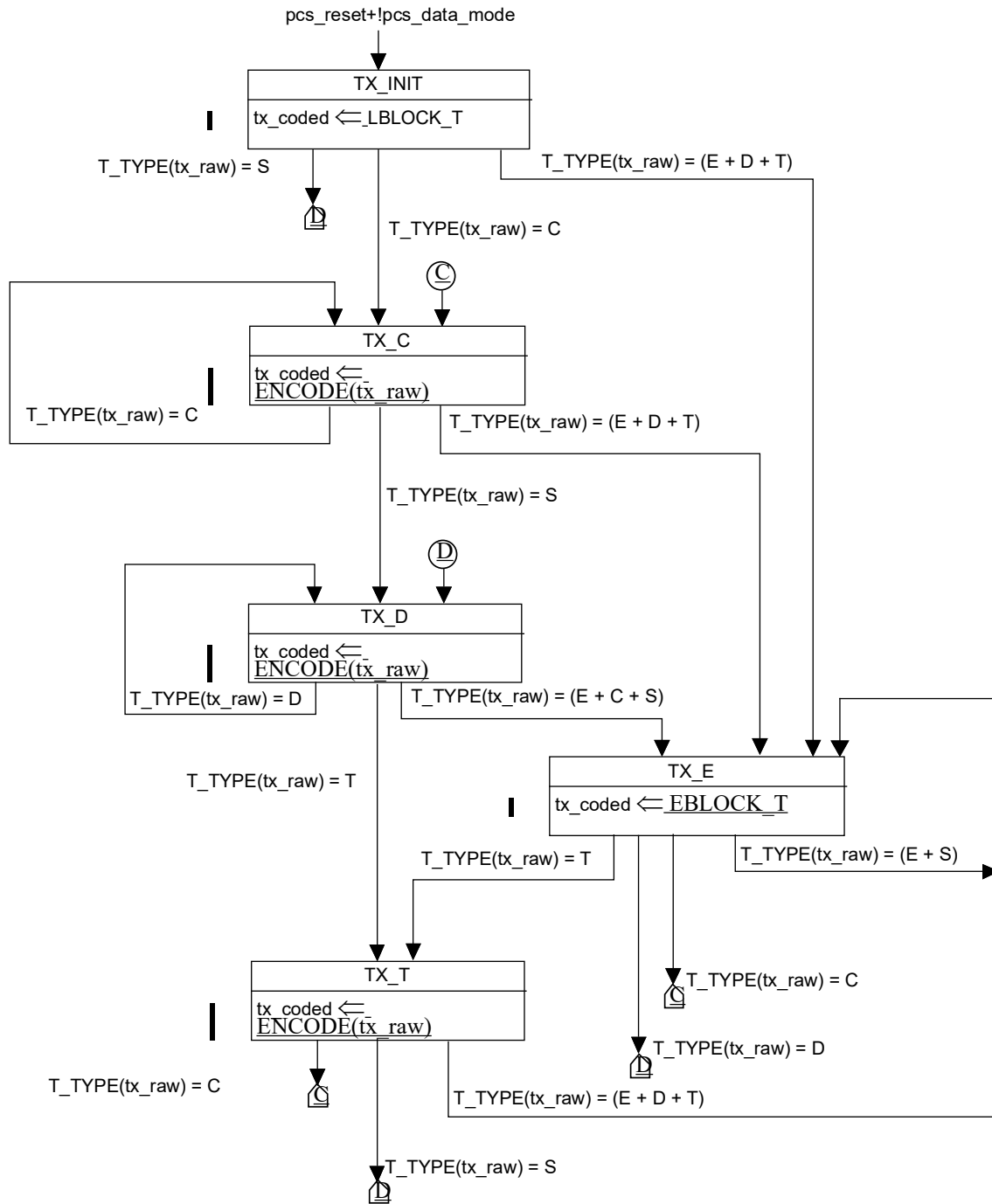


Figure 191-19—PCS 64B/65B Transmit state diagram

The PCS 64B/65B Receive state diagram is shown in Figure 191-20 and controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed except for the transition from RX_WE to RX_E, which occurs immediately after the RX_WE processes are complete.

The PCS shall monitor for errors in the RS-FEC decoding as specified in Figure 191–18.

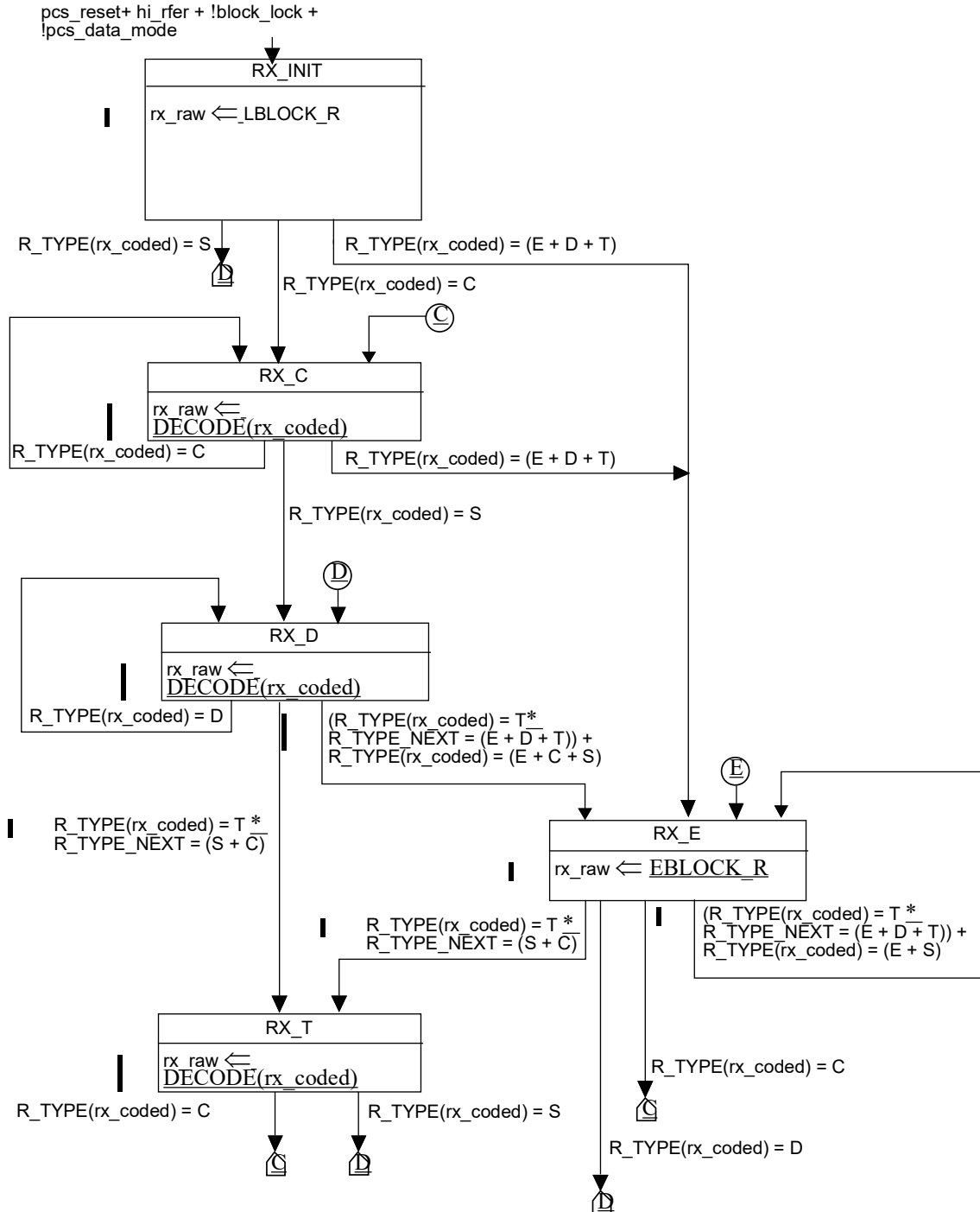


Figure 191–20—PCS 64B/65B Receive state diagram

191.3.6 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

191.3.6.1 Status

pcs_status:

Boolean variable that indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO bit 3.2323.2 and the inverse of this status is reflected in MDIO bit 3.2323.7.

block_lock:

The state diagram variable block_lock (see 191.3.5.1.2) status. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:

The state diagram variable hi_rfer (see 191.3.5.1.2) status. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

191.3.6.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:

6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 191–18) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

191.3.7 PHY_S operations, administration, and maintenance (OAM)

The PHY_S PCS level operations, administration, and maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and messages. When OAM is implemented, behavior shall be as defined in 149.3.9, including the state diagrams in Figure 149–24 and Figure 149–25.

The OAM frame data is carried in the OAM 10-bit field described in 191.3.2.2.13 for HS_PATH.

OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one at a time into the OAM field in each Reed-Solomon frame in the HS_PATH and LS_PATH.

191.3.7.1 Definitions

The definitions for OAM are as defined in 149.3.9.1 for OAM frame, OAM symbol, OAM message, and OAM status.

OAM_field: A 10-bit field in each RS-FEC frame reserved for the OAM symbol as described in 191.3.2.2.13.

191.3.7.2 Functional specifications

PHY_S OAM functions shall be as defined for a MultiGBASE-T1 PHY in 149.3.9.2 with the exception that the PHY_S OAM frame structure, PHY health, and PHY health indicator are defined in 191.3.7.2.1, 191.3.7.2.2, and 191.3.7.2.3, respectively.

191.3.7.2.1 PHY_S OAM frame structure

The PHY_S OAM frame structure is defined in 149.3.9.2.1 with the removal of Low Power Idle operation.

Each OAM frame is made up of 16 OAM symbols. Each of the first 14 symbols is made up of one octet of data, one framing bit, and one reserved bit. The last 2 symbols are the Reed-Solomon (16,14) parity symbols.

One OAM symbol is placed in the 10-bit OAM field in each PHY frame during normal power operation in the data mode. The sixteen OAM symbols are consecutively inserted into sixteen consecutive PHY frames. Once the sixteen symbols of the current OAM frame are inserted, the sixteen symbols of the next OAM frame are inserted. This process is continuous without any break in the insertion of OAM symbols.

When the PCS frame is operating in interleaved mode of 2x or 4x, the first symbol (OAM<0>) is inserted in the first RS frame in the superframe so that the full OAM frame can be packed into eight superframes in the 2x interleaved mode, and into four superframes in the 4x interleaved mode.

Bit 0 of each OAM symbol is the first bit transmitted in the 10-bit OAM field. Symbol 0 is the first symbol transmitted in each OAM frame.

The OAM frame boundary can be found at the receiver by looking at bit D8. The boundary is a 0 followed by thirteen 1's followed by two don't care.

If OAM is not implemented then the 10-bit OAM field is set to all 0's. If the link partner does not implement OAM, the 10-bit OAM field will remain static.

191.3.7.2.2 PHY health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

The PHY sets this status to indicate the status of the receiver. The definitions of good, marginal, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame
- 01: Reserved
- 10: PHY SNR is marginal
- 11: PHY SNR is good

191.3.7.2.3 PHY health indicator

The PHY current health is sent to the link partner on a per OAM frame basis using the SNR<1:0> bits as described in 191.3.7.2.2. It lets the link partner have an early indication of potential problems that can cause the PHY to drop link or have high error rates.

191.3.7.3 State diagram variable to OAM register mapping

See 149.3.9.3.

191.3.7.4 Detailed functions and state diagrams

See 149.3.9.4.

191.4 Physical Coding Sublayer (PCS) functions, low speed path (LS_PATH)

191.4.1 PCS service interface (XGMII)

The LS_TX PCS service interface allows the PHY_D PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46. The nominal transmit or receive bit rate of the XGMII for the LS_Path is 100 Mb/s.

191.4.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions, one of which is the LS_PATH and the other is the HS_PATH. This subclause discusses the LS_PATH. The LS_PATH PCS comprises the following functions: PCS Reset, LS_TX PCS Transmit in the PHY_D device, LS_RX PCS Receive in the PHY_S device, and an optional PCS OAM. All operating functions start immediately after the successful completion of the PCS Reset function.

The PHY_D PCS reference diagram, Figure 191–8, and PHY_S PCS reference diagram, Figure 191–7, show how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 191–8 and Figure 191–7.

191.4.2.1 PCS Reset function

See 191.3.2.1.

191.4.2.2 PCS Transmit function

The PCS Transmit function shall comply with the PCS 64B/65B Transmit state diagram in Figure 191–19 and to the PCS Transmit bit ordering in Figure 191–22.

When communicating with the XGMII, the PHY_D PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals. Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format.

After mapping the eight XGMII transfers to 64B/65B blocks, the subsequent functions of the PCS Transmit process take one group of four 65B blocks and append a 10-bit OAM field followed by a 6-bit CRC field. This forms the input to RS-FEC which adds 24 parity bits. The resulting 300 bits are then scrambled. These bits are then sent one bit at a time. Transmit data-units are sent to the PMA service interface via the PMA_UNITDATA.request primitive.

In each symbol period, when communicating with the PMA, the PCS Transmit generates a symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T , is $1000 \div 117.1875$ ns.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a Z symbol at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (S_n) defined in 191.4.4 to the PMA via the PMA_UNITDATA.request primitive.

During training mode an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes requests for remote transmitter settings. (See 191.5.2.4.4.)

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control. During transmission, four blocks of 65B encoded bits are appended with a 10-bit OAM field followed by a 6-bit CRC field to form the RS-FEC input frame. During data encoding, PCS Transmit utilizes Reed-Solomon encoders to generate and append 24 parity check bits to form 300-bit (50,46,6) RS-FEC frames.

A block diagram of the low speed path PCS Transmit functions is shown in Figure 191–21.

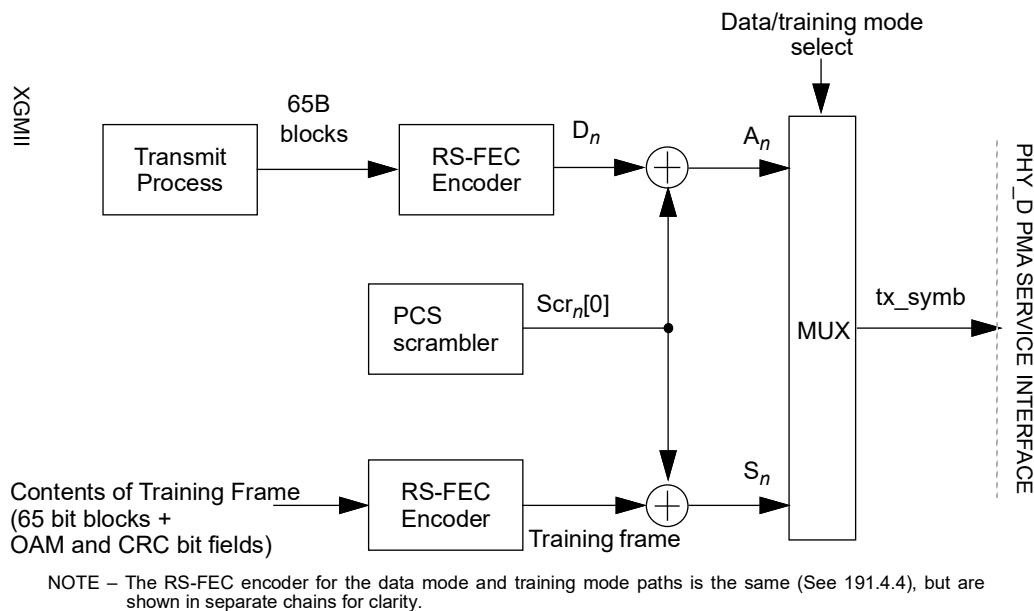


Figure 191–21—PCS Transmit function block diagram for low speed path

191.4.2.2.1 Use of blocks

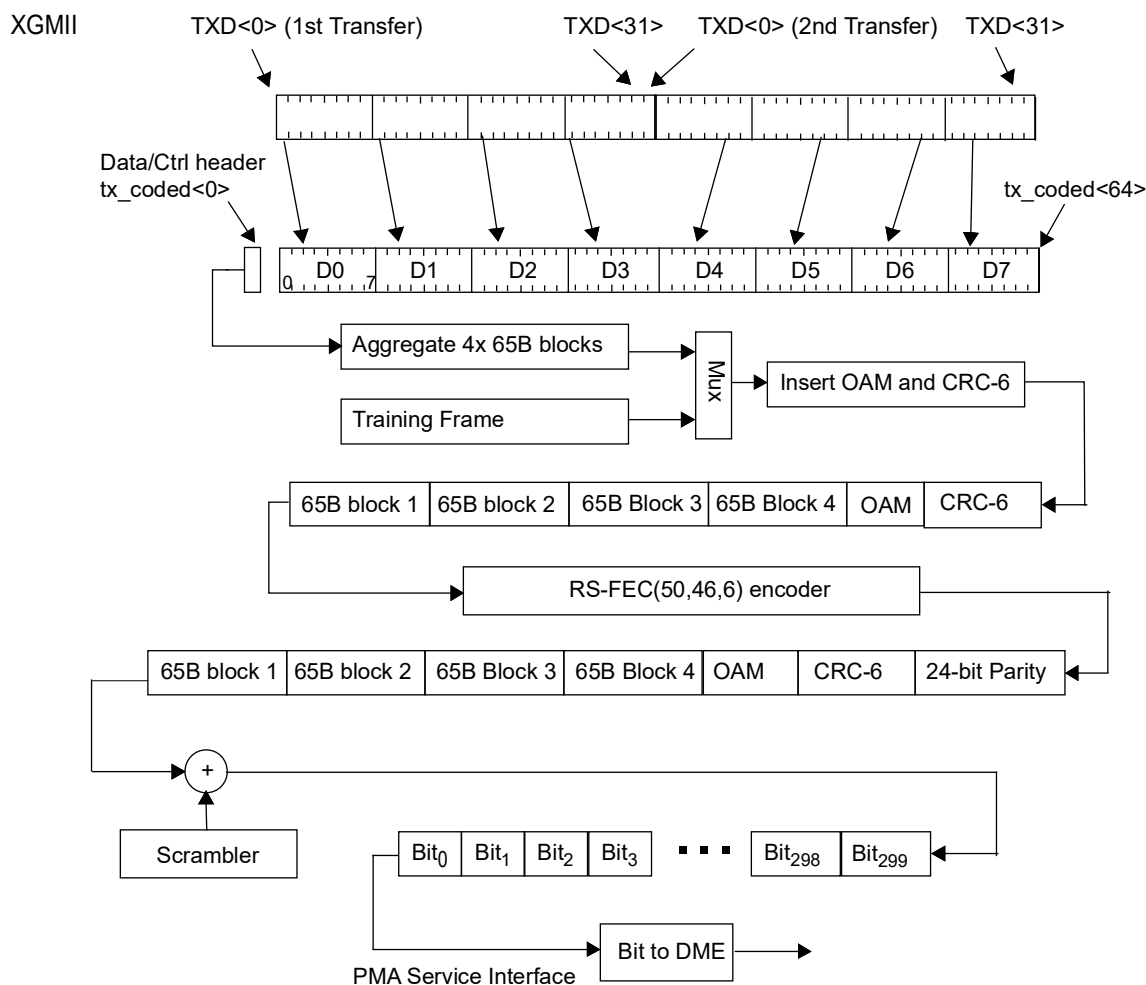
The PCS Transmit function maps XGMII signals into 65-bit blocks that are inserted into an RS-FEC frame. The PCS Receive function extracts the 65-bit blocks from the RS-FEC frame and maps them to the receiver XGMII interface. The PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS.

The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 149.3.2.2.4.

191.4.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is illustrated in Figure 191–22 for transmit and Figure 191–23 for receive. These figures illustrate the processing of a multiplicity of blocks containing 8 data octets. See 149.3.2.2.4 for information on how blocks containing control characters are mapped.

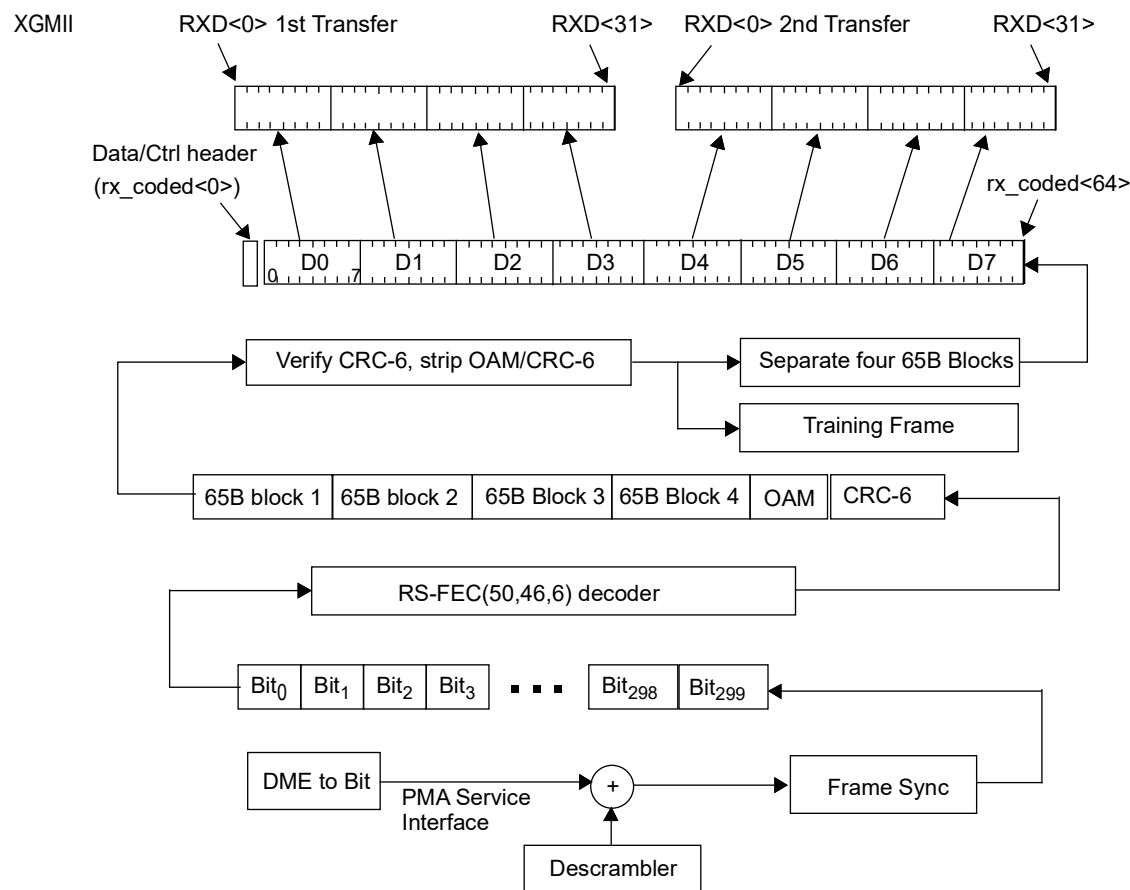


NOTE 1—Bit to DME mapping is done in the PMA.

Figure 191–22—PCS Transmit bit ordering for data mode and training mode, LS_TX

191.4.2.2.3 Notation conventions

In all figures, for values shown as binary, the leftmost bit is the first transmitted bit.



NOTE 1—DME to bit mapping is done in the PMA.

Figure 191-23—PCS Receive bit ordering for data mode and training mode, LS_RX

The 64B/65B encoding, encodes eight data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D_0 to D_7 . Control characters other than /O/, /S/, and /T/ are labeled C_0 to C_7 . The control character for an ordered set is labeled as O_0 or O_4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S_0 or S_4 for the same reason. The control character for terminate is labeled as T_0 to T_7 .

For PHY_D, two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

191.4.2.2.4 Block structure

See 149.3.2.2.4.

191.4.2.2.5 Control codes

The same set of control characters are supported by the XGMII and the LS_TX PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The LS_TX PCS encodes the start and terminate control characters implicitly by the block type field. The LS_TX PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The LS_TX PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to LS_TX control codes and XGMII control codes are specified in Table 149–2. The LPI Control character is not used by the PHY_D PHY. All XGMII control code values that do not appear in the table shall not be transmitted and shall be treated as an error if received.

191.4.2.2.6 Ordered sets

The low data rate ordered sets are as specified in 191.3.2.2.6.

191.4.2.2.7 Idle (/I/)

The low data rate Idle control characters shall be as specified in 149.3.2.2.7.

191.4.2.2.8 Start (/S/)

The low data rate Start control characters are as specified in 149.3.2.2.9.

191.4.2.2.9 Terminate (/T/)

The low data rate Terminate control characters are as specified in 149.3.2.2.10.

191.4.2.2.10 Ordered set (/O/)

The low data rate Ordered set control characters shall be as specified in 149.3.2.2.11.

191.4.2.2.11 Error (/E/)

The low data rate Error control characters are as specified in 149.3.2.2.12.

191.4.2.2.12 Transmit process

The transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. Eight XGMII data transfers are encoded into an RS-FEC frame. It takes 300 PMA_UNITDATA transfers to send an RS-FEC frame of data. Therefore, for PHY_D, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 2:75, then the transmit process does not need to perform rate adaptation. Where the XGMII and PMA sublayer data rates are not synchronized to that ratio, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 191–19). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to

the RS-FEC encoder and PCS scrambler. tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

191.4.2.2.13 RS-FEC framing and RS-FEC encoder

The resulting RS-FEC frame of four 65B blocks, followed by ten OAM bits, a 6-bit CRC field, and 24 parity bits is 300 bits. See Figure 191–22 and 191.4.2.2.14 for details on PCS bit ordering and RS-FEC encoding.

The RS-FEC encoding takes the 276-bit vector, consisting of tx_group4x65B, the ten OAM bits, and the six CRC bits, and shall generate the four 6-bit parity symbols (24 bits total).

191.4.2.2.14 Reed-Solomon encoder

The data frame is encoded using a Reed-Solomon encoder (see Figure 191–24) operating over the Galois Field GF(2⁶) where the symbol size is six bits. The encoder processes forty-six 6-bit RS-FEC message symbols to generate four 6-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 50 6-bit RS-FEC symbols. The particular Reed-Solomon code is denoted as RS-FEC(50,46,6).

The code is based on the generating polynomial given by Equation (191–4).

$$g(x) = \prod_{j=0}^3 (x - \alpha^j) = g_4x^4 + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (191-4)$$

In Equation (191–4), α , is a primitive element of the finite field defined by the primitive polynomial $0x43 = x^6 + x + 1$.

Equation (191–5) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{45} to m_0 .

$$m(x) = m_{45}x^{49} + m_{44}x^{48} + \dots + m_1x^5 + m_0x^4 \quad (191-5)$$

Each message symbol m_i is the bit vector $(m_{i,5}, m_{i,4}, \dots, m_{i,1}, m_{i,0})$, which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<275:0> where $m_{i,j} = \text{tx\_RSmessage} \langle (45 - i) \times 6 + j \rangle$, for $i = 0$ to 45, and $j = 0$ to 5.

tx_RSmessage<275:0> prior to RS-FEC(50,46,6) encoder is formed as follows:

tx_RSmessage<259:0> = tx_group4x65B<259:0>.
tx_RSmessage<269:260> = OAM_field<9:0>.
tx_RSmessage<275:270> = CRC_field<5:0>.

The CRC_field<5:0> contains the 6-bit CRC computed over tx_RSmessage<269:0> as specified in 191.4.2.2.15.

The first symbol input to the encoder is m_{45} .

Equation (191–6) defines the parity polynomial $p(x)$ whose coefficients are the parity symbols p_3 to p_0 .

$$p(x) = p_3x^3 + p_2x^2 + p_1x + p_0 \quad (191-6)$$

Each parity symbol p_i is the bit vector $(p_{i,5}, p_{i,4}, \dots, p_{i,1}, p_{i,0})$, which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation illustrated in Figure 191–24. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0 , is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x , $c_{49} = m_{45}$ is transmitted first and the coefficient of the lowest power of x , $c_0 = p_0$ is transmitted last. The first bit transmitted from each symbol is bit 0.

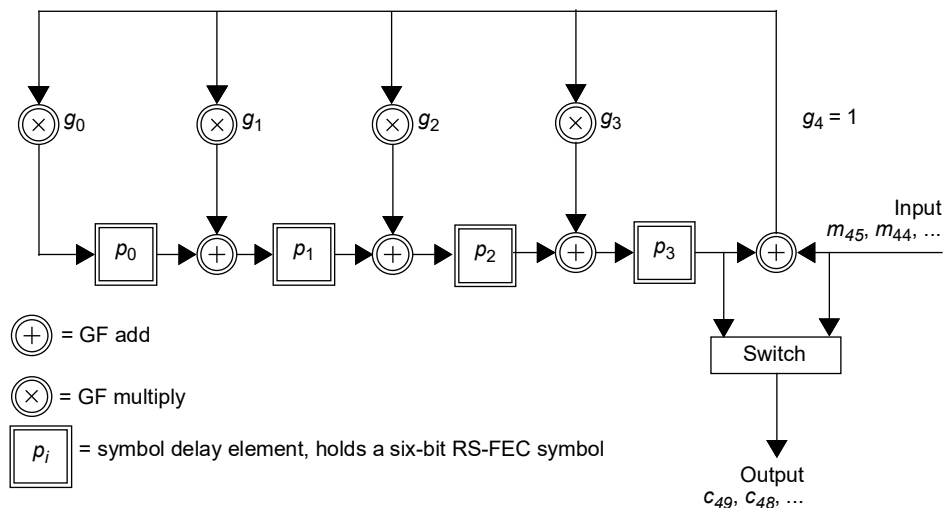


Figure 191–24—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 191–3.

Table 191–3—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(50,46,6)
0	3
1	59
2	54
3	15
4	1

191.4.2.2.15 CRC-6 calculation

For the low-speed path, a 6-bit cyclic redundancy check (CRC-6) shall be calculated over the 270 bits of information payload (comprising tx_group4x65B<259:0> and OAM_field<9:0>).

The CRC-6, shown by Equation (191–7), is the remainder of the division of the payload polynomial by the generator polynomial:

$$g(x) = x^6 + x + 1 \quad (191-7)$$

The CRC6 shall produce the same result as the implementation shown in Figure 191–25. In Figure 191–25, the 6 delay elements S0,...S5, shall be initialized to zero.

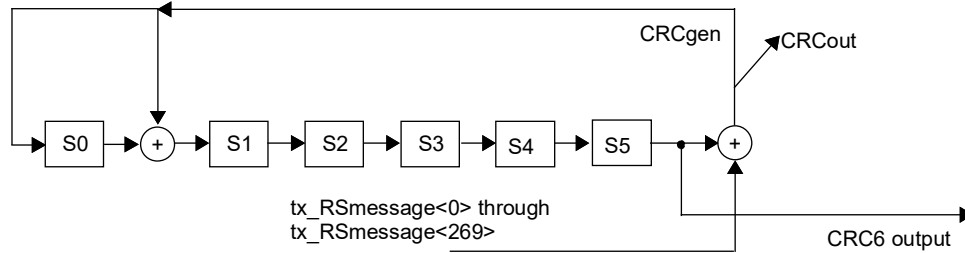


Figure 191–25—CRC6

The coefficients of the payload polynomial are mapped from tx_RSmessage<269:0> such that tx_RSmessage<0> corresponds to the highest power term (x^{269}) and tx_RSmessage<269> corresponds to the lowest power term (x^0). The division is performed serially, MSB-first. The resulting 6-bit remainder is mapped to CRC_field<5:0> where CRC_field<0> is mapped to tx_RSmessage<270> and CRC_field<5> is mapped to tx_RSmessage<275>.

191.4.2.2.16 PCS scrambler

The bits of the RS-FEC frame are scrambled using an additive PCS scrambler. For each bit, D_n , a scrambler bit is generated from the PCS scrambler. The scrambler bit, DS_n , is equal to $Scr_n[0]$ of $g_D(x)$ defined in 191.4.2.2.17.

DS_n is applied as additive scrambler sequences to incoming data bits D_n to generate the scrambled data bit A_n as shown in Equation (191–8).

$$A_n = D_n \oplus DS_n \quad (191-8)$$

The parameter tx_symb is set to A_n for passing to the PMA when PHY control is in SEND_N mode.

191.4.2.2.17 PCS scrambler polynomial

The PHY_D PCS Transmit process shall employ Equation (191–9) as PHY_D transmitter side-stream scrambler generator polynomial. Equation (191–9) is applied regardless of whether PHY_D is Leader or Follower.

$$g_D(x) = 1 + x^{13} + x^{33} \quad (191-9)$$

An implementation of side-stream scramblers by linear-feedback shift registers is shown in Figure 191–26. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter side-stream scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of

the 33-bit vector representing the side-stream scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA TRAINING STATE, shall continue to run uninterrupted during transition from SEND_T to SEND_N.

Side-stream scrambler employed by the PHY_D Transmit

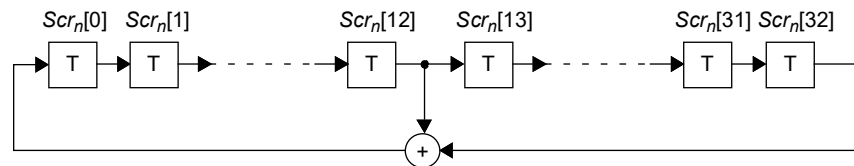


Figure 191–26—PHY_D realization of side-stream scramblers by linear feedback shift registers

191.4.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 191–20, and the PCS Receive bit ordering in Figure 191–23 including compliance with the associated state variables as specified in 191.3.5.1.2.

The PCS Receive function accepts received code-groups provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received symbols are demapped and descrambling is performed.

Following descrambling, the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. The RS-FEC decoded frame is then separated into ten OAM bits, a 6-bit CRC field, and four 64B/65B blocks. The receiver computes the CRC-6 checksum over the decoded 270 bits of information payload (comprising the four 64B/65B blocks and the ten OAM bits) and compares it with the received CRC field. If the computed CRC does not match the received CRC field, the frame is marked as invalid. This process generates the 64B/65B block vector rx_coded<64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 191–20). Two XGMII data transfers are decoded from each block. Where the XGMII and PMA sublayer data rates are not synchronized, the receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and indicates that the PCS descrambler state has been acquired by setting the scr_status parameter PMA_SCRSTATUS.request primitive to OK. Descrambler acquisition is a prerequisite to RS-FEC block lock and should be robust to bit errors without RS-FEC.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If forty consecutive RS-FEC frame errors are detected, block_lock is de-asserted. block_lock is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receive channel is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication (loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process. The PCS Synchronization process sets block_lock to indicate whether the PCS has obtained synchronization. The PMA training frame includes an alignment pattern every 300 symbols, which can be used to find the RS-Frame boundary. When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.

191.4.2.3.1 Frame and block synchronization

When operating in the training and data modes, the receiving PCS shall form a bit stream from the PMA_UNITDATA.indication primitive by concatenating requests in order from Bit₀ to Bit₂₉₉ (see Figure 191–23). PCS Receive obtains block_lock to the PHY frames during training using synchronization bits provided in the training frames.

191.4.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. PHY_S shall employ the receiver descrambler generator polynomial defined by Equation (191–9). Equation (191–9) is applied regardless of whether PHY_S is Leader or Follower.

191.4.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

- a) The block type field contains a reserved value.
- b) Any control character contains a value not in Table 149–2.
- c) Any O code contains a value not in Table 149–2.
- d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 191.4.2.2.14. If the check fails, the RS-FEC frame is invalid.

The R_BLOCK_TYPE of an invalid block is set to E.

191.4.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode, it shall transmit continuously by setting zero input and any non-zero initial condition to the PCS scrambler.

When the receiver PCS is operating in test-pattern mode, it shall receive continuously as illustrated in Figure 191–23. In the absence of errors in PMA Receive, the descrambler output should be zeros. The output of the RS-FEC decoder should also be zeros, and may correct errors in the descrambler output. Any nonzero values at the output of the RS-FEC decoder are due to uncorrectable RS-FEC frames. This mode is further described as test mode 7 in 191.6.1.

191.4.4 PMA training frame

During PMA training, the PHY operates as shown in Figure 191–21 and Figure 191–22. The four 64B/65B blocks in the FEC frame are loaded with the internal training frame, consisting of three consecutive blocks

of all zeros and the fourth block being a special control block, containing the Infocfield. The structure of the Infocfield is shown in Figure 191–33.

The fields in the Infocfield are transmitted from left to right starting with C/D. The Block field as well as fields D0 through D6 are transmitted LSB first. Reserved bits in the Infocfield represent unused values and shall be set to zero on transmit and ignored when received by the link partner.

The message and PHY capability fields are as specified in 191.5.2.5.3 and 191.5.2.5.4.

The four 65-bit blocks of the training frame, tx_group4x65B block, as defined in 191.1.3.2, are transmitted as described in 191.4.2.2.14. The four training frame 65-bit blocks are followed by the 10 OAM bits, six CRC bits, and the 24 FEC parity bits, as shown in Figure 191–27. The 6 CRC bits are computed over the 270 bits of the training frame (comprising the four 65-bit blocks and the 10 OAM bits) as specified in 191.4.2.2.15. Zeros shall be transmitted in the OAM field of the training frame. Reserved bits shall be transmitted as defined by 191.5.2.4.1. RS-FEC parity bits are generated from the training frame contents by the RS-FEC encoder specified in 191.4.2.2.14.

After the training frame is assembled, it is scrambled and DME encoded as described in 191.4.2.2.16 and 191.5.2.2.1 respectively.

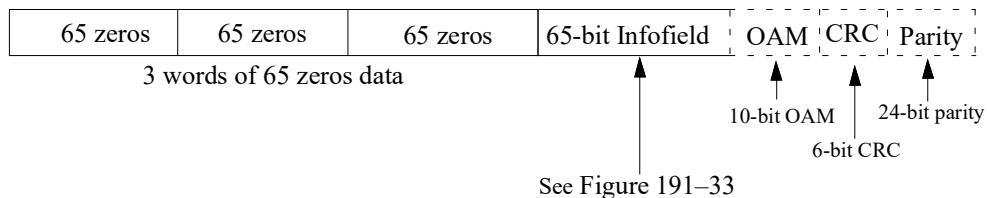


Figure 191–27—Training frame

S_n defines the training frame bit at time n , see Equation (191–10)

$$S_n = \begin{cases} Scr_n[0] \oplus \text{Infocfield}_{((n \bmod 300) - 195)} & 195 \leq (n \bmod 300) \leq 259 \\ Scr_n[0] \oplus \text{OAM}_{((n \bmod 300) - 260)} & 260 \leq (n \bmod 300) \leq 269 \\ Scr_n[0] \oplus \text{CRC}_{((n \bmod 300) - 270)} & 270 \leq (n \bmod 300) \leq 275 \\ Scr_n[0] \oplus \text{Parity}_{((n \bmod 300) - 276)} & 276 \leq (n \bmod 300) \leq 299 \\ Scr_n[0] & \text{otherwise} \end{cases} \quad (191-10)$$

191.4.4.1 PMA training mode PCS descrambler polynomials

The PHY shall acquire PCS descrambler state synchronization to the DME training sequence and report success through scr_status. For PCS descrambling, the low speed receiver employs the receiver PCS descrambler generator polynomial per 191.4.2.3.2. The resulting symbols are transferred to the PMA when PHY control is in SEND_T mode for DME encoding and transmission.

191.4.5 Detailed functions and state diagrams

Detailed functions and state diagrams are as specified for MultiGBASE-T1 PHYs in 191.3.5.

191.4.6 PCS management

See 191.3.6.

191.4.7 PHY_D operations, administration, and maintenance (OAM)

The PHY_D PCS level operations, administration, and maintenance (OAM) provides an optional mechanism useful for monitoring link operation such as exchanging PHY link health status and message exchange. When OAM is implemented, behavior is defined in 149.3.9, including the state diagrams in Figure 149–24 and Figure 149–25.

The OAM frame data is carried in the OAM 10-bit field described in 191.4.2.2.13 for LS_PATH.

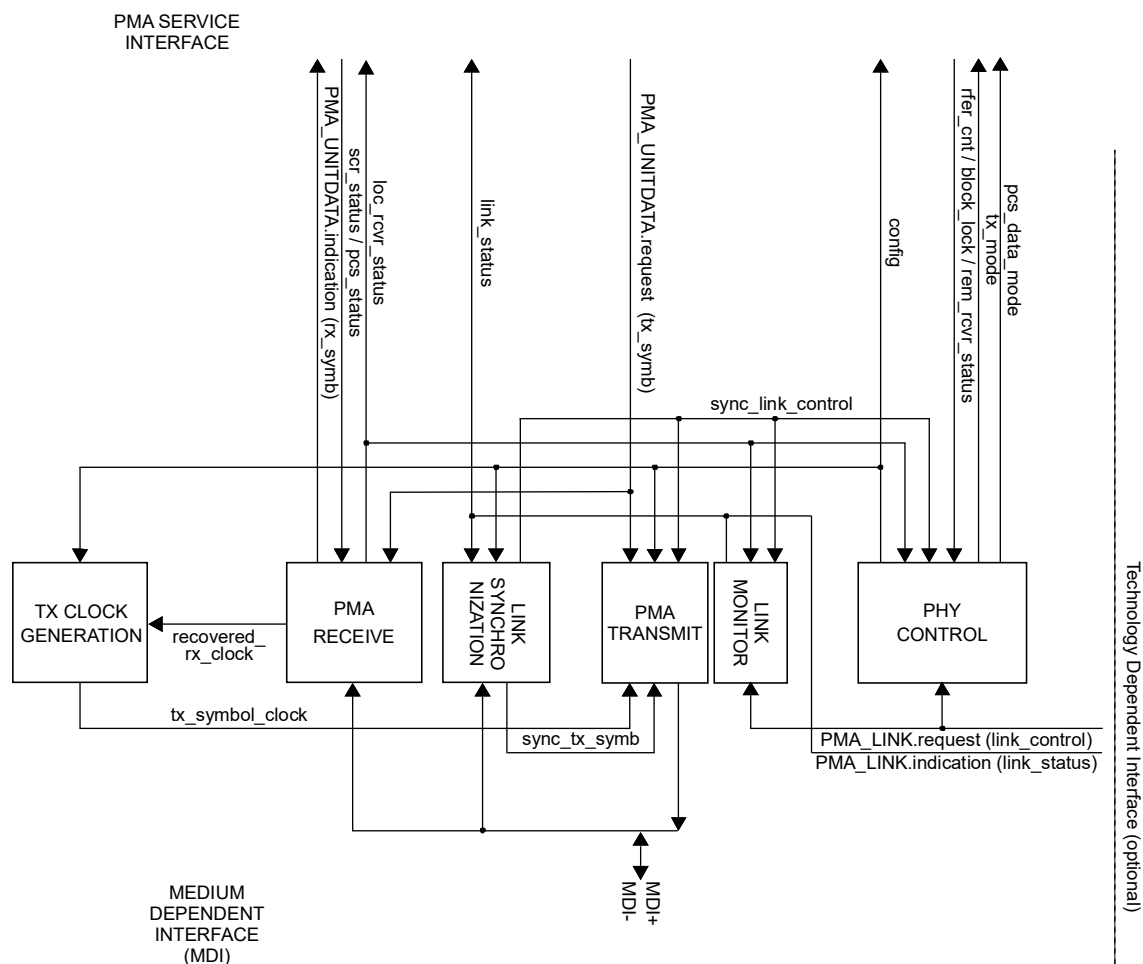
OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one at a time into the OAM field in each Reed-Solomon frame in the HS_PATH and LS_PATH.

191.5 Physical Medium Attachment (PMA) sublayer

191.5.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 191.2.2 to the MultiG+100M/100M+MultiGBASE-T1 baseband medium, specified in 191.9 and to the MultiG+100M/100M+MultiGBASE-V1 baseband medium specified in 191.10.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 191.11 for -T1 and in 191.12 for -V1.



NOTE—The tx_symbol_clock is derived from the recovered_rx_clock when the PHY is loop timed, otherwise it is derived from a local clock source.

Figure 191-28—PMA reference diagram

191.5.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Tx Clock Generation. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 191-28, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 191-28.

191.5.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

- Power for the device containing the PMA has not reached the operating state.
- The receipt of a request for reset from the management entity.

PMA Reset sets `pma_reset` = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended `pma_reset` branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The MultiG+100M/100M+MultiGBASE-T1/V1 PMA takes no longer than 50 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 191–34).

191.5.2.2 PMA Transmit function

The HS_TX PMA Transmit function comprises a transmitter to generate a two-level PAM2 signal for 2.5 Gb/s and 5 Gb/s, and a four-level PAM4 signal for 10 Gb/s. The LS_TX PMA Transmit function generates a DME modulated signal. When the PHY Control state diagram (Figure 191–34) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by `tx_symb` onto the MDI. During Link Synchronization, when `sync_link_control` = DISABLE and Auto-Negotiation is either not enabled or not implemented, the `sync_tx_symb` output by the PHY Link Synchronization function shall be used in place of `tx_symb` as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 191.6.2 for HS_TX and in 191.7.2 for LS_TX.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 191.6.2.1 for HS_TX and 191.7.2.1 for LS_TX. The Leader-Follower relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the `tx_symbol_clock` of 191.5.2.9 while meeting the jitter requirements of 191.6.2.1 for HS_TX and 191.7.2.1 for LS_TX.

Each PHY_D shall support operation as Leader, and may support operation as Follower. Each PHY_S shall support operation as Follower, and may support operation as Leader.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

When `tx_mode` is SEND_Z, see 191.7.2.7 for the encoding of “Z”.

When `tx_mode` is not SEND_Z, the PHY_D PMA Transmit function, and the PHY_S PMA Transmit function in link synchronization, shall encode binary values using Differential Manchester Encoding (DME) according to the rules in 191.5.2.2.1.

191.5.2.2.1 Differential Manchester encoding (DME)

The following rules shall apply when DME encoding is used:

- A “clock transition” is always generated at the start of each bit symbol.
- A “data transition” in the middle of a nominal bit period is generated if the bit to be transmitted is a logical '1'. Otherwise, no transition is generated until the next bit symbol.

See Figure 191–29 and Table 191–4.

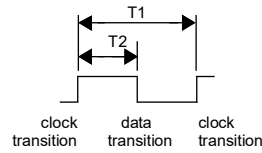


Figure 191–29—DME encoding scheme

Table 191–4—DME timings

Parameter name	Description	Nominal value ^a	Unit of measure
T1	Clock transition to clock transition	8.53	ns
T2	Clock transition to data transition (data = 1)	4.26	ns

^aSee 191.6.2.4 and 191.7.2.4 for details on bit timing tolerance.

191.5.2.3 PMA Receive function

The PMA Receive function includes a receiver for PAM4 and PAM2 for HS_RX and DME for LS_RX on the single balanced pair of conductors for -T1 or the single coax for -V1. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received at the MDI into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 191.9 for -T1 and of 191.10 for -V1.

The PMA Receive function uses the parameters pcs_status and scr_status, along with other applicable receiver status, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 191–34). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for polarity swaps.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.250.7.

191.5.2.4 PHY Control Function, HS_PATH

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control is shown in the state diagram in Figure 191–34 (see 191.5.2.6).

During PMA training (TRAINING and COUNTDOWN states in Figure 191–34), PHY Control information is exchanged between link partners with a 12-octet Infocfield, which is XORed with the first 96 bits of the

16th partial PHY frame (bits 6750 to 6845). The link partner is not required to decode every Infocfield transmitted but is required to decode Infocfields at a rate that enables the correct actions prior to the TX_SWITCH to PCS_TEST transition.

The 12-octet Infocfield shall include the fields in 191.5.2.4.2 through 191.5.2.4.7, also shown in Figure 191–30 and Figure 191–31. For 10 Gb/s and 5 Gb/s, Infocfield shall be transmitted at least 256 times with each change to octets 7 to 10. For 2.5 Gb/s, Infocfield shall be transmitted at least 128 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 191–30—Infocfield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 191–31—Infocfield COUNTDOWN format

191.5.2.4.1 Infocfield notation

For all the Infocfield notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infocfield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

191.5.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0> and so forth.

191.5.2.4.3 Partial PHY frame count (PFC24)

The partial PHY frame count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 16 partial PHY frames per PHY frame and the Infocfield is embedded within the 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 15.

PFC24 continues to run uninterrupted for the duration of the link. The resolution of PFC24 is large enough that it does not rollover during the allotted training time. However, it will rollover if allowed to run indefinitely. PFC24 is defined to rollover to 0 after it reaches 16 776 959.

191.5.2.4.4 Message Field

The Message Field is one octet. For the Leader, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_follower_tx<4>, reserved<3:0>}. For the Follower, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 191–5 for the Leader and Table 191–6 for the Follower. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 191–5 for the Leader and the first or second row of Table 191–6 for the Follower. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 191–5—Infofield Message Field valid Leader settings

PMA_state<7:6>	loc_rcvr_status	en_follower_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 191–6—Infofield Message Field valid Follower settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

191.5.2.4.5 PHY capability bits, HS_PATH

The capability bits set in PHY_S are sent to PHY_D over the HS_PATH.

When PMA_state<7:6> = 00, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 191–7 for the details.

The format of PHY capability bits is Oct10<7> = OAMen, Oct8<7:0> = VendorSpecificData[7:0], and Oct9<7:0> = VendorSpecificData[15:8].

Table 191–7—PHY capability bits, HS_PATH

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	Reserved		Reserved		Reserved	Reserved	OAMen

OAMen indicates PHY_S OAM capability is enabled. The OAMen is advertised in bit 1.2311.1. (See 45.2.1.244.5 for the definition of bit 1.2311.1.) The link partner's OAMen is advertised in bit 1.2312.1. (See 45.2.1.245.4 for the definition of bit 1.2312.1.)

The optional PHY_S OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1.

The VendorSpecificData the PHY sends to its link partner are bits 1.2316.15:0 (see 45.2.1.249). The VendorSpecificData received from the link partner are bits 1.2317.15:0 (see 45.2.1.250).

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining bits shall be reserved and are set to zero per 191.5.2.4.1.

191.5.2.4.6 Data switch partial PHY frame count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from SEND_T to SEND_N, which occurs at the start of an RS-FEC superframe. The last value of PFC24 prior to the transition is DataSwPFC24 – 1. DataSwPFC24 shall be set to an integer multiple of 16. When the value of DataSwPFC24 is a multiple of 16 the switch from SEND_T to SEND_N occurs on a PHY frame boundary. For 10 Gb/s and 5 Gb/s, DataSwPFC24 shall be a minimum of 4081 and a maximum of 4785 from the current PFC24 value. For 2.5 Gb/s, DataSwPFC24 shall be a minimum of 2033 and a maximum of 2385 from the current PFC24 value.

191.5.2.4.7 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 191–32. In Figure 191–32 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 191–32, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

191.5.2.5 PHY Control function, LS_PATH

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control is shown in the state diagram in Figure 191–34 (see 191.5.2.6).

During PMA training (TRAINING state in Figure 191–34), PHY Control information is exchanged between link partners with a 65-bit Infocfield, which is XORed with bits 195 to 259 of the PMA training frame, see

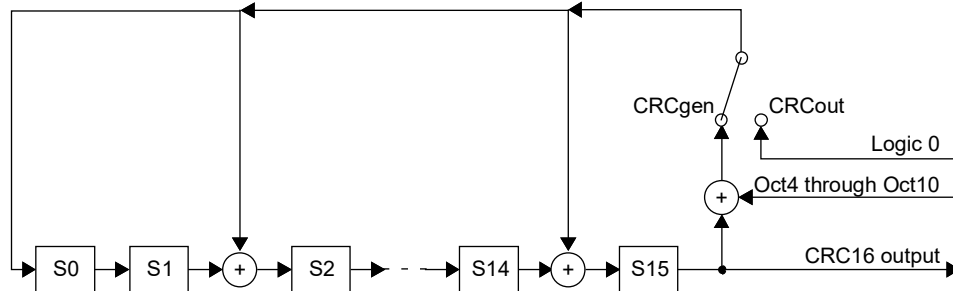


Figure 191-32—CRC16

191.4.4. The link partner is not required to decode every Infocfield transmitted but is required to decode Infocfields at a rate that enables the correct actions prior to the training to data mode transition.

The 65-bit Infocfield shall include the fields in 191.5.2.5.2 through 191.5.2.5.5, also shown in Figure 191-33. Infocfield shall be transmitted at least 128 times with each change to octets 5 to 8.

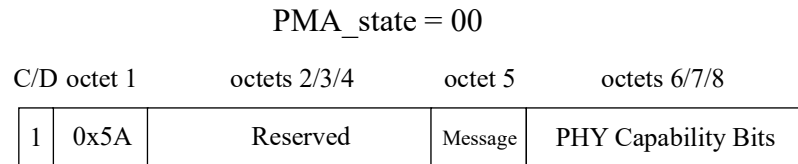


Figure 191-33—Infocfield TRAINING format, LS_PATH

191.5.2.5.1 Infocfield notation

See 191.5.2.4.1.

191.5.2.5.2 Start of Frame Delimiter

The start of Frame Delimiter consists of 9 bits [C/D<0>, Octet 1<7:0>] and shall use the hexadecimal value 0x15A.

191.5.2.5.3 Message Field

The Message Field is one octet. For the Leader, this field is represented by Oct5{PMA_state<7:6>, loc_rcvr_status<5>, en_follower_tx<4>, reserved<3:0>}. For the Follower, this field is represented by Oct5{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING.

All possible Message Field settings are listed in Table 191-5 for the Leader and Table 191-6 for the Follower; however, the PMA_state<7:6> = 01 is not used by the LS_PATH. Any value not listed in Table 191-5 for the Leader and Table 191-6 for the Follower shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 191-5 for the Leader and the first or second row of Table 191-6 for the Follower. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infocfield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

191.5.2.5.4 PHY capability bits, LS_PATH

The capability bits set in PHY_D are sent to PHY_S over the LS_PATH to control the transmitter settings on the HS_PATH.

When PMA_state<7:6> = 00, then [Oct6<7:0>, Oct7<7:0>, Oct8<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 191–8 for the details.

Table 191–8—PHY capability bits, LS_PATH

octet 6							octet 7							octet 8									
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData															Reserved	InterleaverDepth		PrecodeSel		Reserved		Reserved	OAMen

The format of PHY capability bits is Oct8<2:1> = InterleaverDepth[1:0], Oct8<4:3> = PrecodeSel[1:0], Oct8<7> = OAMen, Oct6<7:0> = VendorSpecificData[7:0], and Oct7<7:0> = VendorSpecificData[15:8].

The InterleaverDepth request the PHY sends to its link partner is bits 1.2311.12:11 (see 45.2.1.244.1). The InterleaverDepth requested by the link partner is bits 1.2312.12:11 (see 45.2.1.245.1).

When bit 1.2311.5 (see 45.2.1.244.2) is set to one, the PrecodeSel request is set in bits 1.2311.3:2 (see 45.2.1.244.4); otherwise, the PHY determines the precoder setting. The actual setting transmitted is reflected in bits 1.2310.4:3 (see 45.2.1.243.5).

The received PrecodeSel request is reported in bit 1.2312.3:2 (see 45.2.1.245.3) by the link partner.

OAMen indicates PHY_D OAM capability is enabled.

The optional PHY_D OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1. InterleaverDepth indicates the requested data mode interleaving depth. PrecodeSel indicates the requested precoder, available for 10G only.

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining PHY capability bits shall be reserved and are set to zero per 191.5.2.5.1.

191.5.2.5.5 Reserved fields

[Oct2<7:0>, Oct3<7:0>, Oct4<7:0>] are reserved and are set to zero per 191.5.2.5.1.

191.5.2.6 PHY Control function, HS_PATH and LS_PATH

The startup sequence shall comply with the state diagram description given in Figure 191–34. If the Auto-Negotiation function is not implemented, or disabled (mr_autoneg_enable = FALSE), PMA_CONFIG is

predetermined to be LEADER or FOLLOWER via management control during initialization or via default hardware setup. The Auto-Negotiation function is optional for MultiG+100M/100M+MultiGBASE-T1/V1 PHYs. If the Auto-Negotiation function is implemented and enabled, Auto-Negotiation is the source of control (via link_control), PHY_D, PHY_S, and Leader-Follower configuration; however, if Auto-Negotiation is either not enabled or not implemented, the Link Synchronization function is the source of control (via sync_link_control) and Leader-Follower configuration.

In the TRAINING state, PAM2 transmission is used for the HS_PATH and DME is used for the LS_PATH. PHY capabilities are exchanged with Infocfields as specified in 191.5.2.4.5.

At any time following the TRAINING state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control transitions to the TRAINING_FAILURE state and attempts a retrain.

The follower sets timing_lock_OK to one when it has a stable transmit clock; otherwise, timing_lock_OK is set to zero. The setting of the timing_lock_OK value is implementation specific.

The startup timing shall comply with Table 191–9 for PHY_S as Leader and Table 191–10 for PHY_D as Leader.

Table 191–9—Startup timing maximums for PHY_S as Leader

Timing interval	PHY_S (Leader) Maximum time (ms)	PHY_D (Follower) Maximum time (ms)
Entry to SILENT state until en_follower_tx = 1 is transmitted	20 - 0.384	—
Entry to exit of SILENT state	—	20
Entry to exit of TRAINING state	29.475	29.091
Entry to exit of COUNTDOWN state	0.384	—
Entry to exit of TX_SWITCH state	—	0.384
Entry to exit of PCS_TEST state	0.525	0.525
Total (Entry to SILENT to exit of PCS_TEST state)	50	50

Table 191–10—Startup timing maximums for PHY_D as Leader

Timing interval	PHY_D (Leader) Maximum time (ms)	PHY_S (Follower) Maximum time (ms)
Entry to SILENT state until en_follower_tx = 1 is transmitted	20 - 0.384	—
Entry to exit of SILENT state	—	20
Entry to exit of TRAINING state	29.475	29.091
Entry to exit of COUNTDOWN state	—	0.384
Entry to exit of TX_SWITCH state	0.384	—
Entry to exit of PCS_TEST state	0.525	0.525
Total (Entry to SILENT to exit of PCS_TEST state)	50	50

191.5.2.6.1 State diagram variables

auto_neg_imp

This variable indicates if an optional Auto-Negotiation sublayer is associated with the PMA.

Values:

TRUE: An optional Auto-Negotiation sublayer is associated with the PMA.

FALSE: An optional Auto-Negotiation sublayer is not associated with the PMA.

block_lock

This variable is defined in 191.3.5.1.2.

config

The PMA generates this variable continuously and passes it to the PCS via the PMA_CONFIG.indication primitive.

Values: LEADER or FOLLOWER.

en_follower_tx

The en_follower_tx variable in the Infocfield received by the Follower.

Values:

0: Leader is not ready for the Follower to transmit.

1: Leader is ready for the Follower to transmit.

hi_rfer

This variable is defined in 191.3.5.1.2.

infocfield_complete

This variable indicates that a complete set of Infocfield messages has been sent (see 191.5.2.4 for HS_PATH and 191.5.2.5 for LS_PATH.).

Values:

FALSE: A complete set of Infocfield messages has not been sent since PMA_state changed.

TRUE: A complete set of Infocfield messages has been sent.

link_control

This variable is defined in 191.2.1.1.1.

link_status

The link_status parameter set by PMA Link Monitor state diagram and communicated through the PMA_LINK.indication primitive.

Values: OK or FAIL.

loc_countdown_done

This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to TRUE immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive link for the local PHY.

Values:

OK: The receive link for the local PHY is operating reliably.

NOT_OK: Operation of the receive link for the local PHY is unreliable.

loc_SNR_margin	1
This variable reports whether the local device has sufficient SNR margin to continue to the next state. The criterion for setting the parameter loc_SNR_margin is left to the implementer.	2
Values:	3
OK: The local device has sufficient SNR margin.	4
NOT_OK: The local device does not have sufficient SNR margin.	5
mr_autoneg_enable	6
see 98.5.1.	7
pcs_data_mode	8
This variable is defined in 191.3.5.1.2.	9
phy_role	10
This variable indicates which side of the asymmetrical line the device is on.	11
Values:	12
PHY_S: MultiG+100MBASE-T1/V1 PHY.	13
PHY_D: 100M+MultiGBASE-T1/V1 PHY.	14
pma_reset	15
Forces reset of the PHY Control and Link Monitor state diagrams (see 191.5.2.1).	16
Values: ON or OFF.	17
PMA_state	18
Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.	19
Values:	20
00: TRAINING state	21
01: COUNTDOWN state	22
rem_countdown_done	23
This variable is set to FALSE when the PHY Control state diagram is in the DISABLE_TRANSMITTER state or SILENT state and is set to TRUE immediately after receiving the last bit of the DataSwPFC24-I partial PHY frame.	24
rem_rcvr_status	25
Variable set by the PCS Receive function to indicate whether correct operation of the receive link for the remote PHY is detected or not. The parameter rem_rcvr_status shall be set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY. The rem_rcvr_status is set to OK when remote PHY is transmitting SEND_N.	26
Values:	27
OK: The receive link for the remote PHY is operating reliably.	28
NOT_OK: Reliable operation of the receive link for the remote PHY is not detected.	29
sync_link_control	30
This variable is defined in 191.5.2.8.1.	31
training_failure	32
A Boolean variable indicating whether PHY Control has resulted in a successful training.	33
tx_mode	34
The PMA generates this variable continuously and passes it to the PCS via the	35

PMA_TXMODE.indication primitive.

Values:

- SEND_N: This value is continuously asserted when transmission of sequences of symbols representing a XGMII data stream take place.
- SEND_T: This value is continuously asserted when transmission of sequences of symbols representing the training sequences of symbols is to take place.
- SEND_Z: This value is continuously asserted when transmission of Z symbols is required.

191.5.2.6.2 State diagram timers

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT and TRAINING states, and the minimum time it stays in PCS_TEST state before normal transition to the PCS_DATA state. The timer expires $475\ \mu\text{s} \pm 50\ \mu\text{s}$ after being started.

191.5.2.6.3 State diagrams

The PHY Control state diagram is shown in Figure 191–34.

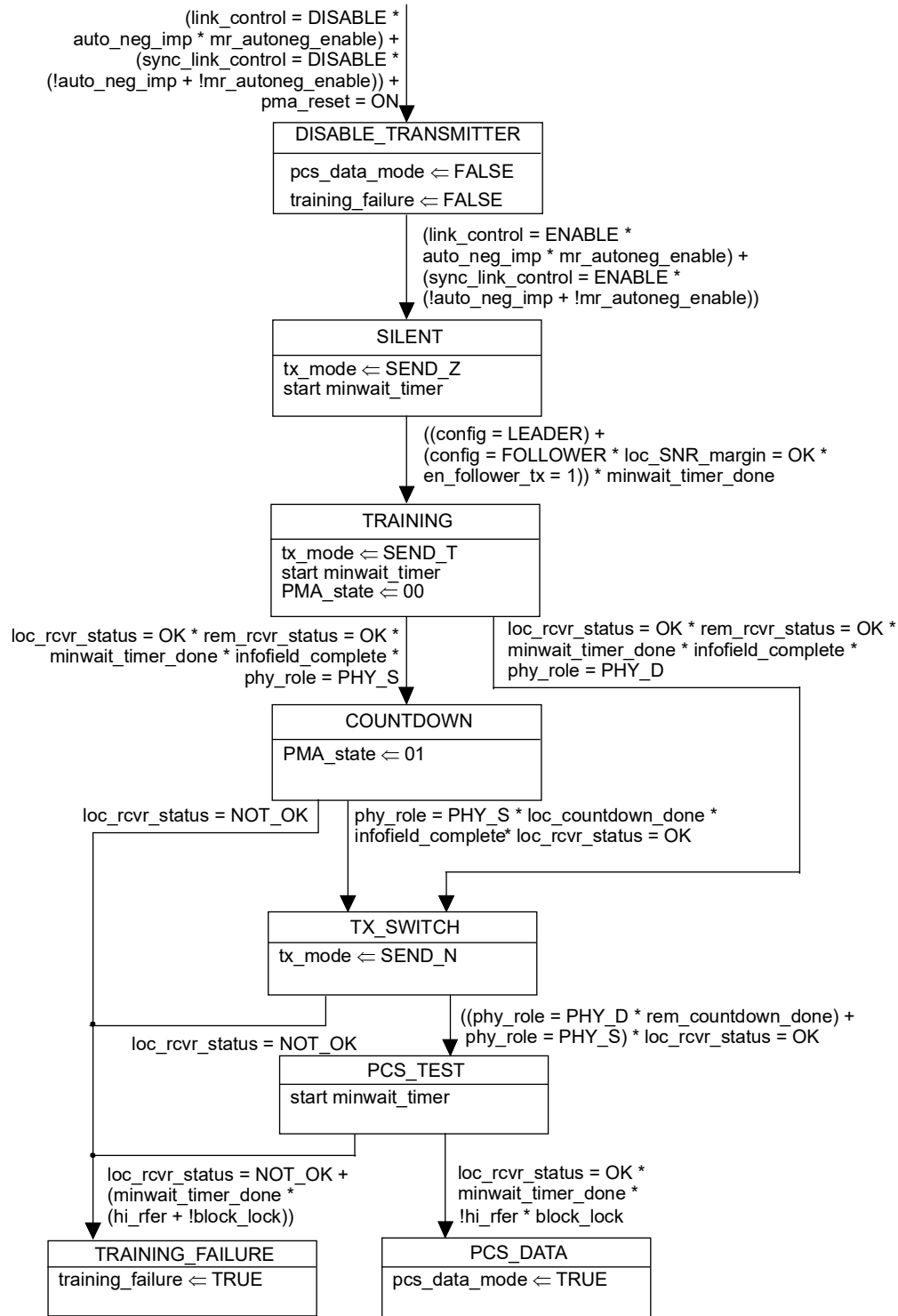


Figure 191–34—PHY Control state diagram

191.5.2.6.4 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 191–11. Mapping of MDIO status variables to PMA status variables is shown in Table 191–12.

Table 191–11—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1/V1 PMA control register	1.0.15 / 1.2309.15	pma_reset

Table 191–12—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive link status	MultiGBASE-T1/V1 PMA status register	1.2310.0	link_status

191.5.2.7 Link Monitor function

Link Monitor determines the status of the underlying receive channel and communicates it via the variable link_status. Failure of the underlying receive channel causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the Auto-Negotiation (if enabled) or Link Synchronization (if Auto-Negotiation is not enabled) process.

The Link Monitor function shall comply with the state diagram of Figure 191–35.

Upon power on, reset, or release from power down, the Auto-Negotiation function sets link_control = DISABLE, or PHY Link Synchronization algorithms set sync_link_control = DISABLE. While in LINK_DOWN state, link_status = FAIL is asserted. When the Auto-Negotiation function establishes the presence of a remote MultiG+100M/100M+MultiGBASE-T1/V1 PHY, link_control is set to ENABLE, or when the PHY Link Synchronization finishes the synchronization function, sync_link_control is set to ENABLE, and the Link Monitor state diagram begins monitoring the PCS and receiver lock status. When pcs_data_mode is TRUE, the variable link_status = OK is asserted.

191.5.2.7.1 State diagram variables

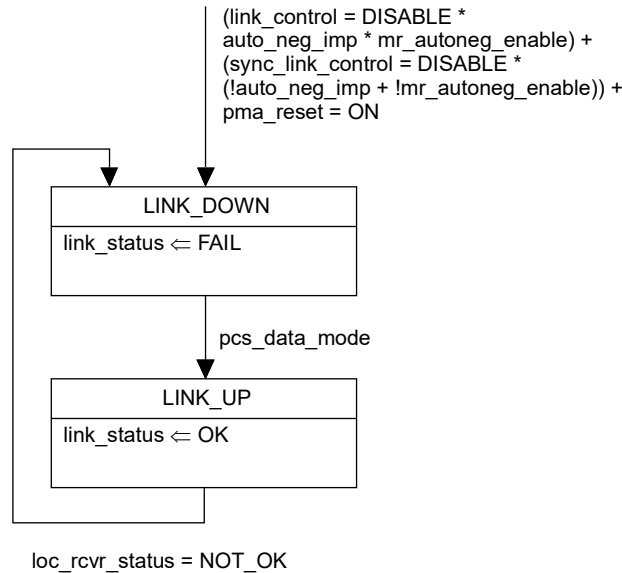
The variables defined in 191.5.2.6.1 apply to this clause.

191.5.2.7.2 State diagram timers

The timers defined in 191.5.2.6.2 apply to this clause.

191.5.2.7.3 State diagrams

The Link Monitor state diagram is shown in Figure 191–35.



NOTE—The variables $link\_control$ and $link\_status$ are designated as $link\_control\_mGigT1$ and $link\_status\_mGigT1$, respectively, by the Auto-Negotiation Arbitration state diagram (Figure 98–7) if the optional Auto-Negotiation function is implemented.

Figure 191–35—Link Monitor state diagram

191.5.2.8 PHY Link Synchronization

If the optional Clause 98 Auto-Negotiation function is disabled or not implemented, then the Link Synchronization function shall conform to the state diagram in Figure 191–38. This section describes and defines the function of Figure 191–38, the link synchronization process.

When operating, the Link Synchronization function is the data source for the PMA Transmit function (see 191.5.2.2), and uses a signal, $SEND\_S$. This signal is used by the Leader and Follower to discover the link partner and synchronize the start of PMA training. The structure of the Link Synchronization signaling is shown in Figure 191–36.

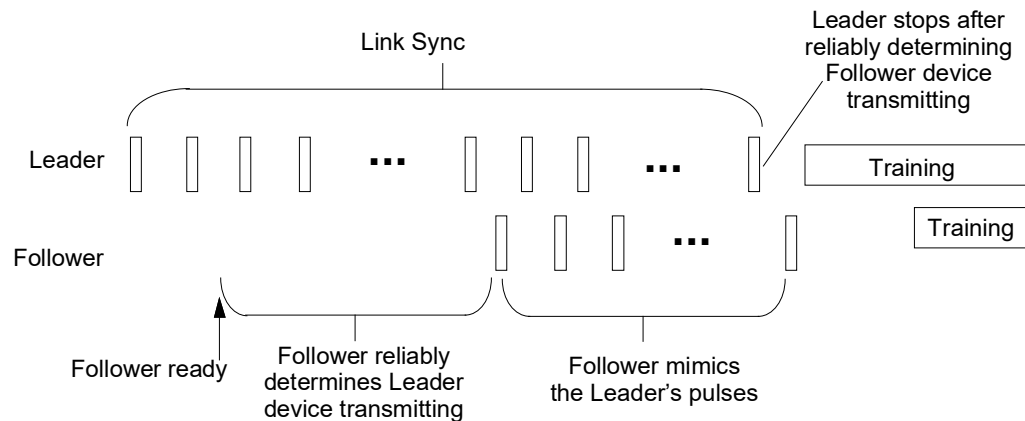


Figure 191-36—Link Synchronization signaling structure

A SEND_S pulse is defined to be a 4-bit pulse of 1001 mapped to DME symbols. The polarity of the DME symbols can be of either polarity and can vary between SEND_S pulses. At the Leader and Follower, each DME symbol time is nominally 25.6/3 ns. See 191.6.2.4 and 191.7.2.4 for details on bit timing tolerance. See 191.5.2.2.1 for details on the DME symbols.

At the Leader, SEND_S signal is defined to be a periodic signal with a SEND_S pulse (34.133 ns) followed by 116 DME symbol periods of quiet for a total of 120 DME symbol periods (1024 ns) per interval.

When the Follower detects a sufficient number of the Leader's SEND_S pulses to determine that the Leader is active, the Follower outputs one SEND_S pulse, with a delay following the detection of the Leader's most-recent SEND_S pulse. For each subsequent SEND_S pulse detected from the Leader, the Follower outputs one SEND_S pulse with timing as shown in Figure 191-37. This pattern repeats until the Leader detects a sufficient number of the Follower's SEND_S pulses to determine that the Follower is active. The Leader then enters the SILENT_WAIT state and stops transmitting SEND_S pulses as specified in Figure 191-38. Likewise, after the Follower determines that the Leader has stopped transmitting SEND_S pulses, the Follower also enters the SILENT_WAIT state.

The SEND_S pulse timing is shown in Figure 191-37.

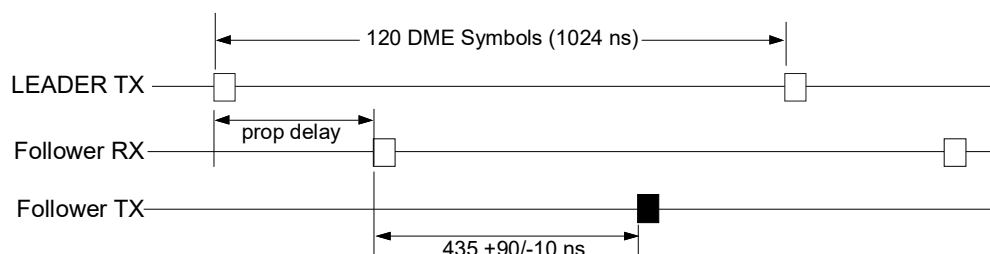


Figure 191-37—Link Synchronization timing

191.5.2.8.1 State diagram variables

force_config

This variable indicates whether the PHY operates as a Leader or as a Follower. The variable takes on one of the following values:

LEADER: This value is continuously asserted when the PHY operates as a Leader.

FOLLOWER: This value is continuously asserted when the PHY operates as a Follower.

force_phy_type

This variable indicates what speed the PHY is to operate when Auto-Negotiation is disabled or not implemented. The variable takes on one of the following values:

10G+100M: If Auto-Negotiation is disabled or not implemented and 10G+100MBASE-T1/V1 is selected.

5G+100M: If Auto-Negotiation is disabled or not implemented and 5G+100MBASE-T1/V1 is selected.

2.5G+100M: If Auto-Negotiation is disabled or not implemented and 2.5G+100MBASE-T1/V1 is selected.

100M+10G: If Auto-Negotiation is disabled or not implemented and 100M+10GBASE-T1/V1 is selected.

100M+5G: If Auto-Negotiation is disabled or not implemented and 100M+5GBASE-T1/V1 is selected.

100M+2.5G: If Auto-Negotiation is disabled or not implemented and 100M+2.5GBASE-T1/V1 is selected.

Other values are implementation-dependent and beyond the scope of this clause.

link_status

The link_status parameter is set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_autoneg_enable

see 98.5.1.

mr_main_reset

see 98.5.1.

power_on

see 98.5.1.

quiet_detect

A Boolean variable indicating whether the link partner has ceased sending SEND_S pulses.

TRUE: No more than two SEND_S pulses have been detected at the specified times (for Leader or Follower see Figure 191–37) within the preceding 5.1 μ sec.

FALSE: At least three SEND_S pulses have been detected at the specified times (for Leader or Follower see Figure 191–37) within the preceding 5.1 μ sec

send_s_sigdet

A Boolean variable indicating whether sufficient SEND_S pulses were detected with proper spacing. The definition of sufficient pulses is implementation dependent.

Values:

TRUE: Sufficient SEND_S pulses have been detected.

FALSE: Sufficient SEND_S pulses have not been detected.

single_send_s_detect	1
A Boolean variable indicating whether a SEND_S pulse has been detected.	2
Values:	3
TRUE: SEND_S pulse detected.	4
FALSE: No SEND_S pulse detected.	5
	6
sync_link_control	7
This variable indicates the data source for the PMA Transmit function.	8
Values:	9
DISABLE: The data source is the PHY Link Synchronization function (sync_tx_symb).	10
ENABLE: The data source is PMA_UNITDATA.request (tx_symb).	11
	12
training_failure	13
See 191.5.2.6.1.	14

191.5.2.8.2 State diagram timers

break_link_timer_[HSM]	17
see 98.5.2.	18
	19
follower_delay_timer	20
This timer is used to control the offset between the Follower detecting a SEND_S pulse from the	21
Leader and the Follower transmitting its SEND_S pulse reply as shown in Figure 191–36.	22
Duration: 435 +90/-10 nsec.	23
	24
leader_pause_timer	25
This timer is used to control the quiet time between SEND_S pulses from the Leader.	26
Duration: 116 DME symbol times.	27
	28
fail_inhibit_timer	29
Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a specific	30
technology link is first being established. A link is considered “failed” only if the	31
fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. This	32
timer expires 50 ms after entering the LINK_GOOD_CHECK state.	33
	34
pulse_timer	35
This timer is used to output the SEND_S pulse. Duration: 4 DME symbol times.	36
	37
sigdet_wait_timer	38
This timer is used to control the wait time after transmitting or detecting the end of SEND_S. The	39
timer expires 5 μ s $\pm$ 0.15 μ s after being started.	40

191.5.2.8.3 Messages

sync_tx_symb	41
The value of sync_tx_symb is set by the Link Synchronization state diagram and indicates the	42
symbols sent from the PHY Link Synchronization block to PMA Transmit. The Link	43
Synchronization block generates sync_tx_symb synchronously with every transmit clock cycle.	44
Values:	45
SEND_S: Transmit the SEND_S pulse defined in 191.5.2.8.	46
SEND_Z: This value is continuously asserted when transmission of Z symbols is required.	47

191.5.2.8.4 State diagrams

The PHY Link Synchronization state diagram is shown in Figure 191–38..

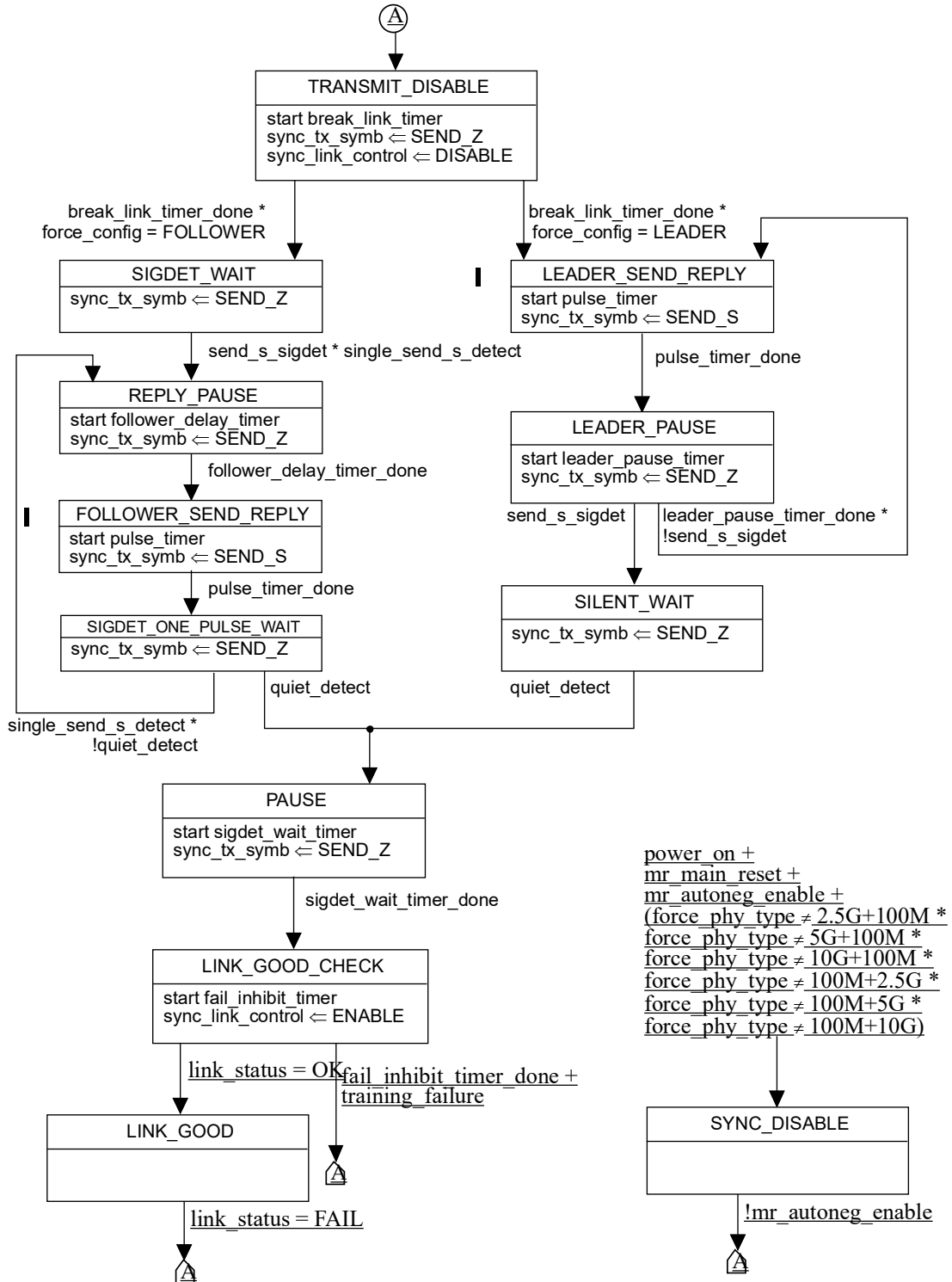


Figure 191–38—PHY Link Synchronization state diagram

191.5.2.9 Tx Clock Generation function

The Tx Clock Generation function provides a clock for use by PMA Transmit, labeled tx_symbol_clock in Figure 191–28. The clock is derived from a local clock source when the parameter config is LEADER, and is derived from the clock recovered from the received signal by PMA Receive when config is FOLLOWER. Derivation of the transmit clock generally involves clock multiplication or division. For the Leader, the tx_symbol_clock signal is expected to be stable and ready for use whenever the transmitter is enabled. For the Follower, the tx_symbol_clock signal is expected to be stable and ready to use when PHY Control has proceeded to the entry to the TRAINING state.

191.5.2.10 MDI, -T1

191.5.2.10.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are as described in the PMA Transmit function (191.5.2.2), tx_symb. The PMA Transmit function generates a pulse-amplitude modulated signal on each single shielded balanced pair of conductors in the following form:

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \quad (191-11)$$

where

a_n is the modulation symbol transmitted at time nT

$h_T(t)$ denotes the system symbol response at the MDI

The symbol response shall comply with the electrical specifications given in 191.6.2 for the HS_TX path and 191.7.2 for the LS_TX path.

191.5.2.10.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as follows:

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \quad (191-12)$$

where

$h_R(t)$ denotes the symbol response of the overall channel impulse response between the transmit symbol source and the receive MDI

$w(t)$ represents the contribution of various noise sources including uncanceled echo

The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb. The link segment is defined in 191.9 for -T1.

191.5.2.11 MDI, -V1

The V1 MDI is as described in 191.5.2.10, with the following exceptions:

- 1) The signal is single-ended and is carried over a single coaxial cable.
- 2) The link segment is defined in 191.10 for -V1.

The symbol response shall comply with the electrical specifications given in 191.6.2 for the HS_TX path and 191.7.2 for the LS_TX path.

191.6 PMA electrical specifications, high speed path

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests for the HS_PATH.

191.6.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 191–13. If MDIO is not implemented then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation

Table 191–13—MDIO management registers settings for test modes, high speed

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting Leader and Follower PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in Leader mode.
011	Test mode 3—Precoder test mode.
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on Leader and Follower transmitters. Leader and Follower PHYs are connected over a link segment defined in 191.9 for -T1 links and 191.10 for -V1 links. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 175.78125 MHz.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in Leader timing mode. When test mode 2 is enabled, when transmitting PAM4, the PHY shall transmit a continuous pattern of JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source. See Table 191–15 for control of jitter test modes. When test mode 2 is enabled, when transmitting PAM2, the PHY shall transmit a continuous pattern of 0101 with the transmitted symbols timed from its local clock source.

Test mode 3 is specified for 10G+100MBASE-T1/V1 PHYs only, and is for testing precoder operation. When test mode 3 is enabled, the PCS shall generate a continuous pattern of {0, 3} symbols to be input to the transmit precoder specified in 149.3.2.2.20, to be precoded according to the transmit precoder settings as

determined by the value set in register 1.2313.10:9, or equivalent functionality if MDIO is not implemented, and transmitted by the PMA timed from its local clock source.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled, a 10G+100MBASE-T1/V1 PHY shall transmit a continuous pattern of PRBS13Q (as specified in 120.5.11.2.1). When test mode 4 is enabled, a 2.5G+100MBASE-T1/V1 PHY or a 5G+100MBASE-T1/V1 PHY shall each transmit a continuous pattern of PRBS13 (as specified in 94.3.10.8).

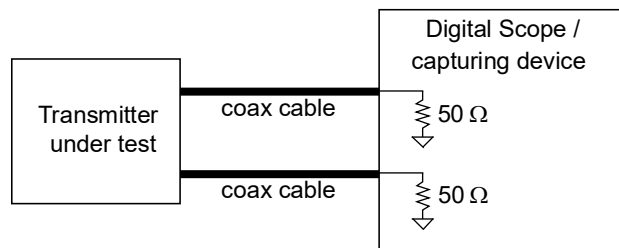
Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the Leader data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of $128 \times S \{+1\}$ symbols followed by $128 \times S \{-1\}$ symbols with the transmitted symbols timed from its local clock source. See Table 191–1 for the definition of S .

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the MultiG+100M/100M+MultiGBASE-T1/V1 normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

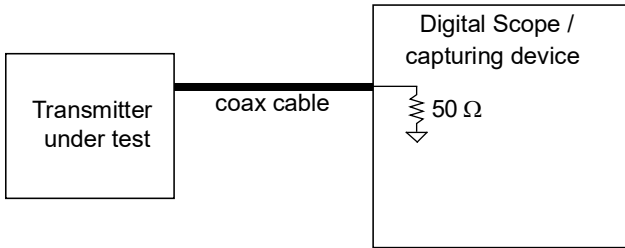
191.6.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 191–39, Figure 191–40, Figure 191–41, Figure 191–42, Figure 191–43, Figure 191–44, and Figure 191–45 in stated respective tests, are defined for measuring the transmitter specifications for data communication only.



NOTE—It is recommended that a Follower PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 191–39—Transmitter test fixture 1 for transmitter droop measurement and transmitter linearity measurement, -T1



NOTE—It is recommended that a Follower PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 191-40—Transmitter test fixture 1 for transmitter droop measurement and transmitter linearity measurement, -V1

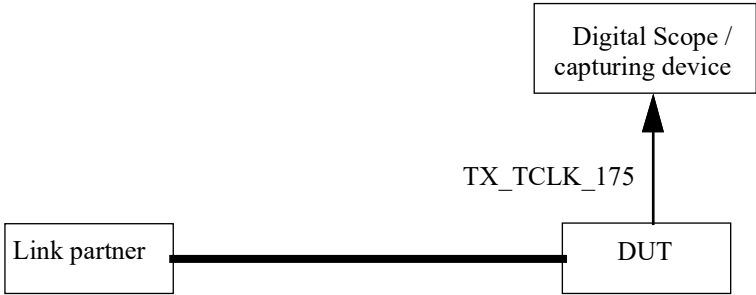


Figure 191-41—Transmitter test fixture 2 for Leader and Follower clock jitter measurement, -T1 and -V1

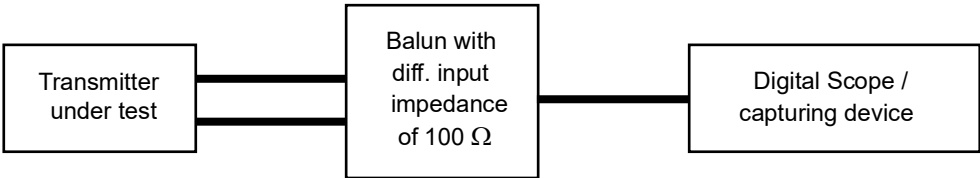
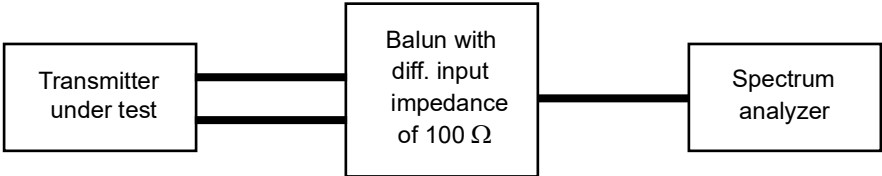


Figure 191-42—Transmitter test fixture 3 for MDI jitter measurement, -T1

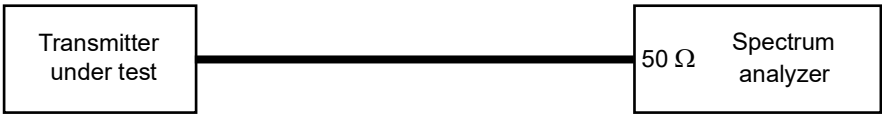


Figure 191-43—Transmitter test fixture 3 for MDI jitter measurement, -V1



NOTE—It is recommended that a Follower PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 191-44—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement, -T1



NOTE—It is recommended that a Follower PHY in XTAL-less mode include a method to use a reference clock provided by an external clock source.

Figure 191-45—Transmitter test fixture 4 for power spectral density measurement and transmit power level measurement, -V1

191.6.2 Transmitter electrical specifications

The MultiG+100M-T1/V1 PMA provides the Transmit function specified in 191.5.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it presents a high dc common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single-ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of $\pm 0.1\%$.

191.6.2.1 Transmitter timing jitter

The allowable jitter varies with the PHY's data rate. The parameter J is used for scaling of the jitter, see Table 191–14.

Table 191–14—Jitter Scaling parameter

PHY type	J
10G+100MBASE-T1/V1	1
5G+100MBASE-T1/V1	2
2.5G+100MBASE-T1/V1	4

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both Leader and Follower configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 191–41. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the Leader TX_TCLK_175 jitter relative to anunjittered reference shall be less than J ps. The peak-to-peak value of the Leader TX_TCLK_175 jitter relative to anunjittered reference shall be less than $10 \times J$ ps. See Table 191–14 for the definition of J .

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the Follower TX_TCLK_175 jitter relative to anunjittered reference shall be less than 6 ps and the RMS jitter shall be less than 3 ps when measured over jitter frequencies greater than 100 kHz. The peak-to-peak value of the Follower TX_TCLK_175 jitter relative to anunjittered reference shall be less than 60 ps.

TX_TCLK_175 jitter is defined when measured over an interval of $1 \text{ ms} \pm 10\%$. Conformance to this specification is defined when a capturing device with at least 200 MHz band-pass bandwidth is used (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

191.6.2.2 Transmit MDI random jitter in Leader mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with the square wave pattern (see Table 191–15) and using test fixture 3 as shown in Figure 191–42 for -T1 and Figure 191–43 for -V1. The RMS value of the MDI output jitter relative to anunjittered reference shall be less than J ps. See Table 191–14 for the definition of J . The peak-to-peak value of the MDI output jitter relative to anunjittered reference shall be less than $10 \times J$ ps. Jitter is defined when measured over an interval of $1 \text{ ms} \pm 10\%$. Conformance to this specification is defined when a capturing device with at least 200 MHz band-pass bandwidth is used. The unjittered reference is a constant clock frequency extracted from each

record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

Table 191–15—Jitter test modes

Modulation	Bit 1.2313.1	Bit 1.2313.0	Test pattern
PAM4	0	0	Square wave: TX_TCLK_175
PAM4	0	1	JP03A (as specified in 94.2.9.1)
PAM4	1	0	JP03B (as specified in 94.2.9.2)
PAM2	1	1	0101 (as specified in 130.7.1.9)

191.6.2.3 Transmit MDI deterministic jitter in Leader mode

Jitter measurements in this subclause are performed with the transmitter enabled in Leader timing mode in test mode 2, with the patterns as defined by Table 191–15, and timed with a local clock.

To measure the peak-to-peak deterministic jitter (DJ_{pk-pk}) follow the steps as specified in 94.3.12.6.1, with the following modifications to step 5:

$$f_n = 1 \times S \text{ MHz}, T = 68 / S \text{ ns. See Table 191–1 for the definition of } S.$$

Using this method, DJ_{pk-pk} shall be less than $9 \times J$ ps. See Table 191–14 for the definition of J .

To measure peak-to-peak even-odd jitter (EOJ_{pk-pk}), for 10 Gb/s follow the steps as specified in 94.3.12.6.2; for 5 Gb/s and 2.5 Gb/s, follow the steps as specified in 130.7.1.9.

Using this method, EOJ_{pk-pk} shall be less than $4 \times J$ ps.

191.6.2.4 Transmitter clock frequency

In test mode 2 and using test fixture 3 as shown in Figure 191–42 for -T1 and Figure 191–43 for -V1, the symbol transmission rate of the Leader PHY shall be within the range $5625 \times S \text{ MHz} \pm 100 \text{ ppm}$. See Table 191–1 for the definition of S .

In test mode 2 and using test fixture 3 as shown in Figure 191–42 for -T1 and Figure 191–43 for -V1, the symbol transmission rate of the Follower PHY, when running off of a free-running clock, shall be within the range $5625 \times S \text{ MHz} +1/-20\%$.

For both PHY_S and PHY_D, Leader and Follower, the short-term rate of frequency variation shall be less than 1% / second.

191.6.2.5 Transmitter linearity

Transmitter linearity is specified with the transmitter in test mode 4, transmitting in MultiG mode, and using the transmitter test fixture 1 shown in Figure 191–39 for -T1 and Figure 191–40 for -V1, according to the test definition in 120D.3.1.2. Annex 191B describes an additional High Pass Filter to be applied to the measured data when the DUT includes any low frequency high pass filtering (e.g. PoC/PoDL).

The ideal PAM4 level of 1/3 should be used for effective symbol levels of ES1 and ES2 for a 10G+100MBASE-T1/V1 PHY. For 5G+100MBASE-T1/V1 or 2.5G+100MBASE-T1/V1 PHYs, only

levels corresponding to PAM2 modulation (−1 and +1) are relevant and ES1, ES2 and levels at ±1/3 are not applicable in the calculation of signal-to-noise-and-distortion ratio (SNDR). The transmitter SNDR distortion, as specified in 120D.3.1.6, shall exceed 36 dB in 10G+100MBASE-T1/V1, 33 dB in 5G+100MBASE-T1/V1, and 30 dB in 2.5G+100MBASE-T1/V1 modes.

191.6.2.6 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the PHY_S PHYs shall be as specified in Table 191–16 and the power spectral density of the transmitter shall be between the upper and lower masks specified in Equation (191–13) and Equation (191–14). The PSD and power are measured using test fixture 4, shown in Figure 191–44, with a 100 Ω load for -T1 and shown in Figure 191–45, with a 50 Ω load for -V1. The upper and lower masks for each data rate, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s, are shown in Figure 191–46 for -T1 and in Figure 191–47 for -V1. When tx_symb is “Z” the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm. See Table 191–1 for the definition of *S*.

Table 191–16—Transmit Power, high speed mode

Transmit Rate	Transmit power, -T1		Transmit power, -V1	
	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
10 Gb/s	-1	2	-4	-1
5 Gb/s	-1	2	-4	-1
2.5 Gb/s	-4	-1	-7	-4

$$\text{UpperPSD}(f) = \begin{cases} P_O & 0 < f \leq 600 \times S \\ P_O + 1 - \frac{f}{600 \times S} & 600 \times S < f \leq 3000 \times S \\ P_O + 8 - \frac{f}{250 \times S} & 3000 \times S < f \leq 5500 \times S \end{cases} \text{dBm/Hz} \quad (191-13)$$

$$\text{LowerPSD}(f) = \begin{cases} P_O - 6 & 5 < f \leq 400 \times S \\ P_O - 5 - \frac{f}{400 \times S} & 400 \times S < f \leq 2000 \times S \\ P_O - \frac{f}{200 \times S} & 2000 \times S < f \leq 3000 \times S \end{cases} \text{dBm/Hz} \quad (191-14)$$

where

P_O is equal to -90 dBm/Hz for -T1
 P_O is equal to -93 dBm/Hz for -V1
 f is the frequency in MHz

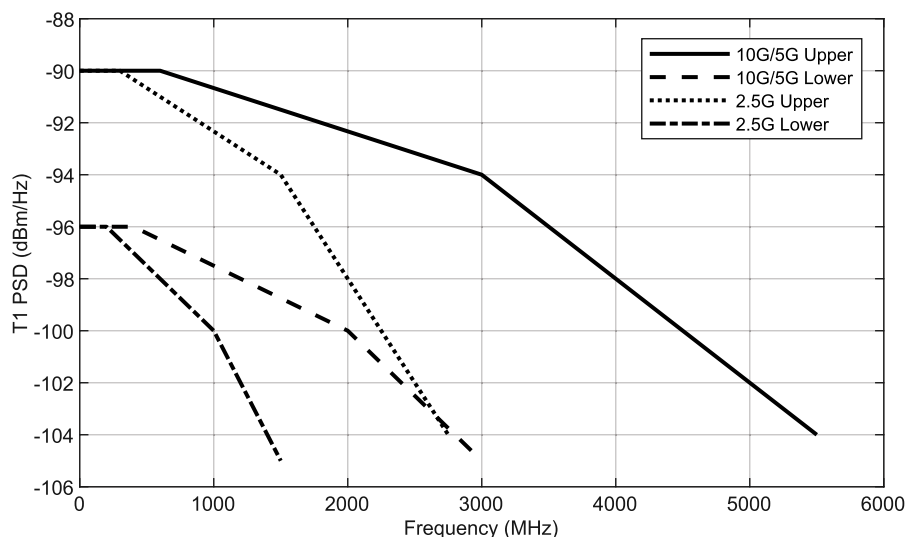


Figure 191-46—T1 MultiG Transmitter Power Spectral Density, upper and lower masks

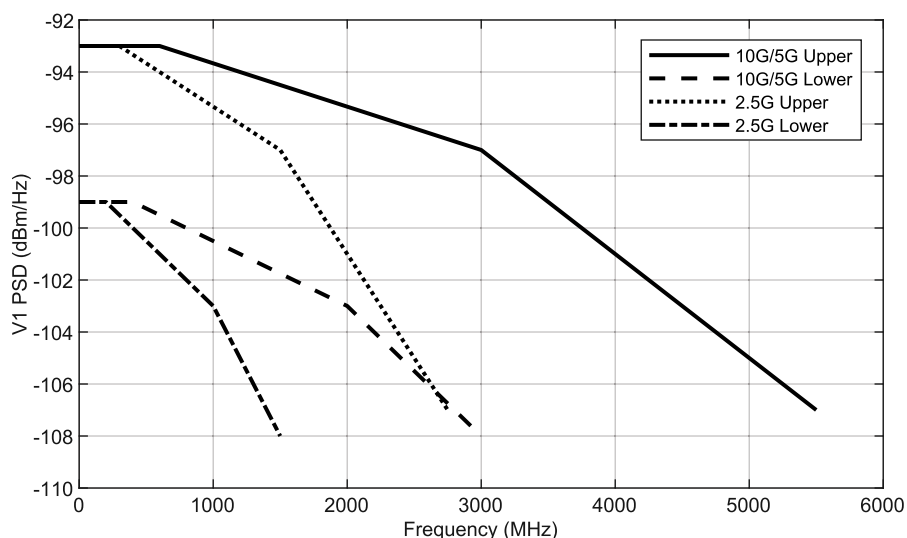


Figure 191-47—V1 MultiG Transmitter Power Spectral Density, upper and lower masks

191.6.2.7 Transmitter peak output

In test mode 5 (normal operation), the transmit signal of a MultiG+100MBASE-T1 transmitter measured using test fixture 4, shown in Figure 191-44, with a 100 Ω load for -T1 and shown in Figure 191-45, with a 50 Ω load for -V1, shall be less than the peak-to-peak limits specified in Table 191-17 at the MDI. These limits apply to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

Table 191–17—Transmit peak-to-peak voltage limits, high speed mode

Transmit Rate	-T1 Max (V)	-V1 Max (V)
10 Gb/s	1.5	0.75
5 Gb/s	1.2	0.6
2.5 Gb/s	0.8	0.4

191.6.2.8 Maximum output droop

With the MultiG+100M-T1/V1 transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 191–39 for -T1 and Figure 191–40 for -V1, the magnitude of both the positive and negative droop shall be less than 30%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 10 ns after the zero crossing (6 ns period).

191.6.3 Receiver electrical specifications

The PMA provides the Receive function specified in 191.5.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 191.9 for -T1 and 191.10 for -V1.

191.6.3.1 Receiver differential input signals

The signal received at the MDI that was transmitted from a remote transmitter within the specifications of 191.6.2 and has passed through a link specified in 191.9 for -T1 and 191.10 for -V1 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

191.6.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver’s tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 191–18. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 191–48, with a link segment as defined in 191.9 for -T1 and shown in Figure 191–49, with a link segment as defined in 191.10 for -V1. The BER shall be less than 10^{-12} , and to satisfy this specification, the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

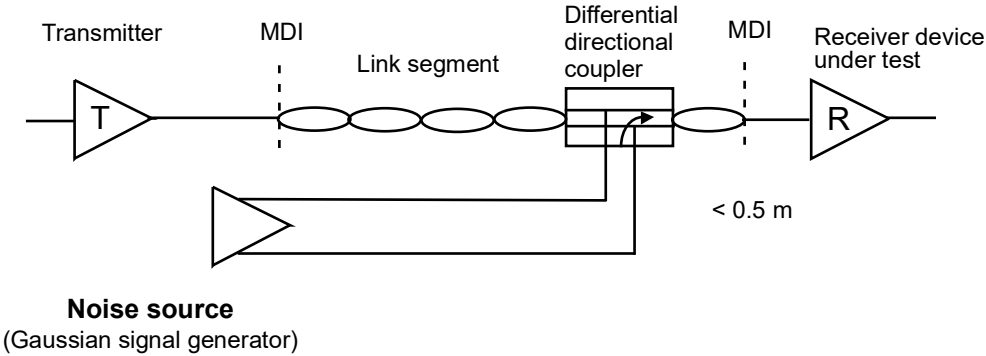


Figure 191-48—Broadband stationary noise rejection test setup, -T1

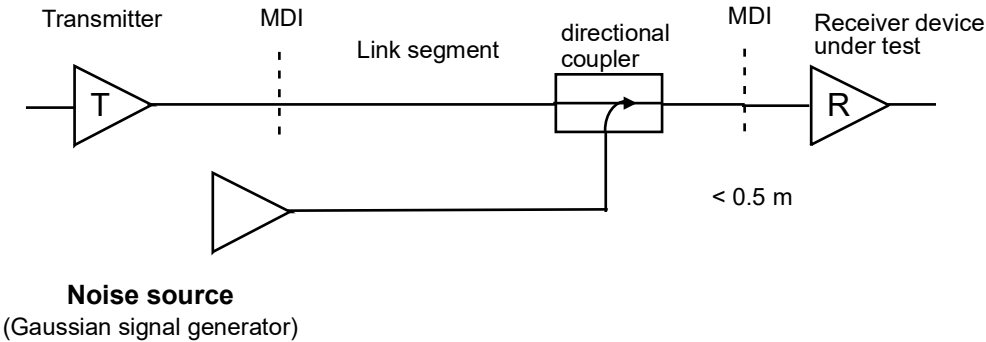


Figure 191-49—Broadband stationary noise rejection test setup, -V1

Table 191-18—Broadband stationary noise source, high speed

PHY type	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)	
		-T1	-V1
10G+100MBASE	3500	-148	-151
5G+100MBASE	3500	-144	-147
2.5G+100MBASE	1750	-140	-143

191.7 PMA electrical specifications, low speed path

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests for the low speed path.

191.7.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 191–19. If MDIO is not implemented then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

Table 191–19—MDIO management registers settings for test modes, low speed

Register value	Register description
000	Normal (non-test mode) operation.
001	Test mode 1—Setting Leader and Follower PHYs for transmit clock jitter test in linked mode.
010	Test mode 2—Transmit MDI jitter test in Leader mode.
011	Test mode 3—Reserved
100	Test mode 4—Transmitter linearity test.
101	Test mode 5—Normal operation in Idle mode. This is for the PSD Mask test.
110	Test mode 6—Transmitter droop test mode.
111	Test mode 7—Normal operation with zero data pattern. This is for BER monitoring.

Test mode 1 enables testing of timing jitter on Leader and Follower transmitters. Leader and Follower PHYs are connected over a link segment defined in 191.9 for -T1 links and 191.10 for -V1 links. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_175. TX_TCLK_175 is equal to 175.78125 MHz.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in Leader timing mode. When test mode 2 is enabled, the PHY shall repeatedly transmit DME encoded ones.

Test mode 4 is for transmitter linearity testing. When test mode 4 is enabled the PHY shall transmit a continuous pattern of PRBS13 (as specified in 94.3.10.8).

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the Leader data mode with data set to normal interframe idle signals.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 3 {+1} baseband symbols followed by 3 {−1} symbols. These symbols are transmitted with no Manchester encoding, generating a square wave with a period of 51.2 ns. The transmit symbols are timed from a free-running local clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the PHY_D normal (non-test) mode with zero data pattern. Instead of encoding data received from the MAC, continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

191.7.1.1 Test fixtures

The test fixtures in 191.6.1.1 are defined for measuring the transmitter specifications for data communication only.

191.7.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 191.5.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be AC-coupled, i.e., it shall present a high dc common-mode impedance at the MDI. There may be various methods for AC-coupling in actual implementations.

Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single-ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of $\pm 0.1\%$.

191.7.2.1 Transmitter timing jitter

The transmitter timing jitter is measured by capturing the TX_TCLK_175 waveform in both Leader and Follower configurations while in test mode 1 using the transmitter test fixture 2 shown in Figure 191–41. When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the Leader TX_TCLK_175 jitter relative to an unjittered reference shall be less than J ps. The peak-to-peak value of the Leader TX_TCLK_175 jitter relative to an unjittered reference shall be less than $10 \times J$ ps. See Table 191–14 for the definition of J . For an LS_TX as Leader, use J for the equivalent HS_TX on its partner PHY_S in Table 191–14.

When in test mode 1 and the link is up and the two PHYs have established link (link_status is set to OK), the RMS value of the Follower TX_TCLK_175 jitter relative to an unjittered reference shall be less than 50 ps. The peak-to-peak value of the Follower TX_TCLK_175 jitter relative to an unjittered reference shall be less than 500 ps.

TX_TCLK_175 jitter is defined when measured over an interval of $1 \text{ ms} \pm 10\%$. Conformance to this specification is defined when a capturing device with at least 200 MHz band-pass bandwidth is used (this is equivalent to phase noise integration of the clock over a bandwidth of at least 100 MHz from the carrier frequency). The unjittered reference is a constant clock frequency extracted from each record of captured TX_TCLK_175. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

191.7.2.2 Transmit MDI random jitter in Leader mode

In addition to jitter measurement for transmit clock, MDI jitter is measured when in test mode 2 with a square wave pattern and using test fixture 3 as shown in Figure 191–42 for -T1 and Figure 191–43 for -V1. The square wave pattern is generated by transmitting constant zero values as the input to the differential Manchester encoder. The RMS value of the MDI output jitter relative to an unjittered reference shall be less than J ps. See Table 191–14 for the definition of J . For an LS transmitter as Leader, use J for the equivalent HS transmitter on its partner PHY_S in Table 191–14. The peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than $10 \times J$ ps. Jitter is defined when measured over an interval of $1 \text{ ms} \pm 10\%$. Conformance to this specification is defined when a capturing device with at least 200 MHz band-pass bandwidth is used. The unjittered reference is a constant clock frequency extracted from each record of captured differential output on MDI. The unjittered reference is based on linear regression of frequency and phase that produces minimum Time Interval Error.

191.7.2.3 Transmit MDI deterministic jitter in Leader mode

This test is not defined for the LS_PATH.

191.7.2.4 Transmitter clock frequency

The baseband symbol transmission rate of the Leader PHY (prior to Manchester encoding) shall be within the range $5625/48 \text{ MHz} \pm 100 \text{ ppm}$. The transmitter clock frequency can be measured at the MDI using test mode 2.

In test mode 2 and using test fixture 3 as shown in Figure 191–42 for -T1 and Figure 191–43 for -V1, the symbol transmission rate of the Follower PHY, when running off of a free-running clock, shall be within the range $5625/48 \text{ MHz} +1/-20\%$.

The short-term rate of frequency variation, for both leader and follower, shall be less than $1\% / \text{second}$.

191.7.2.5 Transmitter Rise and Fall Time

The transmitter rise and fall time requirements specified in this subclause apply when the PHY_D is used to provide a reference clock for XTAL-less operation of PHY_S. Limiting the transmitter transition times reduces deterministic jitter of the derived reference at the receiving PHY.

The rise/fall transition time between 20% and 80% levels of the steady state voltage amplitude shall be less than 1.5 ns. The rise time and fall time is defined as measured at the MDI using test mode 2.

191.7.2.6 Transmitter linearity

With the transmitter in test mode 4, transmitting in 100 Mb/s mode, and using the transmitter test fixture 1 shown in Figure 191–39 for -T1 and Figure 191–40 for -V1, the transmit signal is captured per 85.8.3.3.4 with a minimum of $M=14$. The sequence of effective transmit baseband symbols, $x(n)$, is derived by noting that differential Manchester encoding includes an implicit nonlinear mapping. This nonlinear operation maps the transmitted PRBS13 bits d_{in} to another set of pseudo-random bits d_{out} , which in turn maps to the implicit transmit baseband symbols $x(n)$ according to Table 191–20.

Table 191–20—PRBS13 mapping table

Transmit Bits	Encoded Bits		Baseband Symbols
	previous	current	
$d_{in}(n)=\text{PRBS13}$	$d_{out}(n-1)$	$d_{out}(n)$	$x(n)$
0	0	1	-1
0	1	0	+1
1	0	0	-1
1	1	1	+1

Given the implicit transmit symbols $x(n)$, and the captured waveform $y(k)$, compute the linear fit pulse response $p(k)$ and the standard deviation of linear fit error $e(k)$ according to 85.8.3.3.5 and using $N_p=100$ and $D_p=2$.

The transmitter SNDR distortion is defined as: $\text{SNDR} = 10\log_{10}\left(\frac{\sigma_p^2}{\sigma_e^2 + \sigma_n^2}\right)$

Where $\sigma_p^2 = \frac{1}{M}\sum_k p^2(k)$, and σ_e and σ_n are the standard deviation of $e(k)$ and noise, respectively.

The transmitter SNDR distortion shall exceed 30 dB.

191.7.2.7 Transmitter power spectral density (PSD) and power level

In test mode 5 (normal operation), the transmit power for the PHY_D PHYs shall be as specified in Table 191–21 and the power spectral density of the transmitter shall be between the upper and lower masks specified in Equation (191–15) and Equation (191–16). The PSD and power are measured using test fixture 4, shown in Figure 191–44, with a 100 Ω load for -T1 and shown in Figure 191–45, with a 50 Ω load for -V1. The upper and lower masks are shown in Figure 191–50 for -T1 and in Figure 191–51 for -V1. When tx_symb is “Z” the transmit signal at the MDI is nominally zero, and the transmit signal shall be less than -36dBm.

Table 191–21—Transmit Power, low speed mode

Transmit Rate	Transmit power, -T1		Transmit power, -V1	
	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
100M	-3	0	-6	-3

$$\text{UpperPSD}(f) = \begin{cases} P_O & 3 < f < 150 \\ P_O + 15 - \frac{f}{10} & 150 < f \leq 260 \\ P_O - 11 & 260 < f \leq 3500 \end{cases} \text{dBm/HZ} \quad (191-15)$$

$$\text{LowerPSD}(f) = \begin{cases} P_O - 6 - \frac{90-f}{3} & 45 < f \leq 90 \\ P_O - 6 - \frac{f-90}{4} & 90 < f \leq 150 \end{cases} \text{dBm/HZ} \quad (191-16)$$

where

P_O is equal to -79 dBm/Hz for -T1
 P_O is equal to -82 dBm/Hz for -V1
 f is the frequency in MHz

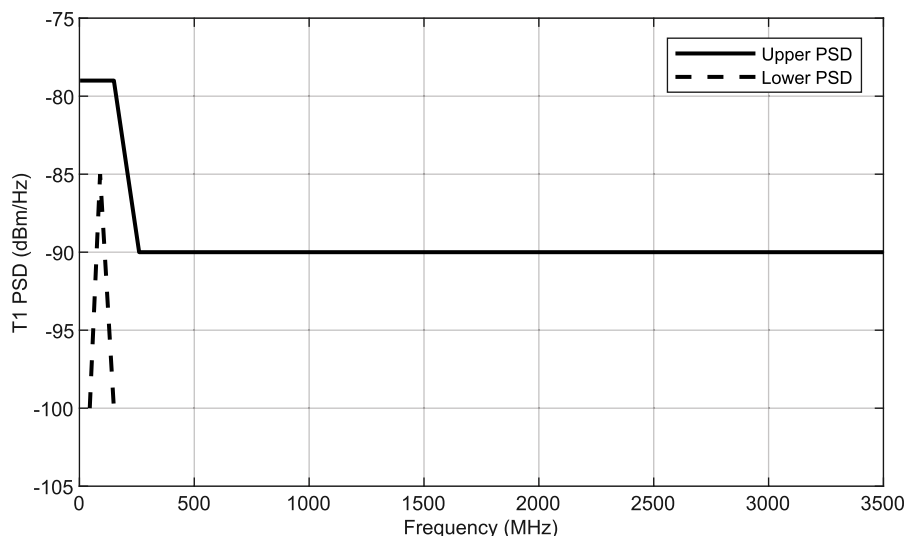


Figure 191-50—T1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

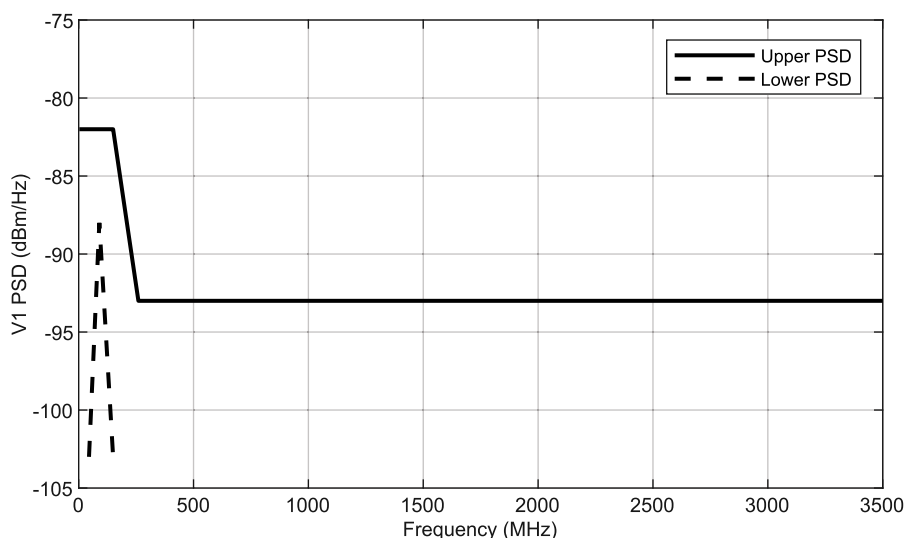


Figure 191-51—V1 100 Mb/s Transmitter Power Spectral Density, upper and lower masks

191.7.2.8 Transmitter peak output

When transmitting at a data rate of 100 Mb/s and measured using the -T1 test fixture 4, shown in Figure 191-44, with a 100 Ω load, the differential transmit signal of a 100M+MultiGBASE-T1 transmitter shall be less than 1.0 V peak-to-peak at the MDI. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

When transmitting at a data rate of 100 Mb/s and measured using the -V1 test fixture 4, shown in Figure 191–45, with a 50 Ω load, the transmit signal shall be less than 0.5 V peak-to-peak at the MDI. This limit applies to all transmitted symbol sequences, including SEND_S, SEND_T, and SEND_N.

The transmitter peak output voltage can be measured at the MDI using test mode 5.

191.7.2.9 Maximum output droop

With the PHY_D transmitter in test mode 6 and using the transmitter test fixture 1 shown in Figure 191–39 for -T1 and Figure 191–40 for -V1, the magnitude of both the positive and negative droop shall be less than 30%, measured with respect to an initial value at 8 ns after the zero crossing and a final value at 14 ns after the zero crossing (6 ns period).

191.7.3 Receiver electrical specifications

The PMA provides the Receive function specified in 191.5.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 191.9 for -T1 and 191.10 for -V1.

191.7.3.1 Receiver input signals

The signal received at the MDI that was transmitted from a remote transmitter within the specifications of 191.7.2 and has passed through a link specified in 191.9 for -T1 and 191.10 for -V1 shall be received with a BER less than 10^{-10} after RS-FEC decoding, and sent to the XGMII after link reset completion. This specification can be verified by a frame error ratio less than 10^{-7} for 125-octet packets measured at the MAC/PLS service interface.

191.7.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver’s tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 191–22. The receive DUT is connected to the noise source through a directional coupler, as shown in Figure 191–48, with a link segment as defined in 191.9 for -T1 and shown in Figure 191–49, with a link segment as defined in 191.10 for -V1. The BER is expected to be less than 10^{-10} , and to satisfy this specification, the frame loss ratio is less than 10^{-7} for 125-octet packets measured at the MAC/PLS service interface.

Table 191–22—Broadband stationary noise rejection, low speed

PHY type	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)	
		-T1	-V1
100M+MultiGBASE	150	-126	-129

191.8 Management interface

191.8.1 Support for Auto-Negotiation

MultiG+100M/100M+MultiGBASE-T1/V1 PHYs optionally provide support for Auto-Negotiation. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.

Auto-Negotiation, when implemented and enabled, is performed as part of the initial set-up of the link and allows the PHYs at each end to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. Auto-Negotiation signaling is used for the following primary purposes for MultiG+100M/100M+MultiGBASE-T1/V1:

- a) To negotiate which PHY types, including speed and direction, can be supported,
- b) To determine the Leader-Follower relationship between the PHYs at each end of the link.

191.9 Link segment characteristics, -T1

MultiG+100M/100M+MultiGBASE-T1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. The single shielded balanced pair of conductors supports an effective data rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in one direction and simultaneously 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

191.9.1 Link transmission parameters

The transmission characteristics for the -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

191.9.1.1 Insertion loss

The insertion loss of each -T1 link segment shall meet the values determined using Equation (191–17).

$$\text{Insertion loss}(f) \leq -0.0015 + 0.001325f + 0.3645\sqrt{f} + \frac{1.1785}{\sqrt{f}} \text{ (dB)} \quad (191-17)$$

where

f is the frequency in MHz; $3 \leq f \leq F_{\max}$

$F_{\max}$ is given by Equation (191–18).

$$F_{\max} = \begin{cases} 2000 \text{ MHz} & \text{for 2.5 Gb/s} \\ 4000 \text{ MHz} & \text{for 5 Gb/s and 10 Gb/s} \end{cases} \quad (191-18)$$

The Insertion loss is illustrated in Figure 191–52.

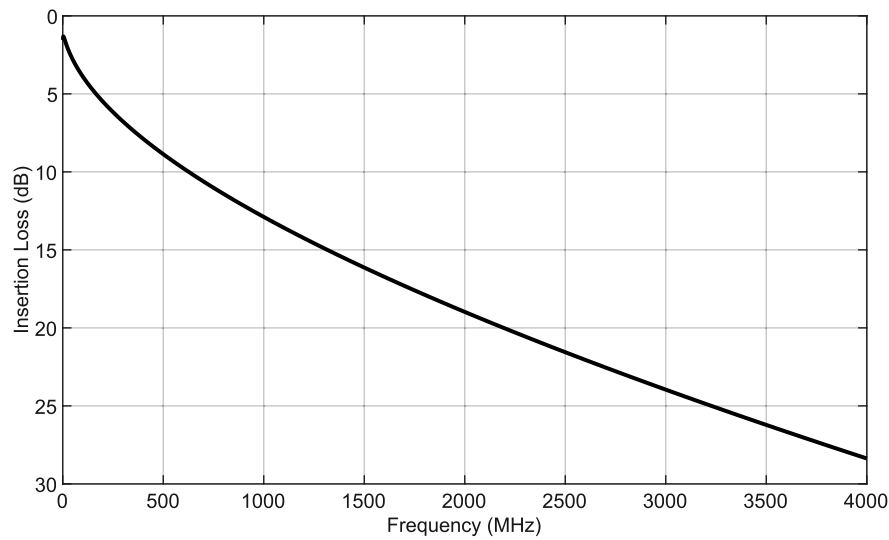


Figure 191-52—Insertion loss using Equation (191-17) for T1 and V1

191.9.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of the -T1 link segment is 100 Ω.

191.9.1.3 Return loss

The return loss of each -T1 link segment shall meet the values determined using Equation (191-19).

$$Return Loss(f) \geq \left\{ \begin{array}{ll} 18 & 3 \leq f < 400 \\ 16.5 - 11.5 \log_{10} \left(\frac{f}{550} \right) & 400 \leq f < 3000 \\ 8 & 3000 \leq f < 4000 \end{array} \right\} \text{ (dB)} \quad (191-19)$$

where

f is the frequency in MHz; $3 \leq f \leq 2000$ for 2.5 Gb/s
 $3 \leq f \leq 4000$ for 5 Gb/s and 10 Gb/s

The Return loss is illustrated in Figure 191-53.

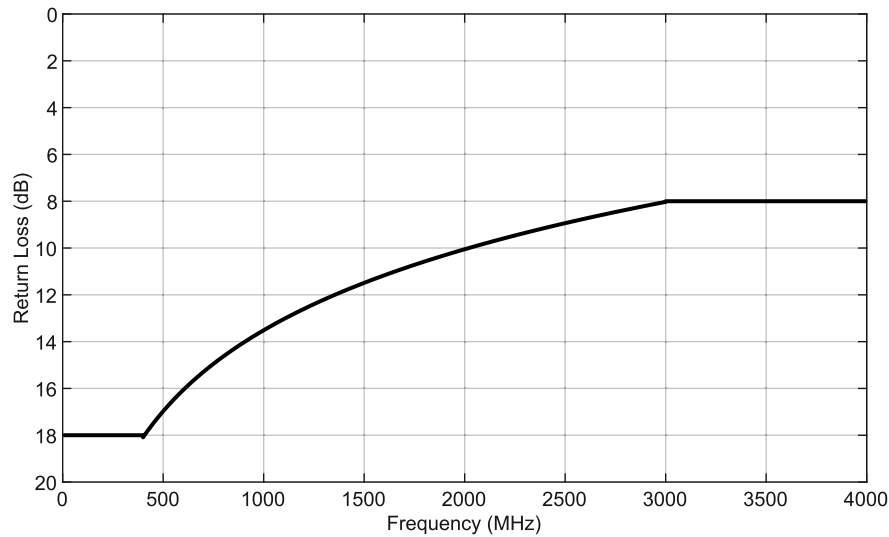


Figure 191-53—Return loss using Equation (191-19) for T1 and V1

191.9.1.4 Coupling attenuation

The coupling attenuation of each -T1 link shall be as specified in 149.7.1.4.

191.9.1.5 Screening attenuation

The screening attenuation of each -T1 link shall be as specified in 149.7.1.5 with $F_{max} = 4000$ MHz.

191.9.1.6 Maximum link segment delay

The propagation delay of a -T1 link segment shall not exceed 160 ns at all frequencies between 3 MHz and F_{max} MHz, see Equation (191-18) for the definition of F_{max} .

191.9.2 Coupling parameters between link segments

The coupling parameters between link segments are described in 149.7.2.

191.9.2.1 Power sum alien near-end crosstalk (PSANEXT)

The PSANEXT shall be as specified in 149.7.2.1.

191.9.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The PSAACRF shall be as specified in 149.7.2.2.

191.10 Link segment characteristics, -V1

MultiG+100M/100M+MultiGBASE-V1 is designed to operate over a single coaxial cable (-V1) that meets the requirements specified in this subclause. The single coaxial cable supports an effective data rate of

2.5 Gb/s, 5 Gb/s, or 10 Gb/s in one direction and simultaneously 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

191.10.1 Link transmission parameters

The transmission characteristics for the -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

191.10.1.1 Insertion loss

The insertion loss of each -V1 link segment shall meet the values determined using Equation (191–17).

The Insertion loss is illustrated in Figure 191–52.

191.10.1.2 Single ended characteristic impedance

The nominal characteristic impedance of the -V1 link segment is 50 Ω.

191.10.1.3 Return loss

The return loss of each -V1 link segment shall meet the values determined using Equation (191–19).

The Return loss is illustrated in Figure 191–53.

191.10.1.4 Coupling attenuation

The coupling attenuation is not defined for coaxial cables.

191.10.1.5 Screening attenuation

The screening attenuation of each -V1 link segment shall meet the values determined using Equation (191–20). Screening attenuation is tested as specified in IEC 62153-4-7 using triaxial tube-in-tube method.

$$\text{Screening attenuation}(f) \geq \begin{cases} 55 & 30 \leq f < 1000 \\ 50 & 1000 \leq f < 3000 \text{ (dB)} \\ 45 & 3000 \leq f < 4000 \end{cases} \quad (191-20)$$

where

f is the frequency in MHz; $30 \leq f \leq 4000$

Screening attenuation is illustrated in Figure 191–54.

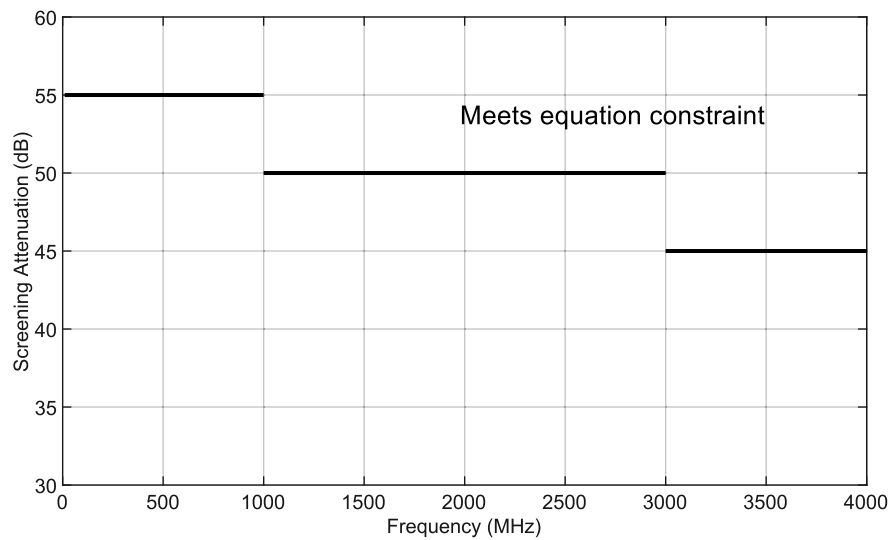


Figure 191–54—Screening attenuation using Equation (191–20) for V1

191.10.1.6 Maximum link segment delay

The propagation delay of a -V1 link segment shall not exceed 160 ns at all frequencies between 3 MHz and Fmax MHz, see Equation (191–18) for the definition of Fmax.

191.10.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in [Annex 97B](#). These methodologies shall be applied with adaptation to unbalanced coaxial cabling and shall use a single 50 Ω termination to ground.

For implementations with multiple MultiG+100M/100M+MultiGBASE-V1 ports on the same MDI connector assembly, coupling between ports on the MDI connector is not considered to be part of the alien crosstalk specifications. The coupling between adjacent ports on a multiport MDI connector is recommended to be at the same level, but not greater, than specified for PSANEXT loss in Equation (191–21).

191.10.2.1 Power sum alien near-end crosstalk (PSANEXT)

The unbalanced coax near-end crosstalk (NEXT) loss between the disturbed link segment and the disturbing link segment is specified to meet the bit error ratio objective by limiting the alien crosstalk at the near end of a link segment. Multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT disturbers. The power ANEXT loss is derived using [Equation \(97–25\)](#) over the frequency range 3 MHz to 4000 MHz.

The power sum ANEXT loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (191–21).

$$\text{PSANEXT loss}(f) \geq \min\left(60, 60 - 5\log_{10}\frac{f}{100}\right) \text{ dB} \quad (191-21)$$

where

f is the frequency in MHz; $3 \leq f \leq 4000$

PSANEXT loss is illustrated in Figure 191–55.

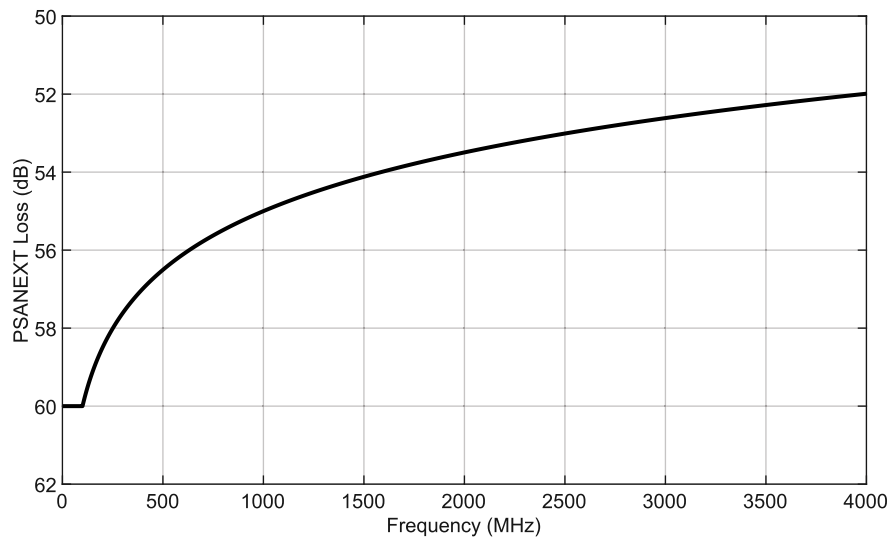


Figure 191–55—PSANEXT loss calculated using Equation (191–21)

191.10.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

In order to limit the alien crosstalk at the far-end of a link segment, the unbalanced coax cable-to-cable alien far-end crosstalk (FEXT) loss between the disturbed link segment and the disturbing link segment is specified to meet the bit error ratio objective. Multiple disturber attenuation to crosstalk ratio far-end AACRF is specified as the power sum of the individual alien AACRF disturbers to limit the total alien FEXT coupled into a link segment. The power AACRF is derived using Equation (97–27) over the frequency range 3 MHz to 4000 MHz.

The power sum AACRF loss between a disturbed link segment and the disturbing link segment shall meet the values determined using Equation (191–22).

$$\text{PSAACRF}(f) \geq \min\left(60, 60 - 5\log_{10}\frac{f}{100}\right) \text{ dB} \quad (191-22)$$

where

f is the frequency in MHz; $3 \leq f \leq 4000$

PSAACRF is illustrated in Figure 191–56.

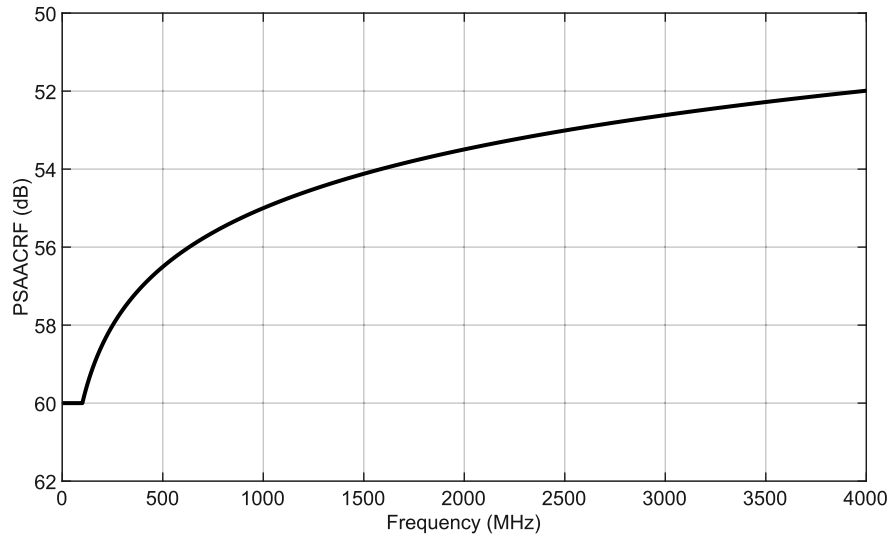


Figure 191–56—PSAACRF calculated using Equation (191–22)

191.11 MDI specification, -T1

MultiG+100M/100M+MultiGBASE-T1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

191.11.1 MDI connectors

The MDI connectors are as specified in 149.8.1.

191.11.2 MDI electrical specification

191.11.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmit/receive channel shall be such that any reflection due to signals incident upon the MDI from the cabling relative to the incident signal are per the relationship shown in Equation (191–23). For the -T1 PHY, a nominal differential characteristic impedance of 100 Ω is used.

$$MDI\_Return\_Loss(f) > \left\{ \begin{array}{ll} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < F_{max} \end{array} \right\} \text{ (dB)} \quad (191-23)$$

where

f is the frequency in MHz; $10 \leq f \leq F_{max}$

F_{max} is given by Equation (191–18).

The MDI return loss for 10G-T1 and 5G-T1 is illustrated in Figure 191–57.

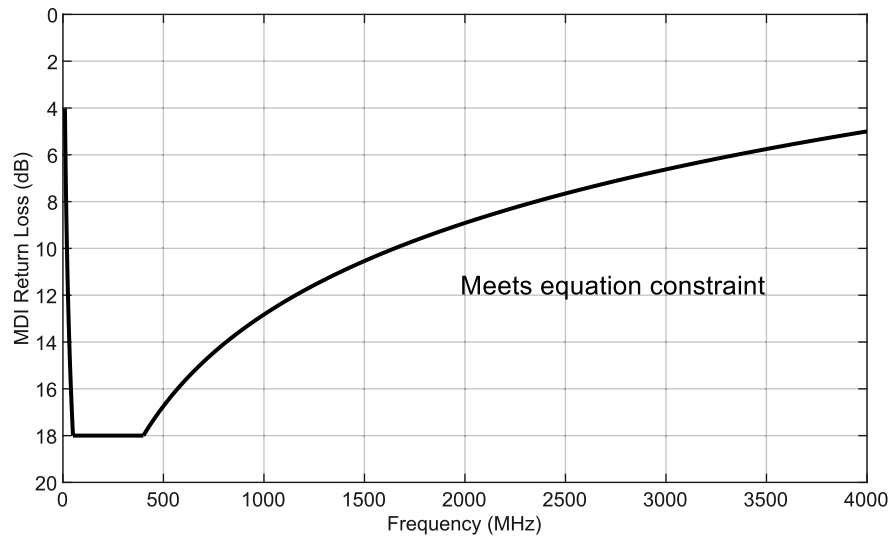


Figure 191–57—T1 MDI return loss using Equation (191–23)

191.11.3 MDI fault tolerance

The MDI fault tolerance shall comply with 96.8.3.

191.12 MDI specification, -V1

MultiG+100M/100M+MultiGBASE-V1 is designed to operate over a single coaxial cable MDI (-V1) that meets the requirements specified in this subclause.

191.12.1 MDI connectors

The mechanical interface to the coaxial cable is a single pin connector with a shield. Further specification of the mechanical interface is beyond the scope of this standard.

191.12.2 MDI electrical specification

191.12.2.1 MDI return loss

The characteristic impedance at the -V1 MDI for each transmit/receive channel shall be such that any reflection due to signals incident upon the MDI from the cabling relative to the incident signal are per the relationship shown in Equation (191–24). For the -V1 PHY, a nominal characteristic impedance of 50 Ω is used.

$$MDI\_Return\_Loss(f) > \left\{ \begin{array}{ll} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < F_{max} \end{array} \right\} \text{ (dB)} \quad (191-24)$$

where

f is the frequency in MHz; $10 \leq f \leq F_{max}$

F_{max} is given by Equation (191-18).

The MDI return loss for 10G-V1 and 5G-V1 is illustrated in Figure 191-58.

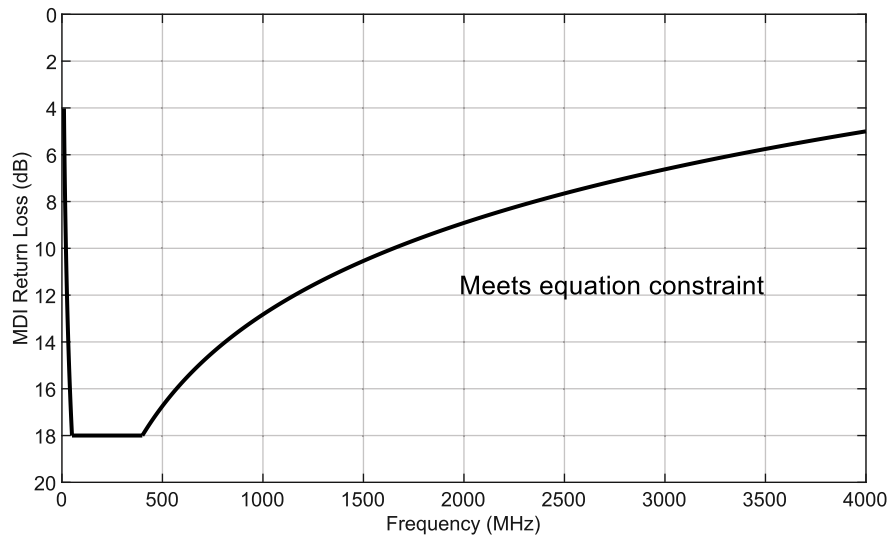


Figure 191-58—V1 MDI return loss using Equation (191-24)

191.12.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 191-23, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI should withstand, without damage, high-voltage transient noises and ESD per application requirements.

191.13 Environmental specifications

The environmental specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.

Table 191–23—Connection fault, -V1

Center Conductor	Shield
No fault	Ground
MDI+	Ground
Ground	Ground
+50 V dc	Ground

191.13.1 General safety

The general safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.1.

191.13.2 Network safety

The network safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.

191.13.2.1 Environmental safety

The environmental safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.1.

191.13.3 Electromagnetic compatibility

The electromagnetic compatibility safety specifications for MultiG+100M/100M+MultiGBASE-T1/V1 are as specified in 149.9.2.2.

191.14 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B) demands that there be an upper bound on the propagation delays through the network.

The HS_PATH delay is defined as the time needed for a given unit of data to traverse from the input at the PHY_S XGMII to its presentation at the PHY_D XGMII, minus the link segment propagation delay.

The LS_PATH delay is defined as the time needed for a given unit of data to traverse from the input at the PHY_D XGMII to its presentation at the PHY_S XGMII, minus the link segment propagation delay.

These delays shall not exceed the limits shown in Table 191–24.

See Annex 191A for informative guidance on the allocation of delay between the transmit and receive portions of the PHYs.

Table 191–24—Delay constraints

PATH	Interleave	Maximum delay (BT)	Maximum delay (pause_quanta)	Maximum delay (ns)
2.5G+100MBASE-T1/V1	1x	10 240	20	4096
5G+100MBASE-T1/V1	1x	10 240	20	2048
5G+100MBASE-T1/V1	2x	13 824	27	2764.8
10G+100MBASE-T1/V1	1x	10 240	20	1024
10G+100MBASE-T1/V1	2x	13 824	27	1382.4
10G+100MBASE-T1/V1	4x	20 480	40	2048
100M+MultiGBASE-T1/V1	—	512	1	5120

191.15 Protocol implementation conformance statement (PICS) proforma for Clause 191, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium for MultiG+100M/100M+MultiGBASE-T1/V1⁵

191.15.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 191, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium for MultiG+100M/100M+MultiGBASE-T1/V1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in [Clause 21](#).

191.15.2 Identification

191.15.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

191.15.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3dm-202x, Clause 191, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium for MultiG+100M/100M+MultiGBASE-T1/V1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [] Yes [] (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

⁵Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

191.15.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*AN	Auto-Negotiation	98		O	Yes [] No []
*INS-T	Installation/cabling, -T1	191.9	Items marked with INS-T include installation practices and cabling specifications applicable when the link segment is balanced pair cabling, and not applicable to backplane link segments.	O	Yes [] No []
*INS-V	Installation/cabling, -V1	191.10	Items marked with INS-V include installation practices and cabling specifications applicable when the link segment is a single coaxial cable, and not applicable to backplane link segments.	O	Yes [] No []
*OAM_ HS	Support of MultiG+100MBASE-T1/V1 PCS level operations, administration, and maintenance	191.3.7		O	Yes [] No []
*OAM_ LS	Support of 100M+MultiGBASE-T1/V1 PCS level operations, administration, and maintenance	191.4.7		O	Yes [] No []
*MDIO	Support of MDIO capability	45.1	Register and Interface support.	O	Yes [] No []
*PHY_ S	Support of PHY_S capability, HS_TX, LS_RX	191.2		O	Yes [] No []
*PHY_ D	Support of PHY_D capability, LS_TX, HS_RX	191.2		O	Yes [] No []
*2.5G	Support of 2.5 Gb/s for transmit when PHY_S and receive when PHY_D	191.1		O	Yes [] No []
*5G	Support of 5 Gb/s for transmit when PHY_S and receive when PHY_D	191.1		O	Yes [] No []
*10G	Support of 10 Gb/s for transmit when PHY_S and receive when PHY_D	191.1		O	Yes [] No []
*Lead	Support of Leader capability	191.1.3		O	Yes [] No []
*Follow	Support of Follower capability	191.1.3		O	Yes [] No []

191.15.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium for MultiG+100M/100M+MultiGBASE-T1/V1

191.15.4.1 General

Item	Feature	Subclause	Value/Comment	Status	Support
G1	If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.	98		AN:M	Yes [] N/A []
G2	Capable of operating as Leader or Follower, per runtime configuration.	191.1.3		M	Yes []
G3	If Auto- Negotiation is not used, a Leader-Follower relationship shall be established by management or hardware configuration of the PHYs.	149.1.3		AN:M	Yes [] N/A []

191.15.4.2 Physical Coding Sublayer (PCS)

191.15.4.2.1 PCS, HS_TX

Item	Feature	Subclause	Value/Comment	Status	Support
PCT1	PCS Reset	191.3.2.1	Described in 191.3.2.1.	M	Yes []
PCT2	Management interface restore to operation	191.3.2.1	Within 10 ms from the setting of bit 3.2322.15.	M	Yes []
PCT3	PCS 64B/65B Transmit state diagram	191.3.2.2	Figure 191–19.	M	Yes []
PCT4	PCS Transmit bit ordering	191.3.2.2	Figure 191–11.	10G* PHY_S: M	Yes [] N/A []
PCT5	PCS Transmit bit ordering	191.3.2.2	Figure 191–12.	(2.5G+ 5G)* PHY_S: M	Yes [] N/A []
PCT6	If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a Z symbol at each symbol period to the PMA via the PMA_UNITDATA.request primitive.	191.3.2.2		M	Yes []
PCT7	If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 191.3.4.1 to the PMA via the PMA_UNITDATA.request primitive.	191.3.2.2		M	Yes []
PCT8	If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control.	191.3.2.2		M	Yes []
PCT9	All XGMII control code values that do not appear in the Table 149–2 shall not be transmitted and shall be treated as an error if received.	191.3.2.2.5		M	Yes []
PCT10	Idle control characters	191.3.2.2.7	/I/ insertion and deletion shall occur in groups of 4.	M	Yes []
PCT11	Adding Idle control characters	191.3.2.2.7	/I/s shall not be added while data is being received.	M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
PCT12	Deleting Idle control characters	191.3.2.2.7	When deleting /I/s, the first four characters after a /T/ shall not be deleted.	M	Yes []
PCT13	Ordered set	191.3.2.2.10	Sequence ordered set deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two.	M	Yes []
PCT14	RS-FEC encoding	191.3.2.2.13	Generates 34 10-bit parity symbols (340 bits total).	PHY_S: M	Yes [] N/A []
PCT15	Interleave set to depth setting	191.3.2.2.14	Interleaver depth set to value requested by link partner during Infocfield exchange.	PHY_S: M	Yes [] N/A []
PCT16	Round-robin interleaving scheme	191.3.2.2.14	Figure 149–9.	PHY_S: M	Yes [] N/A []
PCT17	The PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe.	191.3.2.2.14		PHY_S: M	Yes [] N/A []
PCT18	PHY_S transmitter side-stream scrambler generator polynomial.	191.3.2.2.19	Equation (191–2).	PHY_S: M	Yes [] N/A []
PCT19	In no case shall the scrambler state be initialized to all zeros.	191.3.2.2.19	Never initialized to all zeros.	PHY_S: M	Yes [] N/A []
PCT20	This scrambler, once started during PMA TRAINING STATE, shall continue to run uninterrupted during transition from SEND_T to SEND_N.	191.3.2.2.19	Runs continuously once started during PMA TRAINING state.	PHY_S: M	Yes [] N/A []
PCT21	Gray mapping for PAM4 encoding	191.3.2.2.20	Described in 191.3.2.2.20.	PHY_S* 10G:M	Yes [] N/A []
PCT22	Selectable precoder	191.3.2.2.21	Described in 191.3.2.2.21.	PHY_S* 10G:M	Yes [] N/A []
PCT23	PAM4 encoding	191.3.2.2.22	Described in 191.3.2.2.22.	PHY_S* 10G:M	Yes [] N/A []
PCT24	PAM2 encoding	191.3.2.2.23	Described in 191.3.2.2.23.	PHY_S* (2.5G+ 5G):M	Yes [] N/A []

191.15.4.2.2 PCS, HS_RX

Item	Feature	Subclause	Value/Comment	Status	Support
PCR1	PCS 64B/65B Receive state diagram	191.3.2.3	Figure 191–20.	M	Yes []
PCR2	10G PCS receive bit ordering	191.3.2.3	Figure 191–14.	PHY_D* 10G:M	Yes [] N/A []
PCR3	5G & 2.5G PCS receive bit ordering	191.3.2.3	Figure 191–15.	PHY_D* (2.5G+ 5G):M	Yes [] N/A []
PCR4	10G Frame and block synchronization	191.3.2.3.1	Described in 191.3.2.3.1.	PHY_D* 10G:M	Yes [] N/A []
PCR5	5G & 2.5G Frame and block synchronization	191.3.2.3.1	Described in 191.3.2.3.1.	PHY_D* (2.5G+ 5G):M	Yes [] N/A []
PCR6	PHY_D receiver descrambler.	191.3.2.3.2	Equation (191–2).	PHY_D: M	Yes [] N/A []
PCR7	RS-FEC parity bits	191.3.2.3.3	Checks RS-FEC parity per 191.3.2.2.13.	PHY_D: M	Yes [] N/A []

191.15.4.2.3 Test-pattern generators, HS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
TPG1	10G Transmit PCS operating in test-pattern mode.	191.3.3	Transmit continuously as illustrated in Figure 191–11, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value.	PHY_S* 10G:M	Yes [] N/A []
TPG2	5G & 2.5G Transmit PCS operating in test-pattern mode.	191.3.3	Transmit continuously as illustrated in Figure 191–12, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value.	PHY_S* (2.5G+ 5G):M	Yes [] N/A []
TPG3	10G Receive PCS operating in test-pattern mode.	191.3.3	Receive continuously as illustrated in Figure 191–14.	PHY_D* 10G:M	Yes [] N/A []
TPG4	5G & 2.5G Receive PCS operating in test-pattern mode.	191.3.3	Receive continuously as illustrated in Figure 191–15.	PHY_D* (2.5G+ 5G):M	Yes [] N/A []

191.15.4.2.4 OAM

Item	Feature	Subclause	Value/Comment	Status	Support
OAM1	State diagram behavior	191.3.7	Conforms to Figure 149–24 and Figure 149–25	OAM:M	Yes [] N/A []
OAM2	OAM frame data	149.3.9.2.2	Reserved fields shall be set to 0	OAM:M	Yes [] N/A []
OAM3	OAM frame data symbol encoding	149.3.9.2.13	Using Reed-Solomon code (16,14)	OAM:M	Yes [] N/A []
OAM4	Parity calculation	149.3.9.2.13	Same result as the shift register implementation shown in Figure 149–23	OAM:M	Yes [] N/A []
OAM5	BASE-T1 OAM Frame acceptance criteria	149.3.9.2.14	Described in 149.3.9.2.14	OAM:M	Yes [] N/A []
OAM6	mr_tx_received	149.3.9.4.3	Clear on read	OAM:M	Yes [] N/A []
OAM7	OAM frame structure	191.3.7.2	As defined in 191.3.7.2.1	OAM:M	Yes [] N/A []
OAM8	PHY health	191.3.7.2	As defined in 191.3.7.2.2	OAM:M	Yes [] N/A []
OAM9	PHY health indicator	191.3.7.2	As defined in 191.3.7.2.3	OAM:M	Yes [] N/A []

191.15.4.2.5 PCS, LS_TX

Item	Feature	Subclause	Value/Comment	Status	Support
PCT_L1	PCS 64B/65B Transmit state diagram	191.4.2.2	Figure 191–19.	PHY_D: M	Yes []
PCT_L2	PCS Transmit bit ordering	191.4.2.2	Figure 191–22.	PHY_D: M	Yes [] N/A []
PCT_L3	If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass a Z symbol at each symbol period to the PMA via the PMA_UNITDATA.request primitive.	191.4.2.2		PHY_D: M	Yes []
PCT_L4	If a PMA_TXMODE.indication message has the value SEND_T, PCS Transmit shall generate a sequence (T_n) defined in 191.3.4.1 to the PMA via the PMA_UNITDATA.request primitive.	191.4.2.2		PHY_D: M	Yes []
PCT_L5	If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation and the PCS Transmit function shall use a 65B coding technique to generate, at each symbol period, code-groups that represent data or control.	191.4.2.2		PHY_D: M	Yes []
PCT_L6	All XGMII control code values that do not appear in the Table 149–2 shall not be transmitted and shall be treated as an error if received.	191.4.2.2.5		PHY_D: M	Yes []
PCT_L7	Idle control characters	191.4.2.2.7	/I/ insertion and deletion shall occur in groups of 4.	PHY_D: M	Yes []
PCT_L8	Adding Idle control characters	191.4.2.2.7	/I/s shall not be added while data is being received.	PHY_D: M	Yes []
PCT_L9	Deleting Idle control characters	191.4.2.2.7	When deleting /I/s, the first four characters after a /T/ shall not be deleted.	PHY_D: M	Yes []
PCT_L10	Ordered set	191.4.2.2.10	Sequence ordered set deletion shall only occur when two consecutive sequence ordered sets have been received and shall delete only one of the two.	PHY_D: M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
PCT_L11	RS-FEC encoding.	191.4.2.2.13	Generates six 8-bit parity symbols (24 bits total).	PHY_D: M	Yes []
PCT_L12	CRC-6 calculation.	191.4.2.2.15	(CRC-6) shall be calculated over the 270 bits of information payload (comprising tx_group4x65B<259:0> and OAM_field<9:0>).	PHY_D: M	Yes [] N/A []
PCT_L13	CRC-6.	191.4.2.2.15	Equation (191–7) and Figure 191–25.	PHY_D: M	Yes [] N/A []
PCT_L14	CRC-6 delay elements shall be initialized to zero.	191.4.2.2.15	Always initialized to all zeros	PHY_D: M	Yes [] N/A []
PCT_L15	PHY_D transmitter side-stream scrambler generator polynomial.	191.4.2.2.17	Equation (191–9).	PHY_D: M	Yes [] N/A []
PCT_L16	In no case shall the scrambler state be initialized to all zeros.	191.4.2.2.17	Never initialized to all zeros.	PHY_D: M	Yes [] N/A []
PCT_L17	This scrambler, once started during PMA TRAINING STATE, shall continue to run uninterrupted during transition from SEND_T to SEND_N.	191.4.2.2.17	Runs continuously once started during PMA TRAINING state.	PHY_D: M	Yes [] N/A []

191.15.4.2.6 PCS, LS_RX

Item	Feature	Subclause	Value/Comment	Status	Support
PCRL1	PCS 64B/65B Receive state diagram	191.4.2.3	Figure 191–20.	PHY_S: M	Yes []
PCRL2	LS_RX PCS receive bit ordering	191.4.2.3	Figure 191–23.	PHY_S: M	Yes [] N/A []
PCRL3	LS_RX Frame and block synchronization	191.4.2.3.1	Described in 191.4.2.3.1.	PHY_S: M	Yes [] N/A []
PCRL4	PHY_S receiver descrambler.	191.4.2.3.2	Equation (191–9).	PHY_D: M	Yes [] N/A []
PCRL5	RS-FEC parity bits	191.4.2.3.3	Checks RS-FEC parity per 191.4.2.2.14.	PHY_D: M	Yes [] N/A []

191.15.4.2.7 Test-pattern generators, LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
TPGL1	LS_TX PCS operating in test-pattern mode.	191.4.3	Transmit continuously as illustrated in Figure 191–11, with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value.	PHY_D: M	Yes [] N/A []
TPG2	LS_RX PCS operating in test-pattern mode.	191.4.3	Receive continuously as illustrated in Figure 191–14.	PHY_S: M	Yes [] N/A []

191.15.4.2.8 PMA training frame, LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
PTFL1	Infobfield Reserved Bits.	191.4.4	Set to zero.	PHY_D: M	Yes [] N/A []
PTFL2	OAMfield.	191.4.4	Zeros sent in the OAM field of the training frame.	PHY_D: M	Yes [] N/A []
PTFL3	Reserved bits.	191.4.4	As in 191.5.2.4.1.	PHY_D: M	Yes [] N/A []
PTFL4	Scramber sync.	191.4.4.1	Acquires descrambler synchronization and reports via scr_status.	PHY_S: M	Yes [] N/A []

191.15.4.3 Physical Medium Attachment (PMA)

191.15.4.3.1 PMA Reset function

Item	Feature	Subclause	Value/Comment	Status	Support
PR1	PMA Reset	191.5.2.1	Described in 191.5.2.1	M	Yes []

191.15.4.3.2 PMA Transmit function

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT1	PMA Transmit Operation.	191.5.2.2	When not in DISABLE_TRANSMITTER state, Continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI.	M	Yes []
PMAT2	Tx_symb during Link Synchronization.	191.5.2.2	When sync_link_control = DISABLE and Auto-Negotiation is either not implemented or not enabled, use sync_tx_symb in place of tx_symb	M	Yes []
PMAT3	Signals generated by HS_TX PMA.	191.5.2.2	Comply with 191.6.2.	PHY_S: M	Yes [] N/A []
PMAT4	Signals generated by LS_TX PMA.	191.5.2.2	Comply with 191.7.2.	PHY_D: M	Yes [] N/A []
PMAT5	PHY_S as Leader clock source.	191.5.2.2	Sourced from a local clock source while meeting the transmit jitter requirements of 191.6.2.1.	PHY_S: M	Yes [] N/A []
PMAT6	PHY_D as Leader clock source.	191.5.2.2	Sourced from a local clock source while meeting the transmit jitter requirements of 191.7.2.1.	PHY_D: M	Yes [] N/A []
PMAT7	Leader-Follower relationship	191.5.2.2	Include loop timing.	M	Yes []
PMAT8	PHY_S as Follower clock source.	191.5.2.2	Sourced from a the tx_symbol clock of 191.5.2.9 while meeting the transmit jitter requirements of 191.6.2.1.	PHY_S: M	Yes [] N/A []
PMAT9	PHY_D as Follower clock source.	191.5.2.2	Sourced from a the tx_symbol clock of 191.5.2.9 while meeting the transmit jitter requirements of 191.7.2.1.	PHY_D: M	Yes [] N/A []
PMAT10	TX_TCLK when Follower	191.5.2.2	Sourced from the recovered clock of 191.5.2.9 while meeting the transmit jitter requirements of 191.6.2.1.	M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT11	Support operation as Leader	191.5.2.2	PHY_D always supports Leader, PHY_S optionally supports Leader	PHY_D: M PHY_S: O	Yes [] N/A []
PMAT12	Support operation as Follower	191.5.2.2	PHY_S always supports Follower, PHY_D optionally supports Follower	PHY_D: O PHY_S: M	Yes [] N/A []
PMAT13	PMA transmit fault function	191.5.2.2	Mapped to the transmit fault bit as specified in 45.2.1.7.4.	MDIO:M	Yes [] N/A []
PMAT14	DME Encoding.	191.5.2.2	Encoding per 191.5.2.2.1 when not in SEND_Z, used by PHY_D. Used by PHY_S in link synchronization.	M	Yes []
PMAT15	DME Encoding rules.	191.5.2.2.1	See 191.5.2.2.1.	M	Yes []

191.15.4.3.3 PMA Receive function

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	Quality of received symbols	191.5.2.3	RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 191.9 for -T1 and 191.10 for -V1.	M	Yes []
PMAR2	If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.250.7.	191.5.2.3		MDIO:M	Yes [] N/A []

191.15.4.3.4 PHY Control function, HS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
PCF1	12-octet Infocfield	191.5.2.4	Include the fields in 191.5.2.4.2 through 191.5.2.4.7	PHY_S: M	Yes [] N/A []
PCF2	Infocfield repetition (10G & 5G).	191.5.2.4	Transmitted at least 256 times with each change to octets 7 to 10.	PHY_S* (5G+ 10G):M	Yes [] N/A []
PCF3	Infocfield repetition (2.5G).	191.5.2.4	Transmitted at least 128 times with each change to octets 7 to 10.	PHY_S* 2.5G:M	Yes [] N/A []
PCF4	Infocfield reserved bits	191.5.2.4.1	Set to zero on transmit and ignored when received by the link partner	PHY_S: M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
PCF5	Start of Frame Delimiter hexadecimal value	191.5.2.4.2	0xBBA700	PHY_S: M	Yes [] N/A []
PCF6	PMA_state<7:6>	191.5.2.4.4	Communicate the state of the transmitting transceiver to the link partner	PHY_S: M	Yes [] N/A []
PCF7	Valid Infocfield message field.	191.5.2.4.4	Only values in Table 191–5 and Table 191–6 are transmitted, and any other value is ignored by the receiver.	PHY_S: M	Yes [] N/A []
PCF8	Initial Message setting.	191.5.2.4.4	First row of Table 191–5 for the Leader and first row of Table 191–6 for the Follower.	PHY_S: M	Yes [] N/A []
PCF9	Message Field transition.	191.5.2.4.4	Subsequent settings are either the same setting or the next row of Table 191–5 (Leader) or Table 191–6 (Follower).	PHY_S: M	Yes [] N/A []
PCF10	OAM enablement.	191.5.2.4.4	OAM enabled only if both PHYs set OAMen = 1.	OAM:M	Yes [] N/A []
PCF11	Capability validity.	191.5.2.4.5	PHY capability bits are only valid when loc_rcvr_status = 1.	PHY_S: M	Yes [] N/A []
PCF12	Reserved portion of infocfield.	191.5.2.4.5	Remaining bits are reserved and are set to zero per 191.5.2.4.1.	PHY_S: M	Yes [] N/A []
PCF13	DataSwPFC24	191.5.2.4.6	Set to an integer multiple of 16	PHY_S: M	Yes [] N/A []
PCF14	DataSwPFC24 for countdown value for 5 Gb/s & 10 Gb/s.	191.5.2.4.6	Minimum of 4081 and a maximum of 4785 from the current PFC24 value.	PHY_S* (5G+10G):M	Yes [] N/A []
PCF15	DataSwPFC24 for countdown value for 2.5 Gb/s.	191.5.2.4.6	Minimum of 2033 and a maximum of 2385 from the current PFC24 value.	PHY_S* 2.5G:M	Yes [] N/A []
PCF16	CRC16 polynomial	191.5.2.4.7	$(x + 1)(x^{15} + x + 1)$ of the previous 7 octets	PHY_S: M	Yes [] N/A []
PCF17	CRC16	191.5.2.4.7	Figure 191–32	PHY_S: M	Yes [] N/A []
PCF18	CRC16 delay elements	191.5.2.4.7	All initialized to zero	PHY_S: M	Yes [] N/A []

191.15.4.3.5 PHY Control function, LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
PCFL1	65-bitt Infofield	191.5.2.5	Include the fields in 191.5.2.5.2 through 191.5.2.5.5	PHY_D: M	Yes [] N/A []
PCFL2	Infofield repetition.	191.5.2.5	Transmitted at least 128 times with each change to octets 5 to 8.	PHY_D: M	Yes [] N/A []
PCFL3	Start of Frame Delimiter hexadecimal value	191.5.2.5.2	0x15A	PHY_S: M	Yes [] N/A []
PCFL4	PMA_state<7:6>	191.5.2.5.3	Communicate the state of the transmitting transceiver to the link partner	PHY_S: M	Yes [] N/A []
PCFL5	Valid Infofield message field.	191.5.2.5.3	Only values in Table 191–5 and Table 191–6 are transmitted, and any other value is ignored by the receiver.	PHY_S: M	Yes [] N/A []
PCFL6	Initial Message setting.	191.5.2.5.3	First row of Table 191–5 for the Leader and first row of Table 191–6 for the Follower.	PHY_S: M	Yes [] N/A []
PCFL7	Message Field transition.	191.5.2.5.3	Subsequent settings are either the same setting or the next row of Table 191–5 (Leader) or Table 191–6 (Follower).	PHY_S: M	Yes [] N/A []
PCFL8	OAM enablement.	191.5.2.5.4	OAM enabled only if both PHYs set OAMen = 1.	OAM:M	Yes [] N/A []
PCFL9	Capability validity.	191.5.2.5.4	PHY capability bits are only valid when loc_rcvr_status = 1.	PHY_S: M	Yes [] N/A []

191.15.4.3.6 PHY Control function, HS_PATH and LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
PCFB1	PHY Control State diagram	191.5.2.6	Figure 191–34.	M	Yes []
PCFB2	Startup timing.	191.5.2.6	Complies with Table 191–9 for PHY_S Leader and Table 191–10 for PHY_D as Leader.	M	Yes []

191.15.4.3.7 Link Monitor function

Item	Feature	Subclause	Value/Comment	Status	Support
LMK1	Link Monitor function	191.5.2.7	Comply with Figure 191–35	M	Yes []

191.15.4.3.8 PHY Link Synchronization

Item	Feature	Subclause	Value/Comment	Status	Support
PLS1	Link Synchronization function.	191.5.2.8	Figure 191–38 if Auto-Negotiation is not implemented or not enabled.	M	Yes []

191.15.4.3.9 MDI

Item	Feature	Subclause	Value/Comment	Status	Support
MDIS1	HS_TX -T1 Symbol response $s(t)$	191.5.2.10.1	Comply with the electrical specifications given in 191.6.2	T1* PHY_S: M	Yes [] N/A []
MDIS2	LS_TX -T1 Symbol response $s(t)$	191.5.2.10.1	Comply with the electrical specifications given in 191.7.2	T1* PHY_D: M	Yes [] N/A []
MDIS3	HS_TX -V1 Symbol response $s(t)$	191.5.2.11	Comply with the electrical specifications given in 191.6.2	V1* PHY_S: M	Yes [] N/A []
MDIS4	LS_TX -V1 Symbol response $s(t)$	191.5.2.11	Comply with the electrical specifications given in 191.7.2	V1* PHY_D: M	Yes [] N/A []

191.15.4.4 PMA electrical specifications

191.15.4.4.1 Test modes, HS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Test modes	191.6.1	Provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER testing	PHY_S: M	Yes [] N/A []
TM2	Test mode enabling	191.6.1	Enabled by setting a control register, 1.2313.15:13, or equivalent functionality	PHY_S* MDIO:M	Yes [] N/A []
TM3	Test modes do not alter electrical or jitter characteristics.	191.6.1	Only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.	PHY_S: M	Yes [] N/A []
TM4	Test Mode 1, clock access	191.6.1	Provide access to frequency-reduced version of transmit clock, TX_CLK_175.	PHY_S: M	Yes [] N/A []
TM5	Test Mode 2, PAM4	191.6.1	Transmit JP03A (see 94.2.9.1) or JP03B (see 94.2.9.2) per Table 191–15.	PHY_S* 10G:M	Yes [] N/A []
TM6	Test Mode 2, PAM2	191.6.1	Transmit PAM2 0101.	PHY_S* (2.5G+ 5G):M	Yes [] N/A []
TM7	Test Mode 3, Precoder operation (10G only).	191.6.1	Continuous pattern of {0,3}.	PHY_S* 10G:M	Yes [] N/A []
TM8	Test Mode 4, Transmit linearity, 10G	191.6.1	Generate PRBS13Q.	PHY_S* 10G:M	Yes [] N/A []
TM9	Test Mode 4, Transmit linearity, 2.5G & 5G	191.6.1	Generate PRBS13.	PPHY_S *(2.5G+ 5G):M	Yes [] N/A []
TM10	Test Mode 5, PSD mask	191.6.1	Transmit as in normal operation with normal interframe idle as the input.	PHY_S: M	Yes [] N/A []
TM11	Test Mode 6, droop	191.6.1	Transmit $128 \times S \{+1\}$ followed by $128 \times S \{-1\}$ symbols locally timed.	PHY_S: M	Yes [] N/A []

191.15.4.4.2 Transmitter electrical specifications, HS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
TES1	AC Coupling.	191.6.2	Present a high dc common-mode impedance at the MDI.	PHY_S: M	Yes [] N/A []
TES2	Load for -T1 tests.	191.6.2	Meet electrical requirements with a 100 Ω differential load.	PHY_S* T1:M	Yes [] N/A []
TES3	Load for -V1 tests.	191.6.2	Meet electrical requirements with a 50 Ω load.	PHY_S* V1:M	Yes [] N/A []
TES4	Leader RMS timing jitter at TX_TCLK.	191.6.2.1	Less than J ps (see Table 191–14).	PHY_S: M	Yes [] N/A []
TES5	Leader peak-to-peak value of timing jitter at TX_TCLK.	191.6.2.1	Less than $10 \times J$ ps (see Table 191–14).	PHY_S: M	Yes [] N/A []
TES6	Follower RMS timing jitter at TX_TCLK	191.6.2.1	Less than 6 ps and less than 3 ps over 100 kHz.	PHY_S: M	Yes [] N/A []
TES7	Follower peak-to-peak timing jitter at TX_TCLK.	191.6.2.1	Less than 60 ps.	PHY_S: M	Yes [] N/A []
TES8	Leader RMS timing jitter at the MDI.	191.6.2.2	Less than J ps (see Table 191–14), using test mode 2 and test fixture 3.	PHY_S: M	Yes [] N/A []
TES9	Leader peak-to-peak timing jitter at the MDI.	191.6.2.2	Less than $10 \times J$ ps (see Table 191–14), using test mode 2 and test fixture 3.	PHY_S: M	Yes [] N/A []
TES10	Leader deterministic jitter at the MDI.	191.6.2.3	Less than $9 \times J$ ps (see Table 191–14), using test mode 2 and test fixture 3.	PHY_S: M	Yes [] N/A []
TES11	Leader EOJ at the MDI.	191.6.2.3	Less than $4 \times J$ ps (see Table 191–14), using test mode 2 and test fixture 3.	PHY_S: M	Yes [] N/A []
TES12	Leader transmitter clock frequency	191.6.2.4	Within the range $5625 \times S$ MHz $\pm$ 100 ppm	PHY_S: M	Yes [] N/A []
TES13	Short-term frequency variation	191.6.2.4	Less than 1%/second	PHY_S: M	Yes [] N/A []
TES14	Transmitter SNDR distortion for 10G+100MBASE-T1/V1.	191.6.2.5	Exceed 36 dB	PHY_S* 10G:M	Yes [] N/A []
TES15	Transmitter SNDR distortion for 5G+100MBASE-T1/V1.	191.6.2.5	Exceed 33 dB	PHY_S* 5G:M	Yes [] N/A []
TES16	Transmitter SNDR distortion for 2.5G+100MBASE-T1/V1.	191.6.2.5	Exceed 30 dB	PHY_S* 2.5G:M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
TES17	Transmit power level	191.6.2.6	Table 191–16.	PHY_S: M	Yes [] N/A []
TES18	PSD of the transmitter	191.6.2.6	PSD between bounds of Equation (191–13) and Equation (191–14)	PHY_S: M	Yes [] N/A []
TES19	Transmitter quiet signal level.	191.6.2.7	Less than –36 dB	PHY_S: M	Yes [] N/A []
TES20	Transmitter peak-to-peak voltage	191.6.2.7	Table 191–17	PHY_S: M	Yes [] N/A []
TES21	Maximum output droop	191.6.2.8	Positive and negative droop shall be less than 30%	PHY_S: M	Yes [] N/A []

191.15.4.4.3 Receiver electrical specifications, HS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
RES1	Receiver differential input signals	191.6.3.1	BER less than 10^{-12} after RS-FEC decoding	PHY_D: M	Yes [] N/A []
RES1	Broadband noise rejection	191.6.3.2	BER less than 10^{-12} with noise from Table 191–18.	PHY_D: M	Yes [] N/A []

191.15.4.4.4 Test modes, LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
TML1	Test modes	191.7.1	Provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER testing	PHY_D: M	Yes [] N/A []
TML2	Test mode enabling	191.7.1	Enabled by setting a control register, 1.2313.15:13, or equivalent functionality	PHY_D* MDIO:M	Yes [] N/A []
TML3	Test modes do not alter electrical or jitter characteristics.	191.7.1	Only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal operation.	PHY_D: M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
TML4	Test Mode 1, clock access	191.7.1	Provide access to frequency-reduced version of transmit clock, TX_CLK_175.	PHY_D: M	Yes [] N/A []
TML5	Test Mode 2, DME	191.7.1	Transmit DME encoded ones.	PHY_D: M	Yes [] N/A []
TML6	Test Mode 4, Transmit linearity	191.7.1	Generate PRBS13.	PHY_D: M	Yes [] N/A []
TML7	Test Mode 5, PSD mask	191.7.1	Transmit as in normal operation with normal interframe idle as the input.	PHY_D: M	Yes [] N/A []
TML8	Test Mode 6, droop	191.7.1	Transmit a continuous pattern of 3 {+1} followed by 3 {-1} symbols.	PHY_D: M	Yes [] N/A []

191.15.4.4.5 Transmitter electrical specifications, LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
TESL1	AC Coupling.	191.7.2	Present a high dc common-mode impedance at the MDI.	PHY_D: M	Yes [] N/A []
TESL2	Load for -T1 tests.	191.7.2	Meet electrical requirements with a 100 Ω differential load.	PHY_D* T1:M	Yes [] N/A []
TESL3	Load for -V1 tests.	191.7.2	Meet electrical requirements with a 50 Ω load.	PHY_D* V1:M	Yes [] N/A []
TESL4	Leader RMS timing jitter at TX_TCLK.	191.7.2.1	Less than J ps (see Table 191-14).	PHY_D: M	Yes [] N/A []
TESL5	Follower peak-to-peak value of timing jitter at TX_TCLK.	191.7.2.1	Less than $10 \times J$ ps (see Table 191-14).	PHY_D: M	Yes [] N/A []
TESL6	Follower RMS timing jitter at TX_TCLK	191.7.2.1	Less than 50 ps.	PHY_D: M	Yes [] N/A []
TESL7	Follower peak-to-peak timing jitter at TX_TCLK.	191.7.2.1	Less than 5000 ps.	PHY_D: M	Yes [] N/A []
TESL8	Leader RMS timing jitter at the MDI.	191.7.2.2	Less than J ps (see Table 191-14).	PHY_D: M	Yes [] N/A []
TESL9	Leader peak-to-peak timing jitter at the MDI.	191.7.2.2	Less than $10 \times J$ ps (see Table 191-14).	PHY_D: M	Yes [] N/A []
TESL10	Leader transmitter clock frequency	191.7.2.4	Within the range 5625 / 48 MHz $\pm$ 100 ppm	PHY_D: M	Yes [] N/A []
TESL11	Follower transmitter clock frequency	191.7.2.4	Within the range 5625 / 48 MHz $\pm$ 1/-20%	PHY_D: M	Yes [] N/A []
TESL12	Short-term frequency variation	191.7.2.4	Less than 1%/second	PHY_D: M	Yes [] N/A []
TESL13	Transmitter rise/fall time.	191.7.2.5	Less than 1.5 ns.	PHY_D: M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
TESL14	Transmitter SNDR distortion for PHY_D.	191.7.2.6	Shall exceed 30 dB	PHY_D: M	Yes [] N/A []
TESL15	Transmit power level	191.7.2.7	Table 191–21.	PHY_D: M	Yes [] N/A []
TESL16	PSD of the transmitter	191.7.2.7	PSD between bounds of Equation (191–15) and Equation (191–16)	PHY_D: M	Yes [] N/A []
TESL17	Transmitter quiet signal level.	191.7.2.7	Less than –36 dB	PHY_D: M	Yes [] N/A []
TESL18	Transmitter peak-to-peak voltage, T1	191.7.2.8	Less than 1.0 V peak-to-peak at the MDI.	PHY_D* T1:M	Yes [] N/A []
TESL19	Transmitter peak-to-peak voltage, V1	191.7.2.8	Less than 0.5V peak-to-peak at the MDI.	PHY_D* V1:M	Yes [] N/A []
TESL20	Maximum output droop	191.7.2.9	Positive and negative droop shall be less than 30%	PHY_D: M	Yes [] N/A []

191.15.4.4.6 Receiver electrical specifications, LS_PATH

Item	Feature	Subclause	Value/Comment	Status	Support
RESL1	Receiver differential input signals	191.7.3.1	BER less than 10^{-10} after RS-FEC decoding	PHY_S: M	Yes [] N/A []

191.15.4.4.7 Auto-Negotiation support

Item	Feature	Subclause	Value/Comment	Status	Support
ANS1	Auto-Negotiation compliance	191.8.1	Meets requirements of Clause 98.	AN:M	Yes [] N/A []

191.15.4.5 Link segment characteristics, –T1

Item	Feature	Subclause	Value/Comment	Status	Support
LSCT1	Insertion loss	191.9.1.1	See Equation (191–17)	INS*T1: M	Yes [] N/A []
LSCT2	Return loss	191.9.1.3	See Equation (191–19)	INS*T1: M	Yes [] N/A []
LSCT3	Coupling attenuation	191.9.1.4	See Equation (149–24)	INS*T1: M	Yes [] N/A []
LSCT4	Screening attenuation	191.9.1.5	Meets requirements of 149.7.1.5.	INS*T1: M	Yes [] N/A []
LSCT5	Maximum link delay	191.9.1.6	Not to exceed 160 ns at all frequencies between 3 MHz and $F_{\max}$ MHz	INS*T1: M	Yes [] N/A []
LSCT6	PSANEXT	191.9.2.1	See Equation (149–25)	INS*T1: M	Yes [] N/A []
LSCT7	PSAACRF	191.9.2.2	See Equation (149–26)	INS*T1: M	Yes [] N/A []

191.15.4.6 Link segment characteristics, –V1

Item	Feature	Subclause	Value/Comment	Status	Support
LSCT1	Insertion loss	191.10.1.1	See Equation (191–17)	INS*V1: M	Yes [] N/A []
LSCT2	Return loss	191.10.1.3	See Equation (191–19)	INS*V1: M	Yes [] N/A []
LSCT3	Screening attenuation	191.10.1.5	Equation (191–20).	INS*V1: M	Yes [] N/A []
LSCT4	Maximum link delay	191.10.1.6	Not to exceed 160 ns at all frequencies between 3 MHz and $F_{\max}$ MHz	INS*V1: M	Yes [] N/A []
LSCT5	Coupling parameters	191.10.2	See 191.10.2.	INS*V1: M	Yes [] N/A []
LSCT6	PSANEXT	191.10.2.1	Equation (191–21)	INS*V1: M	Yes [] N/A []
LSCT7	PSAACRF	191.10.2.2	Equation (191–22)	INS*V1: M	Yes [] N/A []

191.15.4.7 MDI specifications

Item	Feature	Subclause	Value/Comment	Status	Support
MDI1	Return loss, $-T1$.	191.11.2.1	Equation (191–23)	INS*T1: M	Yes [] N/A []
MDI2	MDI fault tolerance, $-T1$.	191.11.3	See 96.8.3.	INS*T1: M	Yes [] N/A []
MDI3	Return loss, $-V1$.	191.12.2.1	Equation (191–24)	INS*V1: M	Yes [] N/A []
MDI4	MDI fault tolerance, $-V1$.	191.12.3	Withstand short circuits without damage to potentials in Table 191–23.	INS*V1: M	Yes [] N/A []
MDI5	MDI recovery, $-V1$.	191.12.3	Normal operation shall resume after the short circuit(s) is (are) removed.	INS*V1: M	Yes [] N/A []

191.15.4.8 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Path delays.	191.14	Not to exceed the limits in Table 191–24	M	Yes []

192. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

192.1 Overview

MultiGBASE-AT1 and MultiGBASE-AV1 PHYs use a time-division duplex (TDD) transmission structure between two active PHYs, in which one link partner transmits a burst while the other is silent. Each PHY may support multiple data rates. MultiGBASE-A PHYs use a common set of symbol rates across high speed and low speed implementations. They also use the same TDD cycle for all data rates (see 192.3.4) and the same base FEC with different shortening parameters for the high speed and low speed directions.

Each link partner transmits according to a TDD cycle consisting of the following three phases:

- 1) a PAM2 modulated burst refresh header,
- 2) a PAM2, PAM3, or PAM4 modulated burst payload,
- 3) and a QUIET period during which no data is transmitted.

Bursts are aligned so that a PHY transmits its refresh header and burst payload during its link partner's QUIET period. The burst timing provides a gap between transmitted and received bursts to allow for signal propagation delay. Ethernet frames are encoded in 64B/65B blocks and protected in RS-FEC frames (with interleaving at 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates). The RS-FEC frames comprise the burst payload portion of the TDD cycle. Asymmetric data rates are achieved by asymmetric transmission times for the link partners, with one transmitting 25 RS-FEC superframes per burst and the other transmitting one RS-FEC frame per burst. See 192.3.4 for more detail on TDD bursts.

A MultiGBASE-A PHY may operate as the Leader or the Follower. The Leader PHY uses a local clock to time its transmitter operations. The Follower PHY recovers the clock from the received signal and uses it to time its transmitter operations. The Leader-Follower relationship is predetermined via management control during initialization or via default hardware setup.

A device that supports multiple simultaneous MultiGBASE-A PHYs may choose to align the start time of its transmit TDD cycle across links operating as the Leader to reduce crosstalk. Such an alignment is optional and implementation specific.

192.1.1 Nomenclature

The MultiGBASE-AT1 and MultiGBASE-AV1 PHYs described in this clause represent two distinct PHY types that share the same PCS and PMA specifications subject to frequency scaling. In order to efficiently describe the two PHYs, the following nomenclature is used.

HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter
MultiGBASE-A	Refers to all MultiGBASE-AT1 and MultiGBASE-AV1 PHYs regardless of cable type or bit rate
MultiGBASE-AT1	Refers to the asymmetric PHY communicating on a single shielded balanced pair of conductors
MultiGBASE-AV1	Refers to the asymmetric PHY communicating on a single coaxial cable

N_r	Number of symbols transmitted in the refresh header of a TDD burst
N_p	Number of symbols transmitted in the payload of a TDD burst
N_z	Number of transmit symbol periods during which the TDD burst is QUIET
PHY_D	LS_TX, HS_RX mode of operation (high speed XGMII destination)
PHY_S	HS_TX, LS_RX mode of operation (high speed XGMII source)

The six modes of operation and MAC data rate combinations for each of the two PHY types are shown in Table 192–1.

Table 192–1—PHY type definitions

PHY name	Medium interface	Mode of operation	Transmit MAC data rate	Receive MAC data rate
MultiGBASE-AT1	Differential (balanced)	PHY_D	100 Mb/s	2.5 Gb/s
			100 Mb/s	5 Gb/s
			100 Mb/s	7.5 Gb/s
			100 Mb/s	10 Gb/s
		PHY_S	2.5 Gb/s	100 Mb/s
			5 Gb/s	100 Mb/s
			7.5 Gb/s	100 Mb/s
			10 Gb/s	100 Mb/s
MultiGBASE-AV1	Single-ended (unbalanced)	PHY_D	100 Mb/s	2.5 Gb/s
			100 Mb/s	5 Gb/s
			100 Mb/s	7.5 Gb/s
			100 Mb/s	10 Gb/s
		PHY_S	2.5 Gb/s	100 Mb/s
			5 Gb/s	100 Mb/s
			7.5 Gb/s	100 Mb/s
			10 Gb/s	100 Mb/s

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

-T1	represents a single shielded balanced pair of conductors (i.e., differential)
-V1	represents a single coaxial cable (i.e., unbalanced)

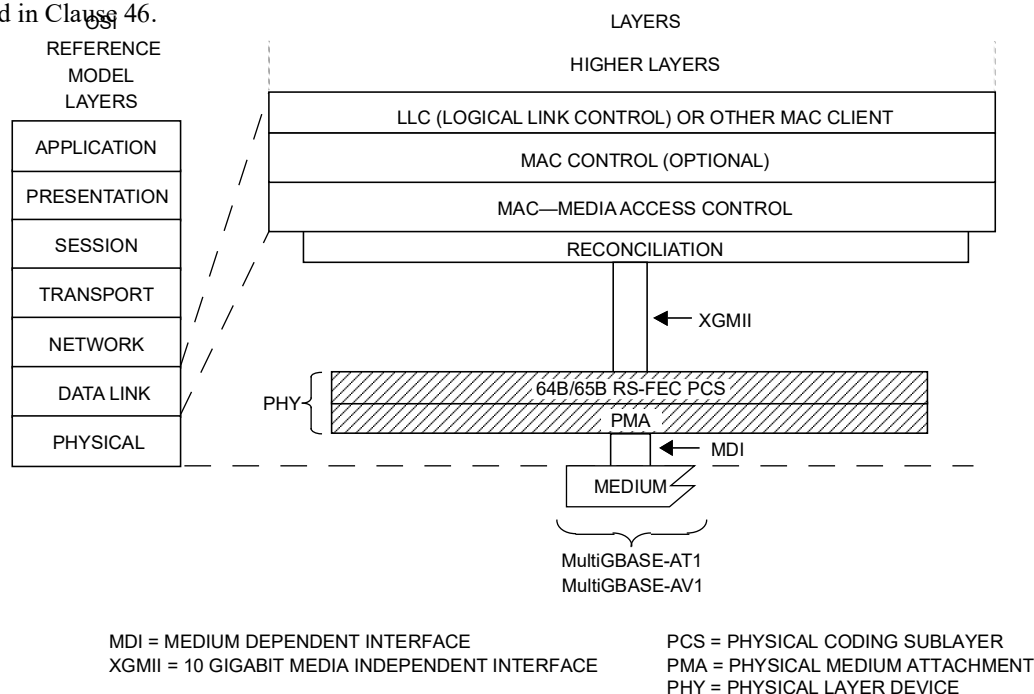
Additionally, for parameters that scale with the PHY's supported MAC data rate, the parameter S is used for scaling as shown in Table 192–2.

Table 192–2—Scaling parameters

Transmit MAC data rate	S
100 Mb/s	0.5
2.5 Gb/s	0.5
5 Gb/s	1
7.5 Gb/s	1
10 Gb/s	1

192.1.2 Relationship of MultiGBASE-A to other standards

The relationship between a MultiGBASE-A PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 192–1. The PHY sublayers (shown shaded) in Figure 192–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. The XGMII is defined in Clause 46.



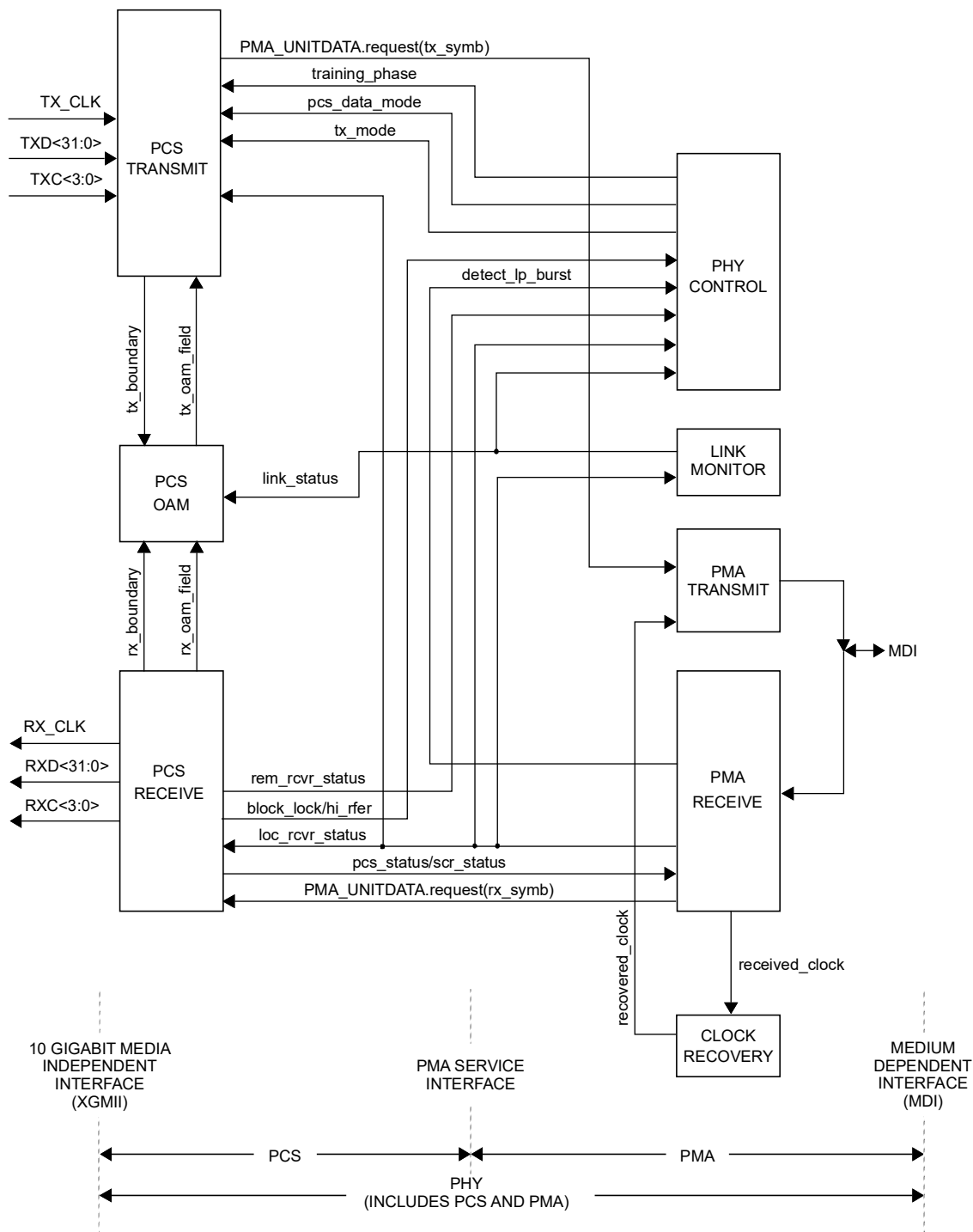
NOTE 1—XGMII is optional.

NOTE 2—Medium is a single shielded balanced pair of conductors for -AT1 and a single coaxial cable for -AV1.

Figure 192–1—Relationship of MultiGBASE-A PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model

192.1.3 Operation of MultiGBASE-A

The MultiGBASE-A functional block diagram is shown in Figure 192–2.



NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

Figure 192–2—Functional block diagram

192.1.3.1 Physical Coding Sublayer (PCS) in PHY_S mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the data mode of operation (see 192.2.1.8), the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in data mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 1-bit OAM field is appended to form a 976-bit block. A number, L (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 3 for 7.5 Gb/s, and L = 4 for 10 Gb/s), of these 976-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC(128,122) and the round-robin interleaving as described in 192.3.2.2.15. The RS-FEC output superframe consists of L × 1024 bits. The duration of the superframe is 1024 / 3 ns.

NOTE—Duration = L × 1024 bits / bits per symbol / baud rate. For 10 Gb/s, Duration = 4 × 1024 / 2 / 6 GBd; for 7.5 Gb/s, Duration = 3 × 1024 / 1.5 / 6 GBd; for 5 Gb/s, Duration = 2 × 1024 / 1 / 6 GBd; for 2.5 Gb/s, Duration = 1 × 1024 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the HS_TX payload. The PCS Transmit functions are described in 192.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where $i = 0$ to 14, $j = 0$ to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded₀<64:0> is the first block transmitted.

In the training mode (see 192.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 192.3. The interface to the PMA is an abstract message-passing interface specified in 192.4.

192.1.3.2 Physical Coding Sublayer (PCS) in PHY_D mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the data mode of operation (see 192.2.1.8), the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in data mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 17-bit OAM field is appended to form a 992-bit block. Each of these 992-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(130,124,8). The RS-FEC output frame consists of 1040 bits. The duration of the frame is $1040 / 3$ ns.

NOTE—Duration = 1040 bits / bits per symbol / baud rate = $1040 / 1 / 3$ GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the LS_TX payload. The PCS Transmit functions are described in 192.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}<65 \times i + j> = \text{tx\_coded}_i<j>$$

where $i = 0$ to 14, $j = 0$ to 64, and tx_coded_{*i*}<64:0> is the i^{th} 64B/65B block where tx_coded0<64:0> is the first block transmitted.

In the training mode (see 192.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 192.3. The interface to the PMA is an abstract message-passing interface specified in 192.4.

192.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto a single balanced pair of conductors (-T1) or a single coaxial cable (-V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides communications at $6 \times S$ GBd. See Table 192–2 for the definition of S .

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled and provides the startup functions required for successful operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link and communicates this status to other functional blocks. A failure of the receive link causes the data mode operation to stop and startup functions to restart.

PMA functions and state diagrams are specified in 192.4 and 192.5. The electrical parameters of the PMA (i.e., test modes and electrical specifications for the transmitter and receiver) are specified in 192.5.

192.1.4 LS_PATH signaling

LS_PATH signaling is performed by the LS_TX PCS generating continuous symbols that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The symbols consist of PAM2 symbols within a burst and Z symbols between bursts. The signaling scheme achieves a number of objectives including:

- Forward error correction (FEC) coded symbol mapping for data.
- Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the transmit path.
- Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
- Uncorrelated symbols in the transmitted symbol stream.
- No correlation between symbol streams traveling in opposite directions.
- Block framing and other control signals.

- g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
- h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the data mode or the training mode.

In both data mode and training mode, the LS_TX PCS generates a continuous stream of symbols that are transferred to the PMA during the payload (see Figure 192–31). The Z symbols are transmitted at the same symbol rate.

192.1.5 HS_PATH signaling

HS_PATH signaling is performed by the HS_TX PCS generating continuous symbols that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The symbols consist of PAM2, PAM3, or PAM4 symbols within a burst and Z symbols between bursts. The refresh headers use PAM2 regardless of the MAC data rate. The signaling scheme achieves a number of objectives including:

- a) Forward error correction (FEC) coded symbol mapping for data.
- b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, PAM3 symbols in the 7.5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
- c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
- d) Uncorrelated symbols in the transmitted symbol stream.
- e) No correlation between symbol streams traveling in opposite directions.
- f) Block framing and other control signals.
- g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
- h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the data mode or the training mode.

In both data and training modes, the HS_TX PCS generates a continuous stream of symbols that are transferred to the PMA during the payload (see Figure 192–31). The Z symbols are transmitted at the same symbol rate.

192.1.6 Interfaces

All MultiGBASE-A PHY implementations are compatible at the XGMII, if implemented. Implementation of the XGMII is optional. All MultiGBASE-AT1 PHY implementations are compatible at the -T1 MDI. All MultiGBASE-AV1 PHY implementations are compatible at the -V1 MDI. The MDI for a single balanced pair of conductors (-T1) and a single coaxial cable (-V1) are different. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

192.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

192.2 Service primitives and interfaces

MultiGBASE-A transfers data and control information across the following three service interfaces:

- a) 10 Gigabit Media Independent Interface (XGMII)
- b) PMA service interface
- c) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46. The PMA service interface is defined in 192.2.1. The -T1 MDI is defined in 192.9. The -V1 MDI is defined in 192.10.

192.2.1 PMA service interface

MultiGBASE-A uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication(pcs_data_mode)
PMA_PCSSYNC.request(block_lock, hi_rfer)

The use of these primitives is shown in Figure 192–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 192–3.

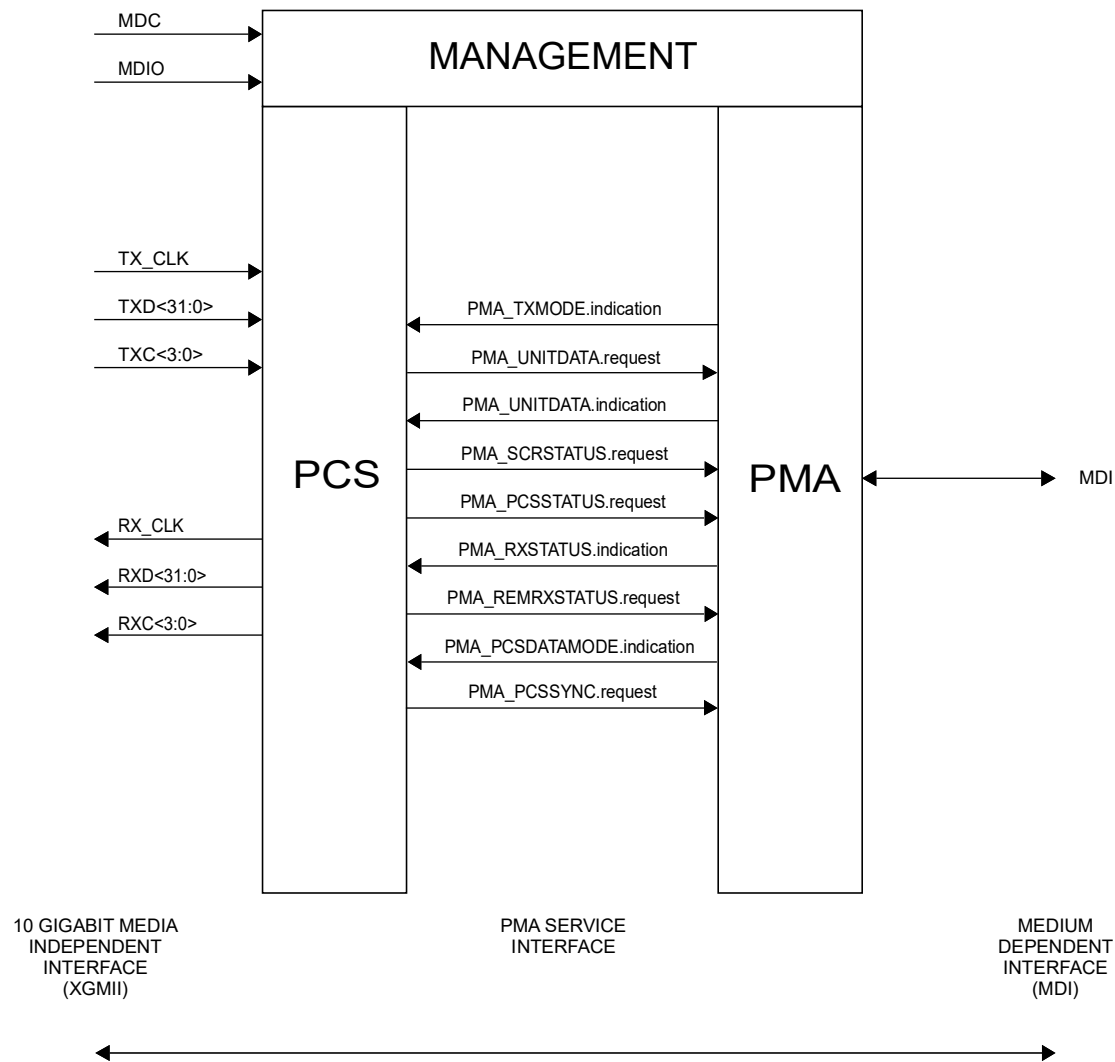


Figure 192-3—MultiGBASE-A service interface

192.2.1.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE-A link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

192.2.1.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values:

- SEND_N This value is continuously asserted during transmission of sequences of symbols representing the TDD bursting (including QUIET periods) of an XGMII data stream in the data mode.
- SEND_TS This value is continuously asserted when transmission of sequences of symbols representing the TDD symmetric training mode is to take place. LS_TX and HS_TX send at 3 GBd with PAM2 TDD training frames.
- SEND_TA This value is continuously asserted when transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. LS_TX sends at 3 GBd with PAM2 TDD training frames. HS_TX sends at 3 GBd or 6 GBd with PAM2 TDD training frames.
- SEND_Z This value is continuously asserted in case continuous transmission of Z symbols is required. See 192.5.2.4 for the encoding of Z.

192.2.1.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

192.2.1.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 192.3.2.2.

192.2.1.2 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 192.3.2.2 to represent XGMII data and control streams or other sequences.

192.2.1.2.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

The PMA_UNITDATA.request primitive conveys the value of the symbol to be transmitted over the MDI via the tx_symb parameter. The tx_symb may take on one of the following values:

- {-1, -1/3, +1/3, +1} 10 Gb/s transmit payload in data mode.
- {-1, 0, +1} 7.5 Gb/s transmit payload in data mode.
- {-1, +1} 2.5 Gb/s or 5 Gb/s transmit payload in data mode and all refresh header symbols in data and training modes.
- Z when Z symbols are to be transmitted (see 192.5.2.4) in the following two cases:
 - 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and
 - 2) during the QUIET period in each TDD cycle.

192.2.1.2.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

192.2.1.2.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 192.5.2.

192.2.1.3 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

192.2.1.3.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception, the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock. The rx_symb may take on the same values defined for tx_symb in 192.2.1.2.1.

192.2.1.3.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive, as governed by the recovered clock, is 3 GHz for 100 Mb/s and 2.5 Gb/s receive modes and 6 GHz for 5 Gb/s, 7.5 Gb/s, and 10 Gb/s receive modes.

192.2.1.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

192.2.1.4 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the PCS descrambler has achieved synchronization.

192.2.1.4.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values:

- OK The PCS descrambler has achieved synchronization.
- NOT_OK The PCS descrambler is not synchronized.

192.2.1.4.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

192.2.1.4.3 Effect of receipt

The effect of receipt of this primitive is specified in 192.4.2.3 and 192.4.2.4.

192.2.1.5 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

192.2.1.5.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values:

- OK The PCS is operating reliably in the data mode.
- NOT_OK The PCS is not operating reliably in the data mode.

192.2.1.5.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

192.2.1.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 192.4.2.3 and 192.4.4.1.

192.2.1.6 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criteria for setting the parameter loc_rcvr_status is left to the implementer. For example, it can be based on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

192.2.1.6.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values:

- OK This value is asserted and remains true during reliable operation of the receive link for the local PHY.
- NOT_OK This value is asserted whenever operation of the link for the local PHY is unreliable.

192.2.1.6.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

192.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–3, 192.3.2.3, 192.4.2.4, and 192.5.

192.2.1.7 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its `loc_rcvr_status` parameter. The parameter `rem_rcvr_status` conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter `rem_rcvr_status` is set to the value received in the `loc_rcvr_status` bit in the Infofield from the remote PHY. The `rem_rcvr_status` is set to `NOT_OK` if the PCS has not decoded a valid Infofield from the remote PHY.

192.2.1.7.1 Semantics of the primitive

PMA_REMRXSTATUS.request(`rem_rcvr_status`)

The `rem_rcvr_status` parameter can take on one of two values:

- OK The receive link for the remote PHY is operating reliably.
- NOT_OK Reliable operation of the receive link for the remote PHY is not detected.

192.2.1.7.2 When generated

The PCS generates PMA_REMRXSTATUS.request message to indicate a change in `rem_rcvr_status` based on the PCS decoding the `loc_rcvr_status` bit in Infofield messages received from the remote PHY during training.

192.2.1.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–31.

192.2.1.8 PMA_PCSDATAMODE.indication

This primitive indicates when the PCS 64B/65B state diagrams are able to process data. The `pcs_data_mode` variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

192.2.1.8.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(`pcs_data_mode`)

The `pcs_data_mode` parameter can take on one of two values:

- TRUE The PCS is transmitting and receiving data from the XGMII.
- FALSE The PCS is in a training or test mode.

192.2.1.8.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

192.2.1.8.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 192.3.2.2.

192.2.1.9 PMA_PCSSYNC.request

This primitive indicates the PCS alignment (`block_lock`) and error status (`hi_rfer`) to the PMA.

192.2.1.9.1 Semantics of the primitive

PMA_PCSSYNC.request(block_lock, hi_rfer)

The PMA_PCSSYNC.request primitive passes the block_lock and hi_rfer parameters from the PCS to the PMA.

The parameter block_lock is defined in 192.3.5.1.2.

The parameter hi_rfer is defined in 192.3.5.1.2.

192.2.1.9.2 When generated

The PCS generates PMA_PCSSYNC.request messages to indicate a change in block_lock or hi_rfer.

192.2.1.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–32 and Figure 192–33.

192.3 Physical Coding Sublayer (PCS) functions

192.3.1 PCS service interface (XGMII)

The PCS service interface allows the PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

192.3.2 PCS functions

The PCS comprises the following functions: PCS Reset, PCS Transmit, PCS Receive, and an optional PCS OAM. The PCS Transmit and PCS Receive functions execute simultaneously and asynchronously. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram (see Figure 192–4) shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 192–4.

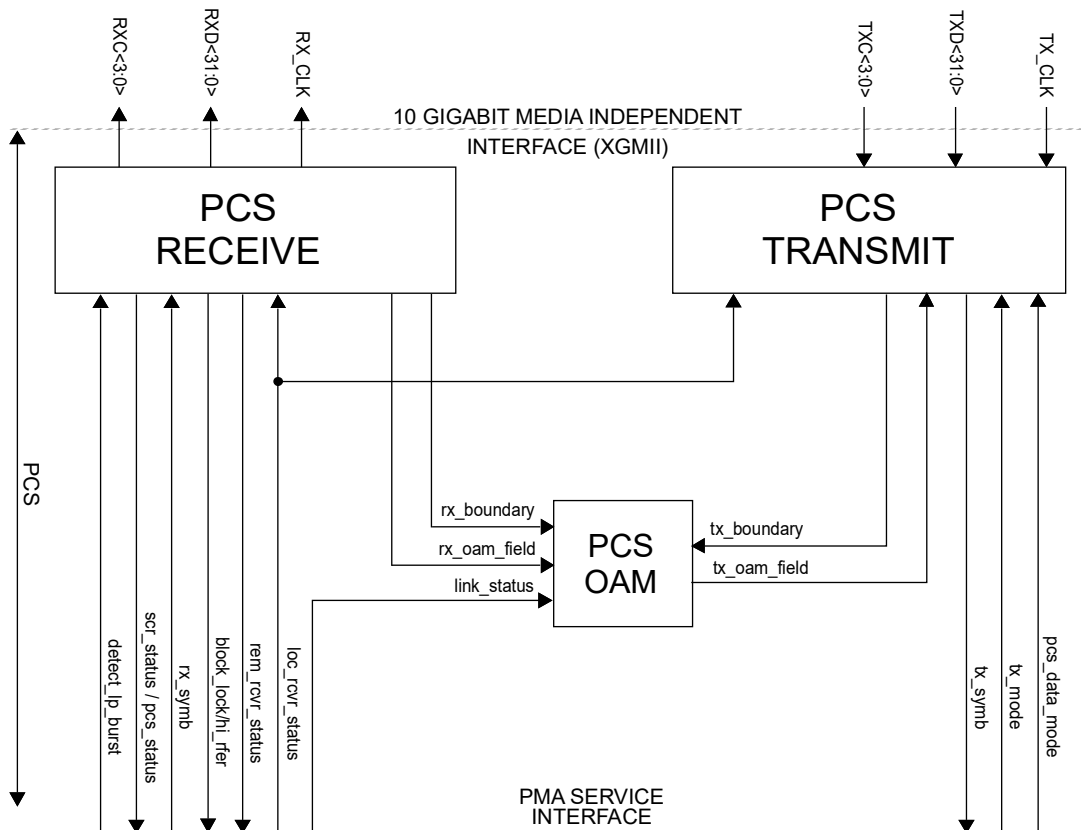


Figure 192-4—PCS reference diagram

192.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of following conditions occur:

- Power on (see 192.3.5.1.2)
- The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

192.3.2.2 PCS Transmit function

The LS_TX PCS Transmit function is shown in Figure 192–5 and the HS_TX PCS Transmit function is shown in Figure 192–6. The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram shown in Figure 192–22 and to the PCS Transmit bit ordering shown in Figure 192–5 and Figure 192–6.

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals.

Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format. In each TDD cycle, the transmit PCS generates a sequence of PAM symbols followed by a sequence of Z symbols representing the QUIET period to the transmit PMA. The transmit QUIET period allows the receive PMA to receive a burst during each TDD cycle.

For LS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the LS_TX PCS Transmit process take one group of 15 65B blocks and append a 17-bit OAM field to it, shown in Figure 192–5. This forms the input to the RS-FEC(130,124) encoder, which adds 48 parity bits. The resulting 1040 bits are then scrambled. These bits are then mapped, one at a time, into PAM2 symbols. Transmit data-units are sent to the LS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For HS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the HS_TX PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC(128,122) superframe which adds $L \times 48$ parity bits, shown in Figure 192–6. 25 such superframes are formed for one data payload. $L = 1$ for 2.5 Gb/s, $L = 2$ for 5 Gb/s, $L = 3$ for 7.5 Gb/s, and $L = 4$ for 10 Gb/s. The resulting $L \times 1024 \times 25$ bits are then scrambled. For 2.5 Gb/s and 5 Gb/s, these bits are then mapped, one at a time, into PAM2 symbols. For 7.5 Gb/s, these bits are then mapped, three at a time, into pairs of PAM3 symbols. For 10 Gb/s, these bits are then mapped, two at a time, into PAM4 symbols. Transmit data-units are sent to the HS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For both LS_TX and HS_TX, each set of transmit data-units forming the payload of a TDD burst are preceded by a PAM-2 mapped refresh header sequence of N_r symbols and followed by a sequence of N_z Z symbols to complete the TDD cycle (see Figure 192–18 and Figure 192–19). In each symbol period of a TDD burst, when communicating with the PMA, the PCS Transmit generates a PAM2, PAM3, or PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. Between TDD bursts, the PCS Transmit transfers Z symbols to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T , is $1000 / (6 \times S)$ ps. See Table 192–2 for the definition of S .

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function. During training, PMA_TXMODE.indication has values SEND_Z, SEND_TS, and SEND_TA before transitioning to SEND_N for data mode.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass Z symbols at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_TS or SEND_TA, PCS Transmit shall generate a sequence (O_n) as defined in 192.3.4.3, which is passed to the PMA via the PMA_UNITDATA.request primitive. These symbols are used for training mode and only transmit the values $\{-1, +1\}$.

During training mode, an Infocfield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and requests the remote transmitter settings (see 192.4.2.4).

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation and the PCS Transmit function shall use a 65B coding technique to generate code-groups that represent data or control. For LS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 17-bit OAM field to form the RS-FEC input frame. During data encoding, LS_TX PCS Transmit utilizes Reed-Solomon encoders to generate and append 48 parity check bits to form 1040-bit RS-FEC(130,124) frames, which become the burst payload for one TDD cycle. For HS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 1-bit OAM field to form the RS-FEC input frame. During data encoding, HS_TX PCS Transmit utilizes L-interleaved ($L = 1$ for 2.5 Gb/s, $L = 2$ for 5 Gb/s, $L = 3$ for 7.5 Gb/s, or $L = 4$ for 10 Gb/s) Reed-Solomon encoders to generate and append 48 parity check bits to form 1024-bit RS-FEC(128,122) frames that are interleaved into an L-interleaved RS-FEC superframe that is $L \times 1024$ bits long. 25 consecutive RS-FEC superframes are concatenated to form the burst payload for one TDD cycle.

In all PCS bursts, a scrambled refresh header bit sequence is concatenated with the scrambled burst payload bit sequence and the bit sequences are mapped to PAM symbols appropriate to the transmit rate. These PAM symbols are then concatenated with the required number of Z symbols to complete a full TDD cycle of symbols. The process is repeated for each TDD cycle.

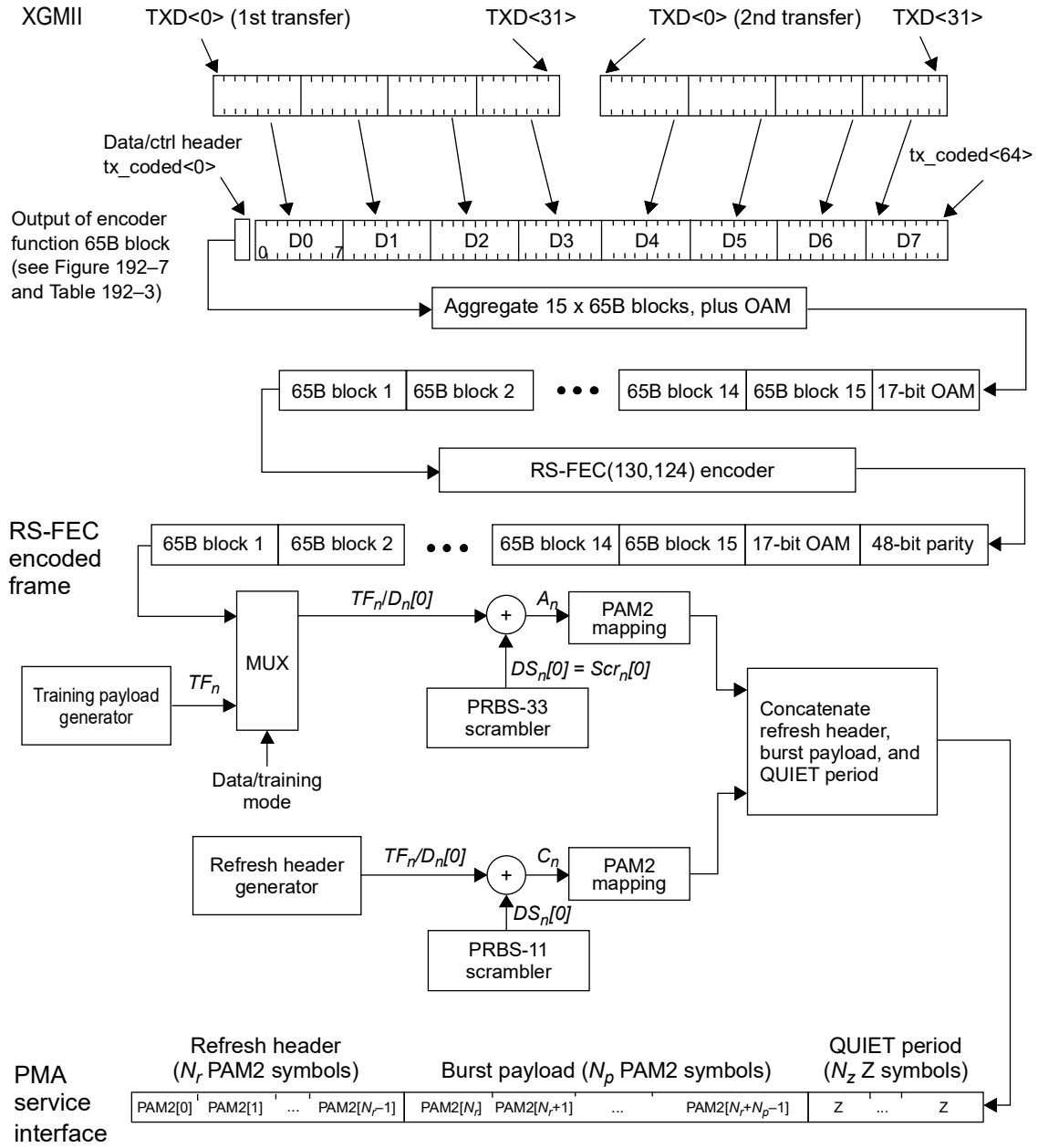
192.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 192.3.2.2.4.

192.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is shown in Figure 192–5 for LS_TX, Figure 192–6 for HS_TX, Figure 192–12 for LS_RX, and Figure 192–13 and Figure 192–14 for HS_RX. These figures show the processing of a multiplicity of blocks containing 8 data octets. See 192.3.2.2.4 for information on how blocks containing control characters are mapped.



NOTE—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

Figure 192-5—LS_TX PCS Transmit bit ordering

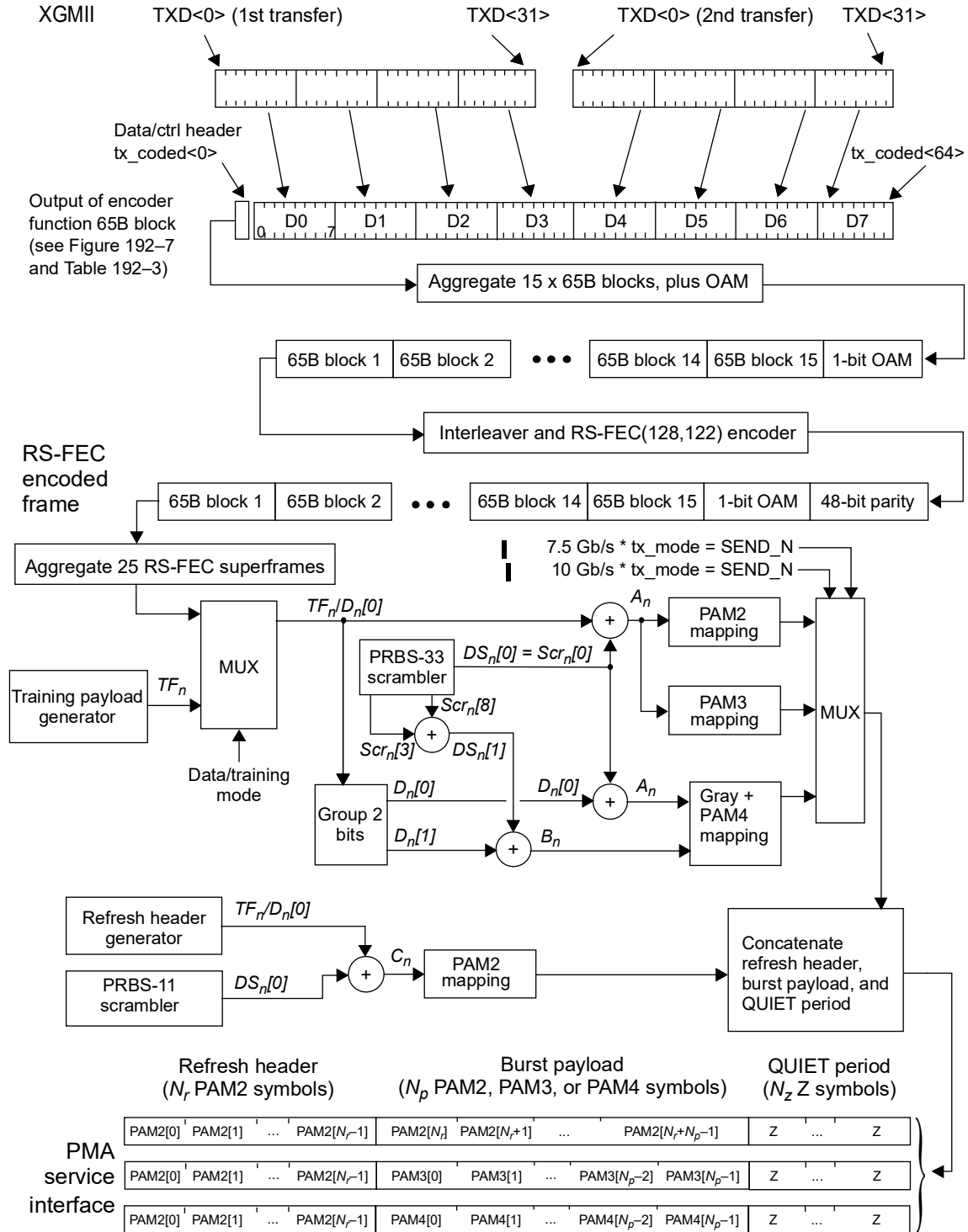


Figure 192-6—HS_TX PCS Transmit bit ordering

192.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D0 to D7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O0 or O4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S0 or S4 for the same reason. The control character for terminate is labeled as T0 to T7.

The two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

192.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block.

64B/65B block formats are shown in shown in Figure 192–7. The column labeled Input data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, D₀ through D₇ are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one.

Each control block contains eight characters. For control blocks containing a start (/S/) or terminate (/T/) character, as indicated by an S or T octet in the Figure 192–7 Input data field, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O code. The single bit fields, represented by unlabeled narrow rectangles in Figure 192–7, are sent with the value zero and ignored upon receipt.

NOTE—The block structure specified in this subclause is identical to that used in 149.3.2.2.4.

Input data	data ctrl header	Block payload									
Bit position:	0	1									
Data block format:											64
D ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ D ₆ D ₇	0	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇		
Control Block Formats:		Block									
C ₀ C ₁ C ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0x1E	C ₀	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	
C ₀ C ₁ C ₂ C ₃ /O ₄ D ₅ D ₆ D ₇	1	0x2D	C ₀	C ₁	C ₂	C ₃	O ₄	D ₅	D ₆	D ₇	
C ₀ C ₁ C ₂ C ₃ /S ₄ D ₅ D ₆ D ₇	1	0x33	C ₀	C ₁	C ₂	C ₃			D ₅	D ₆	D ₇
O ₀ D ₁ D ₂ D ₃ /S ₄ D ₅ D ₆ D ₇	1	0x66	D ₁	D ₂	D ₃	O ₀			D ₅	D ₆	D ₇
O ₀ D ₁ D ₂ D ₃ /O ₄ D ₅ D ₆ D ₇	1	0x55	D ₁	D ₂	D ₃	O ₀	O ₄	D ₅	D ₆	D ₇	
S ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ D ₆ D ₇	1	0x78	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇		
O ₀ D ₁ D ₂ D ₃ /C ₄ C ₅ C ₆ C ₇	1	0x4B	D ₁	D ₂	D ₃	O ₀	C ₄	C ₅	C ₆	C ₇	
T ₀ C ₁ C ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0x87				C ₁	C ₂	C ₃	C ₄	C ₅	C ₆
D ₀ T ₁ C ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0x99	D ₀			C ₂	C ₃	C ₄	C ₅	C ₆	C ₇
D ₀ D ₁ T ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0xAA	D ₀	D ₁			C ₃	C ₄	C ₅	C ₆	C ₇
D ₀ D ₁ D ₂ T ₃ /C ₄ C ₅ C ₆ C ₇	1	0xB4	D ₀	D ₁	D ₂			C ₄	C ₅	C ₆	C ₇
D ₀ D ₁ D ₂ D ₃ /T ₄ C ₅ C ₆ C ₇	1	0xCC	D ₀	D ₁	D ₂	D ₃			C ₅	C ₆	C ₇
D ₀ D ₁ D ₂ D ₃ /D ₄ T ₅ C ₆ C ₇	1	0xD2	D ₀	D ₁	D ₂	D ₃	D ₄			C ₆	C ₇
D ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ T ₆ C ₇	1	0xE1	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅			C ₇
D ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ D ₆ T ₇	1	0xFF	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆		

Figure 192–7—64B/65B block formats for MultiGBASE-A

192.3.2.2.5 Control codes

All control characters are supported by both the XGMII and the PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The PCS encodes the start and terminate control characters implicitly by the block type field. The PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to MultiGBASE-A control codes and XGMII control codes are specified in Table 192–3.

Table 192–3—MultiGBASE-A control codes

Control character	Notation	XGMII control code	Control code	O code
idle	/I/	0x07	0x00	—
start	/S/	0xFB	Encoded by block type field	—
terminate	/T/	0xFD	Encoded by block type field	—
error	/E/	0xFE	0x1E	—
sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0	—	0x1C	0x2D	—
reserved1	—	0x3C	0x33	—
reserved2	—	0x7C	0x4B	—
reserved3	—	0xBC	0x55	—
reserved4	—	0xDC	0x66	—
reserved5	—	0xF7	0x78	—
reserved6	—	0x5C	Encoded by block type field plus O code	0xF

192.3.2.2.6 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as Remote Fault and Local Fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 192–3 for the mappings.

NOTE—The format of the ordered sets specified in this subclause are identical to those used in 149.3.2.2.6.

192.3.2.2.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of four. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

NOTE—The idle control characters (/I/) specified in this subclause are identical to those used in 149.3.2.2.7.

192.3.2.2.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

NOTE—The start control character (/S/) specified in this subclause is identical to that used in 149.3.2.2.9.

192.3.2.2.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

NOTE—The terminate control character (/T/) specified in this subclause is identical to that used in 149.3.2.2.10.

192.3.2.2.10 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

NOTE—The ordered set control characters (/O/) specified in this subclause are identical to those used in 149.3.2.2.11.

192.3.2.2.11 Error (/E/)

The error control character /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 192.3.5.1.3 for further information.

NOTE—The error control character (/E/) specified in this subclause is identical to that used in 149.3.2.2.12.

192.3.2.2.12 Transmit process

The LS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. 30 XGMII data transfers are encoded into an RS-FEC frame. It takes 1040 PMA_UNITDATA transfers to send an RS-FEC frame of data.

The HS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. $L \times 30$ XGMII data transfers are encoded into an RS-FEC superframe. For 2.5 Gb/s and 5 Gb/s

mode, it takes $L \times 1024$ PMA_UNITDATA PAM2 transfers to send an RS-FEC superframe of data. For 7.5 Gb/s mode, it takes $L \times 2/3 \times 1024$ PMA_UNITDATA PAM3 transfers to send an RS-FEC superframe of data. For 10 Gb/s mode, it takes $L \times 512$ PMA_UNITDATA PAM4 transfers to send an RS-FEC superframe of data. Where the XGMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 192–22). The contents of each block are contained in a vector $tx\_coded<64:0>$, which is passed to the RS-FEC encoder and scrambler. The bit $tx\_coded<0>$ contains the data/ctrl header and the remainder of bits contain the block payload.

192.3.2.2.13 RS-FEC framing and RS-FEC encoder

15 65B blocks (tx_coded) are grouped together to form $tx\_group15x65B$ as described in 192.1.3.1. For LS_TX transmission, $tx\_group15x65B$, followed by the 17-bit OAM/Reserved field and 48 parity bits, forms an RS-FEC frame of 1040 bits. See Figure 192–5 and 192.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of $tx\_group15x65B$, and the 17-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

For HS_TX transmission, $tx\_group15x65B$, followed by the 1-bit OAM/Reserved field and 48 parity bits, forms an RS-FEC frame of 1024 bits. See Figure 192–6 and 192.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of $tx\_group15x65B$, and the 1-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

192.3.2.2.14 RS-FEC superframe and round-robin interleaving

The interleaving depth, L , of the transmitter shall be predefined for each data rate and comply with Table 192–4. When $L = 1$, there is no interleaving and the RS-FEC superframe is the same as the RS-FEC frame. When $L > 1$, the round-robin interleaving scheme shown in Figure 192–8 shall be applied.

Table 192–4—Interleaving depth

Transmit MAC data rate	Interleaving depth, L
100 Mb/s	1
2.5 Gb/s	1
5 Gb/s	2
7.5 Gb/s	3
10 Gb/s	4

The HS_TX PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are $976 \times L$ bits, or $122 \times L$ Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are as follows:

$$m_{122 \times L - 1}, m_{122 \times L - 2}, \dots, m_1, m_0$$

These message symbols are distributed to L RS-FEC encoders. When $L > 1$, each RS-FEC encoder receives one out of every L message symbols from the superframe. Otherwise, the RS-FEC encoder operates exactly the same as specified in 192.3.2.2.16.

192.3.2.2.15 RS-FEC recombine

The L encoded RS-FEC frames are combined into an interleaved RS-FEC superframe. The output symbols are as follows:

$$m_{122 \times L-1}, m_{122 \times L-2}, \dots, m_1, m_0, p_{1,5}, \dots, p_{L,5}, \dots, p_{1,0}, \dots, p_{L,0}$$

where $p_{i,r}$ is the r^{th} parity symbol of the i^{th} encoder.

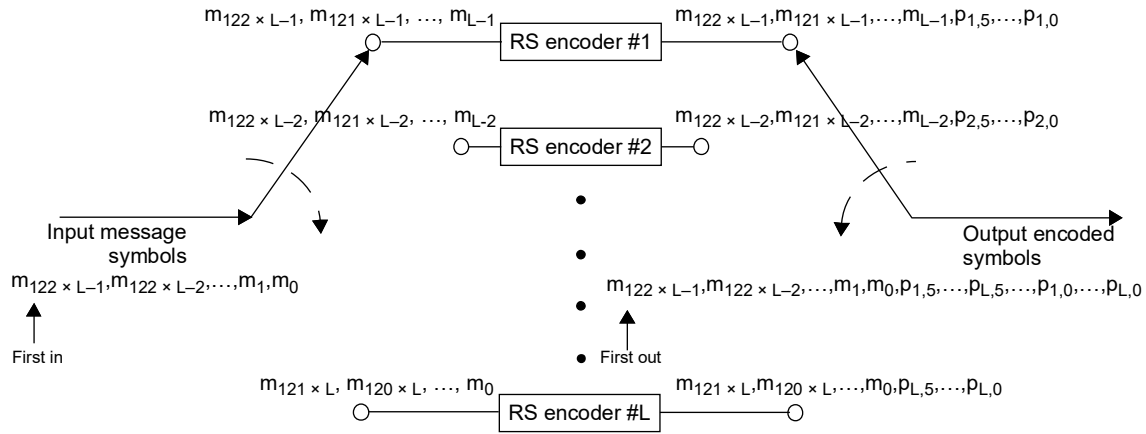


Figure 192-8—Interleaving block diagram with interleaving depth L

192.3.2.2.16 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field $GF(2^8)$ where the symbol size is 8 bits. For the LS_PATH, the encoder processes 124 8-bit RS-FEC message symbols to generate six 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. For the HS_PATH, the encoder processes 122 8-bit RS-FEC message symbols to generate six 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 128 8-bit RS-FEC symbols. For the purposes of this clause, the Reed-Solomon code, $RS-FEC(n,k)$, is denoted as $RS-FEC(130,124)$ for the LS_PATH and $RS-FEC(128,122)$ for the HS_PATH.

The code is based on the generating polynomial shown in Equation (192-1).

$$g(x) = \prod_{j=0}^{n-k-1} (x - \alpha^j) = g_{n-k}x^{n-k} + g_{n-1-k}x^{n-1-k} + \dots + g_3x^3 + g_2x^2 + g_1x + g_0 \quad (192-1)$$

In Equation (192-1), α is a primitive element of the finite field defined by the primitive polynomial $0x11D = x^8 + x^4 + x^3 + x^2 + 1$.

Equation (192–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0 .

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \dots + m_1x^{n-k+1} + m_0x^{n-k} \quad (192-2)$$

Each message symbol m_i is the bit vector $(m_{i,7}, m_{i,6}, \dots, m_{i,1}, m_{i,0})$, which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in $\text{tx\_RSMesssage}\langle(8 \times k - 1):0\rangle$.

For LS_TX, $m_{i,j} = \text{tx\_RSMesssage}\langle(123 - i) \times 8 + j\rangle$, for $i = 0$ to 123, and $j = 0$ to 7.

$\text{tx\_RSMesssage}\langle 991:0\rangle$ prior to RS-FEC(130,124) encoder is formed as follows:

$$\begin{aligned} \text{tx\_RSMesssage}\langle 974:0\rangle &= \text{tx\_group15x65B}\langle 974:0\rangle. \\ \text{tx\_RSMesssage}\langle 991:975\rangle &= \text{OAM\_field}\langle 16:0\rangle. \end{aligned}$$

For HS_TX, $m_{i,j} = \text{tx\_RSMesssage}\langle(121 - i) \times 8 + j\rangle$, for $i = 0$ to 121, and $j = 0$ to 7.

$\text{tx\_RSMesssage}\langle 975:0\rangle$ prior to RS-FEC(128,122) encoder is formed as follows for $L = 1$ (see 192.3.2.2.14):

$$\begin{aligned} \text{tx\_RSMesssage}\langle 974:0\rangle &= \text{tx\_group15x65B}\langle 974:0\rangle. \\ \text{tx\_RSMesssage}\langle 975\rangle &= \text{OAM\_field}\langle 0\rangle. \end{aligned}$$

For $L > 1$, see 192.3.2.2.14 and 192.3.2.2.15.

The first symbol input to the encoder is m_{k-1} .

Equation (192–3) defines the parity polynomial $p(x)$ whose coefficients are the message symbols p_{n-k-1} to p_0 .

$$p(x) = p_{n-k-1}x^{n-k-1} + p_{n-k-2}x^{n-k-2} + \dots + p_2x^2 + p_1x + p_0 \quad (192-3)$$

Each parity symbol p_i is the bit vector $(p_{i,7}, p_{i,6}, \dots, p_{i,1}, p_{i,0})$, which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation shown in Figure 192–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0 , is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x (e.g., $c_{n-1} = m_{k-1}$) is transmitted first and the coefficient of the lowest power of x (e.g., $c_0 = p_0$) is transmitted last. The first bit transmitted from each symbol is bit 0.

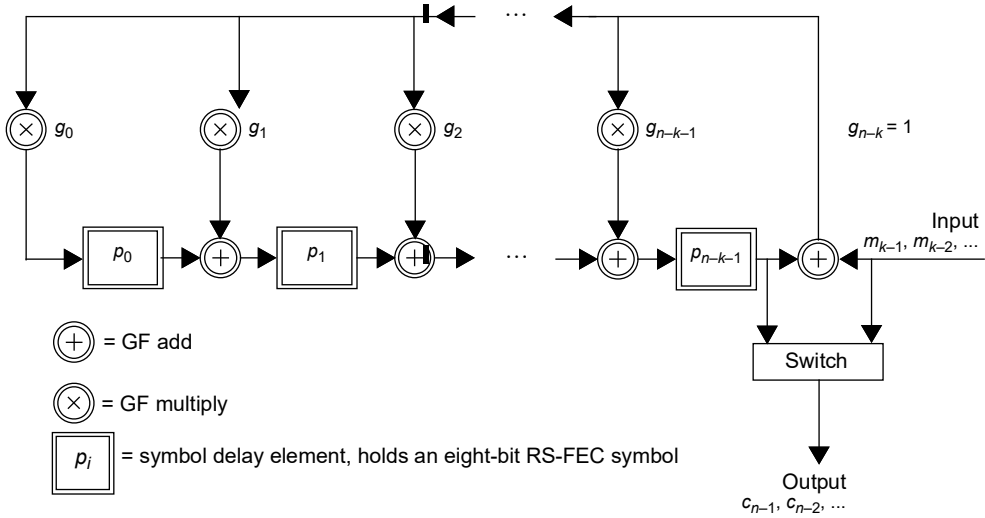


Figure 192-9—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 192-5.

Table 192-5—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(130,124)	RS-FEC(128,122)
0	38	38
1	227	227
2	32	32
3	218	218
4	1	1
5	63	63
6	1	1

192.3.2.2.17 PCS scrambler

Different scramblers are used for the refresh header and for the burst payload (see 192.3.4). The scrambled refresh header data bit, C_n , shall be as in Equation (192-4). Refresh header data bits are mapped to PAM2 symbols for all data rates.

$$C_n = \begin{cases} DS_n[0] \oplus TF_n & \text{tx\_mode} \neq \text{SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode} = \text{SEND\_N} \end{cases} \quad 0 \leq n \leq N_r - 1 \quad (192-4)$$

where

$DS_n[0]$ is produced using the scrambler defined in 192.3.2.2.18

PAM2 or PAM3 symbols are used for rates less than 10 Gb/s. The scrambled payload bits, A_n , for PAM2 and PAM3 are shown in Equation (192-5). Bit $DS_n[0]$ is produced using the scrambler defined in 192.3.2.2.19. It is applied as an additive scrambler sequence to incoming data bit $D_n[0]$ (LSB) to generate the scrambled data bit, A_n .

$$A_n = \begin{cases} DS_n[0] \oplus TF_n & \text{tx\_mode} \neq \text{SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode} = \text{SEND\_N} \end{cases} \quad N_r \leq n \leq N_r + N_p - 1 \quad (192-5)$$

For 10 Gb/s interfaces using PAM4 coding, the burst data bits of the interleaved RS-FEC superframe are grouped into pairs. Each pair of bits, $D_n[0]$ and $D_n[1]$, where n is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the PCS scrambler. The first bit, which is the least significant bit (LSB), is $DS_n[0]$ equal to $Scr_n[0]$. The second bit, which is the most significant bit (MSB), is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$. Bits $DS_n[0]$ and $DS_n[1]$ in Equation (192-6) and Equation (192-7) are produced using the scrambler defined in 192.3.2.2.19. They are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$. PAM4 is only used when the tx_mode value is SEND_N.

$$A_n = \begin{cases} DS_n[0] \oplus D_n[0] & \text{tx\_mode} = \text{SEND\_N} \end{cases} \quad N_r \leq n \leq N_r + N_p - 1 \quad (192-6)$$

$$B_n = \begin{cases} DS_n[1] \oplus D_n[1] & \text{tx\_mode} = \text{SEND\_N} \end{cases} \quad N_r \leq n \leq N_r + N_p - 1 \quad (192-7)$$

192.3.2.2.18 PRBS11 scrambler polynomial

The refresh header specified in 192.3.4 is scrambled from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 192–10. The pattern generator is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 11-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. The scrambler state shall not be initialized to all zeros. This scrambler, once started during PMA training, shall continue to run uninterrupted during the refresh headers of each frame and shall stop during the burst payload field and QUIET. This implements the generator polynomial shown in Equation (192–8), which is the same as Equation (72–1).

$$G(x) = 1 + x^9 + x^{11} \quad (192-8)$$

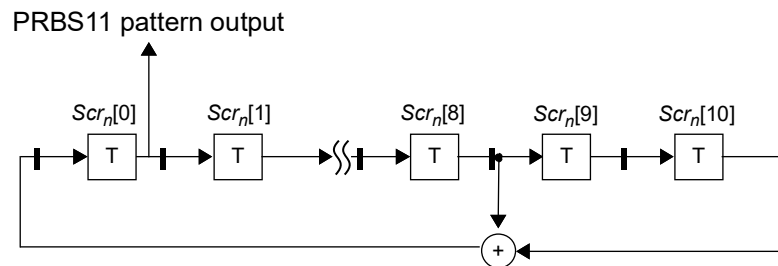


Figure 192–10—PRBS11 pattern generator

192.3.2.2.19 PRBS33 scrambler polynomials

The PCS Transmit function employs additive scrambling. If the management parameter config provided to the PCS assumes the value LEADER, PCS Transmit shall employ Equation (192–9) as the transmitter scrambler generator polynomial.

$$g_L(x) = 1 + x^{13} + x^{33} \quad (192-9)$$

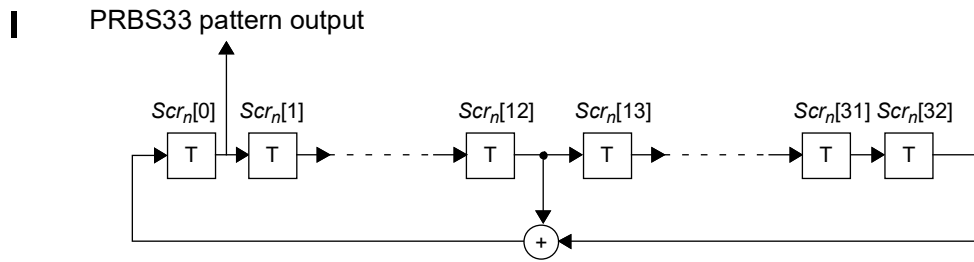
If management parameter config assumes the value FOLLOWER, PCS Transmit shall employ Equation (192–10) as the transmitter scrambler generator polynomial.

$$g_F(x) = 1 + x^{20} + x^{33} \quad (192-10)$$

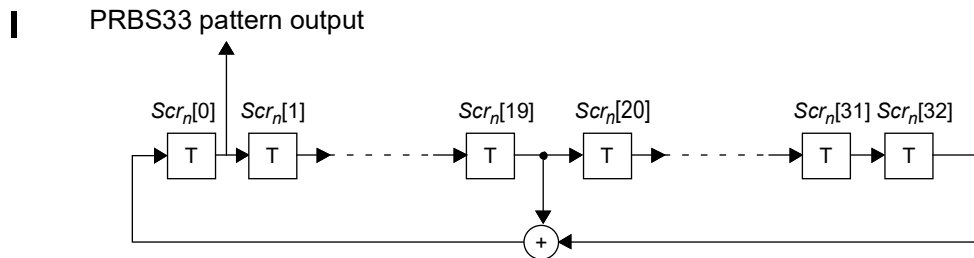
An implementation of the Leader PCS and Follower PCS transmitter scramblers by linear-feedback shift registers is shown in Figure 192–11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. The scrambler state shall not be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the payload of PMA training frames and data mode frames and shall stop during QUIET and refresh headers.

PCS scrambler employed by the Leader transmitter



PCS scrambler employed by the Follower transmitter



NOTE —The output shown corresponds to $Scr_n[0]$. The outputs corresponding to $Scr_n[3]$ and $Scr_n[8]$ are not shown.

Figure 192–11—Realization of PCS scramblers by linear feedback shift registers

192.3.2.2.20 Gray mapping for PAM4 encoding

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where A_n is the bit arriving first, and n is an index indicating the symbol number, to Gray-coded symbols, $G(n)$, with one of four levels as follows:

- $\{0, 0\}$ maps to 0,
- $\{0, 1\}$ maps to 1,
- $\{1, 1\}$ maps to 2, and
- $\{1, 0\}$ maps to 3.

When receiving at 10 Gb/s in the PAM4 transmission period, the PCS Receive process shall map Gray-coded symbols, $G(n)$, with one of four levels, to pairs of bits, $\{A_n, B_n\}$, where A_n is considered to be the first bit as follows:

- 0 maps to $\{0, 0\}$,
- 1 maps to $\{0, 1\}$,
- 2 maps to $\{1, 1\}$, and
- 3 maps to $\{1, 0\}$.

192.3.2.2.21 PAM4 encoding

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall encode each Gray-coded symbol, $G(n)$, to one of four PAM4 levels as specified in this clause.

The PAM4 encoded symbols are denoted $M(n)$, where n is an index indicating the symbol number.

Each consecutive Gray-coded symbol, $G(n)$, is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output, $M(n)$.

Mapping from the Gray-coded symbol, $G(n)$, to a PAM4 encoded symbol, $M(n)$, is as follows:

- 0 maps to -1 ,
- 1 maps to $-1/3$,
- 2 maps to $+1/3$, and
- 3 maps to $+1$.

192.3.2.2.22 PAM3 encoding

3B2T encoding is used to map a group of three consecutive bits into a consecutive pair of three-level (ternary) PAM3 symbols as specified in this clause. When transmitting at 7.5 Gb/s in the PAM3 transmission period, the PCS Transmit process shall encode each of the two PAM3 symbols in the ternary pair $T[1]$, $T[0]$ into the appropriate PAM3 level.

The 3B2T mapping into PAM3 symbols is shown in Table 192–6. $B[0]$ is the first of the three bits received by the mapper (i.e., the LSB of the trio) and $T[0]$ is the first PAM3 ternary symbol of the pair to be transmitted.

Table 192–6—3B2T mapping

Three-bit groups $B[2], B[1], B[0]$	PAM3 ternary symbol pairs $T[1], T[0]$
000	$-1, -1$
001	$0, -1$
010	$-1, 0$
011	$-1, +1$
100	$+1, 0$
101	$+1, -1$
110	$+1, +1$
111	$0, +1$

192.3.2.2.23 PAM2 mapping

During the PAM2 transmission period, the PCS Transmit process sends out PAM2 symbols according to the following mapping:

Input bit S_n is mapped to the transmit symbol T_n as follows:

- if $S_n = 0$, then $T_n = -1$, and
- if $S_n = 1$, then $T_n = +1$.

192.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 192–23 and the PCS Receive bit ordering in Figure 192–12 for the LS_RX and Figure 192–13 and Figure 192–14 for the HS_RX, including compliance with the associated state variable as specified in 192.3.5.1.2.

The PCS Receive function accepts received symbols provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM2, PAM3, or PAM4 symbols are demapped and descrambling is performed.

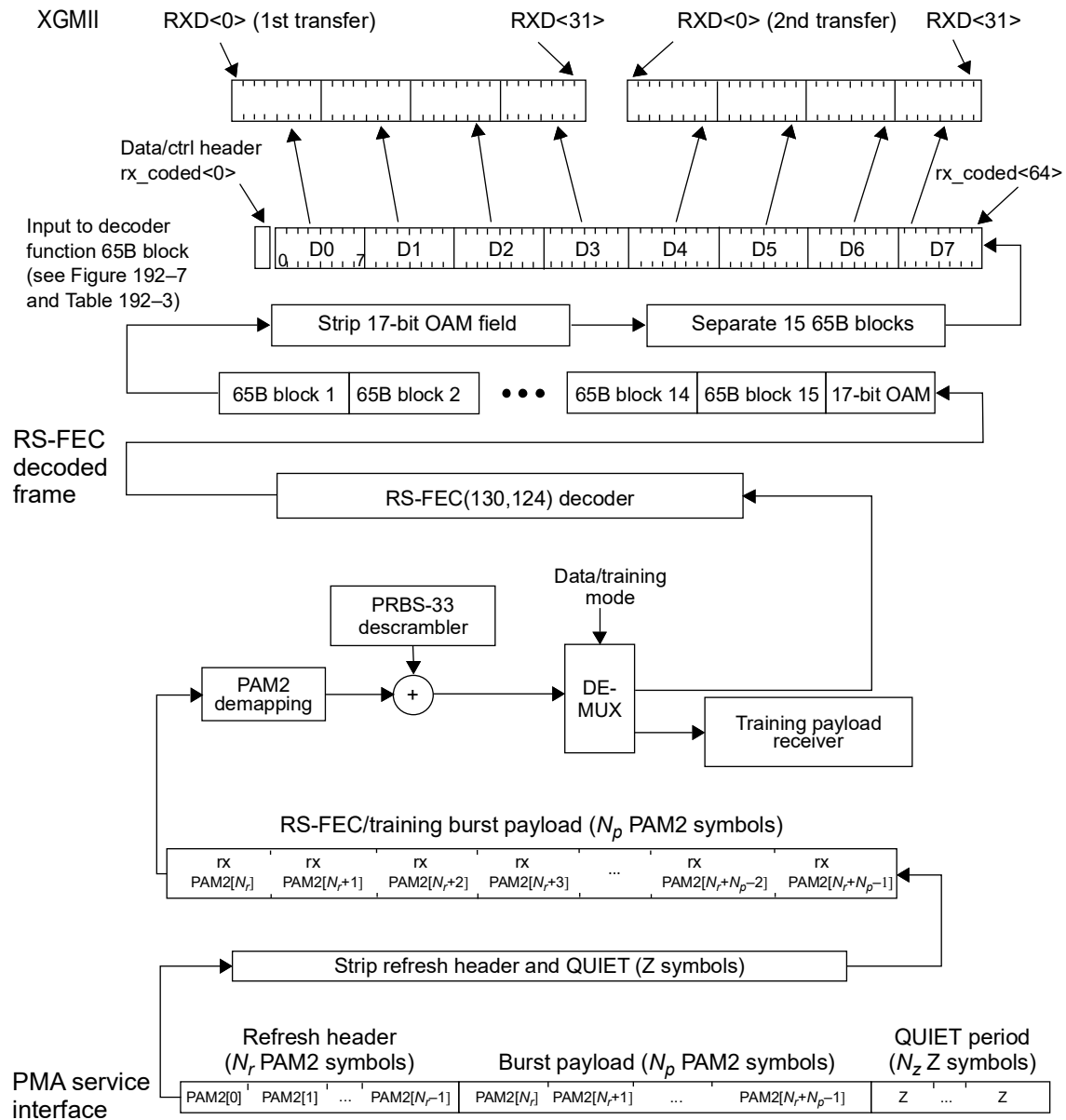
Following descrambling, the L -interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For LS_RX, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks. For HS_RX, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each data payload, the 25 superframes can form a 25-bit OAM field for 2.5 Gb/s mode, a 50-bit OAM field for 5 Gb/s mode, a 75-bit OAM field for 7.5 Gb/s mode, and a 100-bit OAM field for 10 Gb/s mode.

Groups of 15 64B/65B blocks are then separated into individual 64B/65B blocks. The PCS Receive function generates the 64B/65B block vector rx_coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 192–23). Two XGMII data transfers are decoded from each block. Because the received data stream is divided into TDD bursts with silence interspersed, the PCS receive function recombines separated bursts before passing to the XGMII. When the XGMII and PMA sublayer data rates are not frequency synchronized, the PCS receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and indicates that the PCS descrambler state has been acquired by setting the scr_status parameter PMA_SCRSTATUS.request primitive to OK. Descrambler acquisition is a prerequisite to RS-FEC block lock and should be robust to bit errors without RS-FEC.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock is de-asserted. The block_lock is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi_rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receiver is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process when PHY Control is in PCS_TEST or PCS_DATA state. The PCS Synchronization process sets the block_lock to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header (see 192.3.4). It also includes training payload which has an Infofield, inserted in the N_{inf}^{th} bit of the training payload (see 192.3.4.3). When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.



NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

Figure 192-12—LS_RX PCS Receive bit ordering

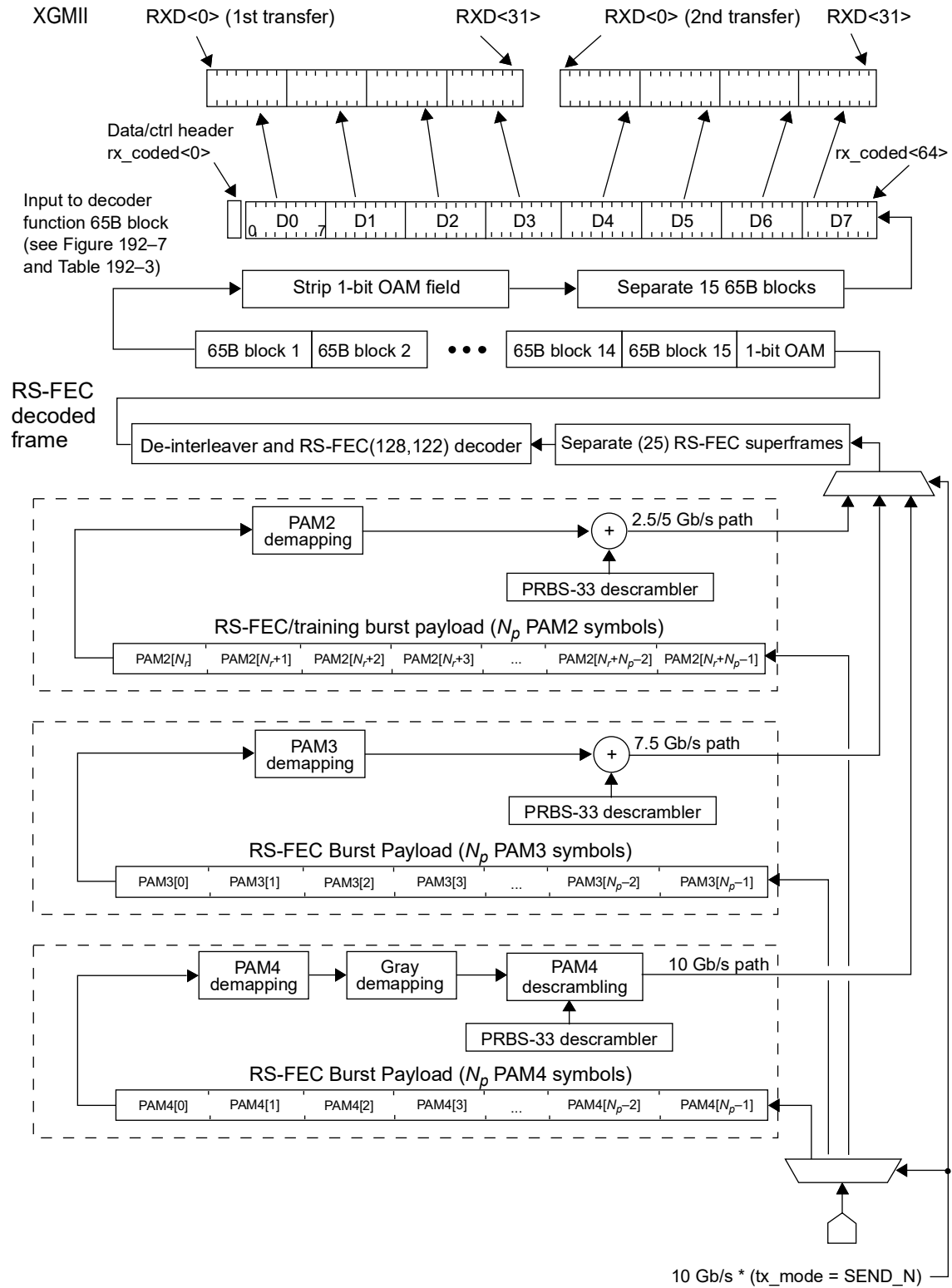
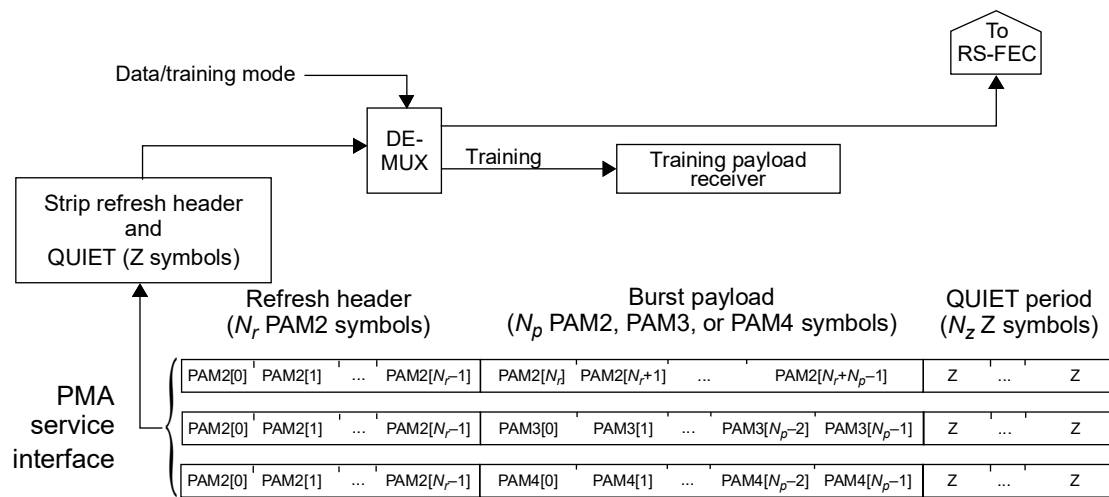


Figure 192-13—HS_RX PCS Receive bit ordering, part a



NOTE 1—Figure 192-13 and Figure 192-14 show the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

NOTE 2—Figure 192-13 and Figure 192-14 shown for L = 1.

NOTE 3—Either the PAM2, PAM3, or PAM4 path and TDD frame at the PMA service interface is used. PAM3 path (and the middle TDD frame shown) is chosen if the bit rate is 7.5 Gb/s and tx_mode = SEND_N. PAM4 path (and the lowest TDD frame shown) is chosen if the bit rate is 10 Gb/s and tx_mode = SEND_N.

Figure 192-14—HS_RX PCS Receive bit ordering, part b

192.3.2.3.1 Frame and block synchronization

When operating in 100 Mb/s, 2.5 Gb/s, or 5 Gb/s data mode, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from PAM2[N_r] to PAM2[N_r + N_p - 1] (see Figure 192-12 for LS_RX or Figure 192-13 and Figure 192-14 for HS_RX). When operating in 7.5 Gb/s data mode, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from PAM3[0] to PAM3[N_p - 1] (see Figure 192-12 for LS_RX or Figure 192-13 for HS_RX). When operating in 10 Gb/s data mode, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from PAM4[0] to PAM4[N_p - 1] (see Figure 192-13 and Figure 192-14).

The receiving PCS obtains block_lock to the PHY frames during training using synchronization sequence and Infocfield provided in the training frames.

192.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For descrambling, the Leader PHY shall employ the receiver descrambler generator polynomial per Equation (192-10) and the Follower PHY shall employ the receiver descrambler generator polynomial per Equation (192-9).

192.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

- a) The block type field contains a reserved value.
- b) Any control character contains a value not in Table 192–3.
- c) Any O code contains a value not in Table 192–3.
- d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 192.3.2.2.13. If the check fails, the RS-FEC frame is invalid. The R_BLOCK_TYPE of an invalid block is set to E.

192.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, channel, and remote receiver.

When the transmit PCS is operating in test-pattern mode, the input to the RS-FEC encoder (see Figure 192–5 or Figure 192–6) is set to zero and the initial condition of the PCS scrambler set to any non-zero value. This has the same effect as setting the input to the PCS scrambler to zero.

When the receiver PCS is operating in test-pattern mode, the received information is processed as shown in Figure 192–12 or Figure 192–13 and Figure 192–14. In the absence of errors in PMA Receive, the descrambler output should be zeros. The output of the RS-FEC decoder should also be zeros, and may correct errors in the descrambler output. Any nonzero values at the output of the RS-FEC decoder are due to uncorrectable RS-FEC frames. This mode is further described as test mode 7 in 192.5.1.

192.3.4 PCS TDD signaling

The PCS generates symbols to be transmitted by the PMA in the form of TDD bursts. TDD burst structure depends on the value of tx_mode and the data rate of transmission. Each TDD burst is comprised of a refresh header and payload followed by a QUIET period. During startup, the PCS transmits TDD bursts in two different formats for the tx_mode values SEND_TS and SEND_TA, before finally switching to SEND_N. SEND_TS uses a symmetric frame format and shall transmit at 3 GBd. PHY data rate and direction may be negotiated during the SEND_TS phase. SEND_TA and SEND_N use an asymmetric frame format, and transmit at either 3 GBd or 6 GBd depending on the selected transmitter rate. QUIET periods (i.e., when the PCS inserts Z symbols) are introduced between TDD bursts. The duration of each QUIET period depends on the state of tx_mode.

The refresh header is a sequence of PAM2 symbols with length of N_r symbols. The refresh header bits are all zeros except for the final 64 bits (see 192.3.4.2).

An 11-bit scrambler (see 192.3.2.2.18) is used to scramble the refresh header. This scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

The burst payload is a sequence of symbols with length of N_p symbols.

The training payload data sequence bits are all zeros, with the exception of a 96-bit Infocfield started at the N_{inf}^{th} symbol of the training payload (see Figure 192–15). The Infocfield is used to exchange messages between link partners during startup. The training data sequence, TF_n , is defined in Equation (192–11). Training payloads are sent when tx_mode is SEND_TS or SEND_TA.

The data mode burst payload consists of RS-FEC superframes that are sent when tx_mode is SEND_N.

The 33-bit scrambler (see 192.3.2.2.19) is used to scramble the payload. Once started at the beginning of the training payload of the first training burst, this scrambler shall continue to run uninterrupted for each symbol during all subsequent payloads and shall maintain its last state during the QUIET period and refresh headers.

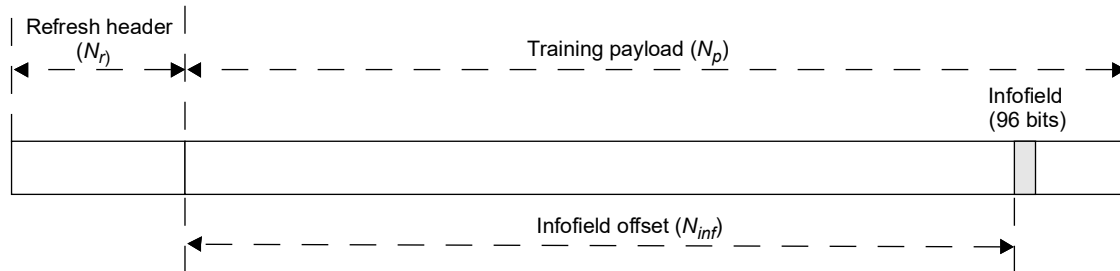
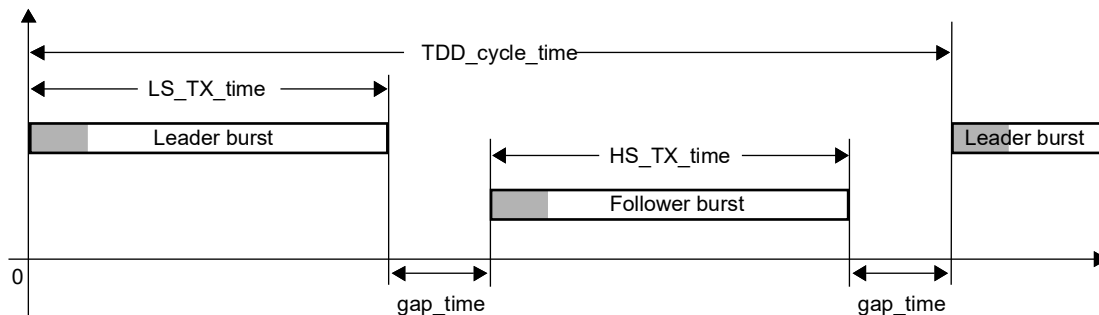


Figure 192-15—PMA Training frame

The timing diagram in Figure 192-16 shows the TDD cycle signaling and TDD frame structures assuming the LS_TX is configured as the Leader and the HS_TX is configured as the Follower. Table 192-7 specifies the LS_TX and HS_TX transmit times in each TDD cycle.



NOTE 1—TDD_cycle_time is the nominal 9.6μs TDD cycle time.

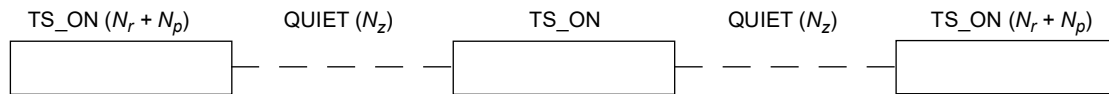
NOTE 2—gap_time is the time between the start of QUIET at one MDI output and end of QUIET at the other MDI output. gap_time is a result of the alignment of the two ends, so is not specified.

Figure 192-16—Leader/Follower TDD cycle illustration

Table 192-7—TDD cycle timing

tx_mode	LS_TX_time (ns)	HS_TX_time (ns)	Totalgap_time per cycle (ns)	TDD cycle time (ns)
SEND_TS	4480	4480	640	9600
SEND_TA	554.67	8693.33	352	
SEND_N				

The symmetric training burst timing and structure are shown in Figure 192–17. TS_ON indicates a symmetric training burst and QUIET (N_z) indicates the QUIET period between bursts when Z symbols are transmitted by the PHY



NOTE—The parameters for SEND_TS are used for N_r , N_p , and N_z (see Table 192–9, Table 192–10, and Table 192–11).

Figure 192–17—Symmetric training timing and frame structure

Figure 192–18 shows the LS_TX timing and frame structure for both the data mode and the asymmetric training modes. TA_ON indicates an asymmetric training burst and QUIET (N_z) indicates the QUIET period between bursts when Z symbols are transmitted by the PHY. The refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 192.3.4. Note that FEC is not used with the training payload.

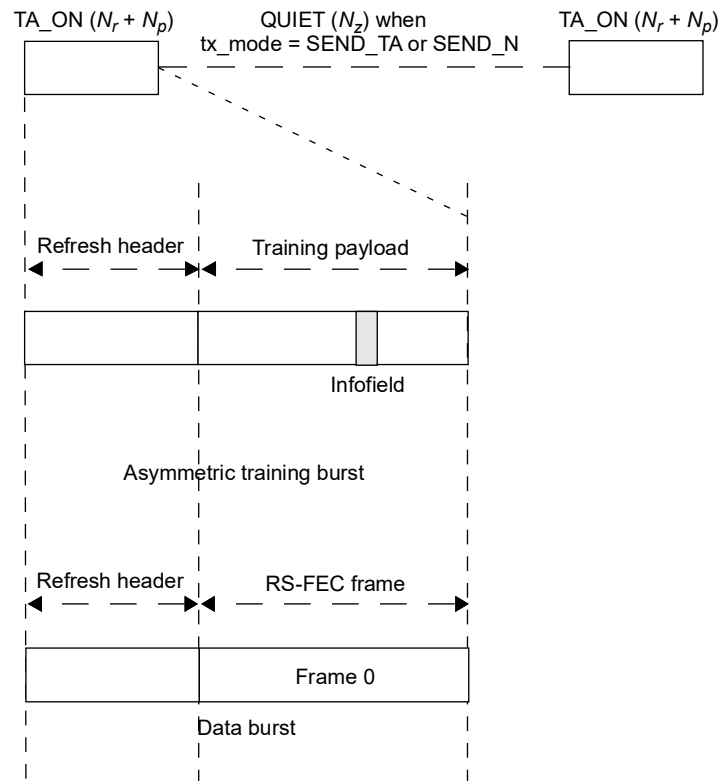


Figure 192–18—Asymmetric training/Data Mode timing and frame structure—LS_TX

Figure 192–19 shows the HS_TX timing and frame structure for both the data mode and the asymmetric training modes. As with the LS_TX direction, the refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 192.3.4 and FEC is not used with the training payload.

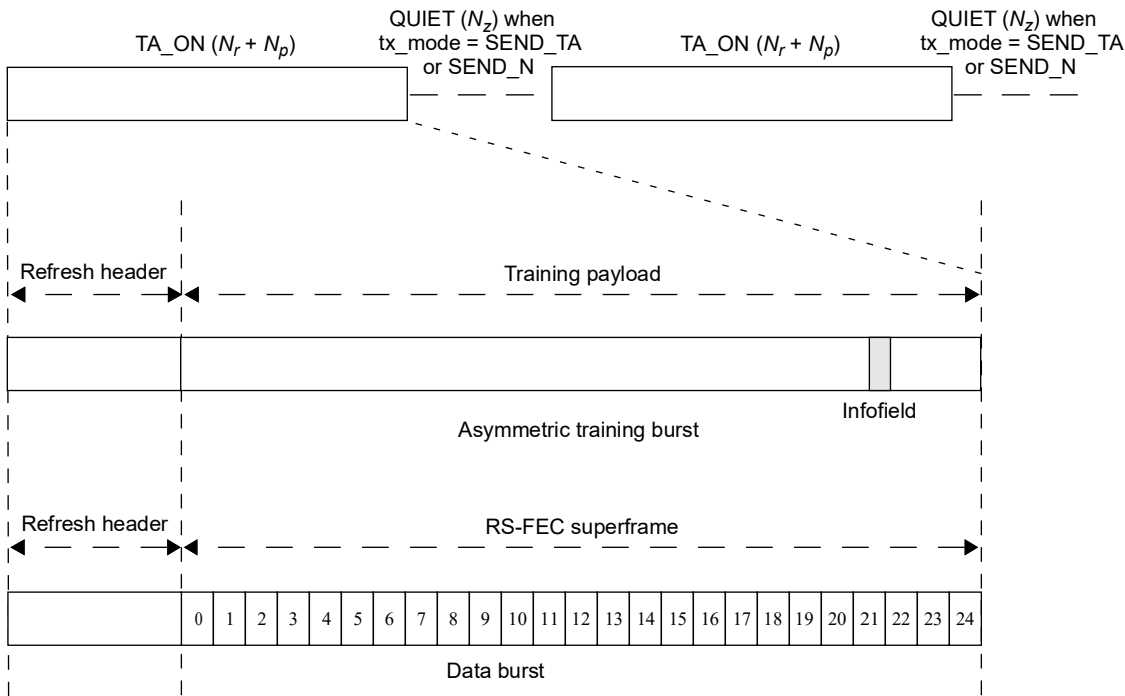


Figure 192–19—Asymmetric training/Data Mode timing and frame structure—HS_TX

The burst payload structures are illustrated in Figure 192–20. Data burst payload information is summarized in Table 192–8.

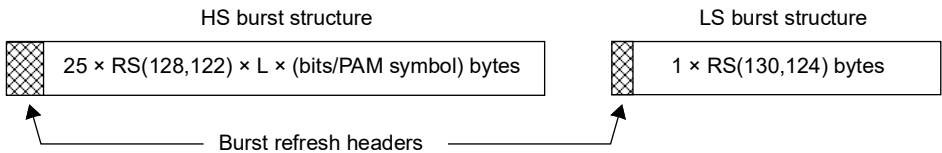


Figure 192–20—Illustration of the data burst payload structure

Table 192–8—Data burst payload summary information

HS burst payload					LS burst payload				
Burst payload rate (Gb/s)	Baud (GBd)	PAM levels	L (Inter-leave depth)	Number of burst payload symbols	Burst payload rate (Mb/s)	Baud (GBd)	PAM levels	L (Inter-leave depth)	Number of burst payload symbols
2.5	3	2	1	25 600	100	3	2	1	1040
5	6	2	2	51 200					
7.5		3	3						
10		4	4						

192.3.4.1 Refresh header, payload, and QUIET period length

The lengths for refresh header (N_r) and payload (N_p) are described in Table 192–9, Table 192–10, and Table 192–11. The length of the QUIET period (N_z) in Table 192–9, Table 192–10, and Table 192–11 is the number of Z symbols sent to complete the TDD cycle.

NOTE—The durations for N_r , N_p , and N_z (expressed in symbols) in Table 192–9 and Table 192–10 correspond to the durations (expressed in ns) in Table 192–7..

Table 192–9— N_r , N_p , and N_z values for 100 Mb/s mode transmission

tx_mode	refresh header N_r (symbols)	payload N_p (symbols)	QUIET N_z (symbols)
SEND_TS	560	12 880	15 360
SEND_TA	624	1040	27 136
SEND_N	624	1040	27 136
NOTE—All symbols are sent at 3 GBd.			

Table 192–10— N_r , N_p , and N_z values for 2.5 Gb/s mode transmission

tx_mode	refresh header N_r (symbols)	payload N_p (symbols)	QUIET N_z (symbols)
SEND_TS	560	12 880	15 360
SEND_TA	480	25 600	2720
SEND_N	480	25 600	2720
NOTE—All symbols are sent at 3 GBd.			

Table 192–11— N_r , N_p , and N_z values for 5 Gb/s, 7.5 Gb/s, and 10 Gb/s mode transmission

tx_mode	refresh header N_r (symbols)	payload N_p (symbols)	QUIET N_z (symbols)
SEND_TS	560	12 880	15 360
SEND_TA	960	51 200	5440
SEND_N	960	51 200	5440
NOTE—SEND_TS symbols are sent at 3 GBd. SEND_TA and SEND_N symbols are sent at 6 GBd.			

192.3.4.2 Refresh header and payload data bits generation

The refresh header shall be composed of a leading sequence of zeros followed by four bytes of 0x01, followed by four bytes of 0xF0. The refresh header bits are scrambled with the PRBS11 scrambler defined in 192.3.2.2.18. The PRBS11 scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

N_p payload bits follow the refresh header in each burst. The payload bits are scrambled with the PRBS33 scrambler defined in 192.3.2.2.19.

The training frame contents are specified in Equation (192–11). N_{inf} is the bit position where Infocfield starts within the training payload. The training frame starts at bit zero, with $0 \leq n \leq N_r - 1$ consisting of the refresh header as shown in Equation (192–11). Per Equation (192–11), TF_n is all zeros from the end of the refresh header to the beginning of the Infocfield, followed by the 96-bit Infocfield, then followed by all zeros from the end of the Infocfield to the end of the training payload, which is the end of the training frame.

$$TF_n = \begin{cases} refresh\_header(n) & 0 \leq n \leq N_r - 1 \\ 0 & N_r \leq n \leq N_r + N_{inf} - 1 \\ Infocfield(n - [N_r + N_{inf}]) & N_r + N_{inf} \leq n \leq N_r + N_{inf} + 95 \\ 0 & N_r + N_{inf} + 96 \leq n \leq N_r + N_p - 1 \end{cases} \quad (192-11)$$

where

N_{inf} is equal to $N_p - 256$

192.3.4.3 PAM mapping and generation of TDD bursts

Except when transmitting 7.5 Gb/s or 10 Gb/s payload symbols and tx_mode is SEND_N, bits are encoded by the PAM2 mapper defined in 192.3.2.2.23. When transmitting 7.5 Gb/s payload symbols and tx_mode is SEND_N, bits are encoded by the PAM3 encoder defined in 192.3.2.2.22. When transmitting 10 Gb/s payload symbols and tx_mode is SEND_N, bits are encoded by the Gray-coded PAM4 encoder defined in 192.3.2.2.20 and 192.3.2.2.21. Z symbols are sent between each TDD burst frame to form the sequence O_n , as defined in Equation (192–12). The values of O_n are then conveyed to the PMA for transmission via the parameter tx_symb of the PMA_UNITDATA.request primitive.

The transmit symbol O_n is selected by TDD control logic. For each TDD cycle (specified in 192.3.4), the Transmit function will send out T_n or Z symbols to the PMA, based on symbol time index n .

$$O_n = \begin{cases} T_n & 0 \leq n \leq N_r + N_p - 1 \\ Z & N_r + N_p \leq n \leq N_{TDD} - 1 \end{cases} \quad (192-12)$$

where

n is the continuous symbol count modulo N_{TDD}
 N_{TDD} is the number of symbols equivalent to a nominal 9.6 μ s TDD cycle time

T_n is the output of the PAM2, PAM3, or PAM4 Mapper as defined in Equation (192-13).

$$T_n = \begin{cases} PAM2\_Mapper(A_n) & \text{tx\_rate} = 100 \text{ Mb/s OR tx\_rate} = 2.5 \text{ Gb/s OR} \\ & \text{tx\_rate} = 5 \text{ Gb/s OR !(tx\_mode} = \text{SEND\_N) OR} \\ & (0 \leq n \leq N_r - 1) \\ PAM3\_Mapper(A_n) & \text{tx\_rate} = 7.5 \text{ Gb/s AND tx\_mode} = \text{SEND\_N AND} \\ & (N_r \leq n \leq N_r + N_p - 1) \\ PAM4\_Mapper(G_n) & \text{tx\_rate} = 10 \text{ Gb/s AND tx\_mode} = \text{SEND\_N AND} \\ & (N_r \leq n \leq N_r + N_p - 1) \end{cases} \quad (192-13)$$

where

A_n is specified in 192.3.2.2.20
 G_n is the Gray-coded symbol specified in 192.3.2.2.20
 $PAM2\_Mapper$ is specified in 192.3.2.2.23
 $PAM3\_Mapper$ is specified in 192.3.2.2.22
 $PAM4\_Mapper$ is specified in 192.3.2.2.21
 tx_rate is the selected transmit data rate

192.3.4.4 PCS descrambler polynomials

The PCS shall acquire descrambler state synchronization to the PAM2 training sequence and report success through `scr_status`, and continue to use the synchronized state in all subsequent bursts in both data and training modes. The Follower PCS employs the receiver descrambler generator polynomial per Equation (192-9) and the Leader PCS employs the receiver descrambler generator polynomial per Equation (192-10).

192.3.5 PCS Detailed functions and state diagrams

192.3.5.1 State diagram parameters

192.3.5.1.1 Constants

`EBLOCK_R<71:0>`
72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>	1
65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.	2
	3
LBLOCK_R<71:0>	4
72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.	5
	6
	7
LBLOCK_T<64:0>	8
65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.	9
	10
IBLOCK_R<71:0>	11
72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.	12
	13
IBLOCK_T<64:0>	14
65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.	15
	16
RFER_CNT_LIMIT	17
TYPE: Integer	18
VALUE: 16	19
Number of Reed-Solomon frames with uncorrectable errors.	20
	21
RFRX_CNT_LIMIT	22
TYPE: Integer	23
VALUE: 88	24
Number of Reed-Solomon frames received over bit error ratio interval.	25
	26
UBLOCK_R<71:0>	27
72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets.	28
The Link Interruption ordered set is defined in 46.3.4.	29

192.3.5.1.2 Variables

block_lock	31
Boolean variable that is set TRUE while the receiver is able to delineate the received burst payload boundaries. Otherwise set to FALSE.	32
	33
hi_rfer	34
Boolean variable. See Figure 192–21. Set to TRUE when the received FEC frame uncorrectable error rate is high, and set to FALSE when the received FEC frame uncorrectable error rate is low.	35
	36
pcs_data_mode	37
Variable set by the PMA PHY Control function. See 192.2.1.8.1.	38
	39
pcs_reset	40
Boolean pcs_reset parameter set by the PCS Reset function. It is TRUE for the duration of a PCS reset. Otherwise set to FALSE.	41
	42
rf_valid	43
Boolean indication that is set TRUE if received Reed-Solomon frame is valid. A Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied. rf_valid is set FALSE when an RS-FEC frame is received and is invalid.	44

rs_fec_frame_done
A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. Otherwise set to FALSE.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 192–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

tx_coded<64:0>
Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 192–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

192.3.5.1.3 Functions

DECODE(rx_coded<64:0>)
In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block as specified in 192.3.2.2.4.

ENCODE(tx_raw<71:0>)
Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 192.3.2.2.4.

R_BLOCK_TYPE = {C, S, T, D, E}
Every case of the vector belongs to only one type.
Values: C; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x1E and seven valid control characters other than /E/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.
S; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.
T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.
D; The vector contains a data/ctrl header of 0.
E; The vector does not meet the criteria for any other value.
A valid control character is one containing a control code specified in Table 192–3. A valid O code is one containing an O code specified in Table 192–3.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains one of the following:

- a) Eight valid control characters other than /O/, /S/, /T/, /E/;
- b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
- c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 192–3. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 192–3.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

192.3.5.1.4 Counters

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt

Count number Reed-Solomon frames received during current period.

192.3.5.1.5 Messages

RX_FRAME

A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

192.3.5.2 State diagrams

The RFER monitor state diagram shown in Figure 192–21 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 192–22 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

The PCS 64B/65B Receive state diagram shown in Figure 192–23 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams.

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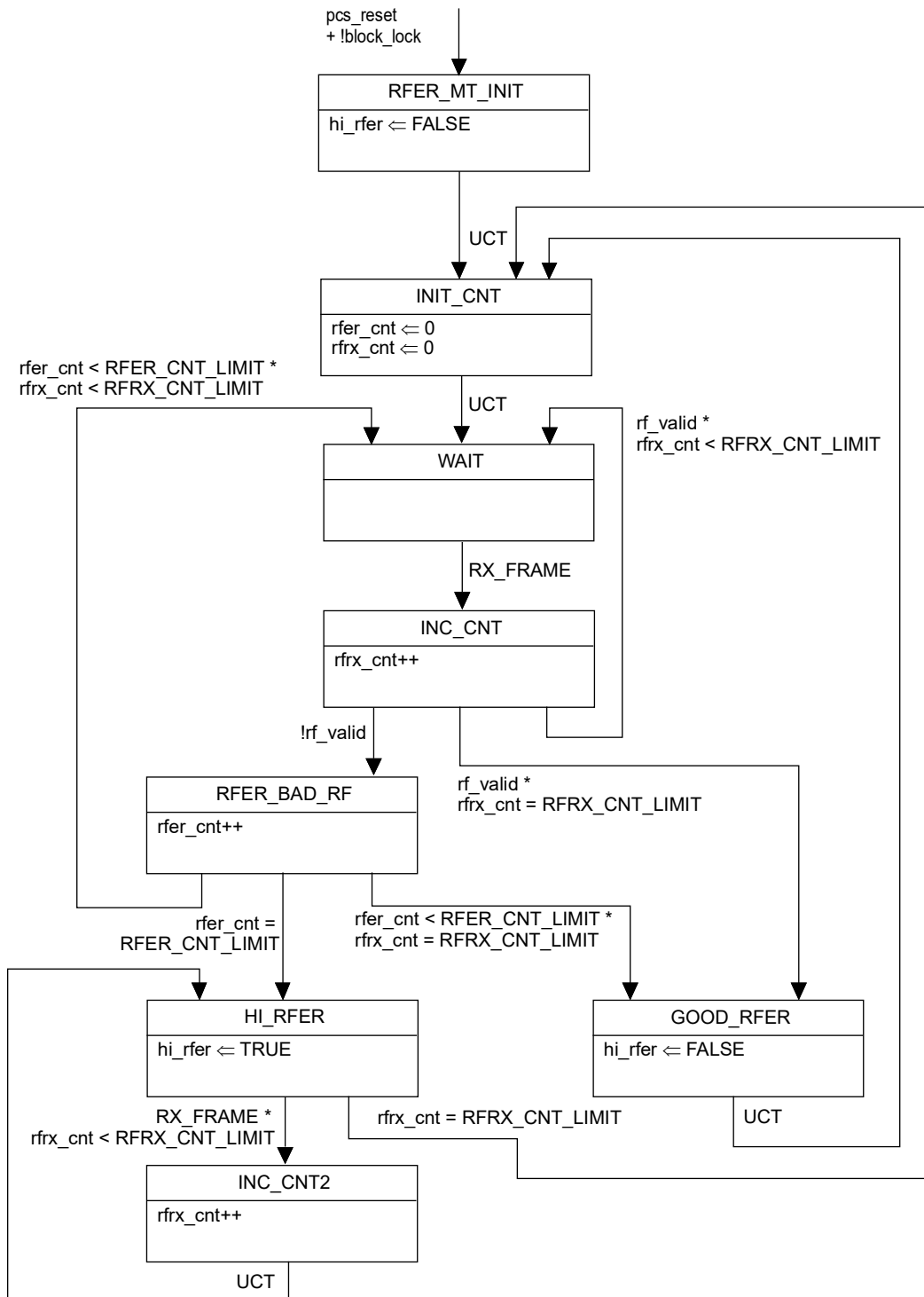
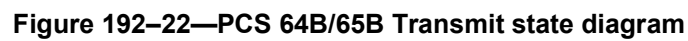


Figure 192-21—RFER monitor block state diagram



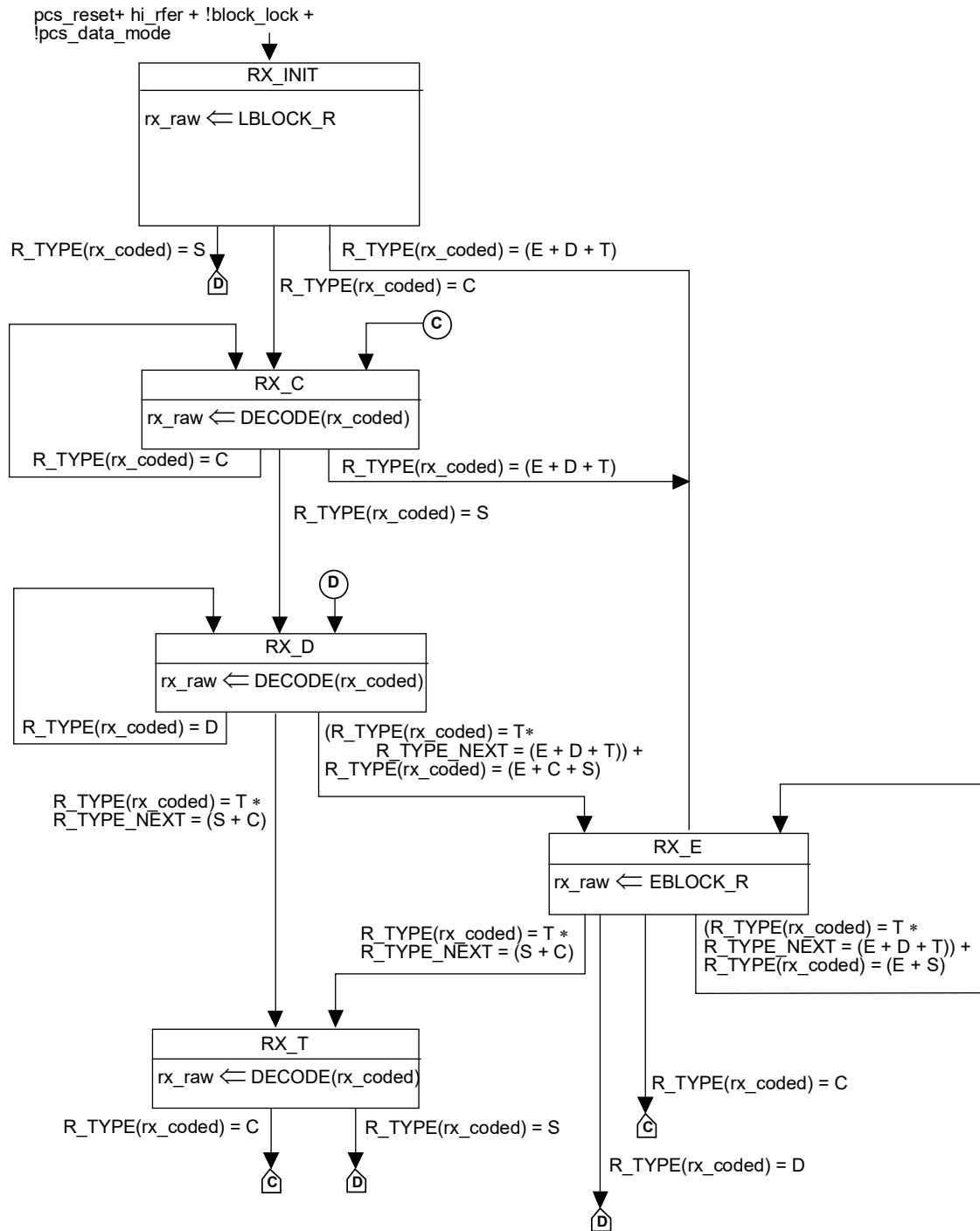


Figure 192-23—PCS 64B/65B Receive state diagram

192.3.6 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

192.3.6.1 Status

pcs_status:

Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO 3.2323.2 and the inverse of this status is reflected in MDIO 3.2323.7.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:

Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

192.3.6.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:

6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 192–21) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

192.3.7 MultiGBASE-A operations, administration, and maintenance (OAM)

MultiGBASE-A operations, administration, and maintenance (OAM) is a subset of OAM specified for MultiGBASE-T1 PHYs in 149.3.9 since EEE is not supported and OAM symbol to field mapping differs. OAM involves both HS_PATH and LS_PATH. The 10-bit OAM symbols are inserted one per TDD burst into the OAM fields in the HS_PATH and LS_PATH. OAM bits after the first ten per burst are reserved.

The MultiGBASE-A PCS level OAM provides an optional mechanism useful for monitoring link operations such PHY link health status exchange and message exchange. When OAM is implemented, behavior shall conform to the state diagrams in Figure 192–25 and Figure 192–26. OAM information is exchanged out of band between two PHYs using excess bandwidth available on the link. The OAM is strictly between two PHYs on the Physical Layer and their associated management entities if present. Passing OAM information to other layers is outside the scope of this standard.

OAM is operational as long as both PHYs implement this mechanism and the link is up.

The OAM frame data is carried in the OAM 10-bit field in the first ten bits of each TDD burst as described in 192.3.7.2.1. This 10-bit field is used to exchange OAM frames. The implementation of the OAM frame exchange function is optional.

For the remainder of this subclause, the term OAM is specific to the MultiGBASE-A PCS level OAM.

192.3.7.1 Definitions

OAM frame: A frame consisting of 14 octets of data, 14 framing bits, 14 reserved bits and two 10-bit Reserved symbols.

OAM symbol: A 10-bit symbol consisting of either one data octet plus a framing bit and a reserved bit, or a 10-bit Reserved symbol. 16 OAM symbols make up an OAM frame.

OAM field: A 10-bit field in each TDD burst reserved for the OAM symbol as described in 192.3.7.2.1.

OAM message: A message contains a 4-bit message number plus eight octets of message data (Message<7:0><7:0>) embedded in an OAM frame. The same OAM message can be repeated on multiple OAM frames.

OAM status: The four octets of status data (Message<11:8><7:0>) that is embedded in each OAM frame.

192.3.7.2 Functional specifications

192.3.7.2.1 MultiGBASE-A OAM frame structure

Each OAM frame is made up of 16 OAM symbols. Each of the first 14 symbols is made up of one octet of data, one framing bit, and one reserved bit. The last two symbols are the Reserved symbols.

One OAM symbol is placed in the 10-bit OAM field in each TDD burst during data mode. The 16 OAM symbols are consecutively inserted into 16 consecutive TDD bursts. Once the 16 symbols of the current OAM frame are inserted, the 16 symbols of the next OAM frame are inserted. This process is continuous without any break in the insertion of OAM symbols with the exception noted below.

When operating in HS_TX mode, the first bit of an OAM symbol (OAM<X><0>) shall be inserted in the OAM bit of the first RS-FEC frame in the first superframe of each TDD burst prior to interleaving. Each subsequent bit shall be inserted in the next nine RS-FEC frames such that the OAM symbol is carried in the first ten RS-FEC frames. When operating in LS_TX mode, an OAM symbol (OAM<X><9:0>) shall be inserted in the first ten OAM bits of the RS-FEC frame such that the OAM symbol is carried in the first ten bits of the OAM field of the RS-FEC frame. In this way, both HS_PATH and LS_PATH send and receive one OAM symbol per TDD burst.

Bit 0 of each OAM symbol is the first bit transmitted in the 10-bit OAM field. Symbol 0 is the first symbol transmitted in each OAM frame.

The OAM frame boundary can be found at the receiver by looking at bit D8. The boundary is a zero followed by 13 ones followed by two don't care.

If OAM is not implemented, then the 10-bit OAM field shall be set to all zeros. If the link partner does not implement OAM, the 10-bit OAM field will remain static.

192.3.7.2.2 OAM frame data

The OAM frame data is shown in Figure 192–24. OAM<x><y> refers to symbol x, bit y of the OAM frame. Reserved fields shall be set to zero.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Reserved	0	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Reserved	1	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Reserved	1	Message<0><7:0>							
Symbol 3	Reserved	1	Message<1><7:0>							
Symbol 4	Reserved	1	Message<2><7:0>							
Symbol 5	Reserved	1	Message<3><7:0>							
Symbol 6	Reserved	1	Message<4><7:0>							
Symbol 7	Reserved	1	Message<5><7:0>							
Symbol 8	Reserved	1	Message<6><7:0>							
Symbol 9	Reserved	1	Message<7><7:0>							
Symbol 10	Reserved	1	Message<8><7:0>							
Symbol 11	Reserved	1	Message<9><7:0>							
Symbol 12	Reserved	1	Message<10><7:0>							
Symbol 13	Reserved	1	Message<11><7:0>							
Symbol 14	Reserved									
Symbol 15	Reserved									

Figure 192–24—OAM frame

192.3.7.2.3 Ping RX

The Ping RX is indicated in OAM<0><3>.

This bit is set by the PHY to the same value as the Ping TX bit received from the link partner.

192.3.7.2.4 Ping TX

The Ping TX is indicated in OAM<0><2>.

This bit is set by the PHY for the link partner to echo on Ping RX.

192.3.7.2.5 PHY health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame
- 01: Reserved
- 10: PHY SNR is marginal
- 11: PHY SNR is good

192.3.7.2.6 OAM message valid

The OAM message valid (Valid) is indicated in OAM<1><7>.

- 0: Current OAM frame does not contain a valid OAM message
- 1: Current OAM frame contains a valid OAM message

192.3.7.2.7 OAM message toggle

The OAM message toggle (Toggle) is indicated in OAM<1><6>.

The toggle bit lets the management entity determine which OAM message is being referenced. The toggle bit in the current OAM message is set to the opposite value of the toggle bit in the previous OAM message only if link partner acknowledges the OAM message is received. This allows one OAM message to be delineated from a second OAM message since the same OAM message may be repeated over multiple OAM frames. This bit is valid only if Valid is set to one.

192.3.7.2.8 OAM message acknowledge

The OAM message acknowledge (Ack) is indicated in OAM<1><5>.

Ack is set by the PHY to let the link partner know that the OAM message sent by the link partner was successfully received as defined in 192.3.7.2.13 and the PHY is ready to accept a new OAM message. An OAM message is defined to be Message_Number<3:0> and Message<7:0><7:0>.

- 0: No acknowledge
- 1: Acknowledge

192.3.7.2.9 OAM message toggle acknowledge

The OAM message toggle acknowledge (TogAck) is indicated in OAM<1><4>.

TogAck is set by the PHY to let the link partner know that the OAM message is being acknowledged. TogAck takes the value of Toggle bit of the OAM message being acknowledged. This bit is valid only if Ack is set to one.

192.3.7.2.10 OAM message number

The OAM message number is indicated in OAM<1><3:0>.

This field is user-defined, but recommended that it be used to indicate the meaning of the 8-octet message that follows. If used this way, up to 16 different 8-octet messages can be exchanged.

The message number is user-defined and its definition is outside the scope of this standard.

192.3.7.2.11 OAM message data

The OAM message data is indicated in OAM<9:2><7:0>.

The 8-octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the OAM frame sent by the link partner is successfully received as defined. The OAM frame octet is the lower 8 bits of the 10-bit OAM symbol.

192.3.7.2.12 OAM status

The OAM status data is indicated in OAM<13:10><7:0> on a per OAM frame basis.

These 32 bits are set by the PHY to convey its status in the mr_tx_message[95:64] to the link partner.

For additional information on the usage of these bits see [Annex 149B](#).

192.3.7.2.13 MultiGBASE-A OAM frame acceptance criteria

All fields of the OAM frame shall be accepted and updated, unless there is an uncorrectable RS-FEC frame on any of the 16 symbols.

192.3.7.2.14 PHY health indicator

The PHY current health is sent to the link partner on a per OAM frame basis using the SNR<1:0> bits as described in 192.3.7.2.5. It lets the link partner have an early indication of potential problems that can cause the PHY to drop link or have high error rates.

192.3.7.2.15 Ping

The PingTx bit is set based on the value in mr_tx_ping. The PingRx bit is set based on the latest PingTx received from the link partner. The value in mr_rx_ping is set based on the received PingRx from the link partner. The user can determine that the link partner OAM is operating properly by toggling mr_tx_ping and observing mr_rx_ping matches after a short delay.

The Ping bits are updated on a per OAM frame basis.

192.3.7.2.16 OAM message exchange

The OAM message exchange operates on a per OAM message basis that occurs over many OAM frames. The OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass OAM messages and verify their delivery.

The OAM message is first written into the OAM transmit registers in the PHY. The OAM message is then read out of the OAM transmit registers and transmitted to the link partner. After the link partner receives the OAM message, it transfers it into the link partner's OAM receive registers and also sends an acknowledge back to the PHY indicating that the next OAM message can be transmitted. One OAM message can be loaded into the OAM transmit registers while another OAM message is being transmitted by the PHY to the link partner, while yet another OAM message is being read out at the link partner's OAM receive registers. The exchange of OAM messages is occurring concurrently and bi-directionally. The transfers between the management entities can be done asynchronously. On the transmit side, mr_tx_valid = 0 indicates that the next OAM message can be written into the OAM transmit registers. Once the registers are written, the management entity sets mr_tx_valid to one to indicate that the OAM transmit registers contain a valid OAM message. Once the message is read out atomically, the state diagram clears the mr_tx_valid to zero to indicate that the registers are ready to accept the next OAM message.

On the receive side, mr_rx_lp_valid indicates that valid OAM message can be read from the OAM receive registers. Once these registers are read, the mr_rx_lp_valid should be cleared to zero to indicate that the registers are ready to receive the next OAM message. If mr_rx_lp_valid is not cleared, then the OAM message transfer will eventually stall since the sender cannot send new OAM messages if the receiver does not acknowledge that an OAM message has been transferred into the OAM receive registers.

The management entities can asynchronously read `mr_tx_valid` and `mr_rx_lp_valid` to know when OAM messages can be transferred in and out of the OAM registers.

The toggle bit alternates between zero and one, which lets the management entity determine which OAM message is being referred to. The toggle bit transitioning rules between one OAM frame and the next OAM frame are shown in Table 192–12.

Table 192–12—Toggle bit transition rules

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
0	0	0	0	No valid OAM message
0	0	0	1	Illegal transition (Error)
0	0	1	0	New OAM message starting
0	0	1	1	Illegal transition (Error)
0	1	0	0	Illegal transition (Error)
0	1	0	1	No valid OAM message
0	1	1	0	Illegal transition (Error)
0	1	1	1	New OAM message starting
1	0	0	0	Illegal transition (Error)
1	0	0	1	Received acknowledge, no new OAM message to send
1	0	1	0	Repeating current OAM message, waiting for link partner's acknowledge
1	0	1	1	Previous OAM message ending, new OAM message starting
1	1	0	0	Received acknowledge, no new OAM message to send
1	1	0	1	Illegal transition (Error)
1	1	1	0	Previous OAM message ending, new OAM message starting
1	1	1	1	Repeating current OAM message, waiting for link partner's acknowledge

192.3.7.3 State diagram variable to OAM register mapping

The state diagrams of Figure 192–25 and Figure 192–26 generate and accept variables of the form “`mr_x`,” where `x` is an individual signal name. These variables comprise a management interface to communicate the OAM information to and from the management entity. Clause 45 MDIO registers are defined in MMD3 to support the OAM. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended.

Assignments for PCS register/bit numbers 3.2308 to 3.231 are shown in Table 45–233. MultiGBASE-A uses the state variable to OAM register/bit number mapping for BASE-T1 shown in Table 97-6 and the state variable to OAM register/bit number mapping for MultiGBASE-T1 shown in Table 149-9.

192.3.7.4 Detailed functions and state diagrams

192.3.7.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

192.3.7.4.2 State diagram parameters

192.3.7.4.3 Variables

frame_boundary

Frame boundary detection based on the latest 16 rx_oam_field<8> received. The leftmost bit is the earliest received bit.

Values:

TRUE: Latest 16 rx_oam_field<8> = 01111111111111xx.

FALSE: Latest 16 rx_oam_field<8> ≠ 01111111111111xx.

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_rx_lp_message[95:0]

12-octet OAM message from the link partner. mr_rx_lp_message[63:0] in this variable is valid only when mr_rx_lp_valid is one. mr_rx_lp_message[95:64] is always valid and continuously updated.

mr_rx_lp_message_num[3:0]

4-bit message number from the link partner. The value in this variable is valid only when mr_rx_lp_valid is one.

mr_rx_lp_SNR[1:0]

Link partner health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.

01: Reserved.

10: PHY SNR is marginal.

11: PHY SNR is good.

The threshold for the status is implementation dependent.

mr_rx_lp_toggle

The toggle bit value associated with the 8-octet MultiGBASE-A OAM message from the link partner.

Values:

The toggle bit alternates between zero and one.

mr_rx_lp_valid	1
Indicates whether the OAM message in mr_rx_lp_message[63:0], mr_rx_lp_message_num[3:0] and the toggle bit in mr_rx_lp_toggle is valid or not. This variable should be cleared when mr_rx_lp_message[63:48] is read and is not explicitly shown in the state diagram. The clearing of this variable indicates to the state diagram that the MultiGBASE-A OAM message is read by the user and the state diagram can proceed to load in the next MultiGBASE-A OAM message.	2
Values:	3
0: Invalid.	4
1: Valid.	5
	6
mr_rx_ping	7
Echoed ping value from the link partner.	8
Values:	9
The value can be zero or one.	10
	11
mr_tx_message[95:0]	12
8-octet MultiGBASE-A OAM message and 4-octet MultiGBASE-A status transmitted by the local PHY. mr_tx_message[63:0] in this variable is valid only when mr_tx_valid is one. mr_tx_message[95:64] in this variable is always valid.	13
	14
mr_tx_message_num[3:0]	15
4-bit message number transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is one.	16
	17
mr_tx_ping	18
Ping value transmitted by the local PHY.	19
Values:	20
The value can be one or zero.	21
	22
mr_tx_received	23
Indicates whether the most recently transmitted MultiGBASE-A OAM message with a toggle bit value of mr_tx_received_toggle was received, read, and acknowledged by the link partner. This variable shall clear on read.	24
Values:	25
0: MultiGBASE-A OAM message was not received and read by the link partner.	26
1: MultiGBASE-A OAM message was received by the link partner.	27
	28
mr_tx_received_toggle	29
Toggle bit value of the MultiGBASE-A OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if mr_tx_received is one.	30
Values:	31
The value can be zero or one.	32
	33
mr_tx_SNR[1:0]	34
Status register indicating PHY health status.	35
Values:	36
00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.	37
01: Reserved.	38
10: PHY SNR is marginal.	39
11: PHY SNR is good.	40
The threshold for the status is implementation dependent.	41
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mr_tx_toggle	1
The toggle bit value associated with the 8-octet MultiGBASE-A OAM message transmitted by the PHY. The value is automatically set by the state diagram and cannot be set by the user. This bit should be read and recorded prior to setting mr_tx_valid to one.	2
Values:	3
The toggle bit alternates between zero and one.	4
mr_tx_valid	5
Indicates whether MultiGBASE-A OAM message in mr_tx_message[63:0] and mr_rx_lp_message_num[3:0] is valid or not. This register will be cleared by the state diagram to indicate whether the next MultiGBASE-A OAM message can be written into the registers.	6
Values:	7
0: Invalid.	8
1: Valid.	9
reset	10
Reset.	11
Values:	12
TRUE: OAM circuit is in reset.	13
FALSE: OAM circuit is not in reset.	14
rs_check	15
Status of the latest rs_correct() operation.	16
Values:	17
GOOD: No errors or correctable error.	18
BAD: Uncorrectable error.	19
rx_ack	20
Acknowledge from link partner in response to PHY's MultiGBASE-A OAM message.	21
Values:	22
0: Not acknowledged.	23
1: Acknowledged.	24
rx_ack_toggle	25
The toggle value corresponding to the PHY's MultiGBASE-A OAM message that the link partner is acknowledging. This value is valid only if the rx_ack is set to one.	26
Values:	27
The toggle bit can take on values of zero or one.	28
rx_boundary	29
This variable is set to TRUE whenever the receive data stream reaches the end of a Reed-Solomon frame and a complete 10-bit OAM symbol is available per 192.3.7.2.1 during data mode. Otherwise set to FALSE.	30
Values:	31
TRUE: Receive stream is at a boundary end.	32
FALSE: Receive stream is not at a boundary end.	33
rx_exp_toggle	34
This variable holds the expected toggle value of the next MultiGBASE-A OAM message. This is normally the opposite value of the current toggle value, but shall reset on error conditions where two back-to-back MultiGBASE-A OAM messages separated by MultiGBASE-A OAM frames without a valid message have the same toggle value.	35
Values:	36
The toggle bit can take on values of zero or one.	37

rx_lp_ack	1
Acknowledge from PHY in response to link partner's MultiGBASE-A OAM message. Indicates whether valid MultiGBASE-A OAM message from the link partner has been sampled into the PHY's registers.	2
Values:	3
0: Not acknowledged/not sampled.	4
1: Acknowledged/sampled.	5
rx_lp_ping	6
Ping value received from the link partner that is looped back.	7
Values:	8
The value can be zero or one.	9
rx_lp_toggle	10
The toggle bit value in the previous MultiGBASE-A OAM frame received from the link partner.	11
Values:	12
The toggle bit alternates between zero and one.	13
rx_lp_valid	14
Indicates whether MultiGBASE-A OAM message in previous MultiGBASE-A OAM frame received from the link partner is valid or not.	15
Values:	16
0: Invalid.	17
1: Valid.	18
rx_oam_field<9:0>	19
10-bit MultiGBASE-A OAM symbol extracted from a received TDD burst during data mode.	20
rx_oam<15 to 0><9:0>	21
Raw 16-symbol OAM frame received from the link partner.	22
SNR[1:0]	23
PHY health status.	24
Values:	25
00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.	26
01: Reserved.	27
10: PHY SNR is marginal.	28
11: PHY SNR is good.	29
Both the status threshold and condition for generating this status are implementation dependent.	30
tx_boundary	31
This variable is set to TRUE whenever the transmit data stream reaches the start of a TDD burst during data mode. Otherwise set to FALSE.	32
Values:	33
TRUE: Transmit stream is at a boundary end.	34
FALSE: Transmit stream is not at a boundary end.	35
tx_oam_field<9:0>	36
10-bit MultiGBASE-A OAM symbol inserted into a transmitted TDD burst during data mode.	37
tx_oam<15 to 0><9:0>	38
Raw 16-symbol OAM frame transmitted from the PHY.	39

tx_lp_ready

Indicates whether the link partner is ready to receive the next MultiGBASE-A OAM message from the PHY. If ready, then the PHY will load the next MultiGBASE-A OAM message from the registers and begin transmitting them.

Values:

0: Not ready.
1: Ready.

tx_toggle

The toggle bit value being sent in the current MultiGBASE-A OAM frame transmitted by the PHY.

Values:

The value can be zero or one.

192.3.7.4.4 Counters

rx_cnt

A count of received OAM frame symbols.

Values:

The value can be any integer from 0 to 16, inclusive.

tx_cnt

OAM frame transmit symbol count.

Values:

The value can be any integer from 0 to 16, inclusive.

192.3.7.4.5 Functions

rs_correct (16 OAM symbols)

This function returns the 14 data symbols unmodified and sets rs_check to GOOD if none of the RS-FEC frames are uncorrectable.

192.3.7.4.6 State diagrams

The receive state diagram is shown in Figure 192–25 and the transmit state diagram is shown in Figure 192–26.

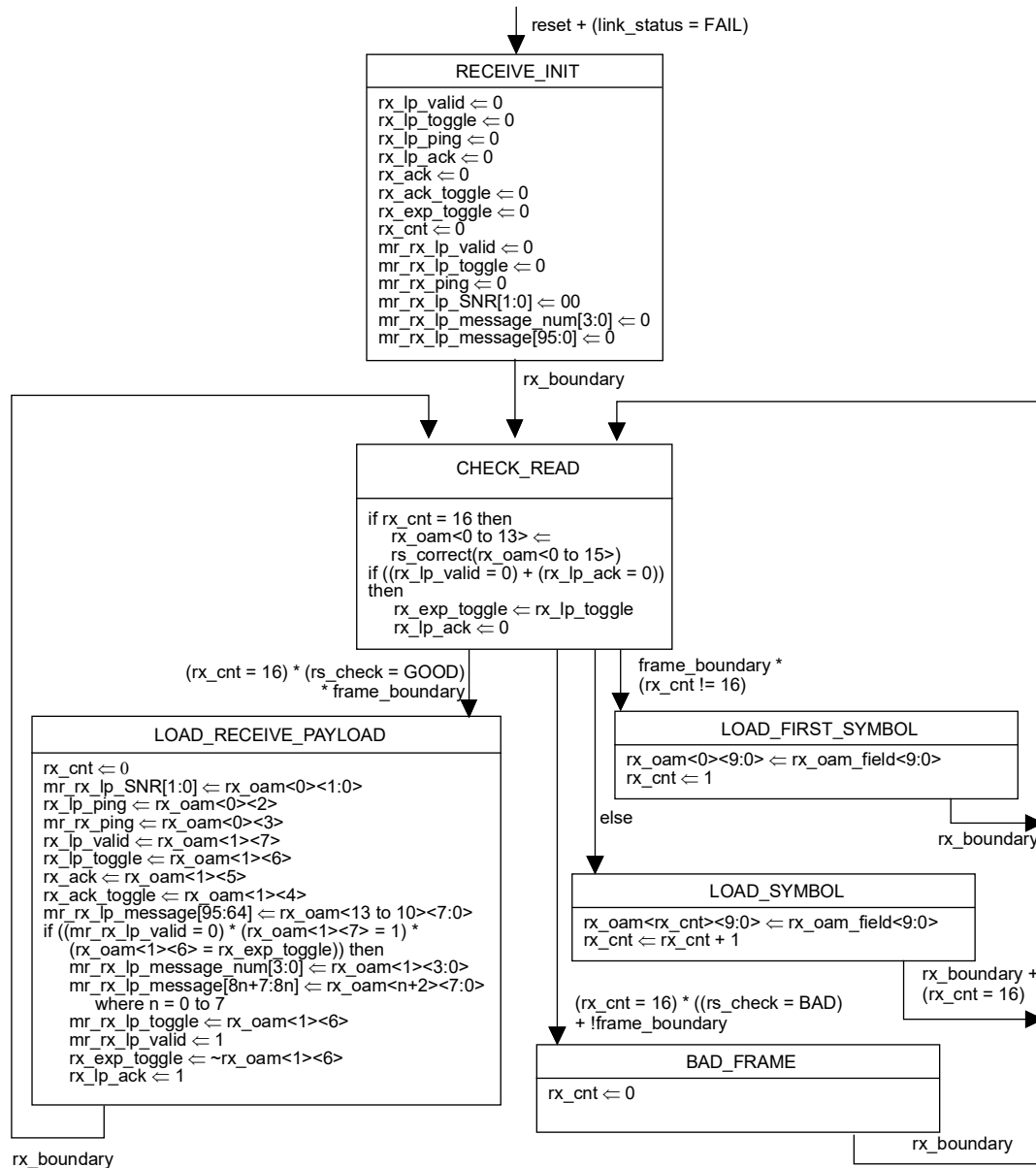


Figure 192–25—Receive state diagram

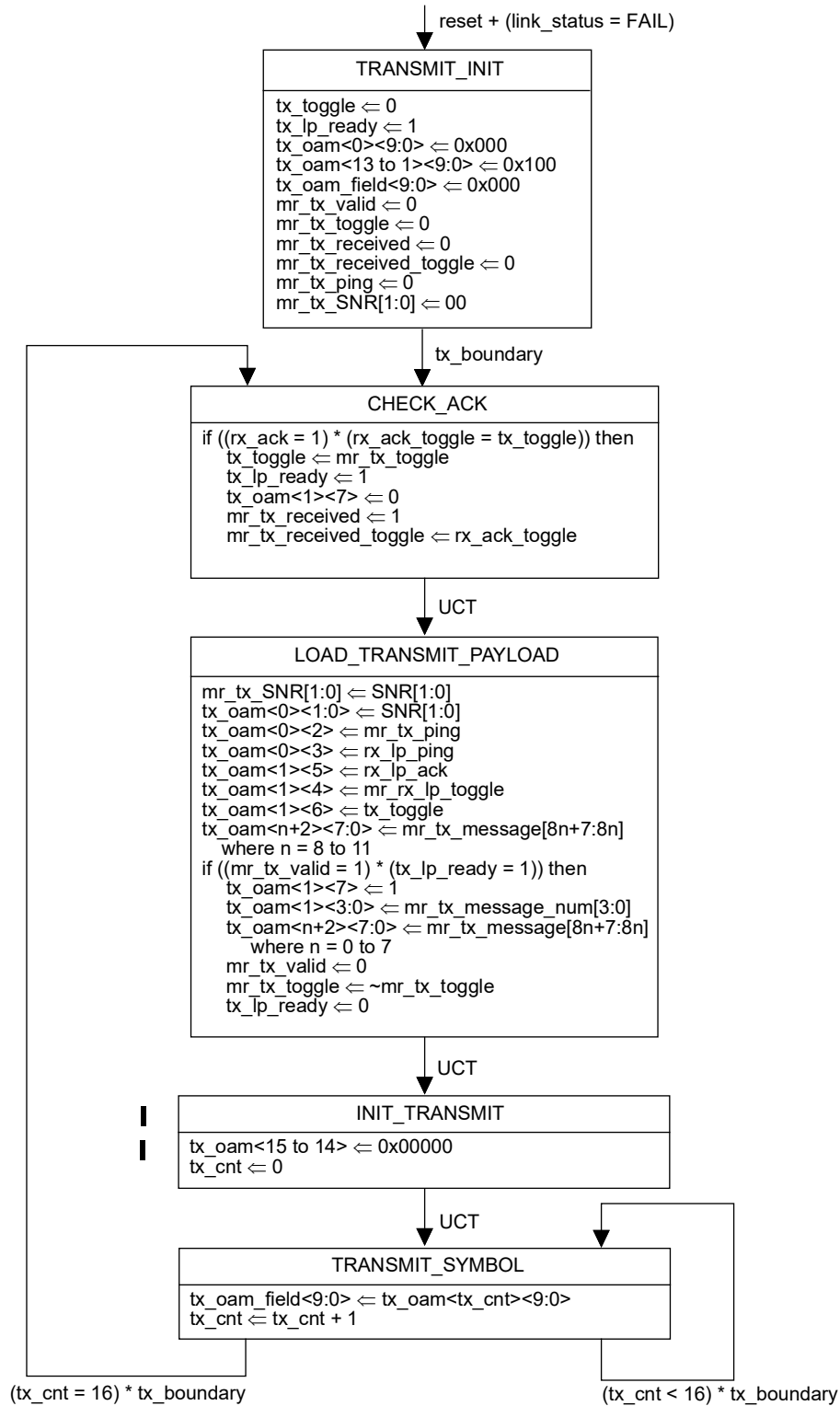


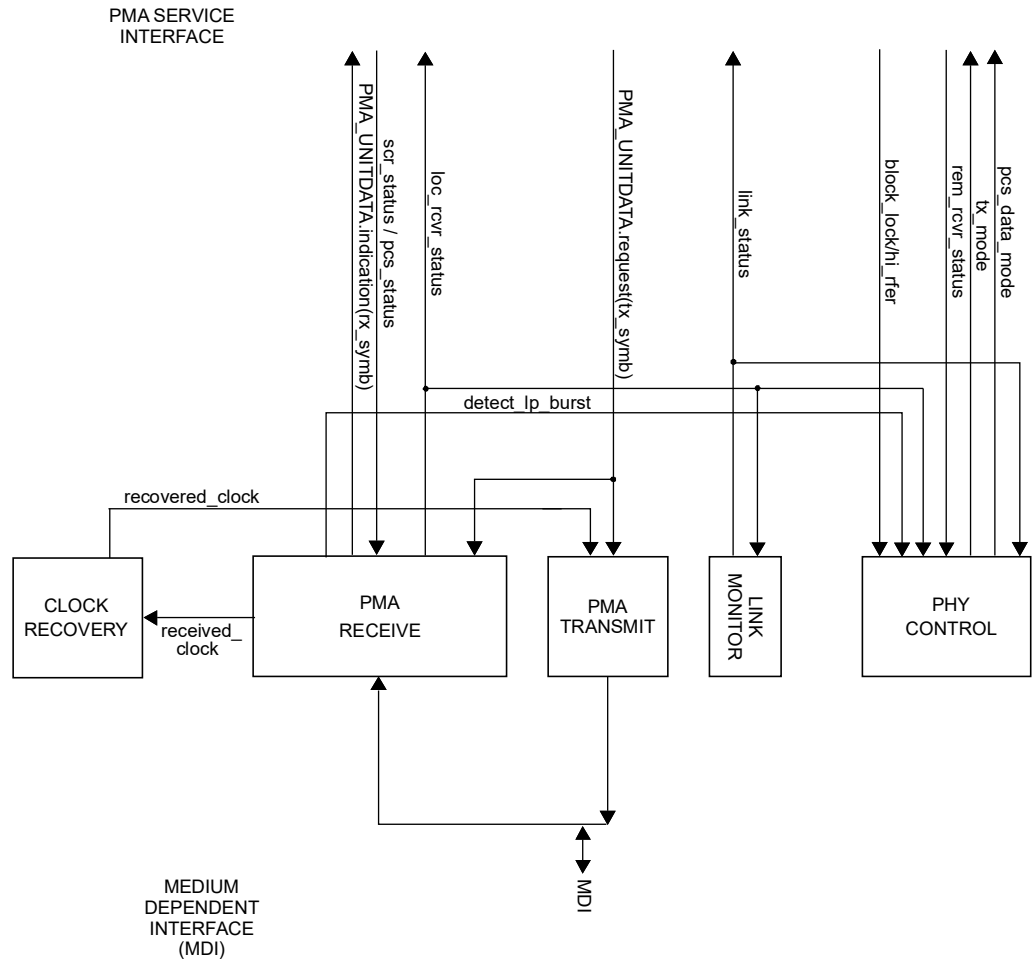
Figure 192–26—Transmit state diagram

192.4 Physical Medium Attachment (PMA) sublayer

192.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 192.2.1 to the baseband medium specified in 192.7 or 192.8.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 192.9 or 192.10.



NOTE—The *recovered_clock* arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

Figure 192–27—PMA reference diagram

192.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram (see Figure 192–27) shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 192–27.

192.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

- a) Power for the device containing the PMA has not reached the operating state.
- b) The receipt of a request for reset from the management entity.

PMA Reset sets `pma_reset` = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended `pma_reset` branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 192–31), if link partner has already exited DISABLE_TRANSMITTER state.

192.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a two-level, three-level, or four-level modulated signal on the single balanced pair of conductors (-T1) or the single coaxial cable (-V1). When the PHY Control state diagram (see Figure 192–31) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by `tx_symb` onto the MDI, followed by a QUIET period to complete a TDD cycle. The signals generated by PMA Transmit shall comply with the electrical specifications given in 192.5.2.

When the management parameter `config` is LEADER, the PMA Transmit function shall source the transmit symbol clock `TX_TCLK` from a local clock source while meeting the transmit jitter requirements of 192.5.2.3. The Leader-Follower relationship shall include loop timing. If the management parameter `config` is FOLLOWER, the PMA Transmit function shall source `TX_TCLK` from the recovered clock of 192.4.2.6 while meeting the jitter requirements of 192.5.2.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

192.4.2.2.1 Global PMA transmit disable

When the `PMA_transmit_disable` variable is set to TRUE, this function shall cause the average launch power of the transmitter to be as specified in 192.5.2.4 when the value of `tx_symb` is Z.

192.4.2.3 PMA Receive function

The PMA Receive function receives a two-level, three-level, or four-level modulated signal on a single balanced pair of conductors (-T1) or single coaxial cable (-V1). It includes a PAM2 receiver for all signal rates and, optionally, a PAM3 receiver for 7.5 Gb/s, a PAM4 receiver for 10 Gb/s, or both. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received into the `PMA_UNITDATA.indication` parameter `rx_symb`. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a -T1 link segment meeting the requirements of 192.7 or a -V1 link segment meeting the requirements of 192.8.

To achieve the indicated performance, it is highly recommended that PMA Receive include the function of signal equalization. No echo cancellation is needed due to the TDD nature of the duplexing method.

The PMA Receive generates the detect_lp_burst signal, which is set to TRUE when the PMA detects reception of PAM2 symbols at the start of a burst and set to FALSE when the PMA detects the QUIET portion of the burst.

The PMA Receive function uses the parameters pcs_status and scr_status, as well as the state of the equalization and estimation functions, to determine the quality of the receiver performance and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see Figure 192–31). Failing to receive the link partner's consecutive TDD bursts could trigger deassertion of loc_rcvr_status. The reception of Z symbols during the TDD QUIET period alone shall not trigger setting loc_rcvr_status to NOT_OK. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for signal inversions.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

192.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 192–31.

During PMA training (TRAINING and COUNTDOWN states in Figure 192–31), PHY Control information is exchanged between link partners with a 12-octet Infocfield, which is XORed with the 96 bits starting after the N_{inf}^{th} bit of the training payload specified in 192.3.4.3. The link partner is not required to decode every Infocfield transmitted but is required to decode Infocfields at a rate that enables the correct actions prior to the training phase transition.

The 12-octet Infocfield shall include the fields in 192.4.2.4.2 through 192.4.2.4.8, also shown in Figure 192–28 and Figure 192–29. When PMA_state = 00, Infocfield shall be transmitted at least 16 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octet 8	octets 9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	delay counter	PHY capability bits	CRC16

Figure 192–28—Infocfield TRAINING format

PMA_state = 01						
octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	PhaseSwBC24	CRC16

Figure 192–29—Infocfield COUNTDOWN format

192.4.2.4.1 Infocfield notation

For all the Infocfield notations in the following subclauses, Reserved <bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infocfield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (i.e., the LSB of octet 1 is sent first).

192.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0> and so forth.

192.4.2.4.3 PHY burst count (BC24)

The PHY burst count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6,7:0>] and indicates the running count of PHY bursts sent LSB first. The BC24 continues to run uninterrupted for the duration of the link.

BC24 is defined to rollover to zero after it reaches 16 776 959. BC24 could roll over in the case the Leader has started long before the Follower sends the first responding burst.

192.4.2.4.4 Message Field

The Message Field is one octet. For both the Leader and Follower, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, training_phase<4:3>, reserved<2:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

The two training_phase-indicator bits training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> = 00 indicates SYMMETRIC TRAINING and training_phase<4:3> = 01 indicates ASYMMETRIC TRAINING.

All possible Message Field settings are listed in Table 192–13 for the Leader or Follower. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 192–13 for the Leader, and the first or second row of Table 192–13 for the Follower. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infocfield variable is set to loc_rcvr_status<5> = 1 and set to zero otherwise.

Table 192–13—Infocfield Message Field valid Leader or Follower settings

PMA_state<7:6>	loc_rcvr_status<5>	training_phase<4:3>	reserved	reserved	reserved
00	0	00	0	0	0
00	1	00	0	0	0
01	1	00	0	0	0
00 ^a	0	01	0	0	0
00	1	01	0	0	0
01	1	01	0	0	0

^aThis row can be skipped if not applicable.

192.4.2.4.5 PHY capability bits

This multi-rate PHY supports bidirectional data transfer with 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s point-to-point transmission or reception in one direction and 100 Mb/s point-to-point reception or transmission in the other direction. The direction of asymmetry and high speed data rate are determined at link startup. The management control configures the Leader to negotiate with the Follower to configure it for the desired high speed data rate that the Follower is expected to use. The PHY capability and negotiated rates of the Infocfield are used to establish the Follower rate and check for misconfiguration.

When PMA_state<7:6> = 00, the Infocfield [Oct9<7:0>,Oct10<7:0>] contains the PHY capability and negotiated ability bits. Each octet is sent LSB first. The field locations (see Table 192–14) carry different values depending on the value of the burst count (BC24) LSB. Table 192–15, Table 192–16, and Table 192–17 show the field encoding bits.

Table 192–14—PHY capability and negotiated ability bits

	octet 9								octet 10							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	PHY_D / PHY_S transmit and receive capability															
	Transmit capability								Receive capability							
	LS rate		HS rate						LS rate		HS rate					
BC24 LSB = 0	Reserved	100 Mb/s	Reserved	Reserved	10 Gb/s	7.5 Gb/s	5 Gb/s	2.5 Gb/s	Reserved	100 Mb/s	Reserved	Reserved	10 Gb/s	7.5 Gb/s	5 Gb/s	2.5 Gb/s
	PHY_D / PHY_S negotiated ability															
BC24 LSB = 1	Vendor specific data								Direction	OAMEn	Reserved	Negotiated rates				

The transmit and receive capabilities depend on whether the PHY supports PHY_S, PHY_D, or both capabilities. For example, PHY_S sets its HS_TX capability and LS_RX capability, and PHY_D set its HS_RX capability and LS_TX capability. The capability bit field assignments are shown in Table 192–15. A one in a field bit indicates that the PHY has that capability and a zero indicates it does not. All zeros indicates that the field is not applicable to this PHY. For example, since a PHY that only supports PHY_S has no HS_RX capability, it would set Oct10<7:2> to zero.

Table 192–15—Rate field encoding

LS rate		HS rate	
00	N/A	000000	N/A
x1	100 Mb/s	xxxxx1	2.5 Gb/s
1x	Reserved	xxxx1x	5 Gb/s
		xxx1xx	7.5 Gb/s
		xx1xxx	10 Gb/s
		x1xxxx	Reserved
		1xxxxx	Reserved

The negotiated rates field encoding is shown in Table 192–16. The Leader selects the negotiated rates based on either management configuration of register bits 1.2319<5:1> or selecting the highest mutually supported advertised rate. In the latter case, the Leader optionally sends the all zeros negotiated rate code when it desires to see the Follower capabilities prior to determining the negotiated rates.

Table 192–16—Negotiated rate field encoding

Code	LS rate	HS rate
00000	In progress	In progress
00001	100 Mb/s	2.5 Gb/s
00010	100 Mb/s	5 Gb/s
00011	100 Mb/s	7.5 Gb/s
00100	100 Mb/s	10 Gb/s
00101	Reserved	Reserved
00110	Reserved	Reserved
00111	Reserved	Reserved
01xxx	Reserved	Reserved
1xxxx	Reserved	Reserved

The Leader uses the direction bit to communicate the desired Follower PHY type as shown in Table 192–17.

Table 192–17—Negotiated direction field encoding

Code	Leader	Follower
0	PHY_D	PHY_S
1	PHY_S	PHY_D

OAMEn: The optional OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1.

The capability bit values shall be considered as valid only when loc_rcvr_status<5> bit is 1.

192.4.2.4.6 TDD delay counter

When PMA_state<7:6>=00, then Oct8<7:0> contains the TDD delay counter, sent LSB first. The format of TDD delay counter is Oct8<0> = Reserved, Oct8<1:6> = delay_count<5:0>, and Oct8<7> = delay_count_valid as shown in Table 192–18.

Table 192–18—TDD delay counter

octet 8							
0	1	2	3	4	5	6	7
Reserved	delay_count						delay_count_valid

After the Leader detects the Follower TDD burst position and estimates the link segment delay, it shall set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to one. The TDD delay counter may be calculated as the estimated link segment delay in symbol times (at the 3 GBd rate) divided by 16, then rounded to the nearest integer. Each LSB unit represents 5.333 ns delay (16 symbols at 3 GBd).

The Follower shall accept the received remote delay_count only when received remote delay_count_valid bit is set to one. The Follower shall store this delay_count number.

As acknowledgment of the reception of this delay_count, the Follower shall send back its received delay count in its own delay_count field and set its delay_count_valid to one, so the Leader can confirm the exchange of this information is completed. When the Leader or the Follower finishes the exchange of delay count and the negotiated data rates, it shall set negotiation_done to OK. The PHY Control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.

Starting from Asymmetric training and continuing through to the data mode, the Follower shall adjust its transmit burst position according to the stored delay_count.

192.4.2.4.7 Phase switch PHY burst count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the phase switch burst count (PhaseSwBC24) sent LSB first. PhaseSwBC24 indicates the burst count when the Leader transmitter switches from current training phase to the next training phase or data mode. PhaseSwBC24 shall be a minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state.

Since phase switch is always initiated from the Leader, the PhaseSwBC24 value of Follower Infocfield may be ignored. The Leader will exit a COUNTDOWN state after sending the last burst (BC24 = PhaseSwBC24 – 1), and receiving the last burst from the Follower. The Follower will exit a COUNTDOWN state after receiving the last burst (BC24 = PhaseSwBC24 – 1) from the Leader and finishing sending the last burst of its own.

192.4.2.4.8 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains a reserved field. All Infocfield fields denoted reserved are reserved for future use.

192.4.2.4.9 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 192–30. After initialization, the switch is set to CRCgen, as shown in Figure 192–30, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order shown, first S15, followed by S14, and so on, until the final value S0. The 16 delay elements shown in Figure 192–30 shall be initialized to zero.

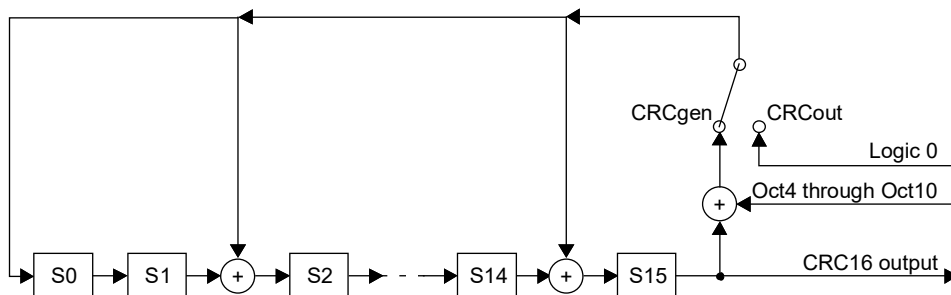


Figure 192–30—CRC16

192.4.2.4.10 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 192–19. Mapping of MDIO status variables to PMA status variables is shown in Table 192–20.

Table 192–19—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1 PMA control register	1.2309.14	PMA_transmit_disable

Table 192–20—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1 PMA status register	1.2310.1	PMA_receive_fault

192.4.2.4.11 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 192–31. The management parameter config is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

Upon entry to the TRAINING0 state, the first symbol of the Follower's transmit PMA training frame at the transmit MDI shall be aligned so that it is 400 ± 1 transmit symbols after the arrival of the last PMA training payload symbol from the Leader at the Follower input MDI. The Follower shall maintain this alignment while in the TRAINING0 and COUNTDOWN0 (i.e., while `tx_mode = SEND_TS`) states. The PHY burst count communicated by the Follower should match the PHY burst count communicated by the Leader during the previous PMA training frame.

In the TRAINING0 state, PAM2 transmission is used and PHY capabilities and `delay_count` are exchanged using Infocfields as specified in 192.4.2.4.5. The final negotiated data rate mode is determined by the Leader. The Leader and Follower transition from TRAINING0 state to COUNTDOWN0 state if `loc_rcvr_status` and `rem_rcvr_status` are both OK, and `negotiation_done` is OK.

If the local receiver status (indicated by `loc_rcvr_status`) transitions to NOT_OK during any COUNTDOWN or PCS_TEST state, then PHY Control returns to the SILENT state and attempts a retrain.

When entering the TRAINING1 state, the Follower shall use the Leader transmitted `delay_count` to align its transmit PMA training frame to be $176 \text{ ns} - \text{delay\_count} \times 5.333 \text{ ns}$ ($\pm 5.333 \text{ ns}$) after the last PMA training payload symbol from the Leader appears on the Follower input MDI. The Follower shall maintain this alignment while `tx_mode` is SEND_TA or SEND_N.

The `link_fail_inhibit_timer` value is defined to be 97.5 ms. It is used to force a restart if the link up cannot be achieved within the maximum allowed time.

The COUNTDOWN0 state synchronizes the link partner's transition from symmetric training TDD bursts (SEND_TS) to asymmetric training TDD bursts (SEND_TA) in the TRAINING1 state. The TRAINING1 state then waits until both local and remote receivers settle and signal that their status is OK, before transitioning to COUNTDOWN1. The PCS is tested after completion of COUNTDOWN1. If the link is reliable as indicated by block lock and the RS-FEC error rate, then the PHY Control transitions to PCS_DATA and begins transferring data.

192.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive link and communicates it via the variable `link_status`. Failure of the underlying receive link causes the PMA to set `link_status` to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the link.

The Link Monitor function shall comply with the state diagram of Figure 192–33.

Upon power on reset, or release from power down, the PHY sets `link_enable = DISABLE`. During this period, `link_status = FAIL` is asserted. When the PHY `link_enable` is set to ENABLE, the Link Monitor state diagram begins monitoring the PMA. As soon as reliable transmission is achieved, with `pcs_data_mode = TRUE`, the variable `link_status = OK` is asserted, upon which further PHY operations can take place.

192.4.2.6 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 192.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by `recovered_clock` for use when the management parameter `config` is set to FOLLOWER.

192.4.3 MDI

Communication through the MDI is summarized in 192.4.3.1 and 192.4.3.2.

192.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The transmit path uses PAM2 for all refresh headers and during RS-FEC frame transmission for 100 Mb/s, 2.5 Gb/s or 5 Gb/s. The transmit path uses PAM3 for the 7.5 Gb/s RS-FEC frame transmission. The transmit path uses PAM4 for the 10 Gb/s RS-FEC frame transmission. PMA Transmit generates a pulse-amplitude modulated signal in the form shown in Equation (192–14).

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT) \quad (192-14)$$

In Equation (192–14), a_n is the PAM4 modulation symbol from the set $\{-1, -1/3, +1/3, +1\}$, the PAM3 modulation symbol from the set $\{-1, 0, +1\}$, or the PAM2 modulation symbol from the set $\{-1, +1\}$ to be transmitted at time nT , and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 192.5.2.

192.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as shown in Equation (192–15).

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t) \quad (192-15)$$

In Equation (192–15) $h_R(t)$ denotes the symbol response of the overall impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

192.4.4 State variables

192.4.4.1 State diagram variables

block_lock

See 192.3.5.1.2. This variable is passed to the PMA via the block_lock parameter of the PMA_PCSSYNC.request primitive.

config

This variable takes the value of the management parameter config based on the value of bit 1.2100.14 (see 45.2.1.214) and specifies to the PHY functions whether the PHY operates as the Leader or Follower.

Values:

LEADER: This value is continuously asserted when the PHY operates as the Leader.

FOLLOWER: This value is continuously asserted when the PHY operates as the Follower.

detect_lp_burst

A Boolean variable indicating whether symbols (either PAM2, PAM3, or PAM4) of a TDD burst have been detected.

Values:

TRUE: TDD PAM2, PAM3, or PAM4 symbols are detected.

FALSE: PMA detects the Z symbols after the PAM2/PAM3/PAM4 burst has ended (PMA could use timer timeout to terminate this detection signal).

hi_rfer	1
See 192.3.5.1.2. This variable is passed to the PMA via the hi_rfer parameter of the PMA_PCSSYNC.request primitive.	2
	3
	4
link_enable	5
This variable is set by management or default to enable or disable the PHY. It is set to disable the link upon power on reset or release from power down (see 192.4.2.5). Transition to ENABLE initiates PHY Control and the Link Monitor state diagram.	6
Values:	7
ENABLE: Enable operation of the PHY.	8
DISABLE: Disable the transmitter and await initiation of training.	9
	10
	11
	12
link_status	13
The link_status parameter set by PMA Link Monitor state diagram.	14
Values:	15
OK: The Link Monitor function indicates that a valid MultiGBASE-A link is established. Reliable reception of signals transmitted from the remote PHY is possible.	16
FAIL: No valid link established.	17
	18
	19
	20
loc_countdown_done	21
This variable is only used by the Leader. It indicates that the Leader has finished sending the last Leader countdown Infofield and received the responding (last) Infofield from the Follower at the current TRAINING stage.	22
Values:	23
TRUE: The Leader has sent its last burst ($BC24 = PhaseSwBC24 - 1$) and received the last burst from the Follower, as indicated by the received InfoField since the latest entry to a TRAINING state.	24
FALSE: The Leader has not sent its last burst ($BC24 = PhaseSwBC24 - 1$) or has not received the last burst from the Follower, as indicated by the received InfoField since the latest entry to a TRAINING state.	25
	26
	27
	28
	29
	30
	31
	32
loc_rcvr_status	33
See 192.2.1.6.	34
	35
negotiation_done	36
During symmetric training phase, after loc_rcvr_status = OK, the Leader and Follower exchange capabilities, delay_count and negotiated data rate, and then set the negotiation_done variable to OK.	37
Values:	38
OK: Negotiation is done, can move to COUNTDOWN0 state.	39
NOT_OK: Negotiation is not done, stay in TRAINING0 state.	40
	41
	42
	43
pcs_data_mode	44
See 192.2.1.8.1.	45
	46
pma_reset	47
Allows reset of all PMA functions. It is set by PMA Reset.	48
Values: ON or OFF.	49
	50
	51
	52
	53
	54

PMA_state	1
Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.	2
Values:	3
00: TRAINING state.	4
01: COUNTDOWN state.	5
	6
rem_countdown_done	7
This variable is only used by the Follower. It indicates that the Follower has finished receiving the last Infofield from the Leader at the current TRAINING stage, and has sent at least one Infofield.	8
Values:	9
TRUE: The Follower has received the last burst (BC24 = PhaseSwBC24 – 1) sent by the Leader and has sent at least one InfoField since the latest entry to a TRAINING state.	10
FALSE: The Follower has not received the last burst (BC24 = PhaseSwBC24 – 1) sent by the Leader or has not sent at least one InfoField since the latest entry to a TRAINING state.	11
	12
	13
	14
	15
	16
	17
rem_rcvr_status	18
The status of the link partner's receiver indicated in the loc_rcvr_status received in the InfoField from the remote PHY. See 192.2.1.7.1.	19
	20
	21
training_active	22
A Boolean variable indicating whether the link_fail_inhibit_timer has started.	23
Values:	24
TRUE: The link_fail_inhibit_timer is running and the link is in a training phase.	25
FALSE: The link is not currently in a training phase.	26
	27
training_phase	28
This variable indicates whether training is currently in the symmetric mode or the asymmetric mode of training. It is transmitted to the link partner in the InfoField. See 192.4.2.4.4.	29
Values:	30
00: PHY Control is currently in either in a silent mode or a symmetric training phase.	31
01: PHY Control is currently in an asymmetric training phase.	32
	33
	34
tx_mode	35
See 192.2.1.1.	36
	37
192.4.4.2 Timers	38
	39
link_fail_inhibit_timer	40
A timer used to determine the maximum amount of time the PHY Control sets training_active = TRUE. The timer shall expire 97.5 ms ± 0.5 ms after being started.	41
	42
	43
minwait_timer	44
A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING1, and PCS_TEST states. The timer shall expire 975 μs ± 50 μs after being started.	45
	46
	47
tdd_watchdog_timer	48
A timer used to determine that the TDD signal has not been detected within the last ten TDD cycles. The timer shall expire 96 μs ± 5 μs after being started.	49
	50
	51
192.4.5 State diagrams	52
	53
The PHY Control state diagram is shown in Figure 192–31 and Figure 192–32.	54

The Link Monitor state diagram is shown in Figure 192–33.

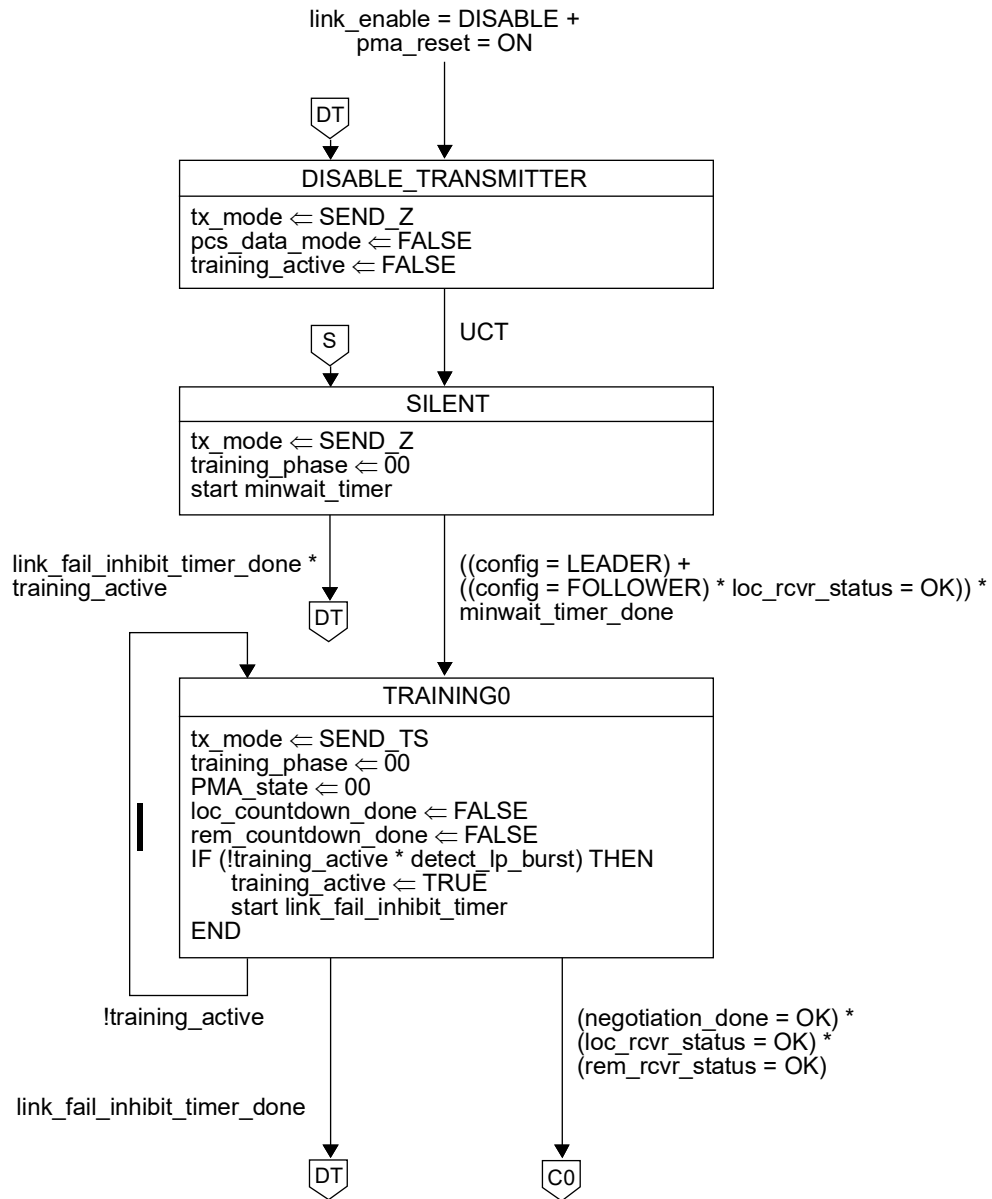


Figure 192–31—PHY Control state diagram, part a

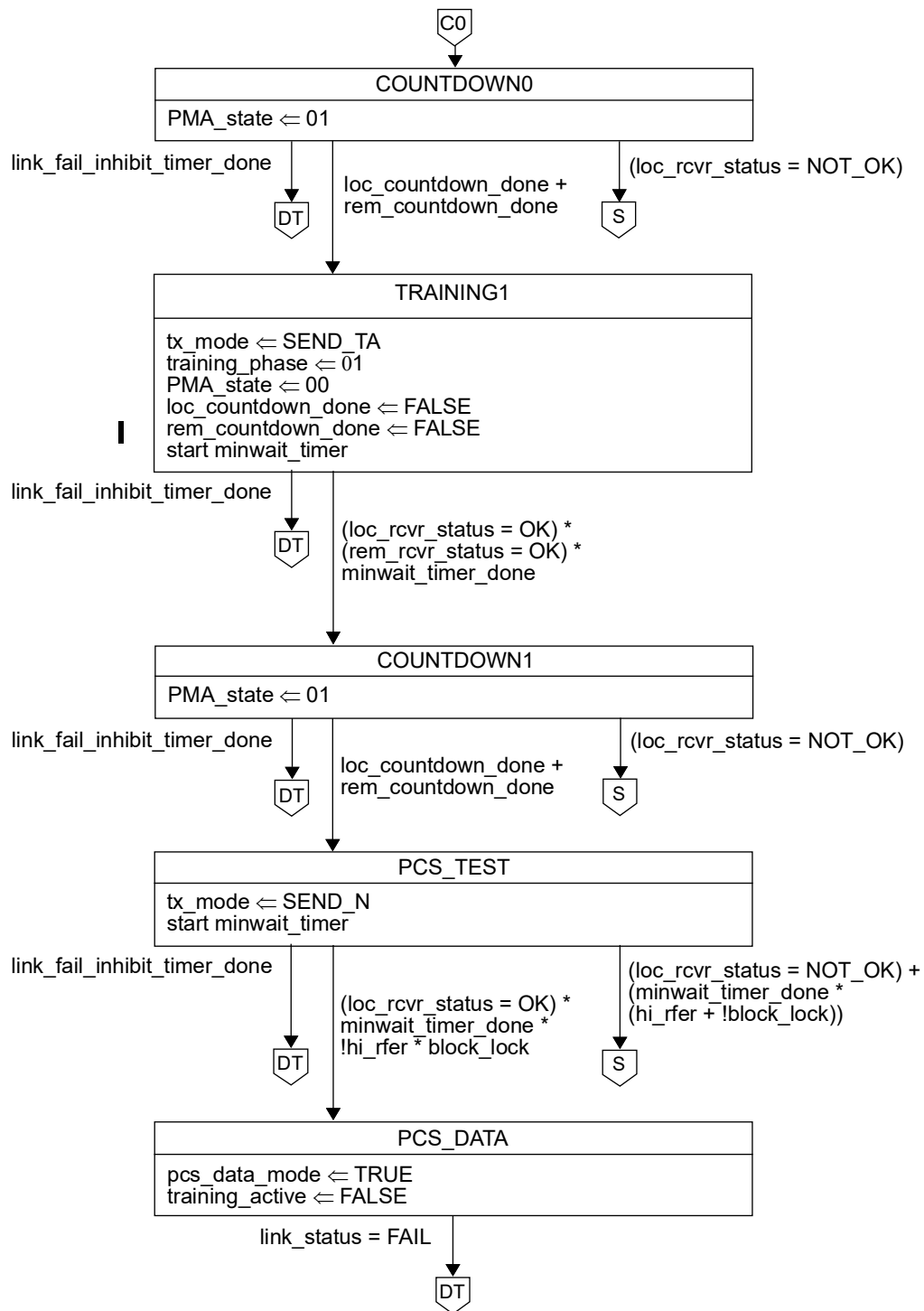


Figure 192–32—PHY Control state diagram, part b

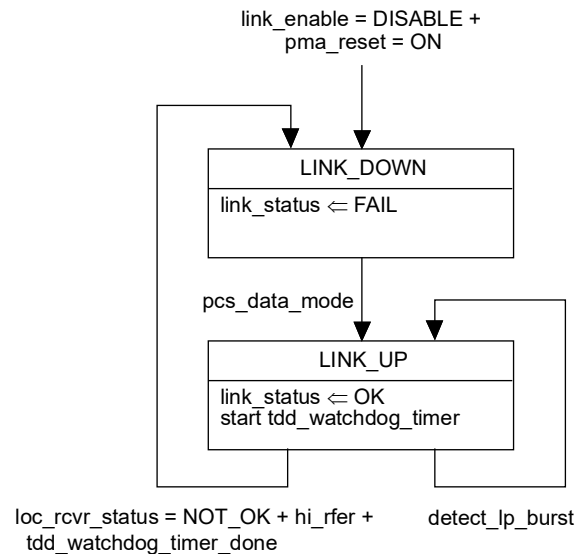


Figure 192–33—Link Monitor state diagram

192.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

192.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 192–21. If MDIO is not implemented, then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of non-test mode operation.

Test mode 1 enables testing of timing jitter on the Leader and Follower transmitters. The Leader and Follower PHYs are connected over a link segment defined in 192.7 or 192.8. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5. TX_TCLK_187.5 is equal to 187.5 MHz and is a divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in Leader timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous repeating pattern of $\{+1, -1\}$ symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference.

Table 192–21—MDIO management registers settings for test modes

Register value	Register description
000	Non-test mode operation
001	Test mode 1—Setting Leader and Follower PHYs for transmit clock jitter test in linked mode
010	Test mode 2—Transmit MDI jitter test in Leader mode
011	Test mode 3—Reserved
100	Test mode 4—Transmitter distortion test
101	Test mode 5—Continuous idle payload transmission (for the PSD Mask test)
110	Test mode 6—Transmitter droop test mode
111	Test mode 7—Data mode with zero data pattern (for BER monitoring)

Test mode 4 is for transmitter distortion testing. When test mode 4 is enabled in PAM2 mode (i.e., 100 Mb/s, 2.5 Gb/s, or 5 Gb/s transmit MAC data rate), the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ (see Figure 192–5 and Figure 192–6). All PHYs shall support transmission of this signal at 3 GBd. PHYs that support 5 Gb/s, 7.5 Gb/s, and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM3 mode (i.e., 7.5 Gb/s transmit MAC data rate), the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ (see Figure 192–6). PHYs that support 7.5 Gb/s transmit rate shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM4 mode (i.e., 10 Gb/s transmit MAC data rate), the PHY shall transmit the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ and $B_n = Scr_n[3] \oplus Scr_n[8]$ (see Figure 192–6). PHYs that support 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

$$g(x) = 1 + x^9 + x^{11} \quad (192-16)$$

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit continuously with no QUIET period or refresh header and with transmit signal level corresponding to the data mode of operation. The PCS Transmit will encode data as when tx_mode = SEND_N, and as if continuously receiving idle control characters from the XGMII. The test applies to both the Leader and Follower. The clock is sourced from a stable clock with 100 ppm accuracy for this test.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the non-test mode with zero data pattern. Instead of encoding data received from the MAC, the input to the RS-FEC is all-zero message symbols and the continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

192.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 192–34, Figure 192–35, and Figure 192–36, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

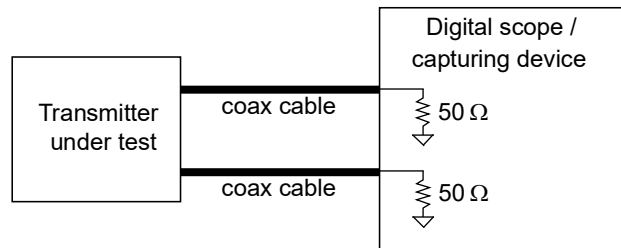


Figure 192–34—Transmitter test fixture 1 for -T1 transmitter droop, transmitter distortion, power spectral density, transmit power level, and MDI jitter

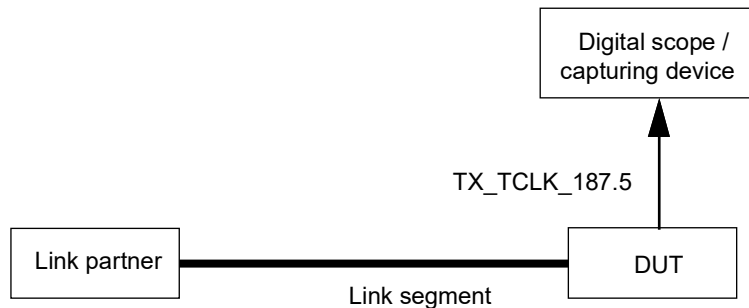


Figure 192–35—Transmitter test fixture 2 for -T1 and -V1 Leader and Follower clock jitter measurement

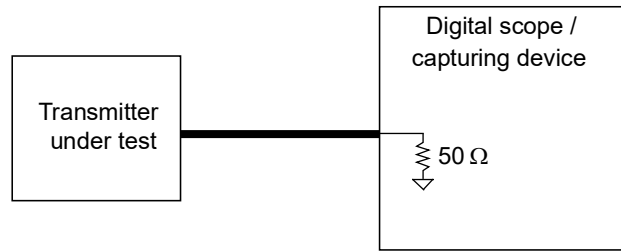


Figure 192-36—Transmitter test fixture 3 for -V1 transmitter droop, transmitter distortion, power spectral density, transmit power level, and MDI jitter measurements

192.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 192.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be ac-coupled (i.e., it presents a high dc common-mode impedance at the MDI). There may be various methods for ac-coupling in actual implementations.

When a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of $\pm 0.1\%$.

192.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using transmitter test fixture 1 (see Figure 192-34) or test fixture 3 (see Figure 192-36), the magnitude of both the positive and negative droop shall be less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing.

192.5.2.2 Transmitter distortion

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 1 (see Figure 192-34) or transmitter test fixture 3 (see Figure 192-36) as appropriate to the MDI.

The peak distortion is determined by sampling the signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signals shall be at least 4000 transmitted symbols long and be sampled with a minimum of 10x oversampling. The transmit baud rate may be reduced to 1 Gbd by repeating the symbols using the same clock edge as in the data mode of operation.

The peak distortion values, measured at a minimum of ten equally spaced phases of a single symbol period, shall be less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM3 and PAM4 transmitters.

```

% Post processing pseudo-code for transmitter distortion
clear
Ns=2^11-1; % Scrambler length
Nc=70; % Canceller length
  
```

```

Modulation=2; % Choices are 2 for PAM2, 3 for PAM3, or 4 for PAM4

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
    scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% Generate tm4 (test mode 4) for a given modulation
if Modulation==2
    tm4=2*scr-1;
elseif Modulation==3
    tm4=ones(Ns,1);
    map=[-1 -1;-1 0;0 -1;1 -1;0 1;-1 1;1 1;1 0];
    scr3=[scr, circshift(scr,1), circshift(scr,2)];
    data = 4*scr3(:,3)+ 2*scr3(:,2)+scr3(:,1);
    for n=1:length(data)
        tm4([2*n-1,2*n]) =map(data(n)+1,:);
    end
elseif Modulation==4
    tm4=ones(Ns,1);
    map=[-1;-1/3;1/3];
    DS=[scr,mod(circshift(scr,3) + circshift(scr,8),2)];
    data = 2*DS(:,1)+DS(:,2);
    for n=1:length(DS)
        tm4(n) =map(data(n)+1);
    end
else
    disp('Error: The code supports either PAM2, PAM3, or PAM4')
    return
end

% Test mode4 matrix
for i=1:Nc
    X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file

% Minimum of 4K Tx symbols, 10X oversampling, high resolution capture
fid=fopen('TestMode4.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF at Nyquist
[A,B]=butter(1,1/10,'low');
tx=filter(A,B,tx);

% HPF (with this HPF, the 70-tap canceller residual linear error is 0.00
tx = filter([1,-1],[1,-0.98],tx);

% Select one period, 10x oversampling, a row vector
tx=tx((1:Ns*10)+2e3)'; % removes HPF transients

% Level normalization
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10

```

```

tx1=tx(n:10:end);
temp=xcorr(tx1,tm4); % Align data and test pattern
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);
coef=tx1/X; % Compute coefficients that minimize squared error in a cyclic
    block
err=tx1-coef*X; % Linear canceller
dist(n) = max(abs(err)); % Peak distortion
SNR(n)=std(tx)/std(err); % SNR
End

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist

```

192.5.2.3 Transmitter timing jitter and jitter at the MDI

The following measurements are performed for a PHY in Leader mode:

- 1) The RMS jitter for jitter frequencies greater than 100 kHz measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1 shall be less than 1 ps when supporting 10 Gb/s, 1.5 ps when supporting 7.5 Gb/s, 2 ps when supporting 5 Gb/s, and 4 ps when supporting 2.5 Gb/s.
- 2) Peak-to-peak of Time Interval Error measured in test mode 1 using test fixture 2 over a period of 100 μ s shall be less than 10 ps when supporting 10 Gb/s, 15 ps when supporting 7.5 Gb/s, 20 ps when supporting 5 Gb/s, and 40 ps when supporting 2.5 Gb/s.

The following measurements are performed using test fixture 2 (see Figure 192–35) for a PHY in Follower mode:

- 1) The RMS jitter for jitter frequencies greater than 1 MHz measured in test mode 1 shall be less than 1 ps when supporting 10 Gb/s, 1.5 ps when supporting 7.5 Gb/s, 2 ps when supporting 5 Gb/s, and 4 ps when supporting 2.5 Gb/s.
- 2) Peak-to-peak of Time Interval Error over any period of 10 μ s measured in test mode 1 over 50 overlapping periods of 10 μ s each shall be less than 15 ps for 10 Gb/s, 22.5 ps when supporting 7.5 Gb/s, 30 ps for 5 Gb/s, and 60 ps for 2.5 Gb/s. The overlapping period of 5 μ s is assumed.

192.5.2.4 Transmitter power spectral density (PSD) and power level

Transmitter power spectral density (PSD) and power level measurements are performed in test mode 5. The measured transmit power shall be in the range specified in Table 192–22 when using the same test fixture as used for PSD measurement. When the value of tx_symb is Z, the transmit signal at the MDI is nominally zero and the transmit signal shall be less than -36 dBm for frequencies greater 10 MHz.

The power spectral density of the transmitter of -T1, measured into a 100 Ω differential load using test fixture 1 (see Figure 192–34), shall be between the upper PSD mask specified in Equation (192–17) and the lower PSD mask specified Equation (192–18).

The upper and lower masks for each MAC data rate are shown in Figure 192–37, Figure 192–38, Figure 192–39, and Figure 192–40. See Table 192–2 for the definition of S . See Table 192–23 for the definition of PSD mask K factor.

Table 192–22—Power levels

Transmit MAC data rate	MDI, -T1		MDI, - V1	
	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
100 Mb/s	0	2	−3	−1
2.5 Gb/s	0	2	−3	−1
5 Gb/s	2	4	−1	1
7.5 Gb/s	1	3	−2	0
10 Gb/s	0	2	−3	−1

Table 192–23—PSD mask K factor

Transmit MAC data rate	K
100 Mb/s	0
2.5 Gb/s	0
5 Gb/s	0
7.5 Gb/s	1
10 Gb/s	2

$$UpperPSD(f) = \begin{cases} -89 - K & \text{dBm/Hz} & 40 < f \leq 1200 \times S \\ -87 - K - \frac{f}{600 \times S} & \text{dBm/Hz} & 1200 \times S < f \leq 3000 \times S \\ -80 - K - \frac{f}{250 \times S} & \text{dBm/Hz} & 3000 \times S < f \leq 5000 \times S \end{cases} \quad (192-17)$$

$$LowerPSD(f) = \begin{cases} -93 - K & \text{dBm/Hz} & 40 < f \leq 600 \times S \\ -92 - K - \frac{f}{600 \times S} & \text{dBm/Hz} & 600 \times S < f \leq 2400 \times S \\ -86.4 - K - \frac{f}{250 \times S} & \text{dBm/Hz} & 2400 \times S < f \leq 3500 \times S \end{cases} \quad (192-18)$$

where

f is the frequency in MHz

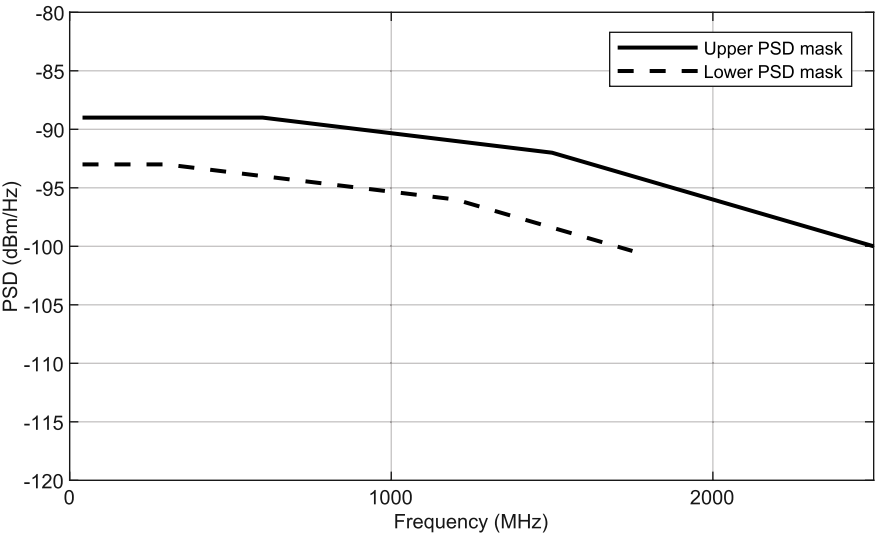


Figure 192-37—Transmitter Power Spectral Density for 100 Mb/s and 2.5 Gb/s MAC data rates, upper and lower masks

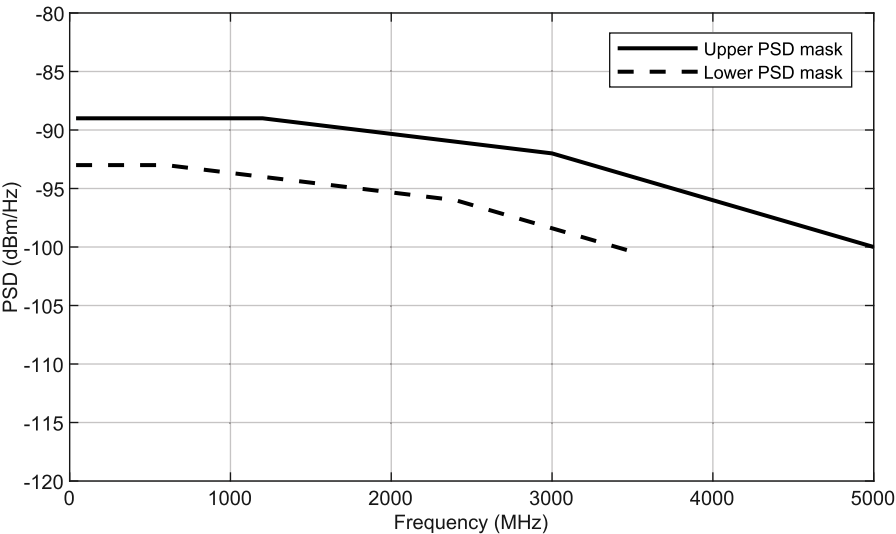


Figure 192-38—Transmitter Power Spectral Density for 5 Gb/s MAC data rate, upper and lower masks

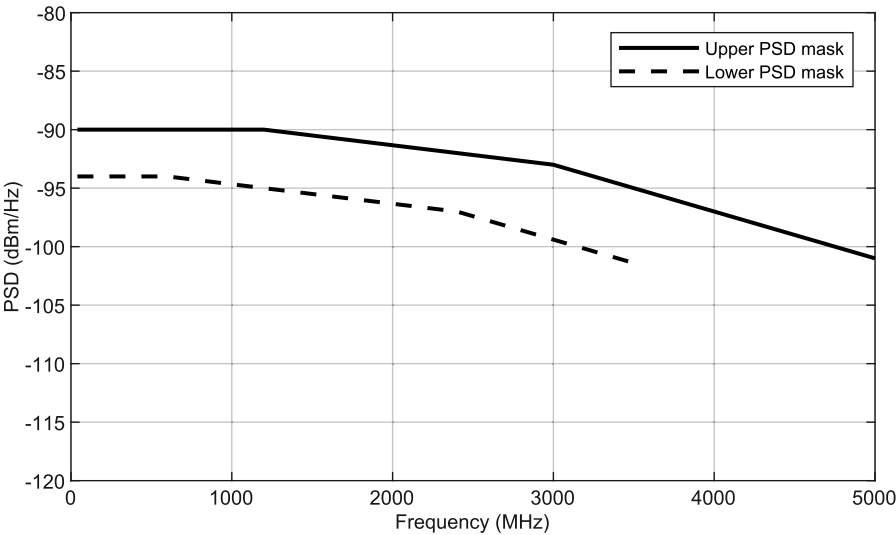


Figure 192-39—Transmitter Power Spectral Density for 7.5 Gb/s MAC data rate, upper and lower masks

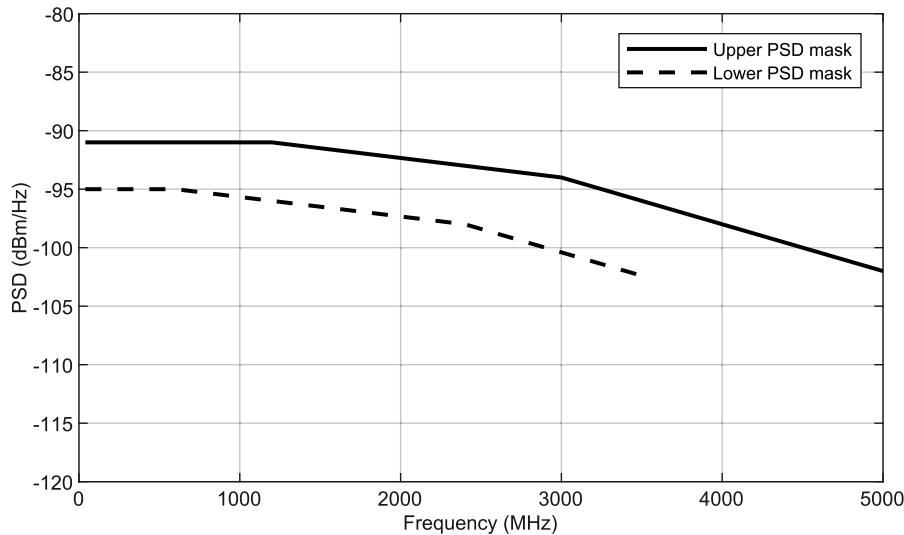


Figure 192-40—Transmitter Power Spectral Density for 10 Gb/s MAC data rate, upper and lower masks

For the power spectral density of -V1, with single ended termination of 50 Ω load and test fixture 3 (see Figure 192-36), both upper and lower PSD Masks are lower by 3 dB from Equation (192-17), Equation (192-18), Figure 192-37, Figure 192-38, Figure 192-39 and Figure 192-40.

192.5.2.5 Transmitter peak output

The transmit differential signal at the -T1 MDI should be less than the peak-to-peak values specified in Table 192–24 when measured with a 100 Ω termination. The transmit signal at the -V1 MDI should be less than the peak-to-peak values specified in Table 192–24 when measured with a 50 Ω termination. The limits in this clause apply to all transmitted symbol sequences, including SEND_N, SEND_TS, and SEND_TA.

Table 192–24—Transmitter peak-to-peak output

Transmit MAC data rate	-T1 MDI peak-to-peak output (V)	-V1 MDI peak-to-peak output (V)
100 Mb/s	1.3	0.65
2.5 Gb/s	1.3	0.65
5 Gb/s	1.5	0.75
7.5 Gb/s	1.5	0.75
10 Gb/s	1.7	0.85

192.5.2.6 Transmitter clock frequency

When using a local timing reference, the symbol transmission rate shall be within the range $6 \times S \text{ Gb/s} \pm 100 \text{ ppm}$ with drift less than 1 ppm/sec.

When the Follower is using a recovered timing reference, the symbol transmission rate (scaled by S) shall be within $\pm 10 \text{ ppm}$ of the recovered clock.

192.5.3 Receiver electrical specifications

The PMA provides the Receive function specified in 192.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 192.7 or 192.8.

192.5.3.1 Receiver input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 192.5.2 and have passed through a link specified in 192.7 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link_status = OK.

Single-ended signals received at the MDI that were transmitted from a remote transmitter within the specifications of 192.5.2 and have passed through a link specified in 192.8 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link_status = OK.

This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

192.5.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver's tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 192–25. The minimum noise frequency is 10 MHz. The -T1 receive DUT is connected to the noise source through a directional coupler with a -T1 link segment (see 192.7) as shown in Figure 192–41. The -V1 receive DUT is connected to the noise source through a directional coupler with a -V1 link segment (see 192.8) as shown in Figure 192–42. The BER is expected to be less than 10^{-12} , and to satisfy this specification, the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

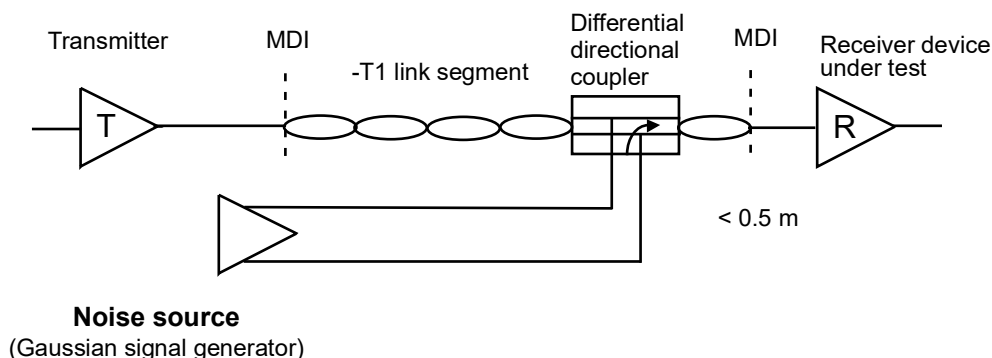


Figure 192–41—Broadband stationary noise rejection test setup, -T1

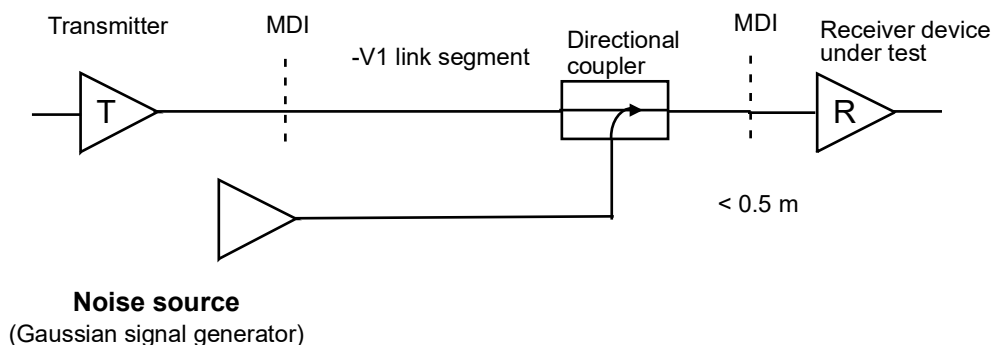


Figure 192–42—Broadband stationary noise rejection test setup, -V1

Table 192–25—Broadband stationary noise source, high speed data rate

Transmit MAC data rate	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)	
		-T1	-V1
2.5 Gb/s	1750	–140	–143
5 Gb/s	3500	–144	–147
7.5 Gb/s	3500	–146	–149
10 Gb/s	3500	–148	–151

192.6 Management interface

MultiGBASE-A makes extensive use of the management functions that may be provided by the optional MDIO (see Clause 45).

192.7 Link segment characteristics, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. -T1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

192.7.1 Link transmission parameters

The transmission characteristics for a -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

192.7.1.1 Insertion loss

The insertion loss of a -T1 link segment shall meet the values determined using Equation (192–19).

$$\text{Insertion loss}(f) \leq 0.322\sqrt{f} + 0.0019f + \frac{1}{\sqrt{f}} \quad (\text{dB}) \quad (192-19)$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–19) is plotted in Figure 192–43, which is provided for information only.

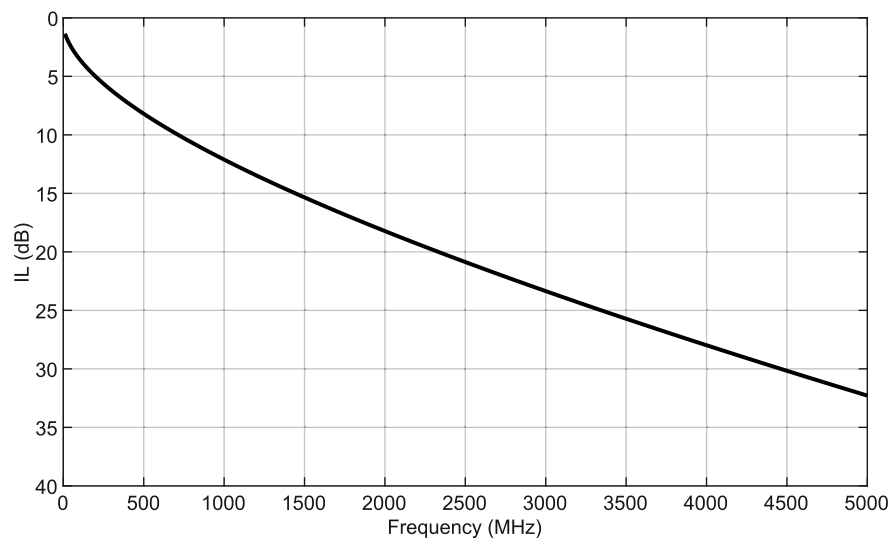


Figure 192–43—T1 link segment insertion loss

192.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of a -T1 link segment is 100 Ω .

192.7.1.3 Return loss

The return loss of a -T1 link segment shall meet the values determined using Equation (192–20).

$$RL(f) \geq \left\{ \begin{array}{ll} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left(\frac{f-500}{1500}\right) & 500 \leq f < 2000 \\ 9.5 - 3\left(\frac{f-2000}{2500}\right) & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{array} \right\} \text{ (dB)} \quad (192-20)$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–20) is plotted in Figure 192–44, which is provided for information only.

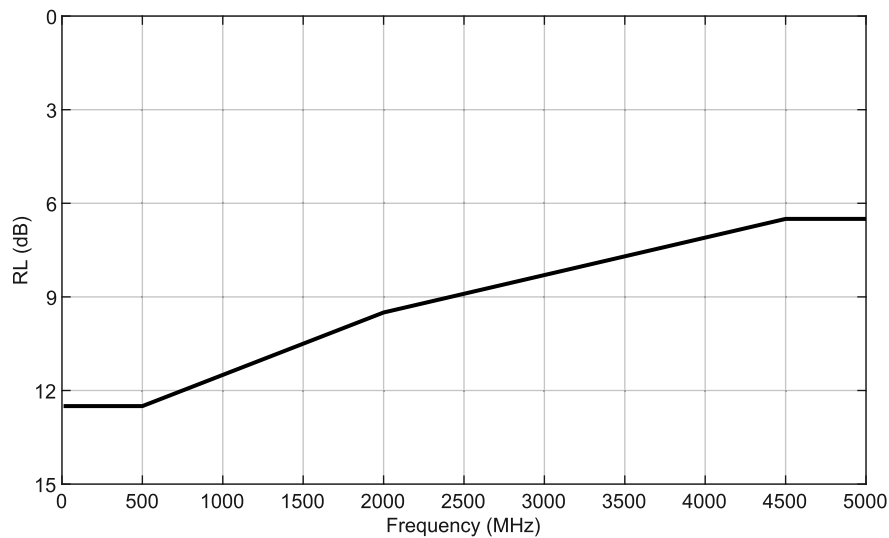


Figure 192–44—T1 link segment return loss

192.7.1.4 Coupling attenuation

The coupling attenuation of a -T1 link segment shall be as specified in 149.7.1.4.

192.7.1.5 Screening attenuation

The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5, where $F_{max} = 4000$ MHz.

192.7.1.6 Maximum link delay

The propagation delay of a -T1 link segment shall not exceed 160 ns for all frequencies between 10 MHz and 5 GHz.

192.7.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in [Annex 97B](#).

192.7.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -T1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -T1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–21).

$$\text{PSANEXT}(f) = -10\log_{10} \sum_{j=1}^m 10^{\frac{-\text{AN}(f)_j}{10}} \text{ dB} \quad (192-21)$$

where the function $\text{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -T1 link segment j (1 to m) for the disturbed -T1 link segment.

The PSANEXT loss between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (192–22).

$$\text{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad (\text{dB}) \quad (192-22)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–29) is plotted in Figure 192–45, which is provided for information only.

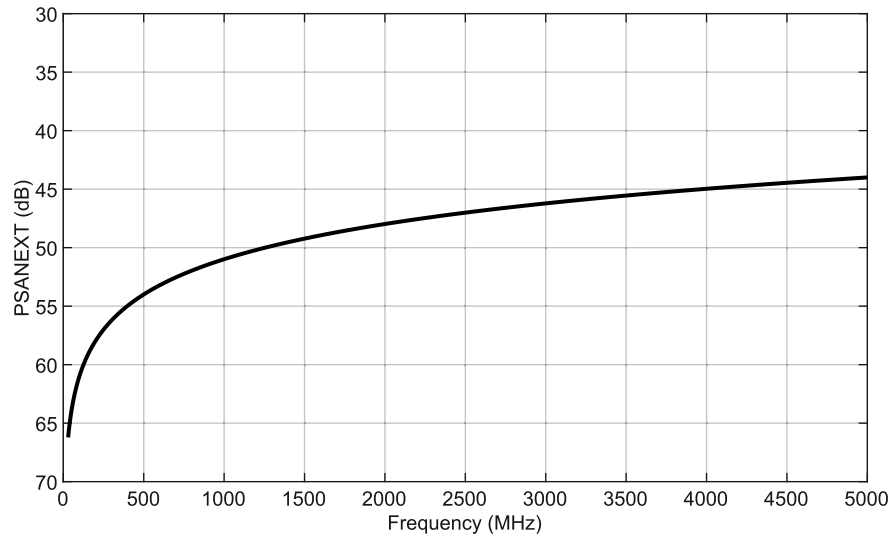


Figure 192–45—T1 link segment PSANEXT loss

192.7.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -T1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -T1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–23).

$$\text{PSAACRF}(f) = \left(-10 \log_{10} \sum_{j=1}^m 10^{\frac{-\text{AFEXT}(f)_j}{10}} \right) - \text{IL}_d(f) \quad \text{dB} \quad (192-23)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$
 $\text{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -T1 link segment j (1 to m) to the disturbed -T1 link segment in dB
 $\text{IL}_d(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (192–24).

$$\text{PSAACRF}(f) \geq 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad (\text{dB}) \quad (192-24)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–31) is plotted in Figure 192–46, which is provided for information only.

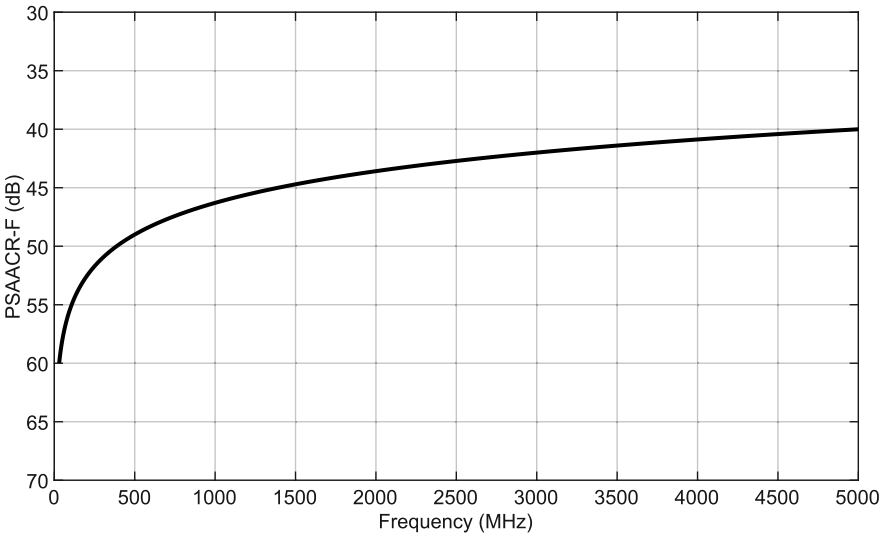


Figure 192–46—T1 link segment PSAACRF

192.8 Link segment characteristics, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial cable (-V1) that meet the requirements specified in this subclause. -V1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

192.8.1 Link transmission parameters

The transmission characteristics for a -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

192.8.1.1 Insertion loss

The insertion loss of a -V1 link segment shall meet the values determined using Equation (192–25).

$$\text{Insertion loss}(f) \leq 0.3 + 0.345\sqrt{f} + 0.000825f + \frac{0.48}{\sqrt{f}} \quad (\text{dB}) \quad (192-25)$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–25) is plotted in Figure 192–47, which is provided for information only.

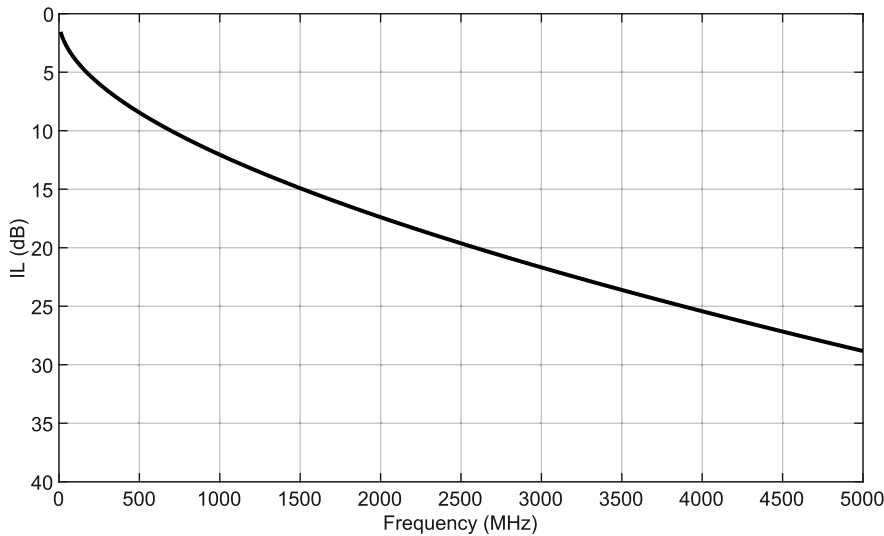


Figure 192–47—V1 link segment insertion loss

192.8.1.2 Single ended characteristic impedance

The nominal characteristic impedance of a -V1 link segment is 50 Ω.

192.8.1.3 Return loss

The return loss of a -V1 link segment shall meet the values determined using Equation (192–26).

$$RL(f) \geq \left\{ \begin{array}{ll} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left(\frac{f-500}{1500}\right) & 500 \leq f < 2000 \\ 9.5 - 3\left(\frac{f-2000}{2500}\right) & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{array} \right\} \text{ (dB)} \quad (192-26)$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–26) is plotted in Figure 192–48, which is provided for information only.

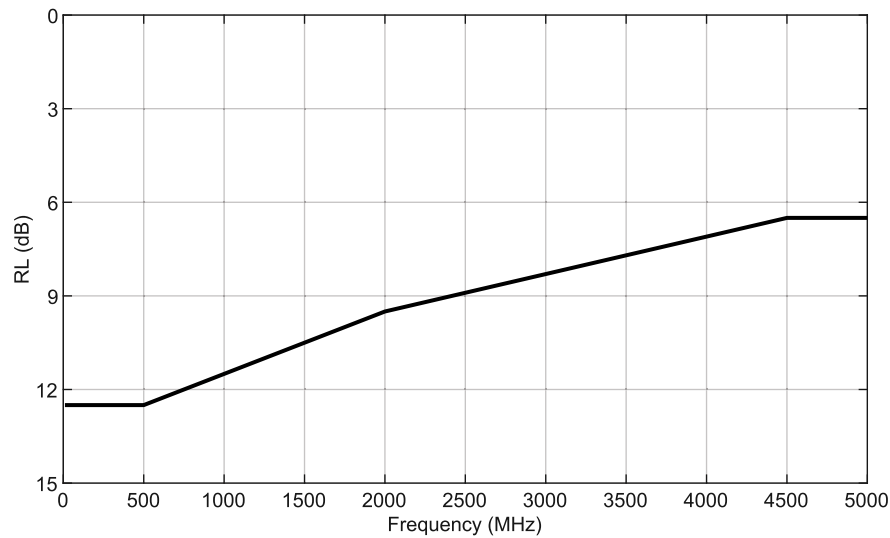


Figure 192–48—V1 link segment return loss

192.8.1.4 Coupling attenuation

Coupling attenuation is not defined for -V1 link segments.

192.8.1.5 Screening attenuation

The screening attenuation of a -V1 link segment shall meet the values determined using Equation (192–27). Screening attenuation is tested as specified in IEC 62153-4-7 using the triaxial tube-in-tube method.

$$\text{Screening attenuation}(f) \geq \begin{cases} 55 & 30 \leq f < 1000 \\ 50 & 1000 \leq f \leq 3000 \\ 45 & 3000 \leq f \leq 4000 \end{cases} \text{ (dB)} \quad (192-27)$$

where

f is the frequency in MHz; $30 \leq f \leq 4000$

Equation (192–27) is plotted in Figure 192–49, which is provided for information only.

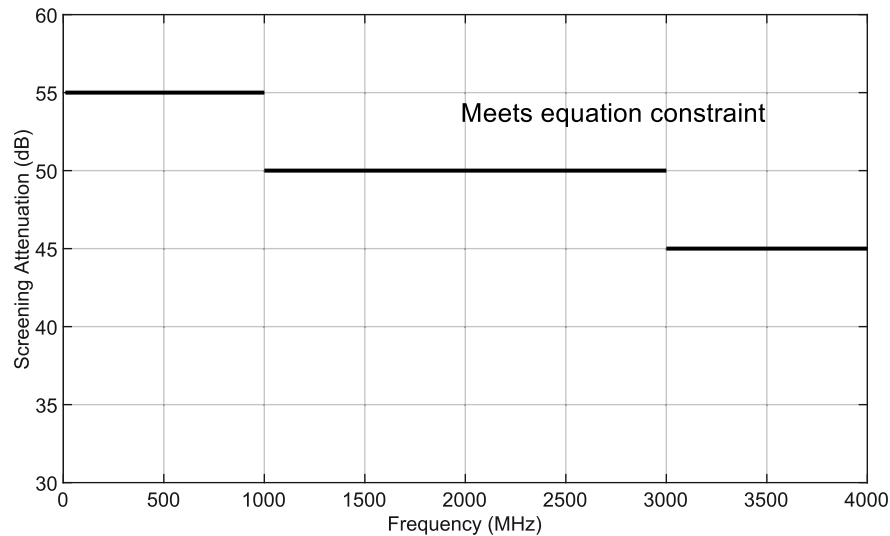


Figure 192–49—V1 link segment screening attenuation

192.8.1.6 Maximum link delay

The propagation delay of a -V1 link segment shall not exceed 160 ns for all frequencies between 10 MHz and 5 GHz.

192.8.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as alien crosstalk noise. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B. These methodologies shall be applied with adaptation to unbalanced coaxial cabling and shall use a single 50 Ω termination to ground.

192.8.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -V1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -V1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–28).

$$\text{PSANEXT}(f) = -10\log_{10} \sum_{j=1}^m 10^{\frac{-\text{AN}(f)_j}{10}} \text{ dB} \quad (192-28)$$

where the function $\text{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -V1 link segment j (1 to m) for the disturbed -V1 link segment.

The PSANEXT loss between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (192–29).

$$\text{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad (\text{dB}) \quad (192-29)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–29) is plotted in Figure 192–50, which is provided for information only.

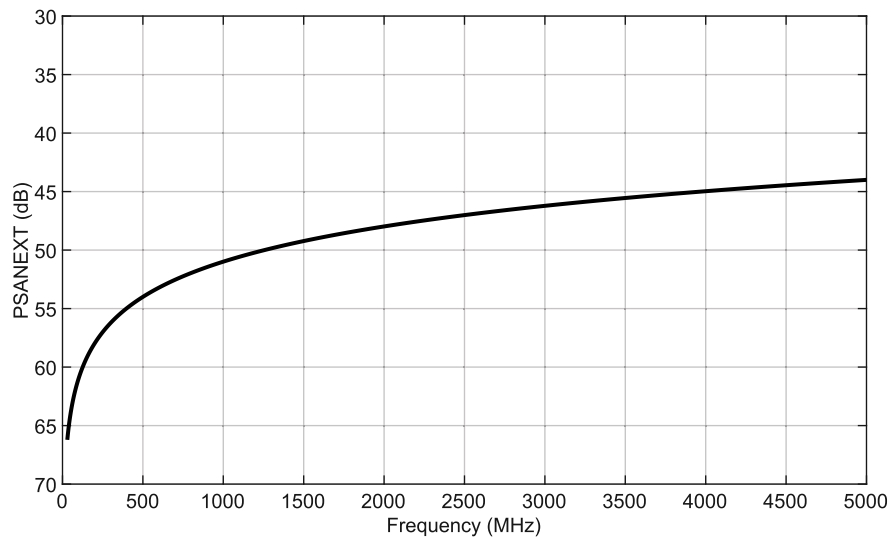


Figure 192–50—V1 link segment PSANEXT loss

192.8.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -V1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -V1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–30).

$$\text{PSAACRF}(f) = \left(-10 \log_{10} \sum_{j=1}^m 10^{\frac{-\text{AFEXT}(f)_j}{10}} \right) - \text{IL}_d(f) \quad \text{dB} \quad (192-30)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$
 $\text{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -V1 link segment j (1 to m) to the disturbed -V1 link segment in dB
 $\text{IL}_d(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (192–31).

$$\text{PSAACRF}(f) \geq 51 - 9 \log_{10} \left(\frac{f}{300} \right) \quad (\text{dB}) \quad (192-31)$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–31) is plotted in Figure 192–51, which is provided for information only.

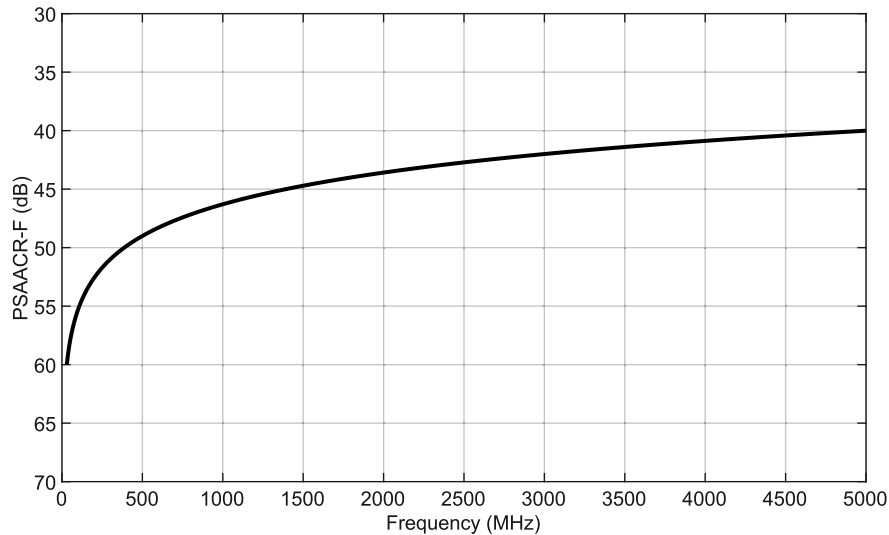


Figure 192–51—V1 link segment PSAACRF

192.9 MDI specification, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

192.9.1 MDI connectors

The -T1 MDI connectors are as specified in 149.8.1.

192.9.2 MDI electrical specification

The electrical requirements specified in 192.5.2 and 192.5.3 shall be met when the PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors.

192.9.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -T1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (192–32). For the -T1 MDI, a nominal differential characteristic impedance of 100 Ω is used.

$$MDI\_Return\_Loss(f) \geq \left\{ \begin{array}{ll} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < F_{max} \end{array} \right\} \text{ (dB)} \quad (192-32)$$

where

f is the frequency in MHz; $10 \leq f \leq F_{max}$
 F_{max} = 3000 MHz for 100 Mb/s and 2.5 Gb/s data rates
= 4000 MHz for 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates

Equation (192–32) is plotted in Figure 192–52, which is provided for information only.

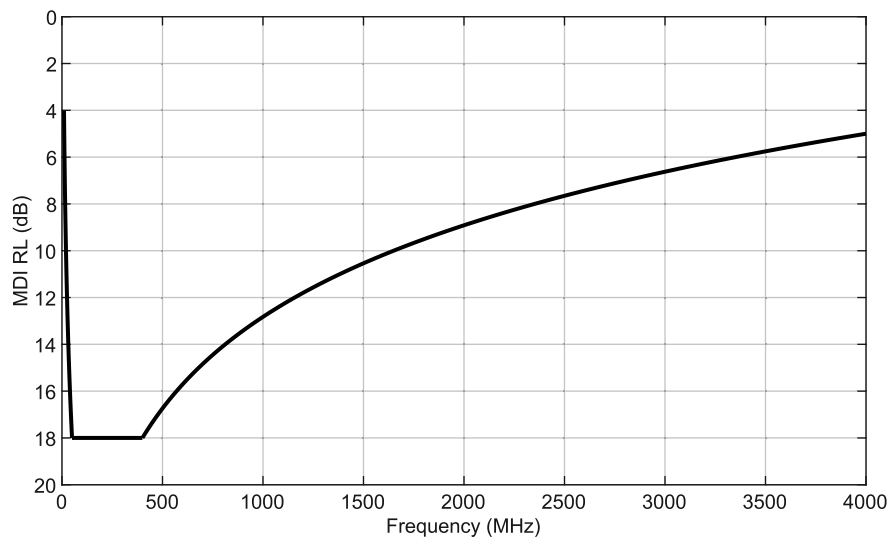


Figure 192–52—T1 MDI return loss using Equation (192–32)

192.9.3 MDI fault tolerance

The -T1 MDI fault tolerance shall comply with 96.8.3.

192.10 MDI specification, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial MDI (-V1) that meets the requirements specified in this subclause.

192.10.1 MDI connectors

The -V1 mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the -V1 mechanical interface is beyond the scope of this standard.

192.10.2 MDI electrical specifications

The electrical requirements specified in 192.5.2 and 192.5.3 shall be met when the PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable.

192.10.2.1 MDI return loss

The differential impedance at the -V1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -V1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (192–33). For the -V1 MDI, a nominal differential characteristic impedance of 50 Ω is used.

$$MDI\_Return\_Loss(f) \geq \left\{ \begin{array}{ll} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{array} \right\} \text{ (dB)} \quad (192-33)$$

where

f is the frequency in MHz; $10 \leq f \leq Fmax$
 $Fmax$ = 3000 MHz for 100 Mb/s and 2.5 Gb/s data rates
= 4000 MHz for 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates

Equation (192–33) is plotted in Figure 192–53, which is provided for information only.

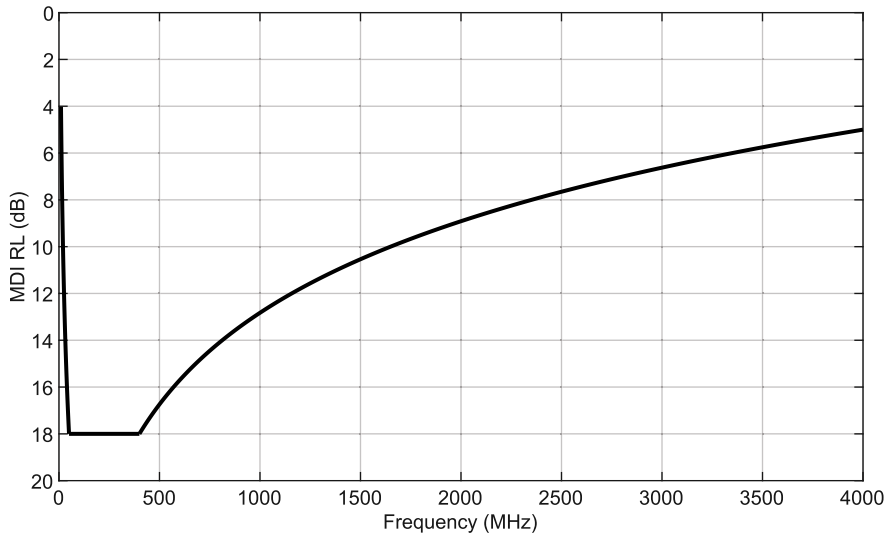


Figure 192–53—V1 MDI return loss using Equation (192–33)

192.10.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 192–26, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

Table 192–26—Connection fault

Center conductor	Shield
No fault	Ground
MDI +	Ground
Ground	Ground
+50 V dc	Ground

192.11 Environmental specifications

192.11.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

192.11.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

192.11.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

- a) General loads: ISO 16750–1
- b) Electrical loads: ISO 16750–2, ISO 7637–2:2008, and ISO 8820–1
- c) Mechanical loads: ISO 16750–3, ASTM D4728, and ISO 12103–1
- d) Climatic loads: ISO 16750–4, IEC 60068–2–1, IEC 60068–2–27, IEC 60068–2–30, IEC 60068–2–38, IEC 60068–2–52, IEC 60068–2–64, and IEC 60068–2–78
- e) Chemical loads: ISO 16750–5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

192.11.3 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

- a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21
- b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21
- c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3
- d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

192.12 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (see [Clause 31](#) and [Annex 31B](#)) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 192–27. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

Table 192–27—Delay constraints

Transmit MAC data rate	Maximum delay (BT)	Maximum delay (pause_quanta)	Maximum delay (ns)
100 Mb/s	1 536	3	15 360
2.5 Gb/s	5 120	10	2 048
5 Gb/s	10 240	20	2 048
7.5 Gb/s	15 360	30	2 048
10 Gb/s	20 480	40	2 048

192.13 Protocol implementation conformance statement (PICS) proforma for Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1⁶

192.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in [Clause 21](#).

192.13.2 Identification

192.13.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model).	

192.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3dm-202x, Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [] Yes [] (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	

⁶Copyright release for PICS proformas: Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

192.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY-T1	MultiGBASE-AT1 capability	192.1.1	Supports MultiGBASE-AT1 operation	O	Yes [] No []
*PHY-V1	MultiGBASE-AV1 capability	192.1.1	Supports MultiGBASE-AV1 operation	O	Yes [] No []
*7.5GTX	7.5 Gb/s transmit MAC data rate	192.1.1	Supports 7.5 Gb/s mode of operation, PHY_S	O	Yes [] No []
*10GTX	10 Gb/s transmit MAC data rate	192.1.1	Supports 10 Gb/s mode of operation, PHY_S	O	Yes [] No []
*10GRX	10 Gb/s receive MAC data rate	192.1.1	Supports 10 Gb/s mode of operation, PHY_D	O	Yes [] No []
*INS-LS, T1	Installation/link segment, -T1	192.7	Items marked with INS-LS, T1 include installation and cabling specifications for link segments and are not applicable to a PHY manufacturer	O	Yes [] No []
*INS-LS, V1	Installation/link segment, -V1	192.8	Items marked with INS-LS, V1 include installation and cabling specifications for link segments and are not applicable to a PHY manufacturer	O	Yes [] No []

192.13.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

192.13.4.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS Reset	192.3.2.1	Meets requirements 192.3.2.1	M	Yes []
PCST2	Control and management interface restoration	192.3.2.1	Restored to operation within 10 ms from the setting of bit 3.2322.15	M	Yes []
PCST3	PCS Transmit compliance	192.3.2.2	Conforms to the PCS 64B/65B Transmit state diagram in Figure 192–22 and to the PCS Transmit bit ordering in Figure 192–5 and Figure 192–6	M	Yes []
PCST4	PMA_TXMODE.indication message SEND_Z value	192.3.2.2	PCS Transmit passes Z symbols at each symbol period to the PMA via the PMA_UNITDATA.request primitive	M	Yes []
PCST5	PMA_TXMODE.indication message SEND_TS or SEND_TA value	192.3.2.2	PCS Transmit generates the O_n sequence defined in 192.3.4 to the PMA via the PMA_UNITDATA.request primitive	M	Yes []
PCST6	PMA_TXMODE.indication message SEND_N value	192.3.2.2	The PCS is in the data mode of operation and the PCS Transmit function uses a 65B coding technique to generate code-groups that represent data or control	M	Yes []
PCST7	Idle /I/ insertion and deletion	192.3.2.2.7	Occurs in groups of four. /I/s may not be added while data is being received. The first four characters after a /T/ are not be deleted when deleting /I/s.	M	Yes []
PCST8	RS-FEC (LS) encoding	192.3.2.2.13	Takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and generates the six 8-bit parity symbols (48 bits total)	M	Yes []
PCST9	RS-FEC (HS) encoding	192.3.2.2.13	Takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and generates the six 8-bit parity symbols (48 bits total)	M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
PCSTI0	Transmitter interleaving depth, L	192.3.2.2.14	Round-robin interleaving scheme shown in Figure 192–8 is applied	M	Yes []
PCSTI1	Transmitter interleaving depth, $L > 1$	192.3.2.2.14	Predefined for each data rate and complies with Table 192–4	M	Yes []
PCSTI2	Superframe aggregation	192.3.2.2.14	HS_TX PCS Transmit aggregates L RS-FEC input frames into an interleaved RS-FEC input	M	Yes []
PCSTI3	Scrambled refresh header data bit	192.3.2.2.17	See Equation (192–4)	M	Yes []
PCSTI4	PRBS11 scrambler polynomial	192.3.2.2.18	The PRBS11 pattern generator produces the same result as the implementation shown in Figure 192–10	M	Yes []
PCSTI5	PRBS11 scrambler state rule	192.3.2.2.18	Scrambler state is never initialized to all zeros	M	Yes []
PCSTI6	PRBS11 scrambler continuity	192.3.2.2.18	Once started, during PMA training, the scrambler continues to run uninterrupted during the refresh headers of each frame	M	Yes []
PCSTI7	PRBS11 scrambler stop rule	192.3.2.2.18	Once started, during PMA training, the scrambler stops during the burst payload field and QUIET	M	Yes []
PCSTI8	PRBS33 scrambler polynomial, Leader	192.3.2.2.19	PCS Transmit uses Equation (192–9) as the transmitter scrambler generator polynomial superframe	M	Yes []
PCSTI9	PRBS33 scrambler polynomial, Follower	192.3.2.2.19	PCS Transmit uses Equation (192–10) as the transmitter scrambler generator polynomial superframe	M	Yes []
PCSTI20	PRBS33 scrambler state rule	192.3.2.2.19	Scrambler state is never initialized to all zeros	M	Yes []
PCSTI21	PRBS33 scrambler continuity	192.3.2.2.19	Once started, during PMA training, the scrambler continues to run uninterrupted during the payload of PMA training frames and data mode frames	M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
PCST22	PRBS33 scrambler stop rule	192.3.2.2.19	Once started, during PMA training, the scrambler stops during QUIET and refresh headers	M	Yes []
PCST23	Gray mapping (Tx) for PAM4	192.3.2.2.20	See 192.3.2.2.20	10GTX:M	Yes [] N/A []
PCST24	Gray mapping (Rx) for PAM4	192.3.2.2.20	See 192.3.2.2.20	10GRX:M	Yes []
PCST25	PAM4 (Tx)	192.3.2.2.21	See 192.3.2.2.21	10GTX:M	Yes []
PCST26	PAM3 (Tx)	192.3.2.2.22	See 192.3.2.2.22	7.5GTX:M	Yes []

192.13.4.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PCSR1	PCS Receive compliance	192.3.2.3	Conforms to the PCS 64B/65B Receive state diagram in Figure 192–23 and the PCS Receive bit ordering in Figure 192–12 for the LS_RX and Figure 192–13 for the HS_RX, including compliance with the associated state variable as specified in 192.3.5.1.2	M	Yes []
PCST2	Frame and block synchronization	192.3.2.3.1	The receiving PCS concatenates rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload according to its data mode (see 192.3.2.3.1)	M	Yes []
PCST3	Descrambler, Leader	192.3.2.3.2	The Leader PHY uses the receiver descrambler generator polynomial in Equation (192–10)	M	Yes []
PCST4	Descrambler, Follower	192.3.2.3.2	The Follower PHY shall uses the receiver descrambler generator polynomial in Equation (192–9)	M	Yes []
PCST5	RS-FEC parity bit integrity check	192.3.2.3.3	The PCS Receive function checks the integrity of the RS-FEC parity bits defined in 192.3.2.2.13	M	Yes []

192.13.4.3 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	SEND_TS frequency	192.3.4	Uses a symmetric frame format and transmits at 3 GBd	M	Yes []
PCS2	33-bit scrambler operation	192.3.4	Once started at the beginning of the training payload of the first training burst, continues to run uninterrupted for each symbol during all subsequent payloads and maintains its last state during the QUIET period and refresh headers	M	Yes []
PCS3	Refresh header content	192.3.4.2	Composed of a leading sequence of zeros followed by four bytes of 0x01, followed by four bytes of 0xF0	M	Yes []
PCS4	Scrambler synchronization acquisition and reporting	192.3.4.4	The PCS acquires descrambler state synchronization to the PAM2 training sequence and reports success through scr_status, and continues to use the synchronized state in all subsequent bursts in both data and training modes	M	Yes []
PCS5	DECODE function rule	192.3.5.1.3	Decodes the block as specified in 192.3.2.2.4	M	Yes []
PCS6	ENCODE function rule	192.3.5.1.3	Encodes the block as specified in 192.3.2.2.4	M	Yes []
PCS7	PCS functions	192.3.5.2	Performs the functions of RFER monitor, Transmit, and Receive as shown in Figure 192–21, Figure 192–22, and Figure 192–23	M	Yes []

192.13.4.4 OAM

Item	Feature	Subclause	Value/Comment	Status	Support
OAM1	State diagram behavior	192.3.7.4	Conforms to Figure 192–25 and Figure 192–26	OAM:M	Yes [] N/A []
OAM2	HS_TX mode OAM frame structure, first bit	192.3.7.2.1	The first bit of the first OAM symbol (OAM<0>) is inserted in the first RS frame in the first superframe of the TDD burst	OAM:M	Yes [] N/A []
OAM3	HS_TX mode OAM frame structure, subsequent bits	192.3.7.2.1	One subsequent bit of OAM<0> is inserted into each of second through tenth RS FEC frames	OAM:M	Yes [] N/A []
OAM4	LS_TX mode OAM frame structure	192.3.7.2.1	The first symbol (OAM<0>) is inserted in the first ten bits of the OAM field of the RS frame so that one OAM symbols is carried in each TDD burst	OAM:M	Yes [] N/A []
OAM5	When OAM is not implemented	192.3.7.2.1	10-bit OAM field is set to all zeros	OAM:M	Yes [] N/A []
OAM6	OAM frame data	192.3.7.2.1	Reserved fields are set to zero	OAM:M	Yes [] N/A []
OAM7	MultiGBASE-A OAM Frame acceptance criteria	192.3.7.2.13	See 192.3.7.2.13	OAM:M	Yes [] N/A []
OAM8	mr_tx_received	192.3.7.4.3	Clear on read	OAM:M	Yes [] N/A []

192.13.4.5 Physical Medium Attachment (PMA)

192.13.4.5.1 PMA Reset

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	PMA Reset function	192.4.2.1	See 192.4.2.1	M	Yes []

192.13.4.5.2 PMA Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT1	PMA Transmit operation	192.4.2.2	Continuously transmits pulses modulated by the symbols given by tx_symb onto the MDI, followed by a QUIET period to complete a TDD cycle, when the PHY Control state diagram (see Figure 192-31) is not in the DISABLE_TRANSMITTER state	M	Yes []
PMAT2	PMA Transmit signal compliance	192.4.2.2	Complies with the electrical specifications given in 192.5.2	M	Yes []
PMAT3	Clock source, Leader	192.4.2.2	The transmit symbol clock TX_TCLK is sourced from a local clock source, while meeting the transmit jitter requirements of 192.5.2.3, when the management parameter config is LEADER	M	Yes []
PMAT4	Loop timing	192.4.2.2	The Leader-Follower relationship include loops timing	M	Yes []
PMAT5	Clock source, Follower	192.4.2.2	The transmit symbol clock TX_TCLK is sourced from the recovered clock of 192.4.2.6, while meeting the jitter requirements of 192.5.2.3, when the management parameter config is FOLLOWER	M	Yes []
PMAT6	Transmit fault function mapping	192.4.2.2	Mapped to the transmit fault bit, as specified in 45.2.1.7.4, if the MDIO interface is implemented	M	Yes []
PMAT7	Launch power disable	192.3.2.2.1	The average launch power of the transmitter is as specified in 192.5.2.4 when the PMA_transmit_disable variable is set to TRUE and the value of tx_symb is Z	M	Yes []

192.13.4.5.3 PMA Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	PMA Receive	192.4.2.3	See 192.4.2.3	M	Yes []
PMAR2	Status constraint	192.4.2.3	The reception of Z symbols during the TDD QUIET period alone does not trigger setting loc_rcvr_status to NOT_OK	M	Yes []
PMAR3	Receive fault function mapping	192.4.2.3	Contributed to the receive fault bit specified in 45.2.1.7.5, if the MDIO interface is implemented	M	Yes []

192.13.4.5.4 PHY Control

Item	Feature	Subclause	Value/Comment	Status	Support
CNIRL1	PHY control compliance	192.4.2.4	Complies with the state diagram in Figure 192–31	M	Yes []

192.13.4.5.5 Infocfield

Item	Feature	Subclause	Value/Comment	Status	Support
IF1	12-octet Infocfield fields	192.4.2.4	Include the fields in 192.4.2.4.2 through 192.4.2.4.8 as shown in Figure 192–28 and Figure 192–29	M	Yes []
IF2	Infocfield transmission	192.4.2.4	Transmit Infocfield at least 16 times with each change to octets 7 to 10 when PMA_state = 00	M	Yes []
IF3	Infocfield reserved bits	192.4.2.4.1	Unused values are set to zero on transmit and ignored when received by the link partner	M	Yes []
IF4	Infocfield start of frame delimiter	192.4.2.4.2	Uses the hexadecimal value 0xBBA700	M	Yes []

192.13.4.5.6 Message Field

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	PMA state communication	192.4.2.4.4	Bits PMA_state<7:6> communicate the state of the transmitting transceiver to the link partner	M	Yes []
MF2	Training phase signal	192.4.2.4.4	Bits training_phase<4:3> communicate the training phase of the transmitting transceiver to the link partner	M	Yes []
MF3	Invalid value transmission	192.4.2.4.4	Values not listed in Table 192–13 for the Leader or Follower are not transmitted and ignored at the receiver	M	Yes []
MF4	Initial Message Field setting	192.4.2.4.4	The Message Field setting for the first transmitted PMA burst is the first row of Table 192–13 for the Leader, and the first or second row of Table 192–10 for the Follower	M	Yes []
MF5	Next Message Field	192.4.2.4.4	Is the same Message Field setting or the Message Field setting corresponding to a row below the current setting in Table 192–13	M	Yes []

192.13.4.5.7 PHY capability

Item	Feature	Subclause	Value/Comment	Status	Support
CAP1	OAM capability	192.4.2.4.5	Enabled only if both PHYs set the capability bit OAMen=1	O	Yes []
CAP2	OAM capability validity	192.4.2.4.5	Valid only when loc_rcvr_status<5> bit is one	O	Yes []

192.13.4.5.8 TDD delay counter

Item	Feature	Subclause	Value/Comment	Status	Support
DLY1	Delay counter rule	192.4.2.4.6	delay_count set to a value between 0 to 63 and the delay_count_valid bit set to one after the Leader detects the Follower TDD burst position and estimates the link segment delay	M	Yes []
DLY2	Delay count acceptance	192.4.2.4.6	The Follower accepts the received remote delay_count only when received remote delay_count_valid bit is set to one	M	Yes []
DLY3	Delay count storage	192.4.2.4.6	The Follower stores delay_count number	M	Yes []
DLY4	Delay acknowledgment	192.4.2.4.6	The Follower sends back its own delay_count field as acknowledgment of delay_count reception, and set its delay_count_valid to one	M	Yes []
DLY5	Negotiation success rule	192.4.2.4.6	The Leader or the Follower sets negotiation_done to OK when it finishes the exchange of delay count and the negotiated data rates	M	Yes []
DLY6	Follower burst adjustment	192.4.2.4.6	The Follower adjusts its transmit burst position according to the stored delay_count, starting from Asymmetric training and continuing through to the data mode	M	Yes []

192.13.4.5.9 Phase switch

Item	Feature	Subclause	Value/Comment	Status	Support
PS1	PhaseSwBC24 burst count	192.4.2.4.7	A minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state	M	Yes []

192.13.4.5.10 CRC16

Item	Feature	Subclause	Value/Comment	Status	Support
CRC1	CRC16 Infofield	192.4.2.4.9	Implements the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>	M	Yes []
CRC2	CRC16 verification	192.4.2.4.9	Produces the same result as the implementation shown in Figure 192–30	M	Yes []
CRC3	CRC16 initialization	192.4.2.4.9	The 16 delay elements in Figure 192–30 are initialized to zero	M	Yes []

192.13.4.5.11 Startup

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	Startup sequence compliance	192.4.2.4.11	Complies with the state diagram description given in Figure 192–31	M	Yes []
ST2	TRAINING0 alignment	192.4.2.4.11	The first symbol of the Follower's transmit PMA training frame at the transmit MDI is aligned at 400 ± 1 transmit symbols after arrival of the last PMA training payload symbol from the Leader at the Follower input MDI	M	Yes []
ST3	Alignment maintenance	192.4.2.4.11	The Follower maintains alignment while in the TRAINING0 and COUNTDOWN0 (i.e., while tx_mode = SEND_TS) states	M	Yes []
ST4	TRAINING1 alignment	192.4.2.4.11	The Follower uses the Leader transmitted delay_count to align its transmit PMA training frame to be $17 \text{ ns} - \text{delay\_count} \times 5.333 \text{ ns}$ ($\pm 5.333 \text{ ns}$) after the last PMA training payload symbol from the Leader appears on the Follower input MDI	M	Yes []
ST5	Alignment maintenance	192.4.2.4.11	The Follower maintains its alignment while tx_mode is SEND_TA or SEND_N	M	Yes []

192.13.4.5.12 Link monitor

Item	Feature	Subclause	Value/Comment	Status	Support
LM1	Link Monitor function compliance	192.4.2.5	Complies with the state diagram of Figure 192–33	M	Yes []

192.13.4.5.13 Clock recovery

Item	Feature	Subclause	Value/Comment	Status	Support
CR1	Clock Recovery function	192.4.2.6	Provides a clock suitable for signal sampling so that the RFER indicated in 192.4.2.3 is achieved	M	Yes []

192.13.4.6 MDI signals

Item	Feature	Subclause	Value/Comment	Status	Support
MDIS1	MDI symbol response compliance	192.4.3.1	Complies with the electrical specifications given in 192.5.2	M	Yes []

192.13.4.7 Timers

Item	Feature	Subclause	Value/Comment	Status	Support
TIM1	link_fail_timer expiration	192.4.4.2	Expires 97.5 ms $\pm$ 5 ms after being started	M	Yes []
TIM2	minwait_timer expiration	192.4.4.2	Expires 975 μ s $\pm$ 50 μ s after being started	M	Yes []
TIM3	tdd_watchdog_timer expiration	192.4.4.2	Expires 96 μ s $\pm$ 5 μ s after being started	M	Yes []

192.13.4.8 PMA electrical specifications

192.13.4.8.1 Test modes

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Test modes	192.5.1	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes []
TM2	Enable test modes	192.5.1	Enable by setting control register, 1.2313.15:13 as described in 192.5.1 when MDIO implemented; enabling of test modes is provided otherwise when MDIO is not implemented	M	Yes []
TM3	Test mode operation	192.5.1	Test modes only change data symbols provided to the transmitter circuitry	M	Yes []
TM4	Test mode 1	192.5.1	When enabled, PHY provides access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5	M	Yes []
TM5	Test mode 2	192.5.1	When enabled, PHY transmits a continuous repeating pattern of $\{+1, -1\}$ symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference	M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
TM6	Test mode 4, PAM2 mode	192.5.1	When enabled, PHY transmits the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16). All PHYs support transmission of this signal at 3 GBd. PHYs that support 5 Gb/s, and 7.5 Gb/s, and 10 Gb/s transmit rates support transmission of this signal at 6 GBd.	M	Yes []
TM7	Test mode 4, PAM3 mode	192.5.1	When enabled, PHY transmits the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 7.5 Gb/s transmit rates support transmission of this signal at 6 GBd.	M	Yes []
TM8	Test mode 4, PAM4 mode	192.5.1	When enabled, PHY transmits the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 10 Gb/s transmit rates support transmission of this signal at 6 GBd.	M	Yes []
TM9	Test mode 5	192.5.1	When enabled, PHY transmits continuously with no QUIET period or refresh header and with transmit signal level corresponding to the data mode of operation	M	Yes []
TM10	Test mode 6	192.5.1	When enabled, PHY transmits a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source	M	Yes []

192.13.4.8.2 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT1	Coupling	192.5.2	Electrical input is ac-coupled	M	Yes []
PMAT2	Transmitter electrical specifications	192.5.2	Meets requirements of 192.5.2	M	Yes []
PMAT3	Transmitter output droop	192.5.2.1	Less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing, when measured in test mode 6 using transmitter test fixture 1 or test fixture 3	M	Yes []
PMAT4	Captured block length and sampling	192.5.2.2	At least 4000 transmitted symbols long and sampled with a minimum of 10x oversampling	M	Yes []
PMAT5	Transmitter peak distortion	192.5.2.2	Less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM4 transmitters, measured at a minimum of ten equally spaced phases of a single symbol period	M	Yes []
PMAT6	RMS jitter, Leader mode	192.5.2.3	Less than 1 ps when supporting 10 Gb/s, less than 1.5 ps when supporting 7.5 Gb/s, less than 2 ps when supporting 5 Gb/s, and less than 4 ps when supporting 2.5 Gb/s for jitter frequencies greater than 100 kHz, measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1	M	Yes []
PMAT7	Time Interval Error, Leader mode	192.5.2.3	Less than 10 ps when supporting 10 Gb/s, less than 15 ps when supporting 7.5 Gb/s, less than 20 ps when supporting 5 Gb/s, and less than 40 ps when supporting 2.5 Gb/s, measured in test mode 1 using test fixture 2 over a period of 100 ms	M	Yes []
PMAT8	RMS jitter, Follower mode	192.5.2.3	Less than 1 ps when supporting 10 Gb/s, less than 1.5 ps when supporting 7.5 Gb/s, less than 2 ps when supporting 5 Gb/s, and less than 4 ps when supporting 2.5 Gb/s for jitter frequencies greater than 1 MHz, measured in test mode 1	M	Yes []

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT9	Time Interval Error, Follower mode	192.5.2.3	Less than 15 ps when supporting 10 Gb/s, less than 22.5 ps when supporting 7.5 Gb/s, less than 30 ps when supporting 5 Gb/s, and less than 60 ps when supporting 2.5 Gb/s, measured in test mode 1 over 50 overlapping periods of 10 ms	M	Yes []
PMAT10	Transmitter power levels	192.5.2.4	In the range of values specified in Table 192–22 when using the PSD measurement test fixture	M	Yes []
PMAT11	MDI transmit signal	192.5.2.4	Nominally zero and less than -36 dBm for frequencies greater 10 MHz	M	Yes []
PMAT12	Transmitter power spectral density, -T1	192.5.2.4	Between the upper mask specified in Equation (192–17) and the lower mask specified in Equation (192–18), measured into a 100 Ω differential load using test fixture 1	*PHY-T1:M	Yes [] N/A []
PMAT13	Symbol transmission rate	192.5.2.6	Within the range of $6 \times S \text{ GBd} \pm 100 \text{ ppm}$ with drift less than 1 ppm/sec	M	Yes []
PMAT14	Recovered symbol rate	192.5.2.6	Within $\pm 10 \text{ ppm}$ of the recovered clock used by the Follower	M	Yes []

192.13.4.8.3 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	Bit error rate, -T1	192.5.3.1	Less than 10^{-12} after RS-FEC decoding	*PHY-T1:M	Yes [] N/A []
PMAR2	Bit error rate, -V1	192.5.3.1	Less than 10^{-12} after RS-FEC decoding	*PHY-V1:M	Yes [] N/A []

192.13.4.9 Link segment

192.13.4.9.1 Link segment characteristics, -T1

Item	Feature	Subclause	Value/Comment	Status	Support
LST1	Insertion loss, -T1	192.7.1.1	Meets requirements of 192.7.1.1	INS-LS, T1:M	Yes [] N/A []
LST2	Return loss, -T1	192.7.1.3	Meets requirements of 192.7.1.3	INS-LS, T1:M	Yes [] N/A []
LST3	Coupling attenuation, -T1	192.7.1.4	Meets requirements of 192.7.1.4	INS-LS, T1:M	Yes [] N/A []
LST4	Screening attenuation, -T1	192.7.1.5	Meets requirements of 192.7.1.5	INS-LS, T1:M	Yes [] N/A []
LST5	Propagation delay, -T1	192.7.1.6	Not more than 160 ns for all frequencies between 10 MHz and 5 GHz	INS-LS, T1:M	Yes [] N/A []
LST6	PSANEXT loss, -T1	192.7.2.1	Meets requirements of 192.7.2.1	INS-LS, T1:M	Yes [] N/A []
LST7	PSAACRF, -T1	192.7.2.2	Meets requirements of 192.7.2.2	INS-LS, T1:M	Yes [] N/A []

192.13.4.9.2 Link segment characteristics, -V1

Item	Feature	Subclause	Value/Comment	Status	Support
LSV1	Insertion loss, -V1	192.8.1.1	Meets requirements of 192.8.1.1	INS-LS, V1:M	Yes [] N/A []
LSV2	Return loss, -V1	192.8.1.3	Meets requirements of 192.8.1.3	INS-LS, V1:M	Yes [] N/A []
LST3	Screening attenuation, -V1	192.8.1.5	Measured in accordance with ISO 19642-11 and meets requirements of 192.8.1.5	INS-LS, V1:M	Yes [] N/A []
LST4	Propagation delay, -V1	192.8.1.6	Not more than 160 ns for all frequencies between 10 MHz and 5 GHz	INS-LS, V1:M	Yes [] N/A []
LST5	Coupling parameter test methodologies, -V1	192.8.2	Applied with adaptation to unbalanced coaxial cabling and using a 50 Ω termination to ground	INS-LS, V1:M	Yes [] N/A []
LST6	PSANEXT loss, -V1	192.8.2.1	Meets requirements of 192.8.2.1	INS-LS, V1:M	Yes [] N/A []
LST7	PSAACRF, -V1	192.8.2.2	Meets requirements of 192.8.2.2	INS-LS, V1:M	Yes [] N/A []

192.13.4.10 MDI

192.13.4.10.1 MDI specification, -T1

Item	Feature	Subclause	Value/Comment	Status	Support
MDIT1	Electrical requirements, -T1	192.9.2	Electrical requirements are for when a PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors	*PHY-T1:M	Yes [] N/A []
MDIT2	Return loss, -T1	192.9.2.1	For each transmitter/receiver, measured with a nominal impedance of 50 Ω	*PHY-T1:M	Yes [] N/A []
MDIT3	Fault tolerance, -T1	192.9.3	Meets requirements of 96.8.3	*PHY-T1:M	Yes [] N/A []

192.13.4.10.2 MDI specification, -V1

Item	Feature	Subclause	Value/Comment	Status	Support
MDIV1	Electrical requirements, -V1	192.10.2	Electrical requirement are for when a PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable	*PHY-V1:M	Yes [] N/A []
MDIV2	Return loss, -V1	192.10.2.1	For each transmitter/receiver, measured with a nominal impedance of 50 Ω	*PHY-V1:M	Yes [] N/A []
MDIT3	Fault tolerance, -V1	192.10.3	MDI coaxial cable interface withstands, without damage, 50 V dc with the source current limited to 150 mA. Normal operation resumes after all short circuits are removed. Single MDI conductor withstands, without damage, high-voltage transient noises and ESD per application requirements.	*PHY-V1:M	Yes [] N/A []

192.13.4.11 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Delay constraints	192.12	Complies with Table 192–27	M	Yes []

Annex 31B

(normative)

MAC Control PAUSE operation

31B.3 Detailed specification of PAUSE operation

31B.3.7 Timing considerations for PAUSE operation

Change the first seven paragraphs of 31B.3.7 as shown:

In a full duplex mode DTE, it is possible to receive PAUSE frames asynchronously with respect to the transmission of MAC frames. For effective flow control, it is necessary to place an upper bound on the length of time that a DTE can transmit data frames after receiving a valid PAUSE frame with a non-zero pause_time request_operand.

Reception of a PAUSE frame shall not affect the transmission of a MAC frame that has been submitted by the MAC Control sublayer to the underlying MAC (i.e., the MAC:MA_DATA.request service primitive is synchronous, and is never interrupted).

At operating speeds of 100 Mb/s or less, a station that implements an exposed MII, shall not begin to transmit a (new) frame (assertion of TX_EN at the MII, see 22.2.2.3) more than one pause_quantum after the reception of a valid PAUSE frame (deassertion of RX_DV at the MII, see 22.2.2.7) that contains a nonzero value of pause_time. Stations that do not implement an exposed MII, shall measure this time at the MDI, with the timing specification increased to one pause_quantum + 64 BT.

At an operating speed of 1000 Mb/s, a station shall not begin to transmit a (new) frame more than two pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

At operating speeds of 2.5 Gb/s, a station with a 2.5GBASE-T PHY shall not begin to transmit a (new) frame more than 34 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 2.5 Gb/s PHY shall not begin to transmit a (new) frame more than 6 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Asymmetric PHYs operating with 2.5 Gb/s transmit and 100 Mb/s receive operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 4 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII. Asymmetric PHYs operating with 2.5 Gb/s receive and 100 Mb/s transmit operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 1 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII.

At operating speeds of 5 Gb/s, a station with a 5GBASE-T PHY shall not begin to transmit a (new) frame more than 42 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 5 Gb/s PHY shall not begin to transmit a (new) frame more than 12 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Asymmetric PHYs operating with 5 Gb/s transmit and 100 Mb/s receive operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 8 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII. Asymmetric PHYs operating with 5 Gb/s receive and 100 Mb/s transmit operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 1 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII.

Asymmetric PHYs operating with 7.5 Gb/s transmit and 100 Mb/s receive operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 12 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII. Asymmetric PHYs operating with 7.5 Gb/s receive and 100 Mb/s transmit operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 1 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII.

At operating speeds of 10 Gb/s, a station with a 10GBASE-T PHY shall not begin to transmit a (new) frame more than 74 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI. A station using any other 10 Gb/s PHY shall not begin to transmit a (new) frame more than 60 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the MDI.

Asymmetric PHYs operating with 10 Gb/s transmit and 100 Mb/s receive operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 16 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII. Asymmetric PHYs operating with 10 Gb/s receive and 100 Mb/s transmit operating speeds as specified in Clause 192 shall not begin to transmit a (new) frame more than 1 pause_quanta after the reception of a valid PAUSE frame that contains a non-zero value of pause_time, as measured at the XGMII.

31B.4 Protocol implementation conformance statement (PICS) proforma for MAC Control PAUSE operation⁷

31B.4.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 31B, MAC Control PAUSE operation, shall complete the following PICS proforma in addition to the PICS of [Clause 31](#).

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in [Clause 21](#).

31B.4.2 Identification

31B.4.2.1 Implementation identification

Supplier	
Contact point for inquiries about the PICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification— e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)	
NOTE 1—Only the first three items are required for all implementations, other information may be completed as appropriate in meeting the requirements for the identification. NOTE 2—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

31B.4.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3-202x, Annex 31B, MAC Control PAUSE operation
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No ☐ Yes ☐ (See Clause 21 ; The answer Yes means that the implementation does not conform to IEEE Std 802.3-202x)	

Date of Statement	

⁷ *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

31B.4.3 Major capabilities/options

Insert two new rows after row MIIe, four new rows after MIIg, and two new rows after MIIi as follows (unchanged rows not shown):

Item	Feature	Subclause	Value/Comment	Status	Support
...					
*MIIea	At asymmetric operating speeds of 2.5 Gb/s transmit and 100 Mb/s receive as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
*MIIeb	At asymmetric operating speeds of 2.5 Gb/s receive and 100 Mb/s transmit as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
...					
*MIIga	At asymmetric operating speeds of 2.5 Gb/s transmit and 100 Mb/s receive as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
*MIIgb	At asymmetric operating speeds of 5 Gb/s receive and 100 Mb/s transmit as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
*MIIgc	At asymmetric operating speeds of 5 Gb/s transmit and 100 Mb/s receive as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
*MIIgd	At asymmetric operating speeds of 7.5 Gb/s receive and 100 Mb/s transmit as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
...					
*MIIia	At asymmetric operating speeds of 10 Gb/s transmit and 100 Mb/s receive as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
*MIIib	At asymmetric operating speeds of 10.5 Gb/s receive and 100 Mb/s transmit as specified in Clause 192	31B.3.7	N/A	O	Yes [] No []
...					

31B.4.6 PAUSE command MAC timing considerations

Insert two new rows after row TIM6, four new rows after TIM8, and two new rows after TIM10 as follows (unchanged rows not shown and unchanged footnote letter a shown for reference):

Item	Feature	Subclause	Value/Comment	Status	Support
...					
TIM6a	Measurement point for station at 2.5 Gbs transmit and 100 Mb/s receive rates with PHY type of MultiGBASE-A operating as PHY_S	31B.3.7	Delay at MDI $\leq$ 4 pause_quanta ^a	MIlea:M	Yes [] N/A []
TIM6b	Measurement point for station at 2.5 Gbs receive and 100 Mb/s transmit rates with PHY type of MultiGBASE-A operating as PHY_D	31B.3.7	Delay at MDI $\leq$ 1 pause_quanta ^a	MIleb:M	Yes [] N/A []
...					
TIM8a	Measurement point for station at 5 Gbs transmit and 100 Mb/s receive rates with PHY type of MultiGBASE-A operating as PHY_S	31B.3.7	Delay at MDI $\leq$ 8 pause_quanta ^a	MIlga:M	Yes [] N/A []
TIM8b	Measurement point for station at 5 Gbs receive and 100 Mb/s transmit rates with PHY type of MultiGBASE-A operating as PHY_D	31B.3.7	Delay at MDI $\leq$ 1 pause_quanta ^a	MIlgb:M	Yes [] N/A []
TIM8c	Measurement point for station at 7.5 Gbs transmit and 100 Mb/s receive rates with PHY type of MultiGBASE-A operating as PHY_S	31B.3.7	Delay at MDI $\leq$ 12 pause_quanta ^a	MIlgc:M	Yes [] N/A []
TIM8d	Measurement point for station at 7.5 Gbs receive and 100 Mb/s transmit rates with PHY type of MultiGBASE-A operating as PHY_D	31B.3.7	Delay at MDI $\leq$ 1 pause_quanta ^a	MIlgd:M	Yes [] N/A []

Item	Feature	Subclause	Value/Comment	Status	Support
...					
TIM10a	Measurement point for station at 10 Gbs transmit and 100 Mb/s receive rates with PHY type of MultiGBASE-A operating as PHY_S	31B.3.7	Delay at MDI $\leq$ 16 pause_quanta ^a	MIlia:M	Yes [] N/A []
TIM10b	Measurement point for station at 10 Gbs receive and 100 Mb/s transmit rates with PHY type of MultiGBASE-A operating as PHY_D	31B.3.7	Delay at MDI $\leq$ 1 pause_quanta ^a	MIlib:M	Yes [] N/A []
...					

^a Delay from receiving valid PAUSE command, with nonzero value for pause_time, to cessation of transmission.

Annex 98B

(normative)

IEEE 802.3 Selector Base Page definition

98B.3 Technology Ability Field bit assignments

Change the reserved row for bits “A11 through A20” (as modified by IEEE Std 802.3dg-202x) and insert new rows before this row in Table 98B-1b as follows (unchanged rows not shown):

Table 98B-1—Category-specific technology bit assignments for NULL category

bit	Selector description
...	
<u>A11</u>	<u>100M+2.5GBASE-T1/V1 ability</u>
<u>A12</u>	<u>2.5G+100MBASE-T1/V1 ability</u>
<u>A13</u>	<u>100M+5GBASE-T1/V1 ability</u>
<u>A14</u>	<u>5G+100MBASE-T1/V1 ability</u>
<u>A15</u>	<u>100M+10GBASE-T1/V1 ability</u>
<u>A16</u>	<u>10G+100MBASE-T1/V1 ability</u>
A17H through A20	Reserved
...	

98B.4 Priority Resolution

Replace the 2nd sentence in the 1st paragraph of 98B.4 (as modified by IEEE Std 802.3dg-202x) as follows:

Table 98B-2 indicates the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value. The lowest numbered capability is the resolved ability.

Since a local device and a link partner may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. When the Leader PHY and Follower PHY both indicate the Technology Ability present in a given row of Table 98B-2, that is considered a common ability. Table 98B-2 specifies the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, the priorities are listed from highest to lowest.

Replace the dashed list in 98B.4 with the following table:

Table 98B–2—Priority Resolution^a

Priority	Leader	Follower	Technology
1	A6	A6	25GBASE-T1
2	A5	A5	10GBASE-T1
3	A15	A16	100M+10GBASE-T1/V1(L) 10G+100MBASE-T1/V1(F)
4	A16	A15	10G+100MBASE-T1/V1(L) 100M+10GBASE-T1/V1(F)
5	A4	A4	5GBASE-T1
6	A13	A14	100M+5GBASE-T1/V1(L) 5G+100MBASE-T1/V1(F)
7	A14	A13	5G+100MBASE-T1/V1(L) 100M+5GBASE-T1/V1(F)
8	A3	A3	2.5GBASE-T1
9	A11	A12	100M+2.5GBASE-T1/V1(L) 2.5G+100MBASE-T1/V1(F)
10	A12	A11	2.5G+100MBASE-T1/V1(L) 100M+2.5GBASE-T1/V1(F)
11	A2	A2	1000BASE-T1
12	A21	A21	100BASE-T1L increased transmit/receive level ability
13	A10	A10	100BASE-T1L transmit/receive level ability
14	A0	A0	100BASE-T1
15	A1	A1	10BASE-T1S full duplex
16	A22	A22	10BASE-T1S half duplex
17	A9	A9	10BASE-T1L

^a NOTE—(L) stands for Leader and (F) stands for Follower

Insert new annexes as follows:

Annex 191A

(informative)

Allocation of delay limit budget

In 191.14, the Delay Limits are set for the HS_PATH and LS_PATH, not including the delays introduced by the physical medium interconnecting the two PHYs.

In Figure 191A–1, XGMII transfers are shown as X(#) where # is sequentially incrementing. Let the first 64B/65B block of an RS-FEC frame contain the X(n) and X(n+1) XGMII transfers.

The TX_Delay is defined from the start of the X(n) transfer on the TX XGMII to the start of the first symbol of the frame at the MDI.

The RX_Delay is defined from the start of the first symbol of the frame at the MDI to the start of the X(n) transfer on the RX XGMII.

The HS_PATH delay of 191.14 is composed of the HS_TX delay in the PHY_S (XGMII to MDI) and the HS_RX delay in the PHY_D (MDI to XGMII).

The LS_PATH delay of 191.14 is composed of the LS_TX delay in the PHY_D (XGMII to MDI) and the LS_RX delay in the PHY_S (MDI to XGMII).

Besides the MAC Control PAUSE operation (Clause 31, Annex 31B), the time synchronization support (Clause 90) requires this information for best interoperability between different implementations. It is therefore recommended to allocate the PATH delay portions as follows:

- a) The HS_TX delay is allocated 10% of the delay budget of Table 191–24.
- b) The HS_RX delay is allocated 90% of the delay budget of Table 191–24.
- c) The LS_TX delay is allocated 25% of the delay budget of Table 191–24.
- d) The LS_RX delay is allocated 75% of the delay budget of Table 191–24.

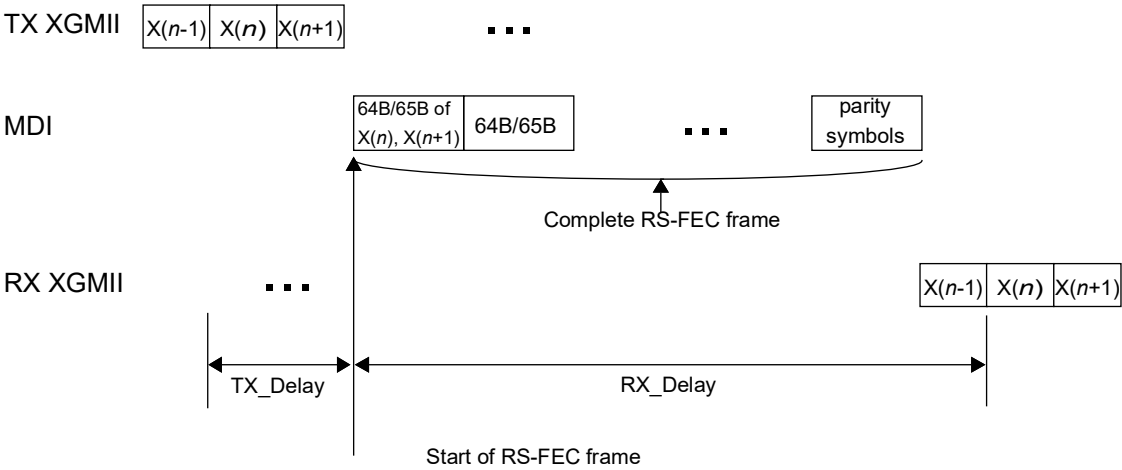


Figure 191A-1—XGMII to MDI to XGMII timing diagram

Since the start of the first symbol of the frame is not easily accessible at the MDI, it is recommended for the PHY implementers to specify TX_Delay and RX_Delay in product documentation and maintain low variation.

Annex 191B

(normative)

High-Pass Filter for SNDR Testing with Low-Frequency High-Pass Networks

191B.1 Introduction

This annex specifies the high-pass filter (HPF) to be applied to the captured MDI waveform during the transmitter distortion test defined in 191.6.2.5 when the device under test (DUT) or test configuration includes any network that introduces a low-frequency high-pass characteristic to the signal path. Examples include, but are not limited to, Power over Coax (PoC) and Power over Data Line (PoDL) bias-tee networks. Low-frequency high-pass networks introduce slow baseline wander (BLW) in the captured MDI waveform. Without compensation, this BLW is misclassified as distortion or noise in the SNDR calculation defined in 191.6.2.5.

The transmitter SNDR distortion is defined as: $SNDR = 10\log_{10}\left(\frac{\sigma_p^2}{\sigma_e^2 + \sigma_n^2}\right)$

This causes the measured SNDR to underestimate the true transmitter performance. A 1st-order HPF applied to the captured MDI waveform removes the BLW contribution before the linear-fit estimation, restoring an accurate SNDR measurement. The corner frequency is chosen to be sufficiently above the typical low-frequency high-pass corner of PoC and PoDL networks (typically 1 MHz to 5 MHz) while preserving the signal band used in the SNDR computation per 120D.3.1.6.

191B.2 Applicability

This annex is required when the DUT or test configuration includes any network that introduces a low-frequency high-pass transfer to the signal path, such as a PoC or PoDL bias-tee. It may be omitted when no such network is present or it is bypassed or disabled. The presence of a low-frequency high-pass may be identified by visible baseline wander in the captured MDI waveform or by knowledge of the DUT or fixture configuration.

191B.3 HPF specification

When a low-frequency high-pass network is present, the following HPF shall be applied to the captured MDI waveform before the linear-fit pulse-response estimation defined in 120D.3.1.6.

Filter type: high-pass, corner frequency: $f_{HPF} = 15$ MHz, filter order: 1st order

191B.4 Constraints

The following constraints shall apply when using the HPF per this annex:

- a) Group delay introduced by the HPF shall be accounted for in symbol timing alignment prior to linear-fit estimation per 120D.3.1.6.

b) $N_p = 300$ shall be used for the linear-fit estimation per 120D.3.1.6.

191B.5 Reporting

The following information should be recorded: whether HPF compensation was applied and the reason (e.g., PoC present, PoDL present, or other low-frequency high-pass network identified).

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191B.6 Protocol implementation conformance statement (PICS) proforma for Annex 191B, High-Pass Filter for SNDR Testing with Low-Frequency High-Pass Networks⁸

191B.6.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Annex 191B, High-Pass Filter for SNDR Testing with Low-Frequency High-Pass Networks, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in [Clause 21](#).

191B.6.2 Identification

191B.6.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

191B.6.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3dm-202x, Annex 191B, High-Pass Filter for SNDR Testing with Low-Frequency High-Pass Networks
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No [] Yes [] (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3dm-202x.)	

Date of Statement	

⁸ *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this annex so that it can be used for its intended purpose and may further publish the completed PICS.

191B.6.2.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
HPFS	High-Pass Filter for SNDR Testing	191B.2		O	Yes [] No []

191B.6.2.4 PICS proforma tables for High-Pass Filter for SNDR Testing with Low-Frequency High-Pass Network

Item	Feature	Subclause	Value/Comment	Status	Support
STF1	HPF shall be applied to the captured MDI waveform	191B.3		M	Yes []
STF2	HPF constraints shall apply	191B.4		M	Yes []