

192. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

192.1 Overview

MultiGBASE-AT1 and MultiGBASE-AV1 PHYs use a time-division duplex (TDD) transmission structure between two active PHYs, in which one link partner transmits a burst while the other is silent. Each PHY may support multiple data rates. MultiGBASE-A PHYs use a common set of symbol rates across high speed and low speed implementations. They also use the same TDD cycle for all data rates (see 192.3.4) and the same base FEC with different shortening parameters for the high speed and low speed directions.

Each link partner transmits according to a TDD cycle consisting of the following three phases:

- 1) a PAM2 modulated burst refresh header,
- 2) a PAM2, PAM3, or PAM4 modulated burst payload,
- 3) and a QUIET period during which no data is transmitted.

Bursts are aligned so that a PHY transmits its refresh header and burst payload during its link partner's QUIET period. The burst timing provides a gap between transmitted and received bursts to allow for signal propagation delay. Ethernet frames are encoded in 64B/65B blocks and protected in RS-FEC frames (with interleaving at 1 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates). The RS-FEC frames comprise the burst payload portion of the TDD cycle. Asymmetric data rates are achieved by asymmetric transmission times for the link partners, with one transmitting 25 RS-FEC superframes per burst and the other transmitting one RS-FEC frame per burst. See 192.3.4 for more detail on TDD bursts.

A MultiGBASE-A PHY may operate as the Leader or the Follower. The Leader PHY uses a local clock to time its transmitter operations. The Follower PHY recovers the clock from the received signal and uses it to time its transmitter operations. The Leader-Follower relationship is predetermined via management control during initialization or via default hardware setup.

A device that supports multiple simultaneous MultiGBASE-A PHYs may choose to align the start time of its transmit TDD cycle across links operating as the Leader to reduce crosstalk. Such an alignment is optional and implementation specific.

192.1.1 Nomenclature

The MultiGBASE-AT1 and MultiGBASE-AV1 PHYs described in this clause represent two distinct PHY types that share the same PCS and PMA specifications subject to frequency scaling. In order to efficiently describe the two PHYs, the following nomenclature is used.

HS_PATH	PHY_S HS_TX to PHY_D HS_RX
HS_RX	High speed receiver
HS_TX	High speed transmitter
LS_PATH	PHY_D LS_TX to PHY_S LS_RX
LS_RX	Low speed receiver
LS_TX	Low speed transmitter

MultiGBASE-A	Refers to all MultiGBASE-AT1 and MultiGBASE-AV1 PHYs regardless of cable type or bit rate
MultiGBASE-AT1	Refers to the asymmetric PHY communicating on a single shielded balanced pair of conductors
MultiGBASE-AV1	Refers to the asymmetric PHY communicating on a single coaxial cable

N_r	Number of symbols transmitted in the refresh header of a TDD burst
N_p	Number of symbols transmitted in the payload of a TDD burst
N_z	Number of transmit symbol periods during which the TDD burst is QUIET
PHY_D	LS_TX, HS_RX mode of operation (high speed XGMII destination)
PHY_S	HS_TX, LS_RX mode of operation (high speed XGMII source)

The six modes of operation and MAC data rate combinations for each of the two PHY types are shown in Table 192–1.

Table 192–1—PHY type definitions

Table 192–1—Formatted Table

PHY name	Medium interface	Mode of operation	Transmit MAC data rate	Receive MAC data rate	Combined operating rate designator
MultiGBASE-AT1	Differential (balanced)	PHY_D	100 Mb/s	2.5 Gb/s	100+2.5G
			100 Mb/s	5 Gb/s	100+5G
			100 Mb/s	7.5 Gb/s	100+7.5G
			100 Mb/s	10 Gb/s	100+10G
			1 Gb/s	5 Gb/s	1000+5G
			1 Gb/s	7.5 Gb/s	1000+7.5G
		PHY_S	2.5 Gb/s	100 Mb/s	2.5G+100
			5 Gb/s	100 Mb/s	5G+100
			7.5 Gb/s	100 Mb/s	7.5G+100
			10 Gb/s	100 Mb/s	10G+100
			5 Gb/s	1 Gb/s	5G+1000
			7.5 Gb/s	1 Gb/s	7.5G+1000
MultiGBASE-AV1	Single-ended (unbalanced)	PHY_D	100 Mb/s	2.5 Gb/s	100+2.5G
			100 Mb/s	5 Gb/s	100+5G
			100 Mb/s	7.5 Gb/s	100+7.5G
			100 Mb/s	10 Gb/s	100+10G
			1 Gb/s	5 Gb/s	1000+5G

			<u>1 Gb/s</u>	<u>7.5 Gb/s</u>	<u>1000+7.5G</u>
		PHY_S	2.5 Gb/s	100 Mb/s	<u>2.5G+100</u>
			5 Gb/s	100 Mb/s	<u>5G+100</u>
			7.5 Gb/s	100 Mb/s	<u>7.5G+100</u>
			10 Gb/s	100 Mb/s	<u>10G+100</u>
			<u>5 Gb/s</u>	<u>1 Gb/s</u>	<u>5G+1000</u>
			<u>7.5 Gb/s</u>	<u>1 Gb/s</u>	<u>7.5G+1000</u>

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

- T1

-V1
- represents a single shielded balanced pair of conductors (i.e., differential)

represents a single coaxial cable (i.e., unbalanced)

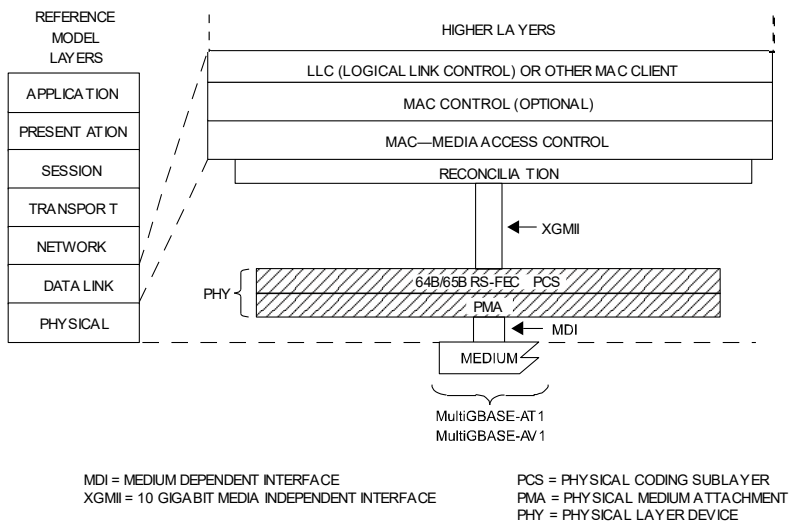
Additionally, for parameters that scale with the PHY’s supported MAC data rate, the parameter *S* is used for scaling as shown in Table 192–2.

Table 192–2—Scaling parameters

Transmit MAC data rate	<i>S</i>
100 Mb/s	0.5
<u>1 Gb/s</u>	<u>1</u>
2.5 Gb/s	0.5
5 Gb/s	1
7.5 Gb/s	1
10 Gb/s	1

192.1.2 Relationship of MultiGBASE-A to other standards

The relationship between a MultiGBASE-A PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 192–1. The PHY sublayers (shown shaded) in Figure 192–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. The XGMII is defined in Clause 46.



NOTE 1—XGMII is optional.
NOTE 2—Medium is a single shielded balanced pair of conductors for -AT1 and a single coaxial cable for -AV1.

Figure 192–1—Relationship of MultiGBASE-A PHYs to the ISO/IEC reference model and the IEEE 802.3 Ethernet Model

192.1.3 Operation of MultiGBASE-A

The MultiGBASE-A functional block diagram is shown in Figure 192–2.

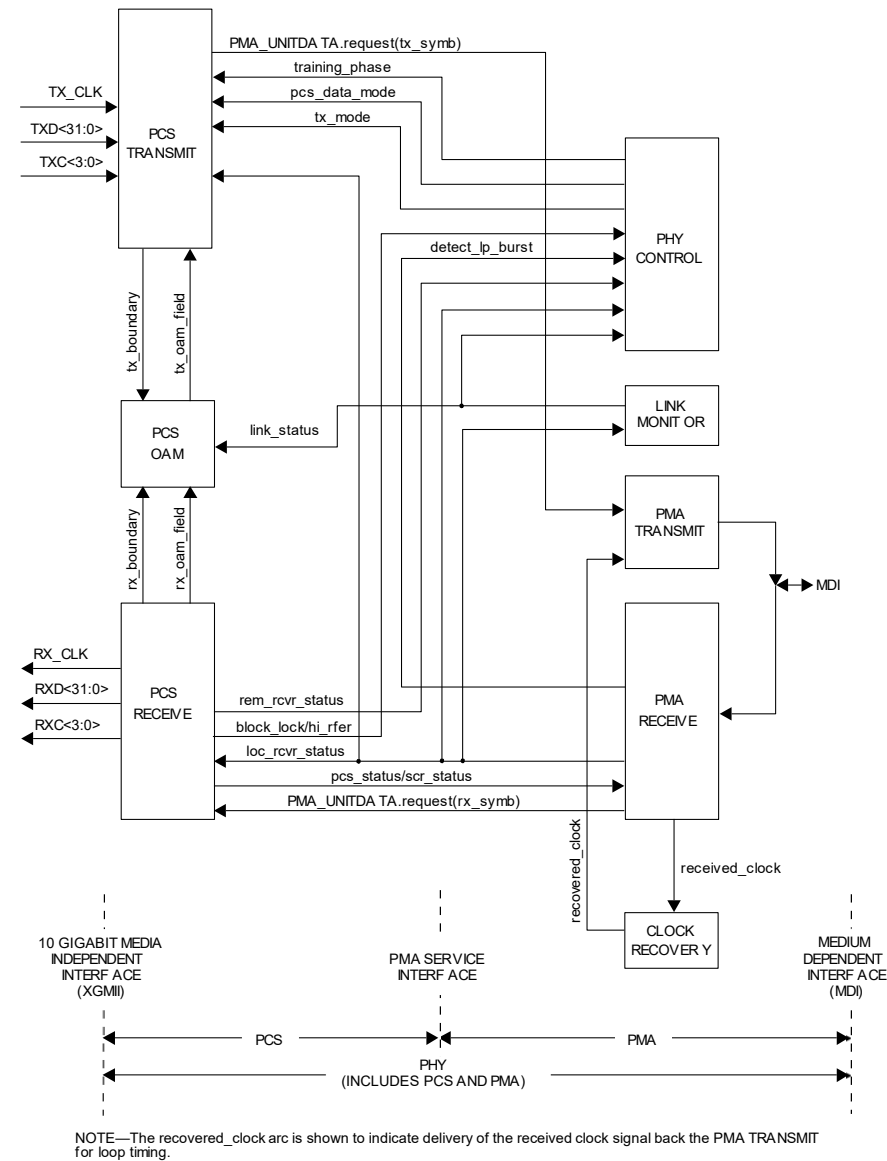


Figure 192–2—Functional block diagram

192.1.3.1 Physical Coding Sublayer (PCS) in PHY_S mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the data mode of operation (see 192.2.1.8), the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in data mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 1-bit OAM field is appended to form a 976-bit block. A number, L (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 3 for 7.5 Gb/s, and L = 4 for 10 Gb/s), of these 976-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC(128,122) and the round-robin interleaving as described in 192.3.2.2.15. The RS-FEC output superframe consists of L × 1024 bits. The duration of the superframe is 1024 / 3 ns.

NOTE—Duration = L × 1024 bits / bits per symbol / baud rate. For 10 Gb/s, Duration = 4 × 1024 / 2 / 6 GBd; for 7.5 Gb/s, Duration = 3 × 1024 / 1.5 / 6 GBd; for 5 Gb/s, Duration = 2 × 1024 / 1 / 6 GBd; for 2.5 Gb/s, Duration = 1 × 1024 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the HS_TX payload. The PCS Transmit functions are described in 192.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx_group15x65B}\langle 65 \times i + j \rangle = \text{tx_coded}_i\langle j \rangle$$

where $i = 0$ to 14, $j = 0$ to 64, and tx_coded_i<64:0> is the i^{th} 64B/65B block where tx_coded₀<64:0> is the first block transmitted.

In the training mode (see 192.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 192.3. The interface to the PMA is an abstract message-passing interface specified in 192.4.

192.1.3.2 Physical Coding Sublayer (PCS) in PHY_D mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the data mode of operation (see 192.2.1.8), the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in data mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 17-bit OAM field is appended to form a 992-bit block. A number, L ($L = 1$ for 100 Mb/s, $L = 2$ for 1 Gb/s) of these 992-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(130,124,8) and the round-robin interleaving as described in 192.3.2.2.15. The RS-FEC output superframe consists of $L \times 1040$ bits. The duration of the superframe is $1040 / 3$ ns.

NOTE—Duration = $L \times 1040$ bits / bits per symbol / baud rate. For 100 Mb/s, Duration = $1040 / 1 / 3$ GBd. For 1 Gb/s, Duration = $2 \times 1040 / 1 / 6$ GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the LS_TX payload. The PCS Transmit functions are described in 192.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx_group15x65B}\langle 65 \times i + j \rangle = \text{tx_coded}_i\langle j \rangle$$

where $i = 0$ to 14, $j = 0$ to 64, and tx_coded _{i} <64:0> is the i^{th} 64B/65B block where tx_coded₀<64:0> is the first block transmitted.

In the training mode (see 192.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 192.3. The interface to the PMA is an abstract message-passing interface specified in 192.4.

192.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto a single balanced pair of conductors (-T1) or a single coaxial cable (-V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides communications at $6 \times S$ GBd. See Table 192–2 for the definition of S .

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled and provides the startup functions required for successful operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link and communicates this status to other functional blocks. A failure of the receive link causes the data mode operation to stop and startup functions to restart.

PMA functions and state diagrams are specified in 192.4 and 192.5. The electrical parameters of the PMA (i.e., test modes and electrical specifications for the transmitter and receiver) are specified in 192.5.

192.1.4 LS_PATH signaling

LS_PATH signaling is performed by the LS_TX PCS generating continuous symbols that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The symbols consist of PAM2 symbols within a burst and Z symbols between bursts. The signaling scheme achieves a number of objectives including:

- a) Forward error correction (FEC) coded symbol mapping for data.
- b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the transmit path.
- c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
- d) Uncorrelated symbols in the transmitted symbol stream.
- e) No correlation between symbol streams traveling in opposite directions.
- f) Block framing and other control signals.
- g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
- h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the data mode or the training mode.

In both data mode and training mode, the LS_TX PCS generates a continuous stream of symbols that are transferred to the PMA during the payload (see Figure 192–31). The Z symbols are transmitted at the same symbol rate.

192.1.5 HS_PATH signaling

HS_PATH signaling is performed by the HS_TX PCS generating continuous symbols that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The symbols consist of PAM2, PAM3, or PAM4 symbols within a burst and Z symbols between bursts. The refresh headers use PAM2 regardless of the MAC data rate. The modulation used by 5 Gb/s and 7.5 Gb/s for the HS_PATH depends on whether the corresponding LS_PATH operates at 100 Mb/s or 1 Gb/s. The HS_PATH PAM encodings are shown in Table 192-yy. The signaling scheme achieves a number of objectives including:

- a) Forward error correction (FEC) coded symbol mapping for data.
- b) When used in combination with a 100 Mb/s LS_PATH, algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, PAM3 symbols in the 7.5 Gb/s transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
- b) When used in combination with a 1 Gb/s LS_PATH, algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM3 symbols in the 5 Gb/s transmit path and PAM4 symbols in the 7.5 Gb/s transmit path.
- c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
- d) Uncorrelated symbols in the transmitted symbol stream.
- e) No correlation between symbol streams traveling in opposite directions.
- f) Block framing and other control signals.
- g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

h) Ability to automatically detect and correct for signal inversion.

<u>HS_PATH data rate</u>	<u>HS_PATH PAM encoding when used with LS_PATH data rate of 100 Mb/s</u>	<u>HS_PATH PAM encoding when used with LS_PATH data rate of 1 Gb/s</u>
<u>2.5 Gb/s</u>	<u>PAM2</u>	<u>N/A</u>
<u>5 Gb/s</u>	<u>PAM2</u>	<u>PAM3</u>
<u>7.5Gb/s</u>	<u>PAM3</u>	<u>PAM4</u>
<u>10 Gb/s</u>	<u>PAM4</u>	<u>N/A</u>

[Editing note: Table 192-yy PAM encoding for the HS_PATH]

The PHY may operate in two basic modes: the data mode or the training mode.

In both data and training modes, the HS_TX PCS generates a continuous stream of symbols that are transferred to the PMA during the payload (see Figure 192–31). The Z symbols are transmitted at the same symbol rate.

192.1.6 Interfaces

All MultiGBASE-A PHY implementations are compatible at the XGMII, if implemented. Implementation of the XGMII is optional. All MultiGBASE-AT1 PHY implementations are compatible at the -T1 MDI. All MultiGBASE-AV1 PHY implementations are compatible at the -V1 MDI. The MDI for a single balanced pair of conductors (-T1) and a single coaxial cable (-V1) are different. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

192.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

192.2 Service primitives and interfaces

MultiGBASE-A transfers data and control information across the following three service interfaces:

- a) 10 Gigabit Media Independent Interface (XGMII)
- b) PMA service interface
- c) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46. The PMA service interface is defined in 192.2.1. The -T1 MDI is defined in 192.9. The -V1 MDI is defined in 192.10.

192.2.1 PMA service interface

MultiGBASE-A uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

```
PMA_TXMODE.indication(tx_mode)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication(pcs_data_mode)
PMA_PCSSYNC.request(block_lock, hi_rfer)
```

The use of these primitives is shown in Figure 192–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 192–3.

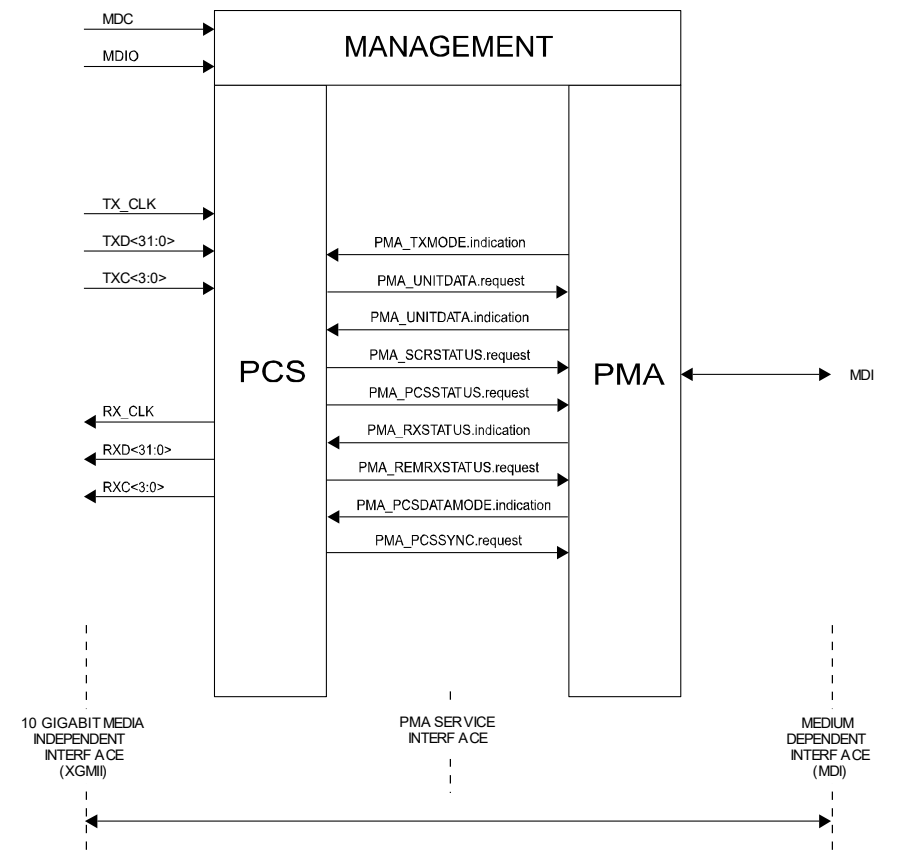


Figure 192–3—MultiGBASE-A service interface

192.2.1.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE-A link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

192.2.1.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values:

- SEND_N This value is continuously asserted during transmission of sequences of symbols representing the TDD bursting (including QUIET periods) of an XGMII data stream in the data mode.
- SEND_TS This value is continuously asserted when transmission of sequences of symbols representing the TDD symmetric training mode is to take place. LS_TX and HS_TX send at 3 GBd with PAM2 TDD training frames.
- SEND_TA This value is continuously asserted when transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. LS_TX sends at 3 GBd or 6 GBd with PAM2 TDD training frames. HS_TX sends at 3 GBd or 6 GBd with PAM2 TDD training frames.
- SEND_Z This value is continuously asserted in case continuous transmission of Z symbols is required. See 192.5.2.4 for the encoding of Z.

192.2.1.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

192.2.1.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 192.3.2.2.

192.2.1.2 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 192.3.2.2 to represent XGMII data and control streams or other sequences.

192.2.1.2.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

The PMA_UNITDATA.request primitive conveys the value of the symbol to be transmitted over the MDI via the tx_symb parameter. The tx_symb may take on one of the following values:

- {-1, -1/3, +1/3, +1} 10 Gb/s transmit payload in data mode: 7.5G+1000 transmit payload in data mode.
- {-1, 0, +1} 7.5G+100-Gb/s transmit payload in data mode: 5G+1000 transmit payload in data mode.
- {-1, +1} 100 Mb/s, 1 Gb/s, or 2.5 Gb/s or 5-Gb/s transmit payload in data mode: 5G+100 transmit payload in data mode, and all refresh header symbols in data and training modes.

- Z when Z symbols are to be transmitted (see 192.5.2.4) in the following two cases:
- 1) when PMA_TXMODE.indication is SEND_Z during PMA training, and
 - 2) during the QUIET period in each TDD cycle.

192.2.1.2.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

192.2.1.2.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 192.5.2.

192.2.1.3 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

192.2.1.3.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception, the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock. The rx_symb may take on the same values defined for tx_symb in 192.2.1.2.1.

192.2.1.3.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive, as governed by the recovered clock, is 3 GHz for 100 Mb/s and 2.5 Gb/s receive modes and 6 GHz for 1 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s receive modes.

192.2.1.3.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

192.2.1.4 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the PCS descrambler has achieved synchronization.

192.2.1.4.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values:

- OK The PCS descrambler has achieved synchronization.
- NOT_OK The PCS descrambler is not synchronized.

192.2.1.4.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

192.2.1.4.3 Effect of receipt

The effect of receipt of this primitive is specified in 192.4.2.3 and 192.4.2.4.

192.2.1.5 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

192.2.1.5.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values:

- OK The PCS is operating reliably in the data mode.
- NOT_OK The PCS is not operating reliably in the data mode.

192.2.1.5.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

192.2.1.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 192.4.2.3 and 192.4.4.1.

192.2.1.6 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criteria for setting the parameter

loc_rcvr_status is left to the implementer. For example, it can be based on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

192.2.1.6.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values:

- OK This value is asserted and remains true during reliable operation of the receive link for the local PHY.
- NOT_OK This value is asserted whenever operation of the link for the local PHY is unreliable.

192.2.1.6.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

192.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–3, 192.3.2.3, 192.4.2.4, and 192.5.

192.2.1.7 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infocfield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infocfield from the remote PHY.

192.2.1.7.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values:

- OK The receive link for the remote PHY is operating reliably.
- NOT_OK Reliable operation of the receive link for the remote PHY is not detected.

192.2.1.7.2 When generated

The PCS generates PMA_REMRXSTATUS.request message to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infocfield messages received from the remote PHY during training.

192.2.1.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–31.

192.2.1.8 PMA_PCSDATAMODE.indication

This primitive indicates when the PCS 64B/65B state diagrams are able to process data. The `pcs_data_mode` variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the `PMA_PCSDATAMODE.indication` primitive.

192.2.1.8.1 Semantics of the primitive

`PMA_PCSDATAMODE.indication(pcs_data_mode)`

The `pcs_data_mode` parameter can take on one of two values:

- TRUE The PCS is transmitting and receiving data from the XGMII.
- FALSE The PCS is in a training or test mode.

192.2.1.8.2 When generated

The PMA PHY Control function generates `PMA_PCSDATAMODE.indication` messages continuously.

192.2.1.8.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 192.3.2.2.

192.2.1.9 PMA_PCSSYNC.request

This primitive indicates the PCS alignment (`block_lock`) and error status (`hi_rfer`) to the PMA.

192.2.1.9.1 Semantics of the primitive

`PMA_PCSSYNC.request(block_lock, hi_rfer)`

The `PMA_PCSSYNC.request` primitive passes the `block_lock` and `hi_rfer` parameters from the PCS to the PMA.

The parameter `block_lock` is defined in 192.3.5.1.2.

The parameter `hi_rfer` is defined in 192.3.5.1.2.

192.2.1.9.2 When generated

The PCS generates `PMA_PCSSYNC.request` messages to indicate a change in `block_lock` or `hi_rfer`.

192.2.1.9.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–32 and Figure 192–33.

192.3 Physical Coding Sublayer (PCS) functions

192.3.1 PCS service interface (XGMII)

The PCS service interface allows the PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

192.3.2 PCS functions

The PCS comprises the following functions: PCS Reset, PCS Transmit, PCS Receive, and an optional PCS OAM. The PCS Transmit and PCS Receive functions execute simultaneously and asynchronously. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram (see Figure 192–4) shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 192–4.

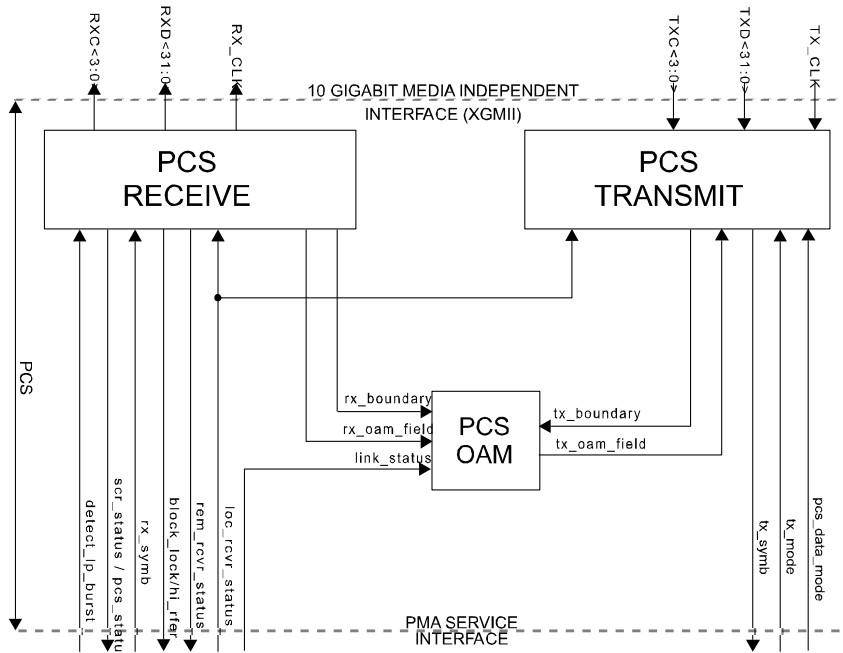


Figure 192-4—PCS reference diagram

192.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of following conditions occur:

- Power on (see 192.3.5.1.2)
- The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

192.3.2.2 PCS Transmit function

The LS_TX PCS Transmit function is shown in Figure 192–5 and the HS_TX PCS Transmit function is shown in Figure 192–6. The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram shown in Figure 192–22 and to the PCS Transmit bit ordering shown in Figure 192–5 and Figure 192–6.

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals.

Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format. In each TDD cycle, the transmit PCS generates a sequence of PAM symbols followed by a sequence of Z symbols representing the QUIET period to the transmit PMA. The transmit QUIET period allows the receive PMA to receive a burst during each TDD cycle.

For LS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the LS_TX PCS Transmit process take ~~one~~L groups of 15 65B blocks and append a 17-bit OAM field to ~~each group~~, shown in Figure 192–5. This forms the input to the L-interleaved RS-FEC(130,124) ~~encoder~~superframe, which adds L × 48 parity bits. 1 such superframe is formed for 100 Mb/s and 5 such superframes are formed for 1 Gb/s. L = 1 for 100 Mb/s, L = 2 for 1 Gb/s. The resulting ~~1040 bits~~1040 bits for 100 Mb/s or 10 400 for 1 Gb/s are then scrambled. These bits are then mapped, one at a time, into PAM2 symbols. Transmit data-units are sent to the LS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For HS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the HS_TX PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC(128,122) superframe which adds L × 48 parity bits, shown in Figure 192–6. 25 such superframes are formed for one data payload. L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 3 for 7.5 Gb/s, and L = 4 for 10 Gb/s. The resulting L × 1024 × 25 bits are then scrambled. For 2.5 Gb/s and 5 Gb/s using PAM2 encoding, these bits are then mapped, one at a time, into PAM2 symbols. For 5 Gb/s and 7.5 Gb/s using PAM3 encoding, these bits are then mapped, three at a time, into pairs of PAM3 symbols. For 7.5 Gb/s and 10 Gb/s using PAM4 encoding, these bits are then mapped, two at a time, into PAM4 symbols. Transmit data-units are sent to the HS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For both LS_TX and HS_TX, each set of transmit data-units forming the payload of a TDD burst are preceded by a PAM-2 mapped refresh header sequence of N_r symbols and followed by a sequence of N_z Z symbols to complete the TDD cycle (see Figure 192–18 and Figure 192–19). In each symbol period of a TDD burst, when communicating with the PMA, the PCS Transmit generates a PAM2, PAM3, or PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. Between TDD bursts, the PCS Transmit transfers Z symbols to the PMA via the PMA_UNITDATA.request primitive. The symbol period, T , is $1000 / (6 \times S)$ ps. See Table 192–2 for the definition of S .

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function. During training, PMA_TXMODE.indication has values SEND_Z, SEND_TS, and SEND_TA before transitioning to SEND_N for data mode.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass Z symbols at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_TS or SEND_TA, PCS Transmit shall generate a sequence (O_n) as defined in 192.3.4.3, which is passed to the PMA via the PMA_UNITDATA.request primitive. These symbols are used for training mode and only transmit the values $\{-1, +1\}$.

During training mode, an Infobfield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and requests the remote transmitter settings (see 192.4.2.4).

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation and the PCS Transmit function shall use a 65B coding technique to generate code-groups that represent data or control. For LS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 17-bit OAM field to form the RS-FEC input frame. During data encoding, LS_TX PCS Transmit utilizes L-interleaved ($L = 1$ for 100 Mb/s or $L = 2$ for 1 Gb/s) Reed-Solomon encoders to generate and append 48 parity check bits to form 1040-bit RS-FEC(130,124) frames that are interleaved into an L-interleaved RS-FEC superframe that is $L \times 1040$ bits long. ~~which One frame becomes the burst payload for one TDD cycle for 100 Mb/s or 5 consecutive RS-FEC superframes are concatenated to form the start of the burst payload for one TDD cycle for 1 Gb/s.~~ For HS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 1-bit OAM field to form the RS-FEC input frame. During data encoding, HS_TX PCS Transmit utilizes L-interleaved ($L = 1$ for 2.5 Gb/s, $L = 2$ for 5 Gb/s, $L = 3$ for 7.5 Gb/s, or $L = 4$ for 10 Gb/s) Reed-Solomon encoders to generate and append 48 parity check bits to form 1024-bit RS-FEC(128,122) frames that are interleaved into an L-interleaved RS-FEC superframe that is $L \times 1024$ bits long. 25 consecutive RS-FEC superframes are concatenated to form the burst payload for one TDD cycle.

The LS_TX operating at 1 Gb/s extends the burst payload by appending one additional RS-FEC superframe followed by 8 bytes of padding. The HS_TX operating at 5 Gb/s using PAM3 extends the burst payload by appending two additional RS-FEC superframes followed by 726 bytes of padding. The HS_TX operating at 7.5 Gb/s using PAM4 extends the burst payload by appending one additional RS-FEC superframe followed by 200 bytes of padding. The content of the message in these appended RS-FEC superframes and padding bytes is vendor specified. The scrambler continues running and scrambles the extended burst payload RS-FEC superframes and padding.

In all PCS bursts, a scrambled refresh header bit sequence is concatenated with the scrambled burst payload bit sequence and the bit sequences are mapped to PAM symbols appropriate to the transmit rate. These PAM symbols are then concatenated with the required number of Z symbols to complete a full TDD cycle of symbols. The process is repeated for each TDD cycle.

192.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 192.3.2.2.4.

192.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is shown in Figure 192–5 for LS_TX, Figure 192–6 for HS_TX, Figure 192–12 for LS_RX, and Figure 192–13 and Figure 192–14 for HS_RX. These figures show the processing of a multiplicity of blocks containing 8 data octets. See 192.3.2.2.4 for information on how blocks containing control characters are mapped.

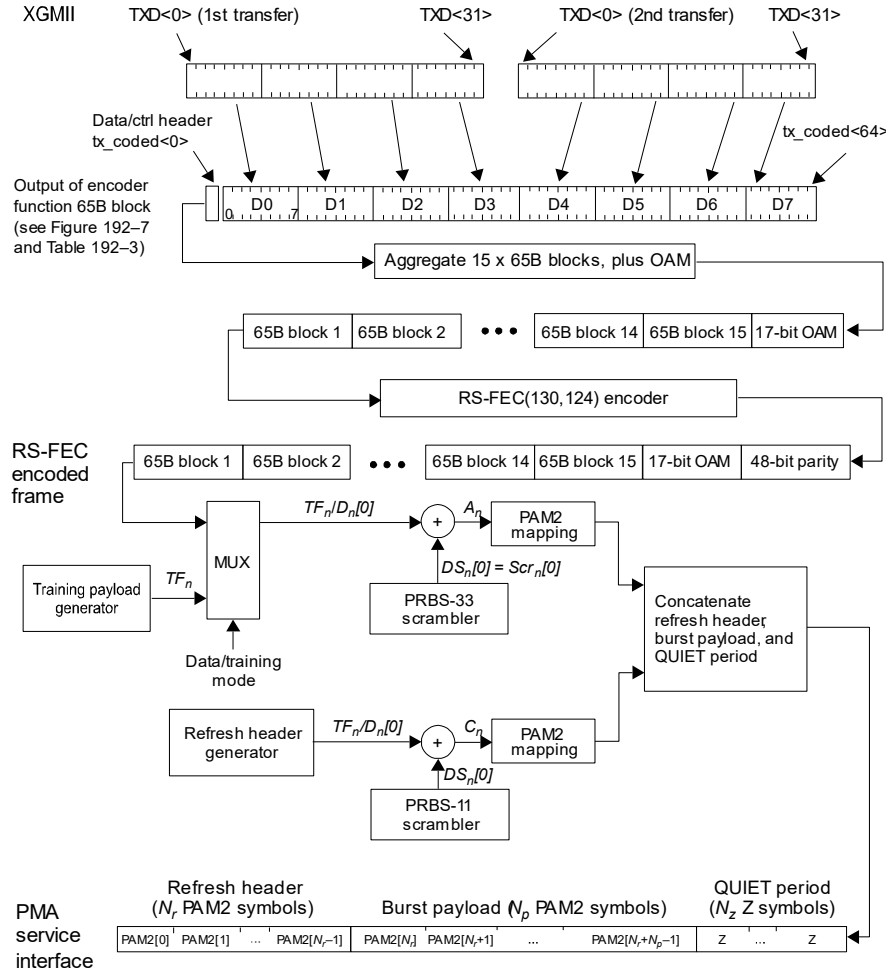


Figure 192–5—LS_TX PCS Transmitt bit ordering

[Editing note for Figure 192-5 changes:

1. For 1 Gb/s add a block which aggregates 6 RS-FEC encode frames before the Data/training mode MUX (similar to Figure 192-6 “Aggregate 25 RS-FEC superframes” block). This block can also

append the extended payload vendor-specific 8 bytes of padding, so label it as “Aggregate 6 RS-FEC superframes, append 8 bytes of vendor-specific padding”.

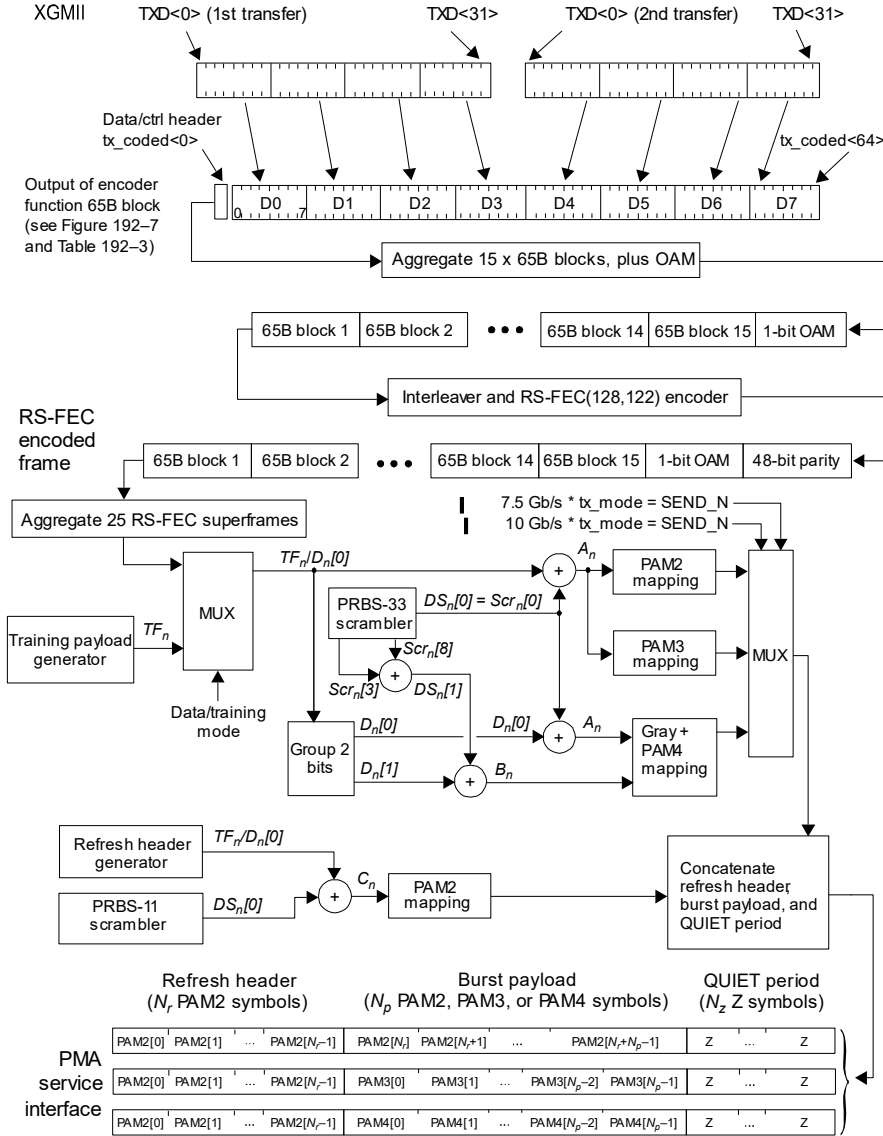
2. For 1 Gb/s add a block which inserts a vendor-specific L x 992-bit vendor-specific message after every five Lx992-bit messages into the input of the RS-FEC encoder block.

3. The 2 blocks above can be shown in dashed lines and a note added indicating dashed line blocks are for 1 Gb/s operation only.

4. Add note that this figure is shown for L=1

5. Relabel “RS-FEC(130, 124) encoder” as “Interleaver and RS-FEC(130, 124) encoder”]

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NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for $L = 1$.

NOTE 3—Either the PAM2, PAM3, or PAM4 path and TDD frame at the PMA service interface is used. PAM3 path (and the middle TDD frame shown) is chosen if the bit rate is 7.5 Gb/s and tx_mode = SEND_N. PAM4 path (and the lowest TDD frame shown) is chosen if the bit rate is 10 Gb/s and tx_mode = SEND_N.

Figure 192-6—RS_TX RCS Transmitter block diagram

[Editing note for Figure 192-6:

1. For 5 Gb/s using PAM3 and 7.5 Gb/s using PAM4 add a block ahead of the Interleaver and RS-FEC(128, 122) encoder which inserts a set of L x 976-bit vendor-specific message after every 25 Lx976-bit messages into the input of the RS-FEC encoder block. The size of the set is 1 for 7.5 Gb/s PAM4 and 2 for 5 Gb/s PAM3.
2. For 5 Gb/s using PAM3 and 7.5 Gb/s using PAM4 add a note for the block which aggregates 25 RS-FEC superframes that it will aggregate 27 superframes for 5Gb/s PAM3 and 26 RS-FEC encoded superframes for 7.5Gb/s PAM4 before the Data/training mode MUX. This block can also append the extended payload vendor-specific 726 or 200 bytes of padding for 5Gb/s or 7.5Gbps respectively, so label it as “Aggregate RS-FEC superframes and append vendor-specific padding”.
3. Add notes indicating the vendor-specific message and padding are only inserted for 5Gb/s PAM3 and 7.5Gb/s PAM4.

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192.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D0 to D7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O0 or O4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S0 or S4 for the same reason. The control character for terminate is labeled as T0 to T7.

The two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

192.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block.

64B/65B block formats are shown in shown in Figure 192–7. The column labeled Input data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, D₀ through D₇ are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one.

Each control block contains eight characters. For control blocks containing a start (/S/) or terminate (/T/) character, as indicated by an S or T octet in the Figure 192–7 Input data field, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O code. The single bit fields, represented by unlabeled narrow rectangles in Figure 192–7, are sent with the value zero and ignored upon receipt.

NOTE—The block structure specified in this subclause is identical to that used in 149.3.2.2.4.

Input data	data ctrl header	Block payload											
Bit position:	0	1											
Data block format:	64												
D ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ D ₆ D ₇	0	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇				
Control Block Formats:		Block											
C ₀ C ₁ C ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0x1E	C ₀	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇			
C ₀ C ₁ C ₂ C ₃ /O ₄ D ₅ D ₆ D ₇	1	0x2D	C ₀	C ₁	C ₂	C ₃	O ₄	D ₅	D ₆	D ₇			
C ₀ C ₁ C ₂ C ₃ /S ₄ D ₅ D ₆ D ₇	1	0x33	C ₀	C ₁	C ₂	C ₃		D ₅	D ₆	D ₇			
O ₀ D ₁ D ₂ D ₃ /S ₄ D ₅ D ₆ D ₇	1	0x66	D ₁	D ₂	D ₃	O ₀		D ₅	D ₆	D ₇			
O ₀ D ₁ D ₂ D ₃ /O ₄ D ₅ D ₆ D ₇	1	0x55	D ₁	D ₂	D ₃	O ₀	O ₄	D ₅	D ₆	D ₇			
S ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ D ₆ D ₇	1	0x78	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇				
O ₀ D ₁ D ₂ D ₃ /C ₄ C ₅ C ₆ C ₇	1	0x4B	D ₁	D ₂	D ₃	O ₀	C ₄	C ₅	C ₆	C ₇			
T ₀ C ₁ C ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0x87		C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇			
D ₀ T ₁ C ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0x99	D ₀		C ₂	C ₃	C ₄	C ₅	C ₆	C ₇			
D ₀ D ₁ T ₂ C ₃ /C ₄ C ₅ C ₆ C ₇	1	0xAA	D ₀	D ₁		C ₃	C ₄	C ₅	C ₆	C ₇			
D ₀ D ₁ D ₂ T ₃ /C ₄ C ₅ C ₆ C ₇	1	0xB4	D ₀	D ₁	D ₂		C ₄	C ₅	C ₆	C ₇			
D ₀ D ₁ D ₂ D ₃ /T ₄ C ₅ C ₆ C ₇	1	0xCC	D ₀	D ₁	D ₂	D ₃		C ₅	C ₆	C ₇			
D ₀ D ₁ D ₂ D ₃ /D ₄ T ₅ C ₆ C ₇	1	0xD2	D ₀	D ₁	D ₂	D ₃	D ₄		C ₆	C ₇			
D ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ T ₆ C ₇	1	0xE1	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	C ₇				
D ₀ D ₁ D ₂ D ₃ /D ₄ D ₅ D ₆ T ₇	1	0xFF	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆				

Figure 192–7—~~6B~~ 6B block formats for MultiBASE-A

192.3.2.2.5 Control codes

All control characters are supported by both the XGMII and the PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The PCS encodes the start and terminate control characters implicitly by the block type field. The PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to MultiGBASE-A control codes and XGMII control codes are specified in Table 192–3.

Table 192–3—MultiGBASE-A control codes

Control character	Notation	XGMII control code	Control code	O code
idle	/I/	0x07	0x00	—
start	/S/	0xFB	Encoded by block type field	—
terminate	/T/	0xFD	Encoded by block type field	—
error	/E/	0xFE	0x1E	—
sequence ordered set	/Q/	0x9C	Encoded by block type field plus O code	0x0
reserved0	—	0x1C	0x2D	—
reserved1	—	0x3C	0x33	—
reserved2	—	0x7C	0x4B	—
reserved3	—	0xBC	0x55	—
reserved4	—	0xDC	0x66	—
reserved5	—	0xF7	0x78	—

reserved6	—	0x5C	Encoded by block type field plus O code	0xF
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192.3.2.2.6 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as Remote Fault and Local Fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 192–3 for the mappings.

NOTE—The format of the ordered sets specified in this subclause are identical to those used in 149.3.2.2.6.

192.3.2.2.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of four. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

NOTE—The idle control characters (/I/) specified in this subclause are identical to those used in 149.3.2.2.7.

192.3.2.2.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

NOTE—The start control character (/S/) specified in this subclause is identical to that used in 149.3.2.2.9.

192.3.2.2.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

NOTE—The terminate control character (/T/) specified in this subclause is identical to that used in 149.3.2.2.10.

192.3.2.2.10 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

NOTE—The ordered set control characters (/O/) specified in this subclause are identical to those used in 149.3.2.2.11.

192.3.2.2.11 Error (/E/)

The error control character /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 192.3.5.1.3 for further information.

NOTE—The error control character (/E/) specified in this subclause is identical to that used in 149.3.2.2.12.

192.3.2.2.12 Transmit process

The LS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. $L \times 30$ XGMII data transfers are encoded into an RS-FEC superframe. It takes $L \times 1040$ PMA_UNITDATA transfers to send an RS-FEC superframe of data.

The HS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. $L \times 30$ XGMII data transfers are encoded into an RS-FEC superframe. For 2.5 Gb/s and 5 Gb/s (5G+100) mode, it takes $L \times 1024$ PMA_UNITDATA PAM2 transfers to send an RS-FEC superframe of data. For 5 Gb/s (5G+1000) and 7.5 Gb/s (7.5G+100) mode, it takes $L \times 2/3 \times 1024$ PMA_UNITDATA PAM3 transfers to send an RS-FEC superframe of data. For 7.5 Gb/s (7.5G+1000) and 10 Gb/s mode, it takes $L \times 512$ PMA_UNITDATA PAM4 transfers to send an RS-FEC superframe of data.

Where the XGMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 192–22). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the RS-FEC encoder and scrambler. The bit tx_coded<0> contains the data/ctrl header and the remainder of the bits contain the block payload.

192.3.2.2.13 RS-FEC framing and RS-FEC encoder

15 65B blocks (tx_coded) are grouped together to form tx_group15x65B as described in 192.1.3.1. For LS_TX transmission, tx_group15x65B, followed by the 17-bit OAM/Reserved field and 48 parity bits, forms an RS-FEC frame of 1040 bits. See Figure 192–5 and 192.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

For HS_TX transmission, tx_group15x65B, followed by the 1-bit OAM/Reserved field and 48 parity bits, forms an RS-FEC frame of 1024 bits. See Figure 192–6 and 192.3.2.2.16 for details on PCS bit ordering

and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

192.3.2.2.14 RS-FEC superframe and round-robin interleaving

The interleaving depth, L, of the transmitter shall be predefined for each data rate and comply with Table 192–4. When L = 1, there is no interleaving and the RS-FEC superframe is the same as the RS-FEC frame. When L > 1, the round-robin interleaving scheme shown in Figure 192–8 shall be applied.

Table 192–4—Interleaving depth	
Transmit MAC data rate	Interleaving depth, L
100 Mb/s	1
1 Gb/s	2
2.5 Gb/s	1
5 Gb/s	2
7.5 Gb/s	3
10 Gb/s	4

The ~~HS_TX~~ PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. ~~In the LS_TX PCS There there~~ are ~~9276~~ × L bits, or ~~422-124~~ × L Reed-Solomon message symbols in total in the input superframe. ~~In the HS_TX PCS there are 976 × L bits, or 122 × L Reed-Solomon message symbols in total in the input superframe.~~ The corresponding message symbols are as follows:

~~$m_{122 \times L - 1}, m_{122 \times L - 2}, \dots, m_1, m_0$~~

~~Where k is the number of symbols in each RS-FEC frame.~~

These message symbols are distributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message symbols from the superframe. Otherwise, the RS-FEC encoder operates exactly the same as specified in 192.3.2.2.16.

192.3.2.2.15 RS-FEC recombine

The L encoded RS-FEC frames are combined into an interleaved RS-FEC superframe. The output symbols are as follows:

~~$m_{122 \times L - 1}, m_{122 \times L - 2}, \dots, m_1, m_0, p_{1,5}, \dots, p_{L,5}, \dots, p_{1,0}, \dots, p_{L,0}$~~

where $p_{i,r}$ is the r^{th} parity symbol of the i^{th} encoder and k is the number of message symbols.

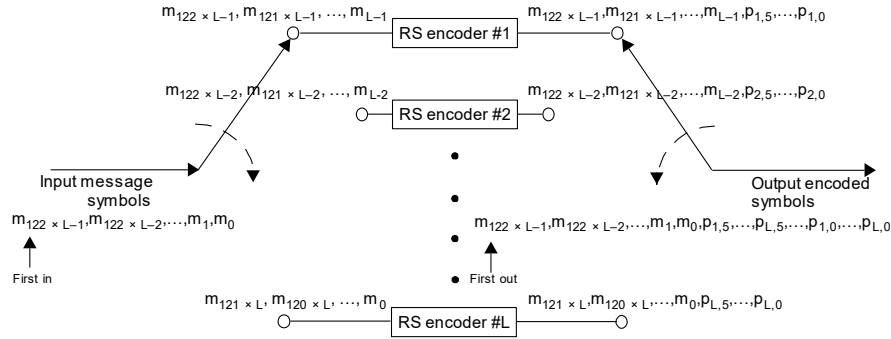


Figure 192-8—Interleaving block diagram with interleaving depth L

[Editing note for Figure 192-8: Replace “122” with “ k ”, and “121” with “ $k-1$ ” and “120” with “ $k-2$ ”]

192.3.2.2.16 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field $GF(2^8)$ where the symbol size is 8 bits. For the LS_PATH, the encoder processes 124 8-bit RS-FEC message symbols to generate six 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. For the HS_PATH, the encoder processes 122 8-bit RS-FEC message symbols to generate six 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 128 8-bit RS-FEC symbols. For the purposes of this clause, the Reed-Solomon code, $RS-FEC(n,k)$, is denoted as $RS-FEC(130,124)$ for the LS_PATH and $RS-FEC(128,122)$ for the HS_PATH.

The code is based on the generating polynomial shown in Equation (192-1).

(192-1)

$$g(x) = \prod_{j=0}^{n-k-1} (x - \alpha^j) = g_{n-k}x^{n-k} + g_{n-1-k}x^{n-1-k} + \dots + g_3x^3 + g_2x^2 + g_1x + g_0$$

In Equation (192-1), α is a primitive element of the finite field defined by the primitive polynomial $0x11D = x^8 + x^4 + x^3 + x^2 + 1$.

Equation (192–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols m_{k-1} to m_0 .

(192–2)

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \dots + m_1x^{n-k+1} + m_0x^{n-k}$$

Each message symbol m_i is the bit vector $(m_{i,7}, m_{i,6}, \dots, m_{i,1}, m_{i,0})$, which is identified with the element of the finite field. $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in $\text{tx_RSMessag}e\langle(8 \times k - 1):0\rangle$.

For LS_TX, $m_{i,j} = \text{tx_RSMessag}e\langle(123 - i) \times 8 + j\rangle$, for $i = 0$ to 123, and $j = 0$ to 7.

$\text{tx_RSMessag}e\langle 991:0\rangle$ prior to RS-FEC(130,124) encoder is formed as follows:

$\text{tx_RSMessag}e\langle 974:0\rangle = \text{tx_group15x65B}\langle 974:0\rangle$.
 $\text{tx_RSMessag}e\langle 991:975\rangle = \text{OAM_field}\langle 16:0\rangle$.

For HS_TX, $m_{i,j} = \text{tx_RSMessag}e\langle(121 - i) \times 8 + j\rangle$, for $i = 0$ to 121, and $j = 0$ to 7.

$\text{tx_RSMessag}e\langle 975:0\rangle$ prior to RS-FEC(128,122) encoder is formed as follows for $L = 1$ (see 192.3.2.2.14):

$\text{tx_RSMessag}e\langle 974:0\rangle = \text{tx_group15x65B}\langle 974:0\rangle$.
 $\text{tx_RSMessag}e\langle 975\rangle = \text{OAM_field}\langle 0\rangle$.

For $L > 1$, see 192.3.2.2.14 and 192.3.2.2.15.

The first symbol input to the encoder is m_{k-1} .

Equation (192–3) defines the parity polynomial $p(x)$ whose coefficients are the message symbols p_{n-k-1} to p_0 .

(192–3)

$$p(x) = p_{n-k-1}x^{n-k-1} + p_{n-k-2}x^{n-k-2} + \dots + p_2x^2 + p_1x + p_0$$

Each parity symbol p_i is the bit vector $(p_{i,7}, p_{i,6}, \dots, p_{i,1}, p_{i,0})$, which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation shown in Figure 192–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, m_0 , is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of x (e.g., $c_{n-1} = m_{k-1}$) is transmitted first and the coefficient of the lowest power of x (e.g., $c_0 = p_0$) is transmitted last. The first bit transmitted from each symbol is bit 0.

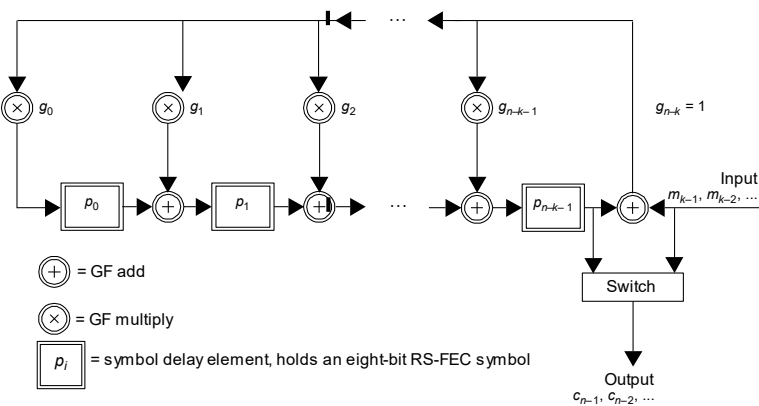


Figure 192-9—Reed-Solomon encoder functional model

The coefficients of the generator polynomial for the code are presented in Table 192-5

Table 192-5—Coefficients of the generator polynomial g_i (decimal)

i	RS-FEC(130,124)	RS-FEC(128,122)
0	38	38
1	227	227
2	32	32
3	218	218
4	1	1
5	63	63
6	1	1

192.3.2.2.17 PCS scrambler

Different scramblers are used for the refresh header and for the burst payload (see 192.3.4). The scrambled refresh header data bit, C_n , shall be as in Equation (192-4). Refresh header data bits are mapped to PAM2 symbols for all data rates.

(192-4)

$$C_n = \begin{cases} DS_n[0] \oplus TF_n & \text{tx_mode} \neq \text{SEND_N} \\ DS_n[0] \oplus D_n[0] & \text{tx_mode} = \text{SEND_N} \end{cases} \quad 0 \leq n \leq N_r - 1$$

where

$DS_n[0]$ is produced using the scrambler defined in 192.3.2.2.18

~~PAM2 or PAM3 symbols are used for rates less than 10 Gb/s.~~ The scrambled payload bits, A_n , for PAM2 and PAM3 are shown in Equation (192-5). Bit $DS_n[0]$ is produced using the scrambler defined in 192.3.2.2.19. It is applied as an additive scrambler sequence to incoming data bit $D_n[0]$ (LSB) to generate the scrambled data bit, A_n .

(192-5)

$$A_n = \begin{cases} DS_n[0] \oplus TF_n & \text{tx_mode} \neq \text{SEND_N} \\ DS_n[0] \oplus D_n[0] & \text{tx_mode} = \text{SEND_N} \end{cases} \quad N_r \leq n \leq N_r + N_p - 1$$

For 10 Gb/s and 7.5 Gb/s

interfaces using PAM4 coding, the burst data bits of the interleaved RS-FEC superframe are grouped into pairs. Each pair of bits, $D_n[0]$ and $D_n[1]$, where n is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the PCS scrambler. The first bit, which is the least significant bit (LSB), is $DS_n[0]$ equal to $Scr_n[0]$. The second bit, which is the most significant bit (MSB), is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$. Bits $DS_n[0]$ and $DS_n[1]$ in Equation (192-6) and Equation (192-7) are produced using the scrambler defined in 192.3.2.2.19. They are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$. PAM4 is only used when the tx_mode value is SEND_N.

(192-6)

$$A_n = \begin{cases} DS_n[0] \oplus D_n[0] & \text{tx_mode} = \text{SEND_N} \end{cases} \quad N_r \leq n \leq N_r + N_p - 1$$

(192-7)

$$B_n = \begin{cases} DS_n[1] \oplus D_n[1] & \text{tx_mode} = \text{SEND_N} \\ & N_r \leq n \leq N_r + N_p - 1 \end{cases}$$

192.3.2.2.18

1 scrambler polynomial

PRBS1

The refresh header specified in 192.3.4 is scrambled from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 192–10. The pattern generator is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 11-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. The scrambler state shall not be initialized to all zeros. This scrambler, once started during PMA training, shall continue to run uninterrupted during the refresh headers of each frame and shall stop during the burst payload field and QUIET. This implements the generator polynomial shown in Equation (192–8), which is the same as Equation (72–1).

(192–8)

$$G(x) = 1 + x^9 + x^{11}$$

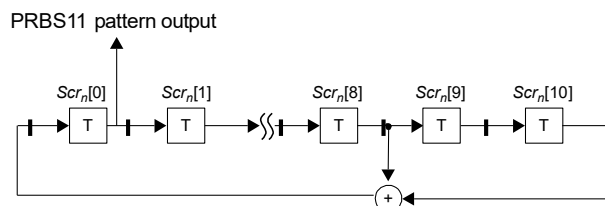


Figure 192–10—PRBS11 pattern generator

192.3.2.2.19 PRBS33 scrambler polynomials

The PCS Transmit function employs additive scrambling. If the management parameter config provided to the PCS assumes the value LEADER, PCS Transmit shall employ Equation (192–9) as the transmitter scrambler generator polynomial.

(192–9)

$g_L(x) = 1 + x^{13} + x^{33}$ If management parameter config assumes the value FOLLOWER, PCS Transmit shall employ Equation (192–10) as the transmitter scrambler generator polynomial.

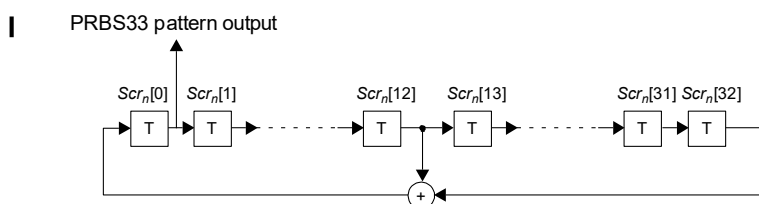
(192–10)

$g_F(x) = 1 + x^{20} + x^{33}$ An implementation of the Leader PCS and Follower PCS transmitter scramblers by linear-feedback shift registers is shown in Figure 192–11. The bits stored in the shift register delay line at time n are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter scrambler is reset upon execution of the PCS

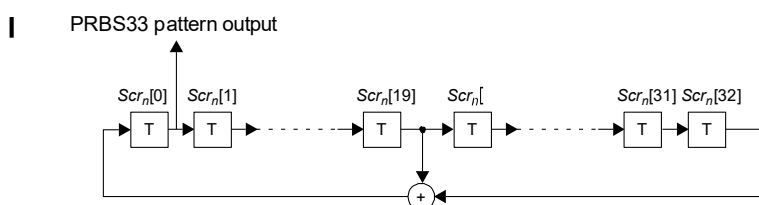
Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. The scrambler state shall not be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the payload of PMA training frames and data mode frames and shall stop during QUIET and refresh headers.

PCS scrambler employed by the ~~header~~ transmitter



PCS scrambler employed by the ~~header~~ transmitter



NOTE —The output shown corresponds to $Scr_n[0]$. The outputs corresponding to $Scr_n[3]$ and $Scr_n[8]$ are not shown.

Figure 192–11—Realization of PCS scramblers by linear feedback shift registers

192.3.2.2.20 Gray mapping for PAM4 encoding

When ~~transmitting-operating~~ at 10 Gb/s ~~or 7.5G+1000 and transmitting~~ in the PAM4 transmission period, the PCS Transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where A_n is the bit arriving first, and n is an index indicating the symbol number, to Gray-coded symbols, $G(n)$, with one of four levels as follows:

- $\{0, 0\}$ maps to 0,
- $\{0, 1\}$ maps to 1,
- $\{1, 1\}$ maps to 2, and
- $\{1, 0\}$ maps to 3.

When ~~receiving-operating~~ at 10 Gb/s ~~or 7.5G+1000 and receiving~~ in the PAM4 transmission period, the PCS Receive process shall map Gray-coded symbols, $G(n)$, with one of four levels, to pairs of bits, $\{A_n, B_n\}$, where A_n is considered to be the first bit as follows:

- 0 maps to $\{0, 0\}$,
- 1 maps to $\{0, 1\}$,
- 2 maps to $\{1, 1\}$, and
- 3 maps to $\{1, 0\}$.

192.3.2.2.21 PAM4 encoding

When ~~transmitting-operating~~ at 10 Gb/s or 7.5G+1000 and transmitting in the PAM4 transmission period, the PCS Transmit process shall encode each Gray-coded symbol, $G(n)$, to one of four PAM4 levels as specified in this clause.

The PAM4 encoded symbols are denoted $M(n)$, where n is an index indicating the symbol number.

Each consecutive Gray-coded symbol, $G(n)$, is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output, $M(n)$.

Mapping from the Gray-coded symbol, $G(n)$, to a PAM4 encoded symbol, $M(n)$, is as follows:

- 0 maps to -1 ,
- 1 maps to $-1/3$,
- 2 maps to $+1/3$, and
- 3 maps to $+1$.

192.3.2.2.22 PAM3 encoding

3B2T encoding is used to map a group of three consecutive bits into a consecutive pair of three-level (ternary) PAM3 symbols as specified in this clause. When ~~transmitting-operating~~ at 7.5G+100 7.5-Gb/s or 5G+1000 and transmitting in the PAM3 transmission period, the PCS Transmit process shall encode each of the two PAM3 symbols in the ternary pair $T[1]$, $T[0]$ into the appropriate PAM3 level.

The 3B2T mapping into PAM3 symbols is shown in Table 192–6. $B[0]$ is the first of the three bits received by the mapper (i.e., the LSB of the trio) and $T[0]$ is the first PAM3 ternary symbol of the pair to be transmitted.

Table 192–6—3B2T mapping

Three-bit groups $B[2]$, $B[1]$, $B[0]$	PAM3 ternary symbol pairs $T[1]$, $T[0]$
000	-1 , -1
001	0 , -1
010	-1 , 0
011	-1 , $+1$
100	$+1$, 0
101	$+1$, -1
110	$+1$, $+1$
111	0 , $+1$

192.3.2.2.23 PAM2 mapping

During the PAM2 transmission period, the PCS Transmit process sends out PAM2 symbols according to the following mapping:

Input bit S_n is mapped to the transmit symbol T_n as follows:

if $S_n = 0$, then $T_n = -1$, and
if $S_n = 1$, then $T_n = +1$.

192.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 192–23 and the PCS Receive bit ordering in Figure 192–12 for the LS_RX and Figure 192–13 and Figure 192–14 for the HS_RX, including compliance with the associated state variable as specified in 192.3.5.1.2.

The PCS Receive function accepts received symbols provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM2, PAM3, or PAM4 symbols are demapped and descrambling is performed.

Following descrambling, the L -interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For LS_RX, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks. For HS_RX, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each data payload, the ~~25-received RS-FEC~~ superframes can form a ~~17-bit OAM field for 100 Mb/s mode, a 204-bit OAM field for 1 Gb/s mode, a 25-bit OAM field for 2.5 Gb/s mode, a 50-bit OAM field for 5 Gb/s mode using PAM2, a 54-bit OAM field for 5 Gb/s mode using PAM3, a 75-bit OAM field for 7.5 Gb/s mode using PAM3, a 78-bit OAM field for 7.5 Gb/s mode using PAM4, and a 100-bit OAM field for 10 Gb/s mode.~~

~~Vendor-specific RS-FEC blocks and padding at the end of the 5 Gb/s PAM3 or 7.5Gb/s PAM4 bursts are removed from the stream while groups of 15 64B/65B blocks continue towards the XGMII.~~

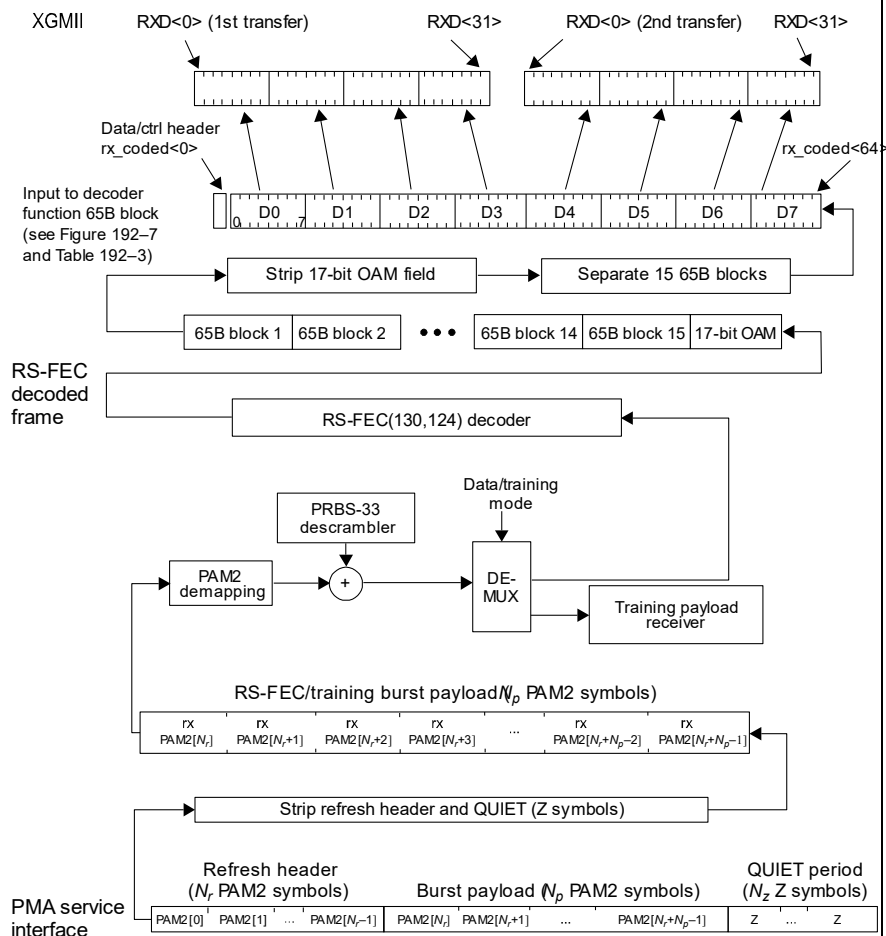
Groups of 15 64B/65B blocks are then separated into individual 64B/65B blocks. The PCS Receive function generates the 64B/65B block vector rx_coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 192–23). Two XGMII data transfers are decoded from each block. Because the received data stream is divided into TDD bursts with silence interspersed, the PCS receive function recombines separated bursts before passing to the XGMII. When the XGMII and PMA sublayer data rates are not frequency synchronized, the PCS receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and indicates that the PCS descrambler state has been acquired by setting the scr_status parameter PMA_SCRSTATUS.request primitive to OK. Descrambler acquisition is a prerequisite to RS-FEC block lock and should be robust to bit errors without RS-FEC.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame

errors. If 40 consecutive RS-FEC frame errors are detected, the `block_lock` is de-asserted. The `block_lock` is re-asserted upon detection of a valid RS-FEC frame. When `block_lock` is asserted and `hi_rfer` is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receiver is in training mode, the PCS Synchronization process continuously monitors `PMA_RXSTATUS.indication(loc_rcvr_status)`. When `loc_rcvr_status` indicates OK, then the PCS Synchronization process accepts data-units via the `PMA_UNITDATA.indication` primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process when PHY Control is in `PCS_TEST` or `PCS_DATA` state. The PCS Synchronization process sets the `block_lock` to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header (see 192.3.4). It also includes training payload which has an Infocfield, inserted in the N_{inf}^{th} bit of the training payload (see 192.3.4.3). When the PCS Synchronization process is synchronized to this pattern, `block_lock` is asserted.



NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

Figure 192-12—IS_RX RS Receive bit ordering

[Editing notes for Figure 192-12:

1. Add a block ahead of the RS-FEC(130, 124) decoder block labelled “Separate RS-FEC superframes”, similar to the block in Figure 192-13.
2. Following the Data/training mode DEMUX block insert a block that removes the end of burst padding for 5 Gb/s PAM3 and 7.5 Gb/s PAM4 reception.

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3. Following the RS-FEC(130, 124) decoder add a block that removes the vendor specific RS-FEC decoded frames.
4. Add note that this figure is shown for L=1
5. Add “De-interleaver and” to RS-FEC(130, 124) decoder block.]

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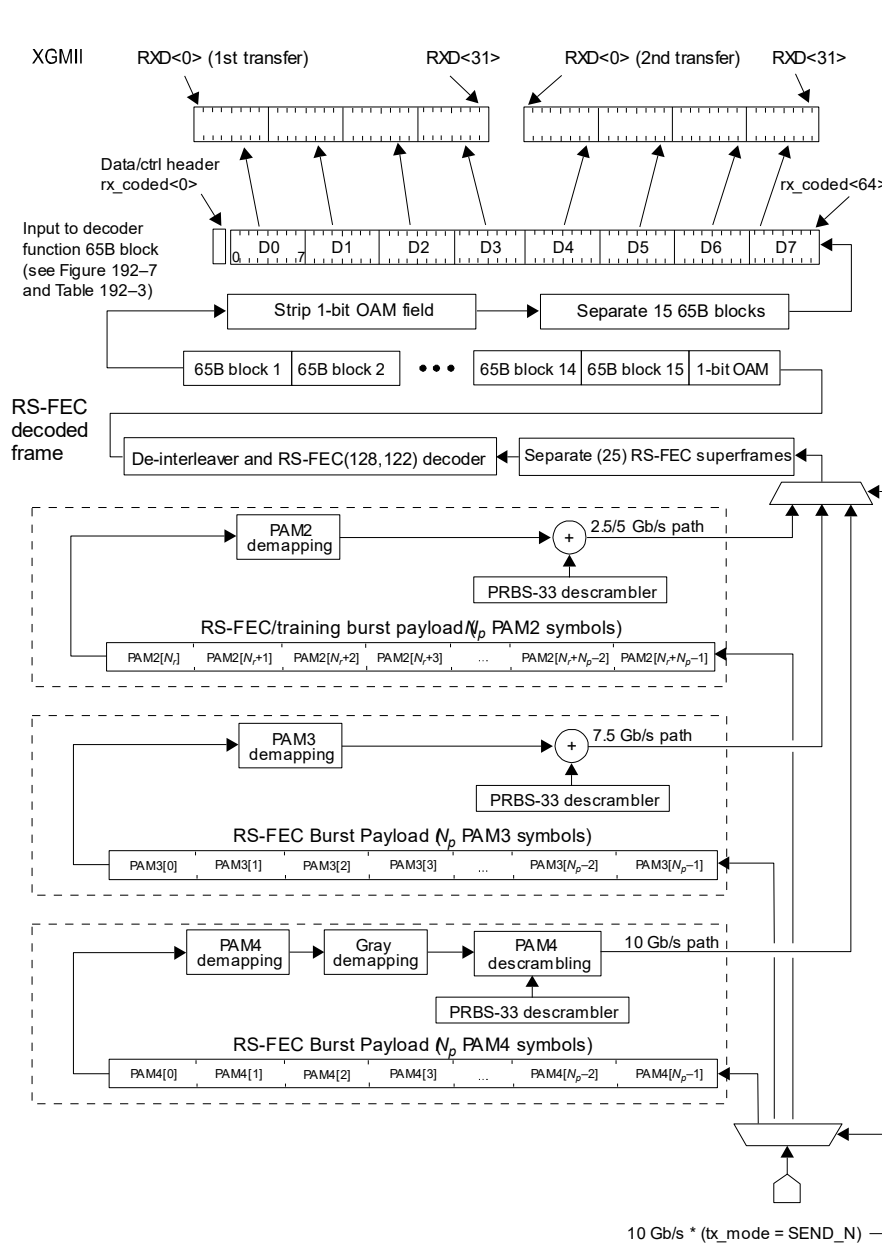


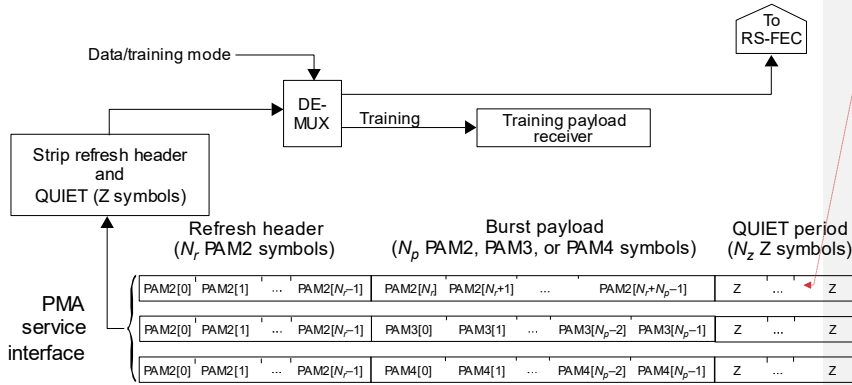
Figure 192-13—IS_RX RS Receive bit ordering, part a

[Editing notes for Figure 192-13:

1. Delete the (25) on the “Separate (25) RS-FEC superframes”.
2. For 5 Gb/s using PAM3 and 7.5 Gb/s using PAM4 add a block after the De-Interleaver and RS-FEC(128, 122) decoder which strips a set of L x 976-bit vendor-specific message after every 25 Lx976-bit messages into the input of the RS-FEC encoder block. The size of the set is 1 for 7.5 Gb/s PAM4 and 2 for 5 Gb/s PAM3.
3. For 5 Gb/s using PAM3 and 7.5 Gb/s using PAM4 add a note for the block which separates RS-FEC superframes this block can also strip the extended payload vendor-specific 726 or 200 bytes of padding for 5Gb/s or 7.5Gbps respectively, so label it as “Separate RS-FEC superframes and remove vendor-specific padding”.
4. Add notes indicating the vendor-specific RS_FEC superframes and padding are only present for 5Gb/s PAM3 and 7.5Gb/s PAM4.]

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NOTE 1—Figure 192-13 and Figure 192-14 show the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

NOTE 2—Figure 192-13 and Figure 192-14 show n for L = 1.

NOTE 3—Either the PAM2, PAM3, or PAM4 path and TDD frame at the PMA service interface is used. PAM3 path (and the middle TDD frame shown) is chosen if the bit rate is 7.5 Gb/s and tx_mode = SEND_N. PAM4 path (and the lowest TDD frame shown) is chosen if the bit rate is 10Gb/s and tx_mode = SEND_N.

Figure 192-14—HS_RX PCS Receive bit ordering, part b

[Editing note for 192-14: Update NOTE 3 to specify PAM3 path is used for 100+7.5G and 1000+5G. PAM4 path is used for 10Gb/s and 1000+7.5G.]

192.3.2.3.1 Frame and block synchronization

When operating in 100 Mb/s, 1 Gb/s, 2.5 Gb/s, or 5 Gb/s data mode using PAM2, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from PAM2[N_r] to PAM2[N_r + N_p - 1] (see Figure 192-12 for LS_RX or Figure 192-13 and Figure 192-14 for HS_RX). When operating in 5Gb/s or 7.5 Gb/s data mode using PAM3, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from PAM3[0] to PAM3[N_p - 1] (see Figure 192-12 for LS_RX or Figure 192-13 for HS_RX). When operating in 7.5 Gb/s or 10 Gb/s data mode using PAM4, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from PAM4[0] to PAM4[N_p - 1] (see Figure 192-13 and Figure 192-14).

The receiving PCS obtains block_lock to the PHY frames during training using synchronization sequence and Infocfield provided in the training frames.

192.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process.

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for generation of RXD<31:0> to the XGMII. For descrambling, the Leader PHY shall employ the receiver descrambler generator polynomial per Equation (192–10) and the Follower PHY shall employ the receiver descrambler generator polynomial per Equation (192–9).

192.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

- a) The block type field contains a reserved value.
- b) Any control character contains a value not in Table 192–3.
- c) Any O code contains a value not in Table 192–3.
- d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 192.3.2.2.13. If the check fails, the RS-FEC frame is invalid. The R_BLOCK_TYPE of an invalid block is set to E.

192.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, channel, and remote receiver.

When the transmit PCS is operating in test-pattern mode, the input to the RS-FEC encoder (see Figure 192–5 or Figure 192–6) is set to zero and the initial condition of the PCS scrambler set to any non-zero value. This has the same effect as setting the input to the PCS scrambler to zero.

When the receiver PCS is operating in test-pattern mode, the received information is processed as shown in Figure 192–12 or Figure 192–13 and Figure 192–14. In the absence of errors in PMA Receive, the descrambler output should be zeros. The output of the RS-FEC decoder should also be zeros, and may correct errors in the descrambler output. Any nonzero values at the output of the RS-FEC decoder are due to uncorrectable RS-FEC frames. This mode is further described as test mode 7 in 192.5.1.

192.3.4 PCS TDD signaling

The PCS generates symbols to be transmitted by the PMA in the form of TDD bursts. TDD burst structure depends on the value of tx_mode and the data rate of transmission. Each TDD burst is comprised of a refresh header and payload followed by a QUIET period. During startup, the PCS transmits TDD bursts in two different formats for the tx_mode values SEND_TS and SEND_TA, before finally switching to SEND_N. SEND_TS uses a symmetric frame format and shall transmit at 3 GBd. PHY data rate and direction may be negotiated during the SEND_TS phase. SEND_TA and SEND_N use an asymmetric frame format, and transmit at either 3 GBd or 6 GBd depending on the selected transmitter rate. QUIET periods (i.e., when the PCS inserts Z symbols) are introduced between TDD bursts. The duration of each QUIET period depends on the state of tx_mode [and operating data rate](#).

The refresh header is a sequence of PAM2 symbols with length of N_r symbols. The refresh header bits are all zeros except for the final 64 bits (see 192.3.4.2).

An 11-bit scrambler (see 192.3.2.2.18) is used to scramble the refresh header. This scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

The burst payload is a sequence of symbols with length of N_p symbols.

The training payload data sequence bits are all zeros, with the exception of a 96-bit Infocfield started at the N_{inf} th symbol of the training payload (see Figure 192–15). The Infocfield is used to exchange messages between link partners during startup. The training data sequence, TF_n , is defined in Equation (192–11). Training payloads are sent when tx_mode is SEND_TS or SEND_TA.

The data mode burst payload consists of RS-FEC superframes that are sent when tx_mode is SEND_N.

The 33-bit scrambler (see 192.3.2.2.19) is used to scramble the payload. Once started at the beginning of the training payload of the first training burst, this scrambler shall continue to run uninterrupted for each symbol during all subsequent payloads and shall maintain its last state during the QUIET period and refresh headers.

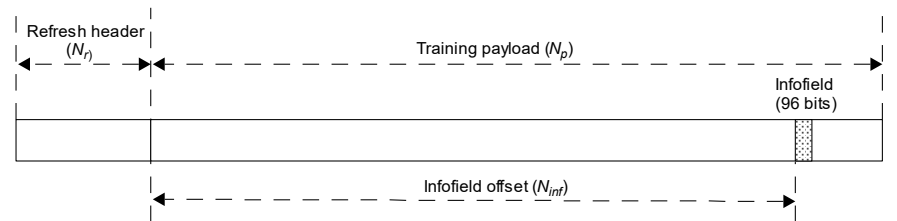
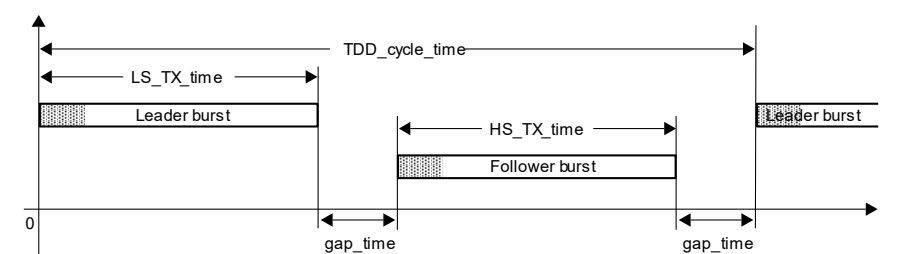


Figure 192–15—IMA Training frame

The timing diagram in Figure 192–16 shows the TDD cycle signaling and TDD frame structures assuming the LS_TX is configured as the Leader and the HS_TX is configured as the Follower. Table 192–7 specifies the LS_TX and HS_TX transmit times in each TDD cycle.



NOTE 1—TDD_cycle_time is the nominal 9.6 μs TDD cycle time.
NOTE 2—gap_time is the time between the start of QUIET at one MDI output and end of QUIET at the other MDI output. gap_time is a result of the alignment of the two ends, so is not specified.

Figure 192–16—Leader/Follower TDD cycle illustration

Table 192–7—TDD cycle timing

tx_mode	LS_TX_time (ns)	HS_TX_time (ns)	Total gap_time per cycle (ns)	TDD cycle time (ns)
SEND_TS	4480	4480	640	9600

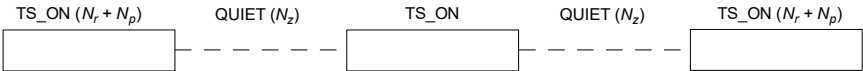
SEND_TA	554.67	8693.33	352	
SEND_N				

[Editing note for Table 192-7:

1. SEND_TA and SEND_N times currently in the table apply when LS path is operating at 100 Mb/s. Add to those cells to indicate path operating at 100 Mb/s.
2. Add 2 additional rows for SEND_TA and SEND_N for LS path operating at 1 Gb/s with LS_TX time of 2298.67 ns and HS_TX time of 6949.33 ns. Total gap time remains 352 ns and TDD cycle time remains 9600 ns.

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The symmetric training burst timing and structure are shown in Figure 192–17. TS_ON indicates a symmetric training burst and QUIET (N_z) indicates the QUIET period between bursts when Z symbols are transmitted by the PHY



NOTE—The parameters for SEND_TS are used for N_r , N_p , and N_z (see Table 192–9, Table 192–10, and Table 192–11).

Figure 192–17—Symmetric training timing and frame structure

Figure 192–18 shows the LS_TX timing and frame structure for both the data mode and the asymmetric training modes. TA_ON indicates an asymmetric training burst and QUIET (N_z) indicates the QUIET period between bursts when Z symbols are transmitted by the PHY. The refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 192.3.4. Note that FEC is not used with the training payload.

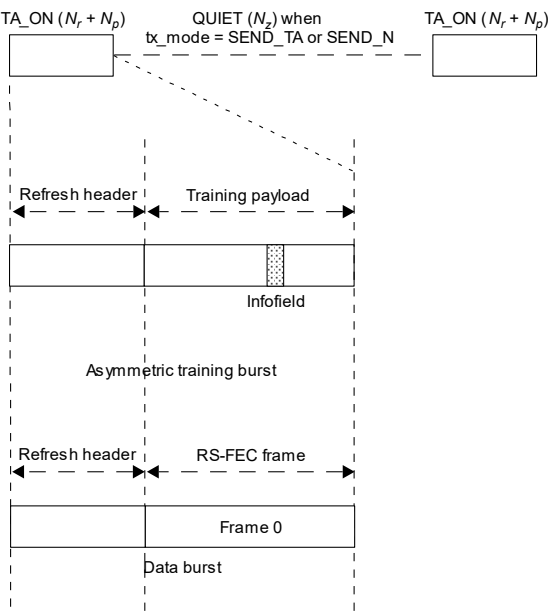


Figure 192-18—Asymmetric training/Data Mode timing and frame structure—LS_TX

Figure 192–19 shows the HS_TX timing and frame structure for both the data mode and the asymmetric training modes. As with the LS_TX direction, the refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 192.3.4 and FEC is not used with the training payload.

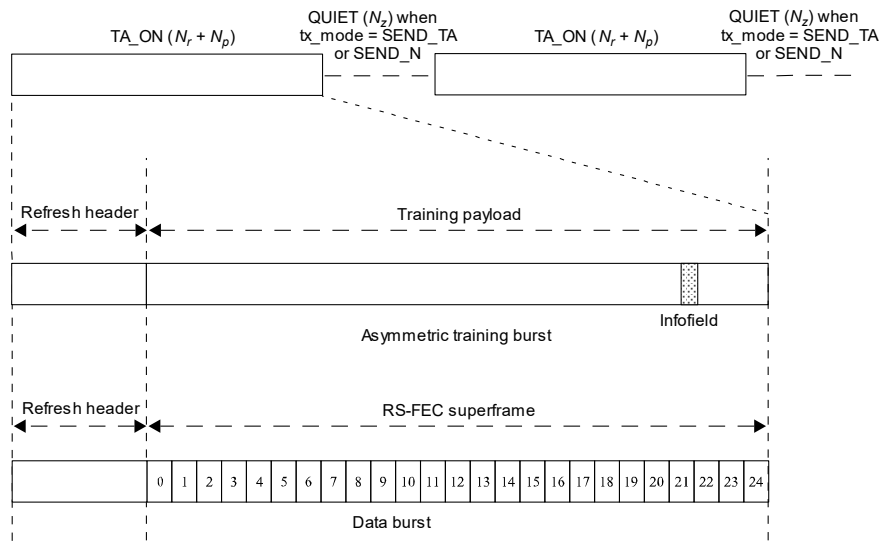


Figure 192–19—Asymmetric training/Data Mode timing and frame structure—HS_TX

The burst payload structures are illustrated in Figure 192–20. Data burst payload information is summarized in Table 192–8.

The data burst structures associated with 1 Gb/s LS and the corresponding 5 Gb/s HS and 7.5 Gbps HS (see Figure 192-hh section b) include padding at the end of the data burst payload area and there is capacity remaining in the last RS-FEC block of the data payload area. The content of the unused RS-FEC block payload bits and the padding fields are vendor specified and outside the scope of IEEE 802.3.

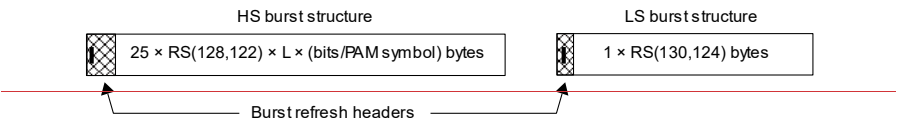


Figure 192–20—Illustration of the data burst payload structure

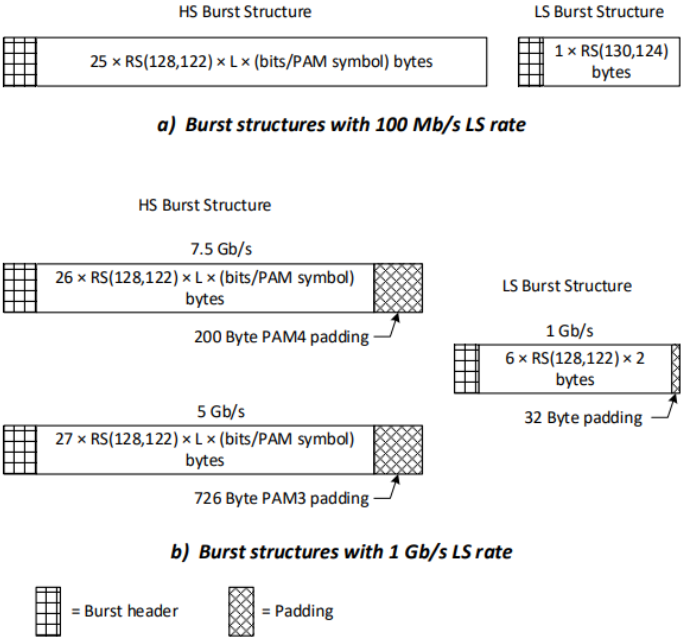


Figure 192-hh – Illustration of the data burst payload structure

[Editing note: Update Figures 192-18, 192-19, and 192-20 as per Figure 192-hh in https://www.ieee802.org/3/dm/public/0726/chini_3dm_02a_D2d0_1G_comments-preview.pdf, using 8 byte padding instead of 32 byte padding and RS(130, 124) instead of RS(128, 122) for the 1 Gb/s LS Burst structure.]

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Table 192–8—Data burst payload summary information

HS burst payload					LS burst payload				
Burst payload rate (Gb/s)	Baud (GBd)	PAM levels	L (Inter-leave depth)	Number of burst payload symbols	Burst payload rate (Mb/s)	Baud (GBd)	PAM levels	L (Inter-leave depth)	Number of burst payload symbols
2.5	3	2	1	25 600	100	3	2	1	1040
5	6	2	2	51 200					
7.5		3	3						

10		4	4						
<u>5G</u>		<u>3</u>	<u>2</u>	<u>40 736*</u>	<u>1000</u>	<u>6</u>	<u>2</u>	<u>2</u>	<u>12 544*</u>
<u>7.5G</u>		<u>4</u>	<u>3</u>	<u>40 736*</u>	<u>1000</u>	<u>6</u>	<u>2</u>	<u>2</u>	<u>12 544*</u>
<u>*Including padding</u>									

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192.3.4.1 Refresh header, payload, and QUIET period length

The lengths for refresh header (N_r) and payload (N_p) are described in Table 192–9, Table 192–10, and Table 192–11. The length of the QUIET period (N_z) in Table 192–9, Table 192–10, and Table 192–11 is the number of Z symbols sent to complete the TDD cycle.

NOTE—The durations for N_r , N_p , and N_z (expressed in symbols) in Table 192–9 and Table 192–10 correspond to the durations (expressed in ns) in Table 192–7.

Table 192–9— N_r , N_p , and N_z values for 100 Mb/s mode transmission

tx_mode	refresh header N_r (symbols)	payload N_p (symbols)	QUIET N_z (symbols)
SEND_TS	560	12 880	15 360
SEND_TA	624	1040	27 136
SEND_N	624	1040	27 136
NOTE—All symbols are sent at 3 GBd.			

Table 192-9a N_r , N_p , and N_z values for 1 Gb/s mode transmission

<u>tx_mode</u>	<u>refresh header</u> <u>N_r</u> (symbols)	<u>payload</u> <u>N_p</u> (symbols)	<u>QUIET</u> <u>N_z</u> (symbols)
<u>SEND_TS</u>	<u>560</u>	<u>12 880</u>	<u>15 360</u>
<u>SEND_TA</u>	<u>1248</u>	<u>12 544</u>	<u>43 808</u>
<u>SEND_N</u>	<u>1248</u>	<u>12 544</u>	<u>43 808</u>
<u>NOTE—SEND_TS symbols are sent at 3 GBd. SEND_TA and SEND_N symbols are sent at 6 GBd.</u>			

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Table 192-9b N_r , N_p , and N_z values for 5 Gb/s and 7.5Gb/s mode transmission with 1 Gb/s LS PATH

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<u>tx_mode</u>	<u>refresh header</u> <u>N_r</u> <u>(symbols)</u>	<u>payload</u> <u>N_p</u> <u>(symbols)</u>	<u>QUIET</u> <u>N_z</u> <u>(symbols)</u>
<u>SEND_TS</u>	<u>560</u>	<u>12 880</u>	<u>15 360</u>
<u>SEND_TA</u>	<u>960</u>	<u>40 736</u>	<u>15 904</u>
<u>SEND_N</u>	<u>960</u>	<u>40 736</u>	<u>15 904</u>
<u>NOTE—SEND_TS symbols are sent at 3 GBd. SEND_TA and SEND_N symbols are sent at 6 GBd.</u>			

Table 192–10— N_r , N_p , and N_z values for 2.5 Gb/s mode transmission

tx_mode	refresh header N_r (symbols)	payload N_p (symbols)	QUIET N_z (symbols)
SEND_TS	560	12 880	15 360
SEND_TA	480	25 600	2720
SEND_N	480	25 600	2720
NOTE—All symbols are sent at 3 GBd.			

Table 192–11— N_r , N_p , and N_z values for 5 Gb/s, 7.5 Gb/s, and 10 Gb/s mode transmission with 100 Mb/s LS PATH

tx_mode	refresh header N_r (symbols)	payload N_p (symbols)	QUIET N_z (symbols)
SEND_TS	560	12 880	15 360
SEND_TA	960	51 200	5440
SEND_N	960	51 200	5440
NOTE—SEND_TS symbols are sent at 3 GBd. SEND_TA and SEND_N symbols are sent at 6 GBd.			

192.3.4.2 Refresh header and payload data bits generation

The refresh header shall be composed of a leading sequence of zeros followed by four bytes of 0x01, followed by four bytes of 0xF0. The refresh header bits are scrambled with the PRBS11 scrambler defined in 192.3.2.2.18. The PRBS11 scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

N_p payload bits follow the refresh header in each burst. The payload bits are scrambled with the PRBS33 scrambler defined in 192.3.2.2.19.

The training frame contents are specified in Equation (192–11). N_{inf} is the bit position where Infofield starts within the training payload. The training frame starts at bit zero, with $0 \leq n \leq N_r - 1$ consisting of the refresh header as shown in Equation (192–11). Per Equation (192–11), TF_n is all zeros from the end of the refresh header to the beginning of the Infofield, followed by the 96-bit Infofield, then followed by all zeros from the end of the Infofield to the end of the training payload, which is the end of the training frame.

(192–11)

$$TF_n = \begin{cases} refresh_header(n) & 0 \leq n \leq N_r - 1 \\ 0 & N_r \leq n \leq N_r + N_{inf} - 1 \\ Infofield(n - [N_r + N_{inf}]) & N_r + N_{inf} \leq n \leq N_r + N_{inf} + 95 \\ 0 & N_r + N_{inf} + 96 \leq n \leq N_r + N_p - 1 \end{cases} \text{ where}$$

N_{inf} is equal to $N_p - 256$

192.3.4.3 PAM mapping and generation of TDD bursts

Except when transmitting 5 Gb/s PAM3, 7.5 Gb/s ~~or~~ 10 Gb/s payload symbols and tx_mode is SEND_N, bits are encoded by the PAM2 mapper defined in 192.3.2.2.23. When transmitting 5 Gb/s PAM3 or 7.5 Gb/s PAM3 payload symbols and tx_mode is SEND_N, bits are encoded by the PAM3 encoder defined in 192.3.2.2.22. When transmitting 7.5 Gb/s PAM4 or 10 Gb/s payload symbols and tx_mode is SEND_N, bits are encoded by the Gray-coded PAM4 encoder defined in 192.3.2.2.20 and 192.3.2.2.21. Z symbols are sent between each TDD burst frame to form the sequence O_n , as defined in Equation (192–12). The values of O_n are then conveyed to the PMA for transmission via the parameter tx_symb of the PMA_UNITDATA.request primitive.

The transmit symbol O_n is selected by TDD control logic. For each TDD cycle (specified in 192.3.4), the Transmit function will send out T_n or Z symbols to the PMA, based on symbol time index n .

$$(192-12) \quad O_n = \begin{cases} T_n & 0 \leq n \leq N_r + N_p - 1 \\ Z & N_r + N_p \leq n \leq N_{TDD} - 1 \end{cases}$$

where

n is the continuous symbol count modulo N_{TDD}
 N_{TDD} is the number of symbols equivalent to a nominal 9.6 μ s TDD cycle time

T_n is the output of the PAM2, PAM3, or PAM4 Mapper as defined in Equation (192-13).

$$(192-13) \quad T_n = \begin{cases} PAM2_Mapper(A_n) & \begin{aligned} &tx_rate = 100 \text{ Mb/s OR } tx_rate = 2.5 \text{ Gb/s OR} \\ &tx_rate = 5 \text{ Gb/s OR } !(tx_mode = SEND_N) \text{ OR} \\ &(0 \leq n \leq N_r - 1) \end{aligned} \\ PAM3_Mapper(A_n) & \begin{aligned} &tx_rate = 7.5 \text{ Gb/s AND } tx_mode = SEND_N \text{ AND} \\ &(N_r \leq n \leq N_r + N_p - 1) \end{aligned} \\ PAM4_Mapper(G_n) & \begin{aligned} &tx_rate = 10 \text{ Gb/s AND } tx_mode = SEND_N \text{ AND} \\ &(N_r \leq n \leq N_r + N_p - 1) \end{aligned} \end{cases}$$

[Editing notes for (192-13):

1. For PAM2_Mapper change to tx_rate = 100 Mb/s OR tx_rate = 1 Gb/s OR tx_rate = 2.5 Gb/s OR tx_rate = 5 Gb/s AND rx_rate = 100 Mb/s OR !(tx_mode = SEND_N) OR (0 <= n <= Nr-1)
2. For PAM3_Mapper change to tx_rate = 5 Gb/s AND rx_rate = 1 Gb/s OR tx_rate = 7.5 Gb/s AND rx_rate = 100 Mb/s AND tx_mode = SEND_N AND (Nr <= n <= Nr+Np-1)
3. For PAM4 Mapper change “tx_rate = 10 Gb/s” to “(tx_rate = 7.5 Gb/s AND rx_rate = 1 Gb/s OR tx_rate = 10 Gb/s)”

where

A_n is specified in 192.3.2.2.20
 G_n is the Gray-coded symbol specified in 192.3.2.2.20
 $PAM2_Mapper$ is specified in 192.3.2.2.23
 $PAM3_Mapper$ is specified in 192.3.2.2.22
 $PAM4_Mapper$ is specified in 192.3.2.2.21
 tx_rate is the selected transmit data rate

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192.3.4.4 PCS descrambler polynomials

The PCS shall acquire descrambler state synchronization to the PAM2 training sequence and report success through `scr_status`, and continue to use the synchronized state in all subsequent bursts in both data and training modes. The Follower PCS employs the receiver descrambler generator polynomial per Equation (192–9) and the Leader PCS employs the receiver descrambler generator polynomial per Equation (192–10).

192.3.5 PCS Detailed functions and state diagrams

192.3.5.1 State diagram parameters

192.3.5.1.1 Constants

`EBLOCK_R<71:0>`

72-bit vector to be sent to the XGMII interface containing `/E/` in all the eight character locations.

`EBLOCK_T<64:0>`

65-bit vector to be sent to the RS-FEC encoder containing `/E/` in all the eight character locations.

`LBLOCK_R<71:0>`

72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in [46.3.4](#).

`LBLOCK_T<64:0>`

65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

`IBLOCK_R<71:0>`

72-bit vector to be sent to the XGMII containing `/I/` in all the eight character locations.

`IBLOCK_T<64:0>`

65-bit vector to be sent to the RS-FEC encoder containing `/I/` in all the eight character locations.

`RFER_CNT_LIMIT`

TYPE: Integer

VALUE: 16

Number of Reed-Solomon frames with uncorrectable errors.

`RFRX_CNT_LIMIT`

TYPE: Integer

VALUE: 88

Number of Reed-Solomon frames received over bit error ratio interval.

`UBLOCK_R<71:0>`

72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets. The Link Interruption ordered set is defined in [46.3.4](#).

192.3.5.1.2 Variables

block_lock

Boolean variable that is set TRUE while the receiver is able to delineate the received burst payload boundaries. Otherwise set to FALSE.

hi_rfer

Boolean variable. See Figure 192–21. Set to TRUE when the received FEC frame uncorrectable error rate is high, and set to FALSE when the received FEC frame uncorrectable error rate is low.

pcs_data_mode

Variable set by the PMA PHY Control function. See 192.2.1.8.1.

pcs_reset

Boolean pcs_reset parameter set by the PCS Reset function. It is TRUE for the duration of a PCS reset. Otherwise set to FALSE.

rf_valid

Boolean indication that is set TRUE if received Reed-Solomon frame is valid. A Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied. rf_valid is set FALSE when an RS-FEC frame is received and is invalid.

rs_fec_frame_done

A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. Otherwise set to FALSE.

rx_coded<64:0>

Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 192–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>

Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

tx_coded<64:0>

Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 192–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>

Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

192.3.5.1.3 Functions

DECODE(rx_coded<64:0>)

In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block as specified in 192.3.2.2.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 192.3.2.2.4.

R_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:
a) A block type field of 0x1E and seven valid control characters other than /E/;
b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;
c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;
b) A block type field of 0x66 and a valid O code;
c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a control code specified in Table 192–3. A valid O code is one containing an O code specified in Table 192–3.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains one of the following:
a) Eight valid control characters other than /O/, /S/, /T/, /E/;
b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;
c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 192–3. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 192–3.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

192.3.5.1.4 Counters

`rfer_cnt`

Count up to a maximum of `RFER_CNT_LIMIT` of the number of invalid Reed-Solomon frames within the current `RFRX_CNT_LIMIT` Reed-Solomon frame period.

`rfrx_cnt`

Count number Reed-Solomon frames received during current period.

192.3.5.1.5 Messages

`RX_FRAME`

A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable `rf_valid` is updated.

192.3.5.2 State diagrams

The RFER monitor state diagram shown in Figure 192–21 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 192–22 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

The PCS 64B/65B Receive state diagram shown in Figure 192–23 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams.

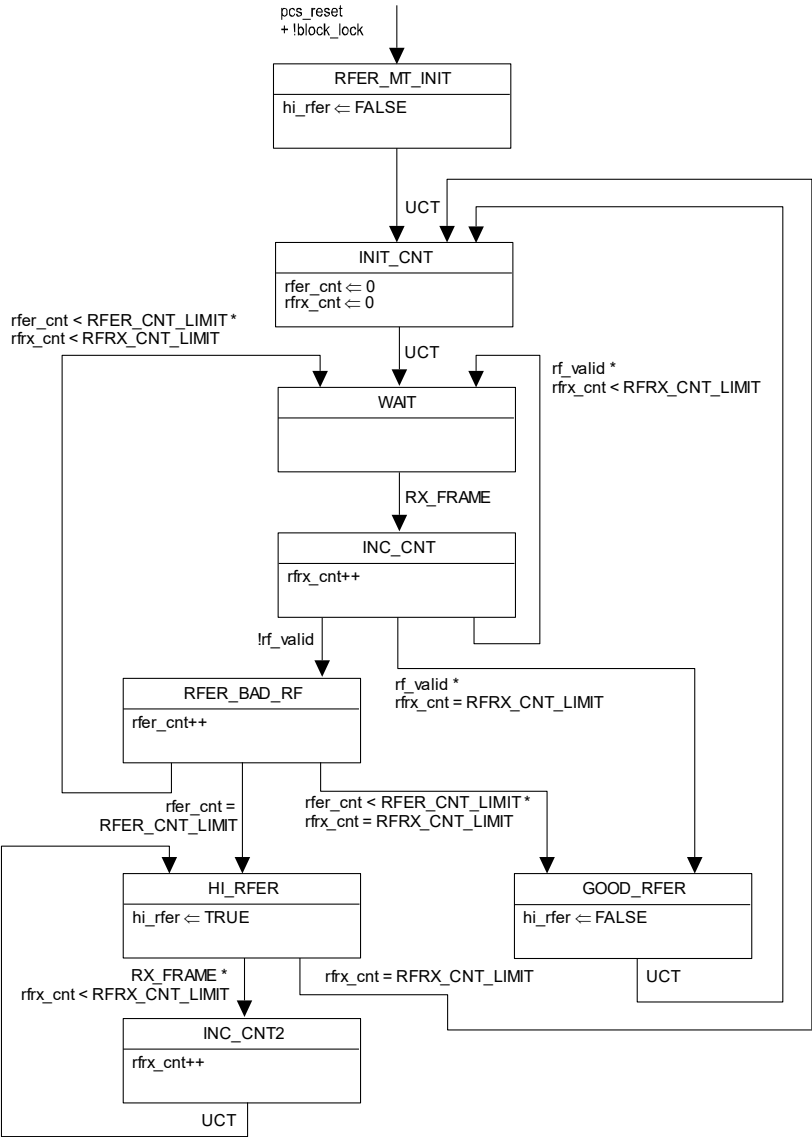


Figure 192-21—RFER monitor block state diagram

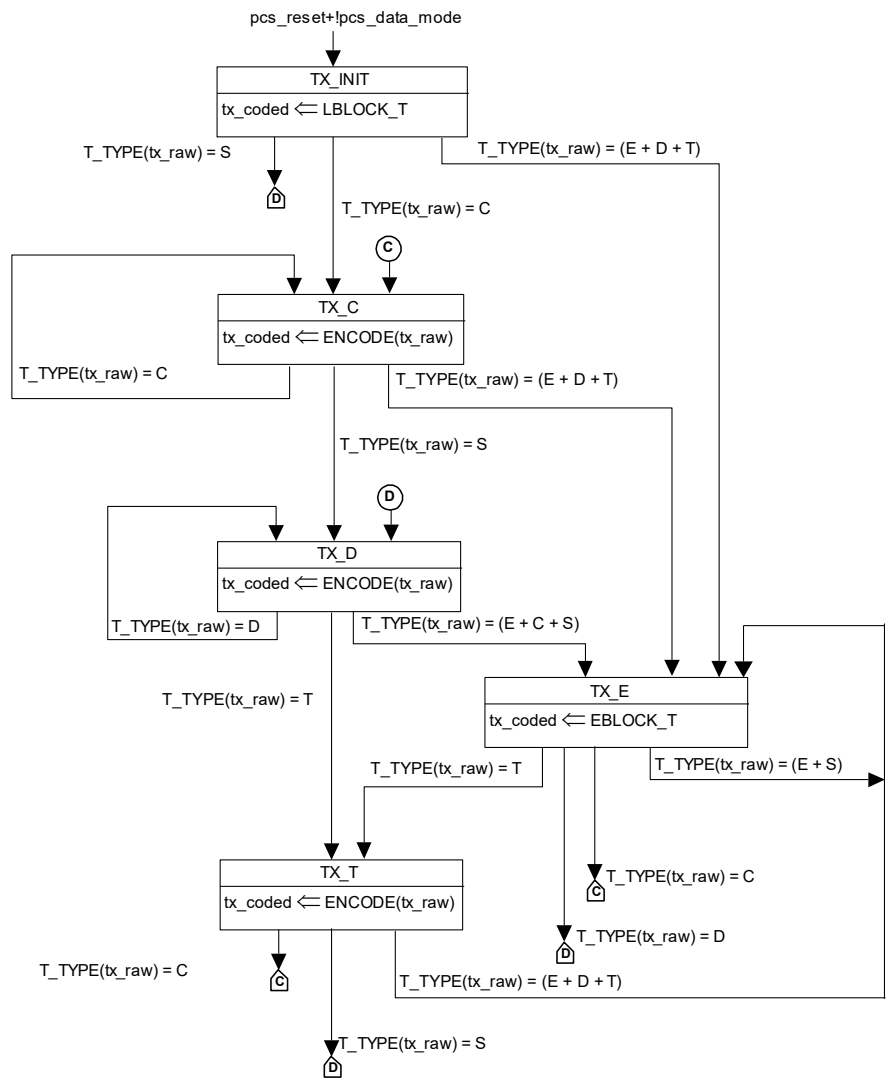


Figure 192-22—CS 6B/6B Transmittal state diagram

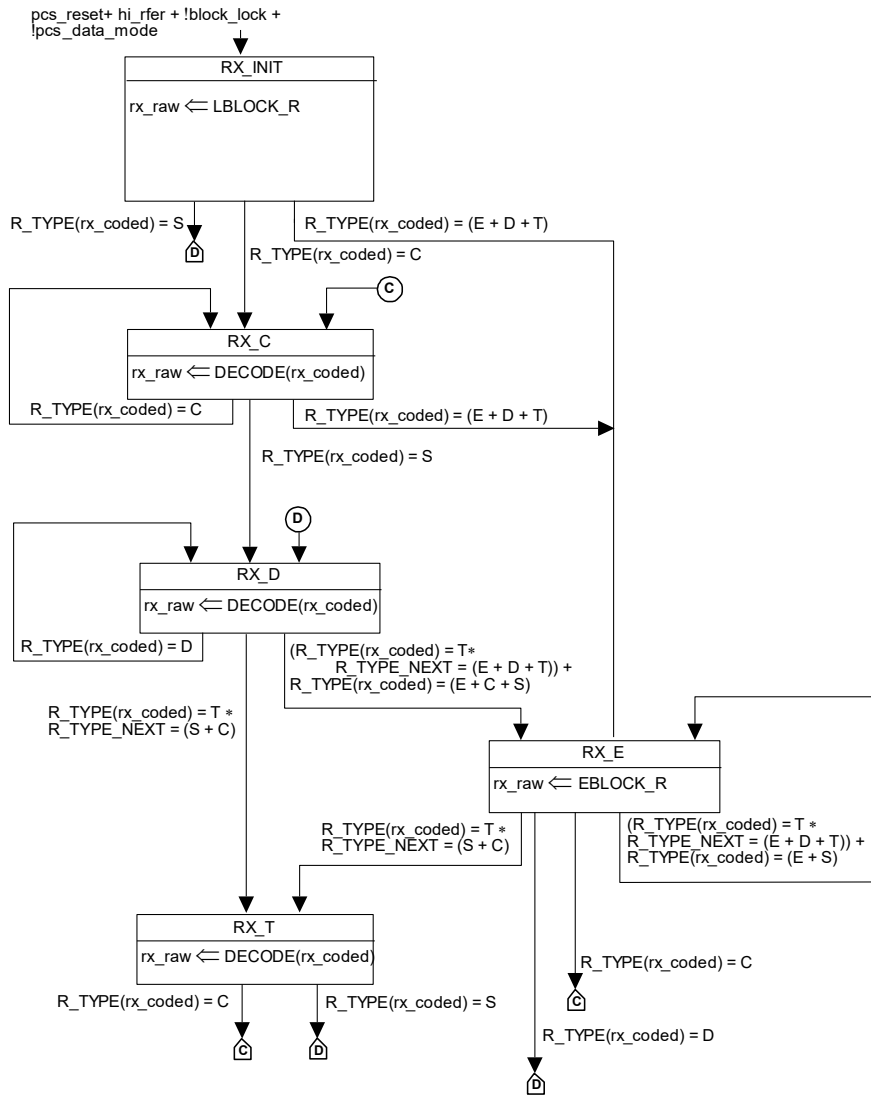


Figure 192-23—CS 6B/ 6B Receive state diagram

192.3.6 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

192.3.6.1 Status

pcs_status:

Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO 3.2323.2 and the inverse of this status is reflected in MDIO 3.2323.7.

block_lock:

Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:

Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

192.3.6.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:

6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 192–21) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

192.3.7 MultiGBASE-A operations, administration, and maintenance (OAM)

MultiGBASE-A operations, administration, and maintenance (OAM) is a subset of OAM specified for MultiGBASE-T1 PHYs in 149.3.9 since EEE is not supported and OAM symbol to field mapping differs. OAM involves both HS_PATH and LS_PATH. The 10-bit OAM symbols are inserted one per TDD burst into the OAM fields in the HS_PATH and LS_PATH. OAM bits after the first ten per burst are reserved.

The MultiGBASE-A PCS level OAM provides an optional mechanism useful for monitoring link operations such as PHY link health status exchange and message exchange. When OAM is implemented, behavior shall conform to the state diagrams in Figure 192–25 and Figure 192–26. OAM information is exchanged out of band between two PHYs using excess bandwidth available on the link. The OAM is strictly between two PHYs on the Physical Layer and their associated management entities if present. Passing OAM information to other layers is outside the scope of this standard.

OAM is operational as long as both PHYs implement this mechanism and the link is up.

The OAM frame data is carried in the OAM 10-bit field in the first ten bits of each TDD burst as described in 192.3.7.2.1. This 10-bit field is used to exchange OAM frames. The implementation of the OAM frame exchange function is optional.

For the remainder of this subclause, the term OAM is specific to the MultiGBASE-A PCS level OAM.

192.3.7.1 Definitions

OAM frame: A frame consisting of 14 octets of data, 14 framing bits, 14 reserved bits and two 10-bit Reserved symbols.

OAM symbol: A 10-bit symbol consisting of either one data octet plus a framing bit and a reserved bit, or a 10-bit Reserved symbol. 16 OAM symbols make up an OAM frame.

OAM field: A 10-bit field in each TDD burst reserved for the OAM symbol as described in 192.3.7.2.1.

OAM message: A message contains a 4-bit message number plus eight octets of message data (Message<7:0><7:0>) embedded in an OAM frame. The same OAM message can be repeated on multiple OAM frames.

OAM status: The four octets of status data (Message<11:8><7:0>) that is embedded in each OAM frame.

192.3.7.2 Functional specifications

192.3.7.2.1 MultiGBASE-A OAM frame structure

Each OAM frame is made up of 16 OAM symbols. Each of the first 14 symbols is made up of one octet of data, one framing bit, and one reserved bit. The last two symbols are the Reserved symbols.

One OAM symbol is placed in the 10-bit OAM field in each TDD burst during data mode. The 16 OAM symbols are consecutively inserted into 16 consecutive TDD bursts. Once the 16 symbols of the current OAM frame are inserted, the 16 symbols of the next OAM frame are inserted. This process is continuous without any break in the insertion of OAM symbols with the exception noted below.

When operating in HS_TX mode, the first bit of an OAM symbol (OAM<X><0>) shall be inserted in the OAM bit of the first RS-FEC frame in the first superframe of each TDD burst prior to interleaving. Each subsequent bit shall be inserted in the next nine RS-FEC frames such that the OAM symbol is carried in the first ten RS-FEC frames. When operating in LS_TX mode, an OAM symbol (OAM<X><9:0>) shall be inserted in the first ten OAM bits of the RS-FEC frame such that the OAM symbol is carried in the first ten bits of the OAM field of the RS-FEC frame. In this way, both HS_PATH and LS_PATH send and receive one OAM symbol per TDD burst.

Bit 0 of each OAM symbol is the first bit transmitted in the 10-bit OAM field. Symbol 0 is the first symbol transmitted in each OAM frame.

The OAM frame boundary can be found at the receiver by looking at bit D8. The boundary is a zero followed by 13 ones followed by two don't care.

If OAM is not implemented, then the 10-bit OAM field shall be set to all zeros. If the link partner does not implement OAM, the 10-bit OAM field will remain static.

192.3.7.2.2 OAM frame data

The OAM frame data is shown in Figure 192–24. OAM<x><y> refers to symbol x, bit y of the OAM frame. Reserved fields shall be set to zero.

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Symbol 0	Reserved	0	Reserved	Reserved	Reserved	Reserved	PingRx	PingTx	SNR<1>	SNR<0>
Symbol 1	Reserved	1	Valid	Toggle	Ack	TogAck	Message_Number<3:0>			
Symbol 2	Reserved	1	Message<0><7:0>							
Symbol 3	Reserved	1	Message<1><7:0>							
Symbol 4	Reserved	1	Message<2><7:0>							
Symbol 5	Reserved	1	Message<3><7:0>							
Symbol 6	Reserved	1	Message<4><7:0>							
Symbol 7	Reserved	1	Message<5><7:0>							
Symbol 8	Reserved	1	Message<6><7:0>							
Symbol 9	Reserved	1	Message<7><7:0>							
Symbol 10	Reserved	1	Message<8><7:0>							
Symbol 11	Reserved	1	Message<9><7:0>							
Symbol 12	Reserved	1	Message<10><7:0>							
Symbol 13	Reserved	1	Message<11><7:0>							
Symbol 14	Reserved									
Symbol 15	Reserved									

Figure 192–24—OAM frame

192.3.7.2.3 Ping RX

The Ping RX is indicated in OAM<0><3>.

This bit is set by the PHY to the same value as the Ping TX bit received from the link partner.

192.3.7.2.4 Ping TX

The Ping TX is indicated in OAM<0><2>.

This bit is set by the PHY for the link partner to echo on Ping RX.

192.3.7.2.5 PHY health

The PHY Health (SNR<1:0>) is indicated in OAM<0><1:0>.

This status is set by the PHY to indicate the status of the receiver. The definitions of good, marginal, and when to request retrain are implementation dependent.

- 00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame
- 01: Reserved
- 10: PHY SNR is marginal
- 11: PHY SNR is good

192.3.7.2.6 OAM message valid

The OAM message valid (Valid) is indicated in OAM<1><7>.

- 0: Current OAM frame does not contain a valid OAM message
- 1: Current OAM frame contains a valid OAM message

192.3.7.2.7 OAM message toggle

The OAM message toggle (Toggle) is indicated in OAM<1><6>.

The toggle bit lets the management entity determine which OAM message is being referenced. The toggle bit in the current OAM message is set to the opposite value of the toggle bit in the previous OAM message only if link partner acknowledges the OAM message is received. This allows one OAM message to be delineated from a second OAM message since the same OAM message may be repeated over multiple OAM frames. This bit is valid only if Valid is set to one.

192.3.7.2.8 OAM message acknowledge

The OAM message acknowledge (Ack) is indicated in OAM<1><5>.

Ack is set by the PHY to let the link partner know that the OAM message sent by the link partner was successfully received as defined in 192.3.7.2.13 and the PHY is ready to accept a new OAM message. An OAM message is defined to be Message_Number<3:0> and Message<7:0><7:0>.

- 0: No acknowledge
- 1: Acknowledge

192.3.7.2.9 OAM message toggle acknowledge

The OAM message toggle acknowledge (TogAck) is indicated in OAM<1><4>.

TogAck is set by the PHY to let the link partner know that the OAM message is being acknowledged. TogAck takes the value of Toggle bit of the OAM message being acknowledged. This bit is valid only if Ack is set to one.

192.3.7.2.10 OAM message number

The OAM message number is indicated in OAM<1><3:0>.

This field is user-defined, but recommended that it be used to indicate the meaning of the 8-octet message that follows. If used this way, up to 16 different 8-octet messages can be exchanged.

The message number is user-defined and its definition is outside the scope of this standard.

192.3.7.2.11 OAM message data

The OAM message data is indicated in OAM<9:2><7:0>.

The 8-octet message data is user-defined and its definition is outside the scope of this standard.

Ack is set by the PHY to let the link partner know that the OAM frame sent by the link partner is successfully received as defined. The OAM frame octet is the lower 8 bits of the 10-bit OAM symbol.

192.3.7.2.12 OAM status

The OAM status data is indicated in OAM<13:10><7:0> on a per OAM frame basis.

These 32 bits are set by the PHY to convey its status in the mr_tx_message[95:64] to the link partner.

For additional information on the usage of these bits see [Annex 149B](#).

192.3.7.2.13 MultiGBASE-A OAM frame acceptance criteria

All fields of the OAM frame shall be accepted and updated, unless there is an uncorrectable RS-FEC frame on any of the 16 symbols.

192.3.7.2.14 PHY health indicator

The PHY current health is sent to the link partner on a per OAM frame basis using the SNR<1:0> bits as described in 192.3.7.2.5. It lets the link partner have an early indication of potential problems that can cause the PHY to drop link or have high error rates.

192.3.7.2.15 Ping

The PingTx bit is set based on the value in mr_tx_ping. The PingRx bit is set based on the latest PingTx received from the link partner. The value in mr_rx_ping is set based on the received PingRx from the link partner. The user can determine that the link partner OAM is operating properly by toggling mr_tx_ping and observing mr_rx_ping matches after a short delay.

The Ping bits are updated on a per OAM frame basis.

192.3.7.2.16 OAM message exchange

The OAM message exchange operates on a per OAM message basis that occurs over many OAM frames. The OAM message exchange mechanism allows a management entity attached to a PHY and its peer attached to the link partner to asynchronously pass OAM messages and verify their delivery.

The OAM message is first written into the OAM transmit registers in the PHY. The OAM message is then read out of the OAM transmit registers and transmitted to the link partner. After the link partner receives the OAM message, it transfers it into the link partner's OAM receive registers and also sends an acknowledge back to the PHY indicating that the next OAM message can be transmitted. One OAM message can be loaded into the OAM transmit registers while another OAM message is being transmitted by the PHY to the link partner, while yet another OAM message is being read out at the link partner's OAM receive registers. The exchange of OAM messages is occurring concurrently and bi-directionally. The transfers between the management entities can be done asynchronously. On the transmit side, `mr_tx_valid = 0` indicates that the next OAM message can be written into the OAM transmit registers. Once the registers are written, the management entity sets `mr_tx_valid` to one to indicate that the OAM transmit registers contain a valid OAM message. Once the message is read out atomically, the state diagram clears the `mr_tx_valid` to zero to indicate that the registers are ready to accept the next OAM message.

On the receive side, `mr_rx_lp_valid` indicates that valid OAM message can be read from the OAM receive registers. Once these registers are read, the `mr_rx_lp_valid` should be cleared to zero to indicate that the registers are ready to receive the next OAM message. If `mr_rx_lp_valid` is not cleared, then the OAM message transfer will eventually stall since the sender cannot send new OAM messages if the receiver does not acknowledge that an OAM message has been transferred into the OAM receive registers.

The management entities can asynchronously read `mr_tx_valid` and `mr_rx_lp_valid` to know when OAM messages can be transferred in and out of the OAM registers.

The toggle bit alternates between zero and one, which lets the management entity determine which OAM message is being referred to. The toggle bit transition rules between one OAM frame and the next OAM frame are shown in Table 192–12.

Table 192–12—Toggle bit transition rules

Previous Valid	Previous Toggle	Current Valid	Current Toggle	Description
0	0	0	0	No valid OAM message
0	0	0	1	Illegal transition (Error)
0	0	1	0	New OAM message starting
0	0	1	1	Illegal transition (Error)
0	1	0	0	Illegal transition (Error)
0	1	0	1	No valid OAM message
0	1	1	0	Illegal transition (Error)
0	1	1	1	New OAM message starting
1	0	0	0	Illegal transition (Error)

1	0	0	1	Received acknowledge, no new OAM message to send
1	0	1	0	Repeating current OAM message, waiting for link partner's acknowledge
1	0	1	1	Previous OAM message ending, new OAM message starting
1	1	0	0	Received acknowledge, no new OAM message to send
1	1	0	1	Illegal transition (Error)
1	1	1	0	Previous OAM message ending, new OAM message starting
1	1	1	1	Repeating current OAM message, waiting for link partner's acknowledge

192.3.7.3 State diagram variable to OAM register mapping

The state diagrams of Figure 192–25 and Figure 192–26 generate and accept variables of the form “mr_x,” where x is an individual signal name. These variables comprise a management interface to communicate the OAM information to and from the management entity. Clause 45 MDIO registers are defined in MMD3 to support the OAM. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the information is recommended.

Assignments for PCS register/bit numbers 3.2308 to 3.231 are shown in Table 45–233. MultiGBASE-A uses the state variable to OAM register/bit number mapping for BASE-T1 shown in Table 97-6 and the state variable to OAM register/bit number mapping for MultiGBASE-T1 shown in Table 149-9.

192.3.7.4 Detailed functions and state diagrams

192.3.7.4.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, counters, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

192.3.7.4.2 State diagram parameters

192.3.7.4.3 Variables

frame_boundary

Frame boundary detection based on the latest 16 rx_oam_field<8> received. The leftmost bit is the earliest received bit.

Values:

TRUE: Latest 16 rx_oam_field<8> = 011111111111xx.
FALSE: Latest 16 rx_oam_field<8> ≠ 011111111111xx.

link_status

The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive. This variable takes the values of OK or FAIL.

mr_rx_lp_message[95:0]

12-octet OAM message from the link partner. mr_rx_lp_message[63:0] in this variable is valid only when mr_rx_lp_valid is one. mr_rx_lp_message[95:64] is always valid and continuously updated.

mr_rx_lp_message_num[3:0]

4-bit message number from the link partner. The value in this variable is valid only when mr_rx_lp_valid is one.

mr_rx_lp_SNR[1:0]

Link partner health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.
01: Reserved.
10: PHY SNR is marginal.
11: PHY SNR is good.

The threshold for the status is implementation dependent.

mr_rx_lp_toggle

The toggle bit value associated with the 8-octet MultiGBASE-A OAM message from the link partner.

Values:

The toggle bit alternates between zero and one.

mr_rx_lp_valid

Indicates whether the OAM message in mr_rx_lp_message[63:0], mr_rx_lp_message_num[3:0] and the toggle bit in mr_rx_lp_toggle is valid or not. This variable should be cleared when mr_rx_lp_message[63:48] is read and is not explicitly shown in the state diagram. The clearing of this variable indicates to the state diagram that the MultiGBASE-A OAM message is read by the user and the state diagram can proceed to load in the next MultiGBASE-A OAM message.

Values:

0: Invalid.
1: Valid.

mr_rx_ping

Echoed ping value from the link partner.

Values:

The value can be zero or one.

mr_tx_message[95:0]

8-octet MultiGBASE-A OAM message and 4-octet MultiGBASE-A status transmitted by the local PHY. mr_tx_message[63:0] in this variable is valid only when mr_tx_valid is one. mr_tx_message[95:64] in this variable is always valid.

mr_tx_message_num[3:0]

4-bit message number transmitted by the local PHY. The value in this variable is valid only when mr_tx_valid is one.

mr_tx_ping

Ping value transmitted by the local PHY.

Values:

The value can be one or zero.

mr_tx_received

Indicates whether the most recently transmitted MultiGBASE-A OAM message with a toggle bit value of mr_tx_received_toggle was received, read, and acknowledged by the link partner. This variable shall clear on read.

Values:

0: MultiGBASE-A OAM message was not received and read by the link partner.

1: MultiGBASE-A OAM message was received by the link partner.

mr_tx_received_toggle

Toggle bit value of the MultiGBASE-A OAM message that was received, read, and most recently acknowledged by the link partner. This bit is valid only if mr_tx_received is one.

Values:

The value can be zero or one.

mr_tx_SNR[1:0]

Status register indicating PHY health status.

Values:

00: PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.

01: Reserved.

10: PHY SNR is marginal.

11: PHY SNR is good.

The threshold for the status is implementation dependent.

mr_tx_toggle

The toggle bit value associated with the 8-octet MultiGBASE-A OAM message transmitted by the PHY. The value is automatically set by the state diagram and cannot be set by the user. This bit should be read and recorded prior to setting mr_tx_valid to one.

Values:

The toggle bit alternates between zero and one.

mr_tx_valid

Indicates whether MultiGBASE-A OAM message in mr_tx_message[63:0] and mr_rx_lp_message_num[3:0] is valid or not. This register will be cleared by the state diagram to indicate whether the next MultiGBASE-A OAM message can be written into the registers.

Values:

0: Invalid.

1: Valid.

reset

Reset.

Values:

TRUE: OAM circuit is in reset.

FALSE: OAM circuit is not in reset.

rs_check

Status of the latest rs_correct() operation.

Values:

GOOD: No errors or correctable error.
BAD: Uncorrectable error.

rx_ack

Acknowledge from link partner in response to PHY's MultiGBASE-A OAM message.

Values:

0: Not acknowledged.
1: Acknowledged.

rx_ack_toggle

The toggle value corresponding to the PHY's MultiGBASE-A OAM message that the link partner is acknowledging. This value is valid only if the rx_ack is set to one.

Values:

The toggle bit can take on values of zero or one.

rx_boundary

This variable is set to TRUE whenever the receive data stream reaches the end of a Reed-Solomon frame and a complete 10-bit OAM symbol is available per 192.3.7.2.1 during data mode. Otherwise set to FALSE.

Values:

TRUE: Receive stream is at a boundary end.
FALSE: Receive stream is not at a boundary end.

rx_exp_toggle

This variable holds the expected toggle value of the next MultiGBASE-A OAM message. This is normally the opposite value of the current toggle value, but shall reset on error conditions where two back-to-back MultiGBASE-A OAM messages separated by MultiGBASE-A OAM frames without a valid message have the same toggle value.

Values:

The toggle bit can take on values of zero or one.

rx_lp_ack

Acknowledge from PHY in response to link partner's MultiGBASE-A OAM message. Indicates whether valid MultiGBASE-A OAM message from the link partner has been sampled into the PHY's registers.

Values:

0: Not acknowledged/not sampled.
1: Acknowledged/sampled.

rx_lp_ping

Ping value received from the link partner that is looped back.

Values:

The value can be zero or one.

rx_lp_toggle

The toggle bit value in the previous MultiGBASE-A OAM frame received from the link partner.

Values:

The toggle bit alternates between zero and one.

rx_lp_valid

Indicates whether MultiGBASE-A OAM message in previous MultiGBASE-A OAM frame received from the link partner is valid or not.

Values:

0:	Invalid.
1:	Valid.

rx_oam_field<9:0>

10-bit MultiGBASE-A OAM symbol extracted from a received TDD burst during data mode.

rx_oam<15 to 0><9:0>

Raw 16-symbol OAM frame received from the link partner.

SNR[1:0]

PHY health status.

Values:

00:	PHY link is failing and will drop link and relink within 2 ms to 4 ms after the end of the current OAM frame.
01:	Reserved.
10:	PHY SNR is marginal.
11:	PHY SNR is good.

Both the status threshold and condition for generating this status are implementation dependent.

tx_boundary

This variable is set to TRUE whenever the transmit data stream reaches the start of a TDD burst during data mode. Otherwise set to FALSE.

Values:

TRUE:	Transmit stream is at a boundary end.
FALSE:	Transmit stream is not at a boundary end.

tx_oam_field<9:0>

10-bit MultiGBASE-A OAM symbol inserted into a transmitted TDD burst during data mode.

tx_oam<15 to 0><9:0>

Raw 16-symbol OAM frame transmitted from the PHY.

tx_lp_ready

Indicates whether the link partner is ready to receive the next MultiGBASE-A OAM message from the PHY. If ready, then the PHY will load the next MultiGBASE-A OAM message from the registers and begin transmitting them.

Values:

0:	Not ready.
1:	Ready.

tx_toggle

The toggle bit value being sent in the current MultiGBASE-A OAM frame transmitted by the PHY.

Values:

The value can be zero or one.

192.3.7.4.4 Counters

rx_cnt

A count of received OAM frame symbols.

Values:
The value can be any integer from 0 to 16, inclusive.

tx_cnt
OAM frame transmit symbol count.
Values:

The value can be any integer from 0 to 16, inclusive.

192.3.7.4.5 Functions

rs_correct (16 OAM symbols)
This function returns the 14 data symbols unmodified and sets rs_check to GOOD if none of the RS-FEC frames are uncorrectable.

192.3.7.4.6 State diagrams

The receive state diagram is shown in Figure 192–25 and the transmit state diagram is shown in Figure 192–

26.

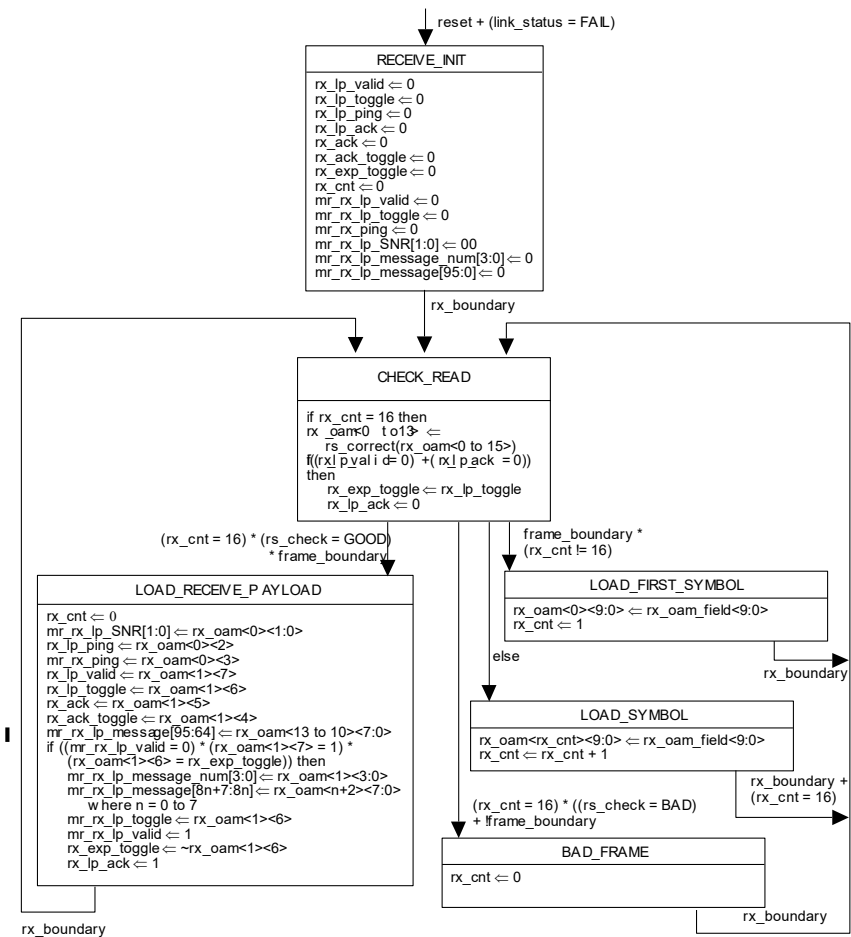


Figure 192-25—Receive state diagram

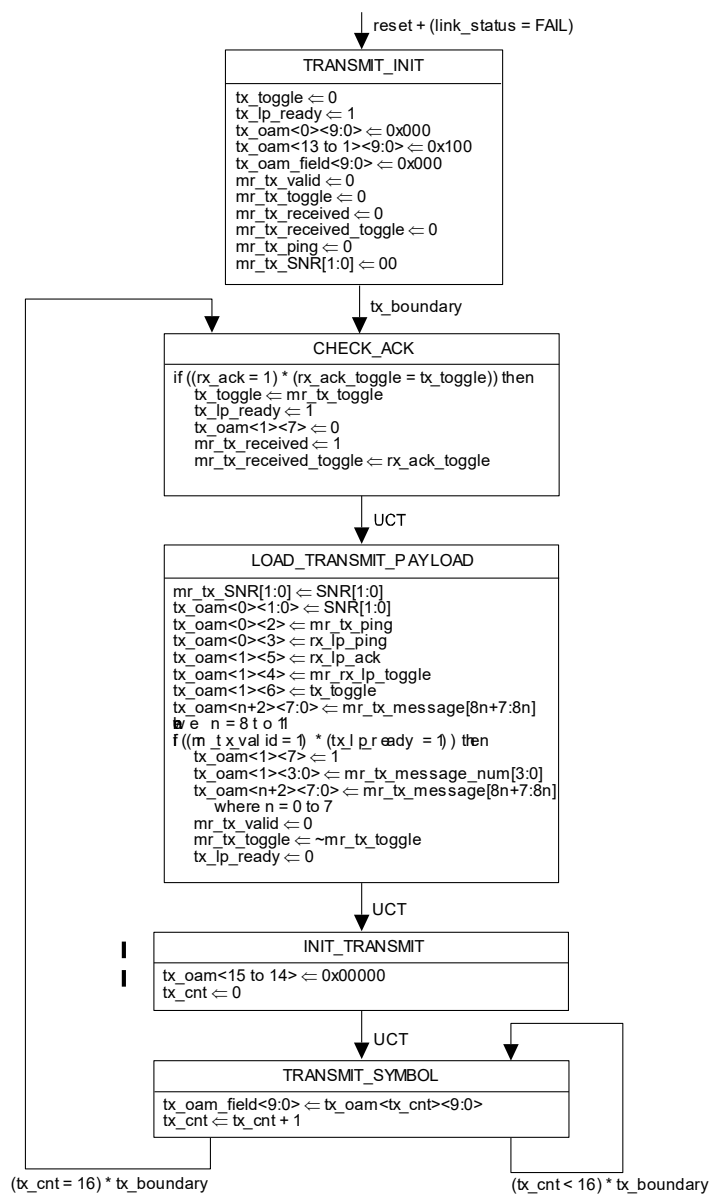


Figure 192-26—Transmit state diagram

192.4.1 PMA functional specifications

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 192.9 or 192.10.

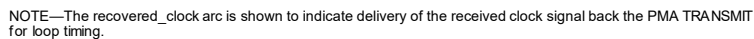


Figure 192-27—IMA reference diagram

192.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram (see Figure 192–27) shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 192–27.

192.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

- a) Power for the device containing the PMA has not reached the operating state.
- b) The receipt of a request for reset from the management entity.

PMA Reset sets `pma_reset` = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended `pma_reset` branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 192–31), if link partner has already exited DISABLE_TRANSMITTER state.

192.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a two-level, three-level, or four-level modulated signal on the single balanced pair of conductors (-T1) or the single coaxial cable (-V1). When the PHY Control state diagram (see Figure 192–31) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by `tx_symb` onto the MDI, followed by a QUIET period to complete a TDD cycle. The signals generated by PMA Transmit shall comply with the electrical specifications given in 192.5.2.

When the management parameter `config` is LEADER, the PMA Transmit function shall source the transmit symbol clock `TX_TCLK` from a local clock source while meeting the transmit jitter requirements of 192.5.2.3. The Leader-Follower relationship shall include loop timing. If the management parameter `config` is FOLLOWER, the PMA Transmit function shall source `TX_TCLK` from the recovered clock of 192.4.2.6 while meeting the jitter requirements of 192.5.2.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

192.4.2.2.1 Global PMA transmit disable

When the `PMA_transmit_disable` variable is set to TRUE, this function shall cause the average launch power of the transmitter to be as specified in 192.5.2.4 when the value of `tx_symb` is Z.

192.4.2.3 PMA Receive function

The PMA Receive function receives a two-level, three-level, or four-level modulated signal on a single balanced pair of conductors (-T1) or single coaxial cable (-V1). It includes a PAM2 receiver for all signal rates and, optionally, a PAM3 receiver ~~for 7.5 Gb/s~~, a PAM4 receiver ~~for 10 Gb/s~~, or both. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a -T1 link segment meeting the requirements of 192.7 or a -V1 link segment meeting the requirements of 192.8.

To achieve the indicated performance, it is highly recommended that PMA Receive include the function of signal equalization. No echo cancellation is needed due to the TDD nature of the duplexing method.

The PMA Receive generates the detect_lp_burst signal, which is set to TRUE when the PMA detects reception of PAM2 symbols at the start of a burst and set to FALSE when the PMA detects the QUIET portion of the burst.

The PMA Receive function uses the parameters pcs_status and scr_status, as well as the state of the equalization and estimation functions, to determine the quality of the receiver performance and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see Figure 192–31). Failing to receive the link partner's consecutive TDD bursts could trigger deassertion of loc_rcvr_status. The reception of Z symbols during the TDD QUIET period alone shall not trigger setting loc_rcvr_status to NOT_OK. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for signal inversions.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

192.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 192–31.

During PMA training (TRAINING and COUNTDOWN states in Figure 192–31), PHY Control information is exchanged between link partners with a 12-octet Infocfield, which is XORed with the 96 bits starting after the N_{mf}^{th} bit of the training payload specified in 192.3.4.3. The link partner is not required to decode every Infocfield transmitted but is required to decode Infocfields at a rate that enables the correct actions prior to the training phase transition.

The 12-octet Infocfield shall include the fields in 192.4.2.4.2 through 192.4.2.4.8, also shown in Figure 192–28 and Figure 192–29. When PMA_state = 00, Infocfield shall be transmitted at least 16 times with each change

to	octets	7	to
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10.

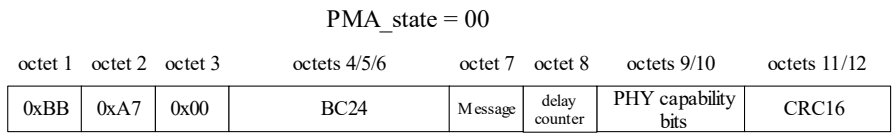


Figure 192–28—If d i d T R A I N I N G f o r m a t

PMA_state = 01						
octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	BC24	Message	PhaseSwBC24	CRC16

Figure 192–29—Infid d COUNTDOWN format

192.4.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved <bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (i.e., the LSB of octet 1 is sent first).

192.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0 > and so forth.

192.4.2.4.3 PHY burst count (BC24)

The PHY burst count consists of 3 octets [Oct4<7:0>,Oct5<7:0>,Oct6,7:0>] and indicates the running count of PHY bursts sent LSB first. The BC24 continues to run uninterrupted for the duration of the link.

BC24 is defined to rollover to zero after it reaches 16 776 959. BC24 could roll over in the case the Leader has started long before the Follower sends the first responding burst.

192.4.2.4.4 Message Field

The Message Field is one octet. For both the Leader and Follower, this field is represented by Oct7{PMA_state<7:6>, loc_revr_status<5>, training_phase<4:3>, reserved<2:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

The two training_phase-indicator bits training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> = 00 indicates SYMMETRIC TRAINING and training_phase<4:3> = 01 indicates ASYMMETRIC TRAINING.

All possible Message Field settings are listed in Table 192–13 for the Leader or Follower. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 192–13 for the Leader, and the first or second row of Table 192–13 for the Follower. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the

current setting. When loc_rcvr_status = OK the Infocfield variable is set to loc_rcvr_status<5> = 1 and set to zero otherwise.

Table 192–13—Infocfield Message Field valid Leader or Follower settings

PMA_state<7:6>	loc_rcvr_status<5>	training_phase<4:3>	reserved	reserved	reserved
00	0	00	0	0	0
00	1	00	0	0	0
01	1	00	0	0	0
00 ¹	0	01	0	0	0
00	1	01	0	0	0
01	1	01	0	0	0

192.4.2.4.5 PHY capability bits

This multi-rate PHY supports bidirectional data transfer with 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s point-to-point transmission or reception in one direction and 100 Mb/s or 1 Gb/s point-to-point reception or transmission in the other direction. The direction of asymmetry and high speed data rate are determined at link startup. The management control configures the Leader to negotiate with the Follower to configure it for the desired high speed data rate that the Follower is expected to use. The PHY capability and negotiated rates of the Infocfield are used to establish the Follower rate and check for misconfiguration.

When PMA_state<7:6> = 00, the Infocfield [Oct9<7:0>,Oct10<7:0>] contains the PHY capability and negotiated ability bits. Each octet is sent LSB first. The field locations (see Table 192–14) carry different values depending on the value of the burst count (BC24) LSB. Table 192–15, Table 192–16, and Table 192–17 show the field encoding bits.

Table 192–14—PHY capability and negotiated ability bits

octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
PHY_D / PHY_S transmit and receive capability															
Transmit capability								Receive capability							

¹This row can be skipped if not applicable.

	LS rate				HS rate					LS rate				HS rate			
	PHY_D / PHY_S negotiated ability																
	Vendor specific data													Negotiated rates			

[Editing note for Table 192-14: See https://www.ieee802.org/3/dm/public/0726/chini_3dm_02a_D2d0_1G_comments-preview.pdf Table 192-11 changes since Table 192-14 is not accurate here. The change is to make Reserved bits 0 in both Octets 9 and 10 change to 1 Gb/s. Pasted here for reference:

BC24 LSB = 0	Octet 9								Octet 10							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
	PHY_D / PHY_S Transmit and Receive Capability															
	Transmit Capability								Receive Capability							
	LS Rate				HS Rate				LS Rate				HS Rate			
	1 Gb/s	100 Mb/s	Reserved	Reserved	10 Gb/s	7.5 Gb/s	5 Gb/s	2.5 Gb/s	1 Gb/s	100 Mb/s	Reserved	Reserved	10 Gb/s	7.5 Gb/s	5 Gb/s	2.5 Gb/s
BC24 LSB = 1	PHY_D / PHY_S Negotiated Abilities															
	Vendor Specific Data								Direction	OAMEn	R	Negotiated Rates				

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The transmit and receive capabilities depend on whether the PHY supports PHY_S, PHY_D, or both capabilities. For example, PHY_S sets its HS_TX capability and LS_RX capability, and PHY_D set its HS_RX capability and LS_TX capability. The capability bit field assignments are shown in Table 192–15. A one in a field bit indicates that the PHY has that capability and a zero indicates it does not. All zeros indicates that the field is not applicable to this PHY. For example, since a PHY that only supports PHY_S has no HS_RX capability, it would set Oct10<7:2> to zero.

Table 192–15—Rate field encoding

LS rate		HS rate	
00	N/A	000000	N/A
~~x101~~	100 Mb/s	xxxxx1	2.5 Gb/s
~~1x10~~	~~1 Gb/s~~	xxxx1x	5 Gb/s
~~11~~	Reserved	xxx1xx	7.5 Gb/s
		xx1xxx	10 Gb/s
		x1xxxx	Reserved
		1xxxxx	Reserved

The negotiated rates field encoding is shown in Table 192–16. The Leader selects the negotiated rates based on either management configuration of register bits 1.2319<5:1> or selecting the highest mutually supported advertised rate. In the latter case, the Leader optionally sends the all zeros negotiated rate code when it desires to see the Follower capabilities prior to determining the negotiated rates.

Table 192–16—Negotiated rate field encoding

Code	LS rate	HS rate
00000	In progress	In progress
00001	100 Mb/s	2.5 Gb/s
00010	100 Mb/s	5 Gb/s
00011	100 Mb/s	7.5 Gb/s
00100	100 Mb/s	10 Gb/s
00101	~~Reserved~~ 1 Gb/s	~~Reserved~~ 5 Gb/s
00110	~~Reserved~~ 1 Gb/s	~~Reserved~~ 7.5 Gb/s
00111	Reserved	Reserved
01xxx	Reserved	Reserved
1xxxx	Reserved	Reserved

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The Leader uses the direction bit to communicate the desired Follower PHY type as shown in Table 192–17.

Table 192–17—Negotiated direction field encoding

Code	Leader	Follower
0	PHY_D	PHY_S
1	PHY_S	PHY_D

OAMen: The optional OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1.

The capability bit values shall be considered as valid only when loc_rcvr_status<5> bit is 1.

192.4.2.4.6 TDD delay counter

When PMA_state<7:6>=00, then Oct8<7:0> contains the TDD delay counter, sent LSB first. The format of TDD delay counter is Oct8<0> = Reserved, Oct8<1:6> = delay_count<5:0>, and Oct8<7> = delay_count_valid as shown in Table 192–18.

Table 192–18—TDD delay counter

octet 8							
0	1	2	3	4	5	6	7
		delay_count					

After the Leader detects the Follower TDD burst position and estimates the link segment delay, it shall set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to one. The TDD delay counter may be calculated as the estimated link segment delay in symbol times (at the 3 GBd rate) divided by 16, then rounded to the nearest integer. Each LSB unit represents 5.333 ns delay (16 symbols at 3 GBd).

The Follower shall accept the received remote delay_count only when received remote delay_count_valid bit is set to one. The Follower shall store this delay_count number.

As acknowledgment of the reception of this delay_count, the Follower shall send back its received delay count in its own delay_count field and set its delay_count_valid to one, so the Leader can confirm the exchange of this information is completed. When the Leader or the Follower finishes the exchange of delay count and the negotiated data rates, it shall set negotiation_done to OK. The PHY Control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.

Starting from Asymmetric training and continuing through to the data mode, the Follower shall adjust its transmit burst position according to the stored delay_count.

192.4.2.4.7 Phase switch PHY burst count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the phase switch burst count (PhaseSwBC24) sent LSB first. PhaseSwBC24 indicates the burst count when the Leader transmitter switches from current training phase to the next training phase or data mode. PhaseSwBC24 shall be a minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state.

Since phase switch is always initiated from the Leader, the PhaseSwBC24 value of Follower Infocfield may be ignored. The Leader will exit a COUNTDOWN state after sending the last burst (BC24 = PhaseSwBC24 – 1), and receiving the last burst from the Follower. The Follower will exit a COUNTDOWN state after receiving the last burst (BC24 = PhaseSwBC24 – 1) from the Leader and finishing sending the last burst of its own.

192.4.2.4.8 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains a reserved field. All Infocfield fields denoted reserved are reserved for future use.

192.4.2.4.9 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 192–30. After initialization, the switch is set to CRCgen, as shown in Figure 192–30, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order shown, first S15, followed by S14, and so on, until the final value S0. The 16 delay elements shown in Figure 192–30 shall be initialized to

zero.

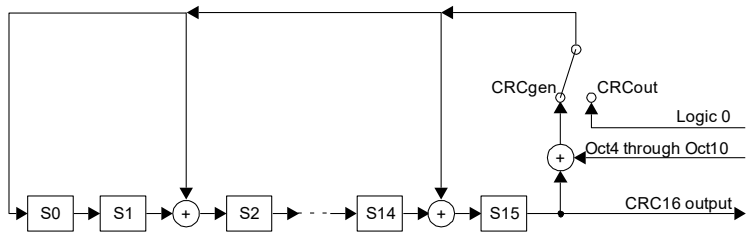


Figure 192-30—CRC 16

192.4.2.4.10 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 192-19. Mapping of MDIO status variables to PMA status variables is shown in Table 192-20.

Table 192-19—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1 PMA control register	1.2309.14	PMA_transmit_disable

Table 192-20—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1 PMA status register	1.2310.1	PMA_receive_fault

192.4.2.4.11 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 192-31. The management parameter config is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

Upon entry to the TRAINING0 state, the first symbol of the Follower's transmit PMA training frame at the transmit MDI shall be aligned so that it is 400 ± 1 transmit symbols after the arrival of the last PMA training payload symbol from the Leader at the Follower input MDI. The Follower shall maintain this alignment while in the TRAINING0 and COUNTDOWN0 (i.e., while `tx_mode = SEND_TS`) states. The PHY burst count communicated by the Follower should match the PHY burst count communicated by the Leader during the previous PMA training frame.

In the TRAINING0 state, PAM2 transmission is used and PHY capabilities and `delay_count` are exchanged using Infofields as specified in 192.4.2.4.5. The final negotiated data rate mode is determined by the Leader. The Leader and Follower transition from TRAINING0 state to COUNTDOWN0 state if `loc_rcvr_status` and `rem_rcvr_status` are both OK, and `negotiation_done` is OK.

If the local receiver status (indicated by `loc_rcvr_status`) transitions to NOT_OK during any COUNTDOWN or PCS_TEST state, then PHY Control returns to the SILENT state and attempts a retrain.

When entering the TRAINING1 state, the Follower shall use the Leader transmitted `delay_count` to align its transmit PMA training frame to be $176 \text{ ns} - \text{delay_count} \times 5.333 \text{ ns}$ ($\pm 5.333 \text{ ns}$) after the last PMA training payload symbol from the Leader appears on the Follower input MDI. The Follower shall maintain this alignment while `tx_mode` is `SEND_TA` or `SEND_N`.

The `link_fail_inhibit_timer` value is defined to be 97.5 ms. It is used to force a restart if the link up cannot be achieved within the maximum allowed time.

The COUNTDOWN0 state synchronizes the link partner's transition from symmetric training TDD bursts (`SEND_TS`) to asymmetric training TDD bursts (`SEND_TA`) in the TRAINING1 state. The TRAINING1 state then waits until both local and remote receivers settle and signal that their status is OK, before transitioning to COUNTDOWN1. The PCS is tested after completion of COUNTDOWN1. If the link is reliable as indicated by block lock and the RS-FEC error rate, then the PHY Control transitions to PCS_DATA and begins transferring data.

192.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive link and communicates it via the variable `link_status`. Failure of the underlying receive link causes the PMA to set `link_status` to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the link.

The Link Monitor function shall comply with the state diagram of Figure 192–33.

Upon power on reset, or release from power down, the PHY sets `link_enable = DISABLE`. During this period, `link_status = FAIL` is asserted. When the PHY `link_enable` is set to ENABLE, the Link Monitor state diagram begins monitoring the PMA. As soon as reliable transmission is achieved, with `pcs_data_mode = TRUE`, the variable `link_status = OK` is asserted, upon which further PHY operations can take place.

192.4.2.6 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 192.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by `recovered_clock` for use when the management parameter `config` is set to FOLLOWER.

192.4.3 MDI

Communication through the MDI is summarized in 192.4.3.1 and 192.4.3.2.

192.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The transmit path uses PAM2 for all refresh headers and during RS-FEC frame and any padding transmission for 100 Mb/s, 1 Gb/s, 2.5 Gb/s or 5 Gb/s 5G+100. The transmit path uses PAM3 for the 7.5 Gb/s RS-FEC frame and any padding transmission for 5G+1000 or 7.5G+100. The transmit path uses PAM4 for the 10 Gb/s RS-FEC frame and any padding transmission for 7.5G+1000 or 10 Gb/s. PMA Transmit generates a pulse-amplitude modulated signal in the form shown in Equation (192–14).

(192–14)

$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT)$ In Equation (192–14), a_n is the PAM4 modulation symbol from the set $\{-1, -1/3, +1/3, +1\}$, the PAM3 modulation symbol from the set $\{-1, 0, +1\}$, or the PAM2 modulation symbol from the set $\{-1, +1\}$ to be transmitted at time nT , and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 192.5.2.

192.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as shown in Equation (192–15).

(192–15)

$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t)$ In Equation (192–15) $h_R(t)$ denotes the symbol response of the overall impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

192.4.4 State variables

192.4.4.1 State diagram variables

block_lock

See 192.3.5.1.2. This variable is passed to the PMA via the block_lock parameter of the PMA_PCSSYNC.request primitive.

config

This variable takes the value of the management parameter config based on the value of bit 1.2100.14 (see 45.2.1.214) and specifies to the PHY functions whether the PHY operates as the Leader or Follower.

Values:

LEADER : This value is continuously asserted when the PHY operates as the Leader.

FOLLOWER: This value is continuously asserted when the PHY operates as the Follower.

detect_lp_burst

A Boolean variable indicating whether symbols (either PAM2, PAM3, or PAM4) of a TDD burst have been detected.

Values:

TRUE: TDD PAM2, PAM3, or PAM4 symbols are detected.

FALSE: PMA detects the Z symbols after the PAM2/PAM3/PAM4 burst has ended (PMA could use timer timeout to terminate this detection signal).

hi_rfer

See 192.3.5.1.2. This variable is passed to the PMA via the **hi_rfer** parameter of the **PMA_PCSSYNC.request** primitive.

link_enable

This variable is set by management or default to enable or disable the PHY. It is set to disable the link upon power on reset or release from power down (see 192.4.2.5). Transition to ENABLE initiates PHY Control and the Link Monitor state diagram.

Values:

ENABLE: Enable operation of the PHY.
DISABLE: Disable the transmitter and await initiation of training.

link_status

The **link_status** parameter set by PMA Link Monitor state diagram.

Values:

OK: The Link Monitor function indicates that a valid MultiGBASE-A link is established. Reliable reception of signals transmitted from the remote PHY is possible.
FAIL: No valid link established.

loc_countdown_done

This variable is only used by the Leader. It indicates that the Leader has finished sending the last Leader countdown Infofield and received the responding (last) Infofield from the Follower at the current TRAINING stage.

Values:

TRUE: The Leader has sent its last burst ($BC24 = \text{PhaseSwBC24} - 1$) and received the last burst from the Follower, as indicated by the received InfoField since the latest entry to a TRAINING state.
FALSE: The Leader has not sent its last burst ($BC24 = \text{PhaseSwBC24} - 1$) or has not received the last burst from the Follower, as indicated by the received InfoField since the latest entry to a TRAINING state.

loc_rcvr_status

See 192.2.1.6.

negotiation_done

During symmetric training phase, after **loc_rcvr_status** = OK, the Leader and Follower exchange capabilities, **delay_count** and negotiated data rate, and then set the **negotiation_done** variable to OK.

Values:

OK: Negotiation is done, can move to COUNTDOWN0 state.
NOT_OK: Negotiation is not done, stay in TRAINING0 state.

pcs_data_mode

See 192.2.1.8.1.

pma_reset

Allows reset of all PMA functions. It is set by PMA Reset.

Values: ON or OFF.

PMA_state

Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.

Values:

- 00: TRAINING state.
- 01: COUNTDOWN state.

rem_countdown_done

This variable is only used by the Follower. It indicates that the Follower has finished receiving the last Infofield from the Leader at the current TRAINING stage, and has sent at least one Infofield.

Values:

- TRUE: The Follower has received the last burst ($BC24 = \text{PhaseSwBC24} - 1$) sent by the Leader and has sent at least one InfoField since the latest entry to a TRAINING state.
- FALSE: The Follower has not received the last burst ($BC24 = \text{PhaseSwBC24} - 1$) sent by the Leader or has not sent at least one InfoField since the latest entry to a TRAINING state.

rem_rcvr_status

The status of the link partner's receiver indicated in the loc_rcvr_status received in the InfoField from the remote PHY. See 192.2.1.7.1.

training_active

A Boolean variable indicating whether the link_fail_inhibit_timer has started.

Values:

- TRUE: The link_fail_inhibit_timer is running and the link is in a training phase.
- FALSE: The link is not currently in a training phase.

training_phase

This variable indicates whether training is currently in the symmetric mode or the asymmetric mode of training. It is transmitted to the link partner in the InfoField. See 192.4.2.4.4.

Values:

- 00: PHY Control is currently in either in a silent mode or a symmetric training phase.
- 01: PHY Control is currently in an asymmetric training phase.

tx_mode

See 192.2.1.1.

192.4.4.2 Timers

link_fail_inhibit_timer

A timer used to determine the maximum amount of time the PHY Control sets training_active = TRUE. The timer shall expire $97.5 \text{ ms} \pm 0.5 \text{ ms}$ after being started.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING1, and PCS_TEST states. The timer shall expire $975 \text{ } \mu\text{s} \pm 50 \text{ } \mu\text{s}$ after being started.

tdd_watchdog_timer

A timer used to determine that the TDD signal has not been detected within the last ten TDD cycles. The timer shall expire $96 \text{ } \mu\text{s} \pm 5 \text{ } \mu\text{s}$ after being started.

192.4.5 State diagrams

The PHY Control state diagram is shown in Figure 192–31 and Figure 192–32.

The Link Monitor state diagram is shown in Figure 192–33.

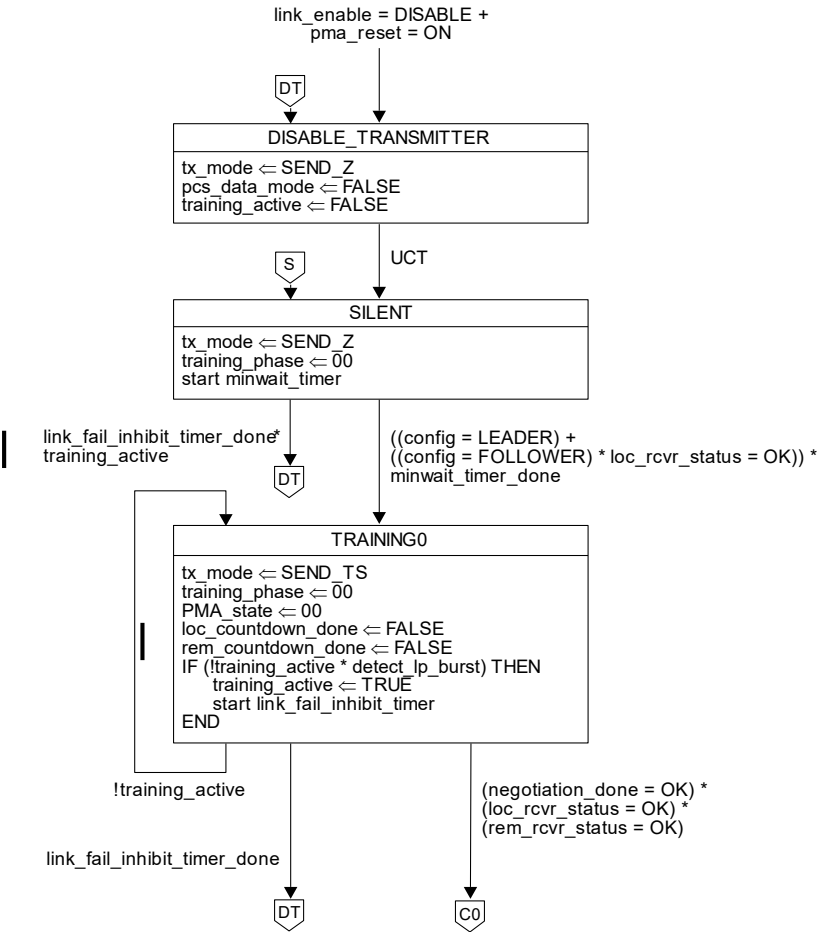


Figure 192–31—PHY Control state diagram part a

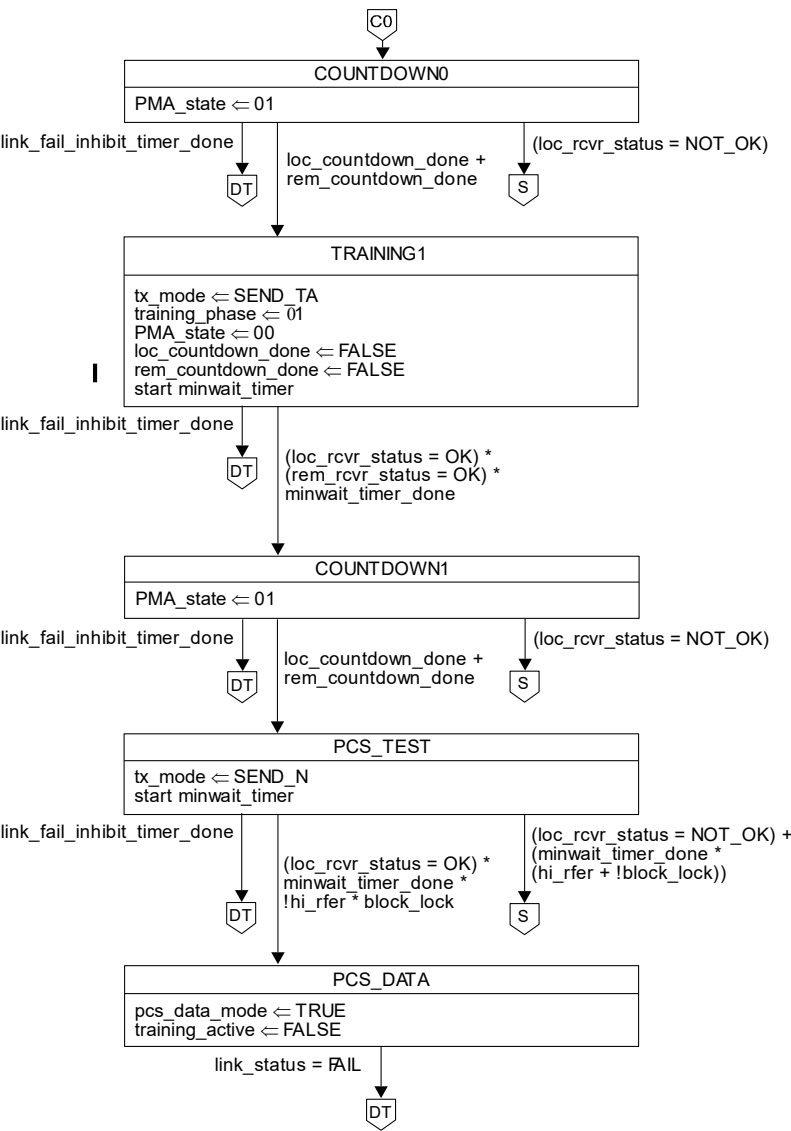


Figure 192-32—PHY Control state diagram part b

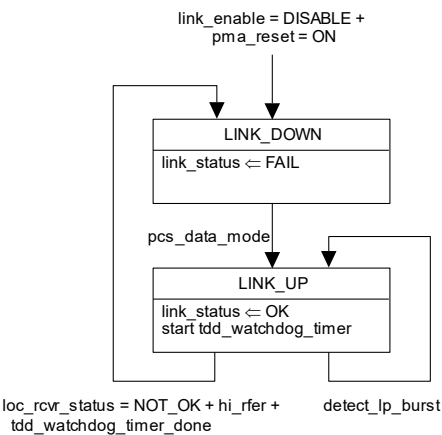


Figure 192-33—Link Monitor state diagram

192.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

192.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 192-21. If MDIO is not implemented, then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of non-test mode operation.

Table 192-21—MDIO management registers settings for test modes

Register value	Register description
000	Non-test mode operation
001	Test mode 1—Setting Leader and Follower PHYs for transmit clock jitter test in linked mode
010	Test mode 2—Transmit MDI jitter test in Leader mode

011	Test mode 3—Reserved
100	Test mode 4—Transmitter distortion test
101	Test mode 5—Continuous idle payload transmission (for the PSD Mask test)
110	Test mode 6—Transmitter droop test mode
111	Test mode 7—Data mode with zero data pattern (for BER monitoring)

Test mode 1 enables testing of timing jitter on the Leader and Follower transmitters. The Leader and Follower PHYs are connected over a link segment defined in 192.7 or 192.8. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5. TX_TCLK_187.5 is equal to 187.5 MHz and is a divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in Leader timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous repeating pattern of $\{+1, -1\}$ symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference.

Test mode 4 is for transmitter distortion testing. When test mode 4 is enabled in PAM2 mode (i.e., 100 Mb/s, 2.5 Gb/s, or 5 Gb/s transmit MAC data rate), the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ (see Figure 192–5 and Figure 192–6). All PHYs shall support transmission of this signal at 3 GBd. PHYs that support 1 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM3 mode (i.e., 5 Gb/s or 7.5 Gb/s transmit MAC data rate using PAM3), the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ (see Figure 192–6). PHYs that support 5G+1000 or 7.5 Gb/s transmit rate 7.5G+100 shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM4 mode (i.e., 7.5 Gb/s or 10 Gb/s transmit MAC data rate using PAM4), the PHY shall transmit the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ and $B_n = Scr_n[3] \oplus Scr_n[8]$ (see Figure 192–6). PHYs that support 7.5G+1000 or 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

$$(192-16)g(x) = 1 + x^9 + x^{11}$$

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit continuously with no QUIET period or refresh header and with transmit signal level corresponding to the data mode of operation. The PCS Transmit will encode data as when tx_mode = SEND_N, and as if continuously receiving idle control

characters from the XGMII. The test applies to both the Leader and Follower. The clock is sourced from a stable clock with 100 ppm accuracy for this test.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {−1} symbols with the transmitted symbols timed from its local 3 GHz clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the non-test mode with zero data pattern. Instead of encoding data received from the MAC, the input to the RS-FEC is all-zero message symbols and the continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

192.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 192–34, Figure 192–35, and Figure 192–36, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

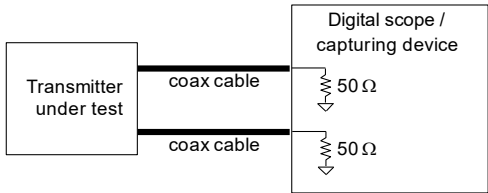


Figure 192–34—Transmitter test fixture 1 for -T1 transmitter d coop, transmitter distortion, power spectral density, transmit power level, and MDI jitter

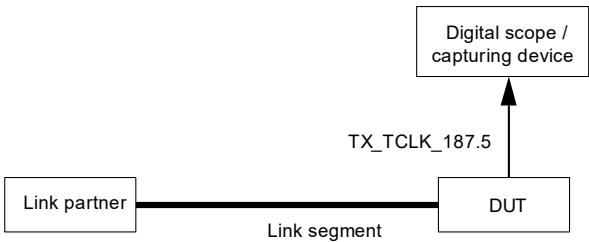


Figure 192–35—Transmitter test fixture 2 for -T1 and -M1 leader and Follower clock jitter measurement

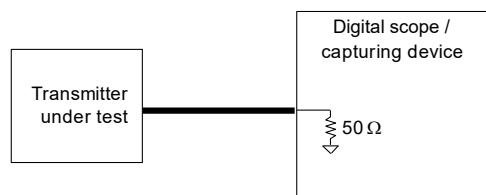


Figure 192–36—Transmitter test fixture 3 for -V1 transmitter drop, transmitter distortion, power spectral density, transmit power level, and MDI jitter measurements

192.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 192.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be ac-coupled (i.e., it presents a high dc common-mode impedance at the MDI). There may be various methods for ac-coupling in actual implementations.

When a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of $\pm 0.1\%$.

192.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using transmitter test fixture 1 (see Figure 192–34) or test fixture 3 (see Figure 192–36), the magnitude of both the positive and negative droop shall be less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing.

192.5.2.2 Transmitter distortion

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 1 (see Figure 192–34) or transmitter test fixture 3 (see Figure 192–36) as appropriate to the MDI.

The peak distortion is determined by sampling the signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signals shall be at least 4000 transmitted symbols long and be sampled with a minimum of 10x oversampling. The transmit baud rate may be reduced to 1 GBd by repeating the symbols using the same clock edge as in the data mode of operation.

The peak distortion values, measured at a minimum of ten equally spaced phases of a single symbol period, shall be less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM3 and PAM4 transmitters.

% Post processing pseudo-code for transmitter distortion

```
clear
Ns=2^11-1; % Scrambler length
Nc=70; % Canceller length
Modulation=2; % Choices are 2 for PAM2, 3 for PAM3, or 4 for PAM4

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
    scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% Generate tm4 (test mode 4) for a given modulation
if Modulation==2
    tm4=2*scr-1;
elseif Modulation==3
    tm4=ones(Ns,1);
    map=[-1 -1;-1 0;0 -1;1 -1;0 1;-1 1;1 1;1 0];
    scr3=[scr, circshift(scr,1), circshift(scr,2)];
    data = 4*scr3(:,3)+ 2*scr3(:,2)+scr3(:,1);
    for n=1:length(data)
        tm4([2*n-1,2*n]) =map(data(n)+1,:);
    end
elseif Modulation==4
    tm4=ones(Ns,1);
    map=[-1;-1/3;1/3];
    DS=[scr,mod(circshift(scr,3) + circshift(scr,8),2)];
    data = 2*DS(:,1)+DS(:,2);
    for n=1:length(DS)
        tm4(n) =map(data(n)+1);
    end
else
    disp('Error: The code supports either PAM2, PAM3, or PAM4')
    return
end

% Test mode4 matrix
for i=1:Nc
    X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file

% Minimum of 4K Tx symbols, 10X oversampling, high resolution capture
fid=fopen('TestMode4.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF at Nyquist
[A,B]=butter(1,1/10,'low');
tx=filter(A,B,tx);

% HPF (with this HPF, the 70-tap canceller residual linear error is 0.00
tx = filter([1,-1],[1,-0.98],tx);

% Select one period, 10x oversampling, a row vector
tx=tx((1:Ns*10)+2e3)'; % removes HPF transients

% Level normalization
```

```
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10
    tx1=tx(n:10:end);
    temp=xcorr(tx1,tm4); % Align data and test pattern
    index=find(abs(temp)==max(abs(temp)));
    X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);
    coef=tx1/X; % Compute coefficients that minimize squared error in a cyclic
        block
    err=tx1-coef*X; % Linear canceller
    dist(n) = max(abs(err)); % Peak distortion
    SNR(n)=std(tx)/std(err); % SNR
End

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist
```

192.5.2.3 Transmitter timing jitter and jitter at the MDI

The following measurements are performed for a PHY in Leader mode:

- 1) The RMS jitter for jitter frequencies greater than 100 kHz measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1 shall be less than 1 ps when supporting 10 Gb/s or 7.5G+1000, 1.5 ps when supporting 7.5-Gb/sG+100 or 5G+1000, 2 ps when supporting 5-Gb/sG+100, and 4 ps when supporting 2.5 Gb/s.
- 2) Peak-to-peak of Time Interval Error measured in test mode 1 using test fixture 2 over a period of 100 μ s shall be less than 10 ps when supporting 10 Gb/s or 7.5G+1000, 15 ps when supporting 7.5-Gb/sG+100 or 5G+1000, 20 ps when supporting 5-Gb/sG+100, and 40 ps when supporting 2.5 Gb/s.

The following measurements are performed using test fixture 2 (see Figure 192–35) for a PHY in Follower mode:

- 1) The RMS jitter for jitter frequencies greater than 1 MHz measured in test mode 1 shall be less than 1 ps when supporting 10 Gb/s or 7.5G+1000, 1.5 ps when supporting 7.5-Gb/sG+100 or 5G+1000, 2 ps when supporting 5-Gb/sG+100, and 4 ps when supporting 2.5 Gb/s.
- 2) Peak-to-peak of Time Interval Error over any period of 10 μ s measured in test mode 1 over 50 overlapping periods of 10 μ s each shall be less than 15 ps for 10 Gb/s or 7.5G+1000, 22.5 ps when supporting 7.5-Gb/sG+100 or 5G+1000, 30 ps for 5G+100-Gb/s, and 60 ps for 2.5 Gb/s. The overlapping period of 5 μ s is assumed.

192.5.2.4 Transmitter power spectral density (PSD) and power level

Transmitter power spectral density (PSD) and power level measurements are performed in test mode 5. The measured transmit power shall be in the range specified in Table 192–22 when using the same test fixture as used for PSD measurement. When the value of tx_symb is Z, the transmit signal at the MDI is nominally zero and the transmit signal shall be less than -36 dBm for frequencies greater 10 MHz.

Table 192–22—Power levels

Transmit MAC data rate	MDI, -T1		MDI, - V1	
	Min (dBm)	Max (dBm)	Min (dBm)	Max (dBm)
100 Mb/s	0	2	−3	−1
~~1 Gb/s~~	~~2~~	~~4~~	~~−1~~	~~1~~
2.5 Gb/s	0	2	−3	−1
~~5 Gb/s~~ ~~5G+100~~	2	4	−1	1
~~5G+1000~~	~~1~~	~~3~~	~~−2~~	~~0~~
~~7.5 Gb/s~~ ~~7.5G+100~~	1	3	−2	0
~~7.5G+1000~~	~~0~~	~~2~~	~~−3~~	~~−1~~
10 Gb/s	0	2	−3	−1

The power spectral density of the transmitter of -T1, measured into a 100 Ω differential load using test fixture 1 (see Figure 192–34), shall be between the upper PSD mask specified in Equation (192–17) and the lower PSD mask specified Equation (192–18).

The upper and lower masks for each MAC data rate are shown in Figure 192–37, Figure 192–38, Figure 192–39, and Figure 192–40. See Table 192–2 for the definition of *S*. See Table 192–23 for the definition of PSD mask *K* factor.

Table 192–23—PSD mask *K* factor

Transmit MAC data rate	<i>K</i>
100 Mb/s	0
~~1 Gb/s~~	~~0~~
2.5 Gb/s	0
~~5G+100~~ ~~5 Gb/s~~	0
~~5G+1000~~	~~1~~

~~7.5G+1007.5 Gb/s~~	1
~~7.5G+1000~~	~~2~~
10 Gb/s	2

(192–17)

$$UpperPSD(f) = \begin{cases} -89 - K & \text{dBm/Hz} & 40 < f \leq 1200 \times S \\ -87 - K - \frac{f}{600 \times S} & \text{dBm/Hz} & 1200 \times S < f \leq 3000 \times S \\ -80 - K - \frac{f}{250 \times S} & \text{dBm/Hz} & 3000 \times S < f \leq 5000 \times S \end{cases}$$

(192–18)

$$LowerPSD(f) = \begin{cases} -93 - K & \text{dBm/Hz} & 40 < f \leq 600 \times S \\ -92 - K - \frac{f}{600 \times S} & \text{dBm/Hz} & 600 \times S < f \leq 2400 \times S \\ -86.4 - K - \frac{f}{250 \times S} & \text{dBm/Hz} & 2400 \times S < f \leq 3500 \times S \end{cases} \text{ where}$$

f is the frequency in MHz

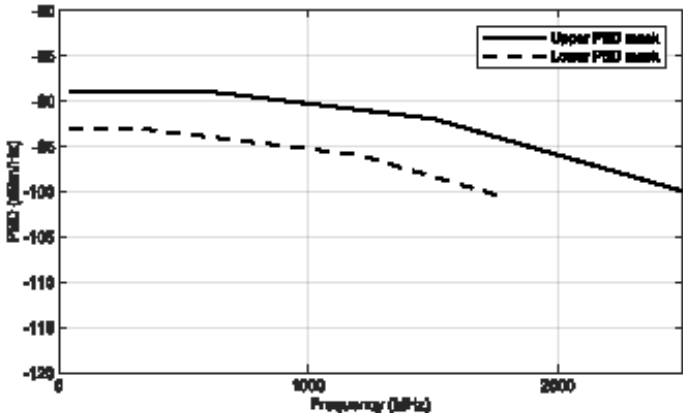


Figure 192–37—Transmitter Power Spectral Density for 10 Mb/s and 25 Gb/s MAC data rates, upper and lower masks

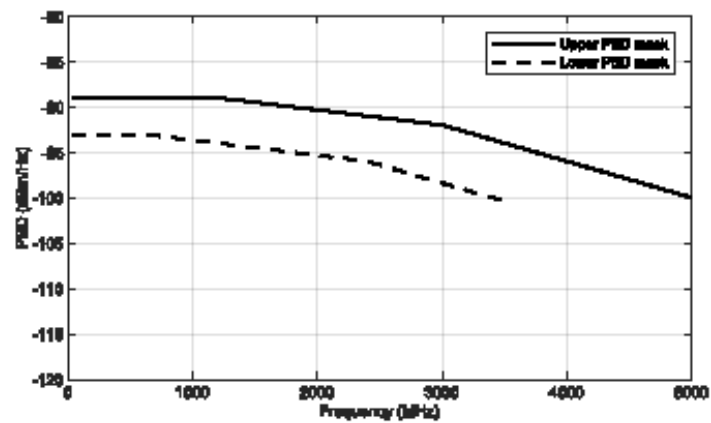


Figure 192-38—Transmitter Power Spectral Density for 5 Gb/s MAC at a rate
upper and lower masks

[Editing note for Figure 192-38: Change title 5 Gb/s to 1 Gb/s or 5Gb/s associated with 100 Mb/s receive]

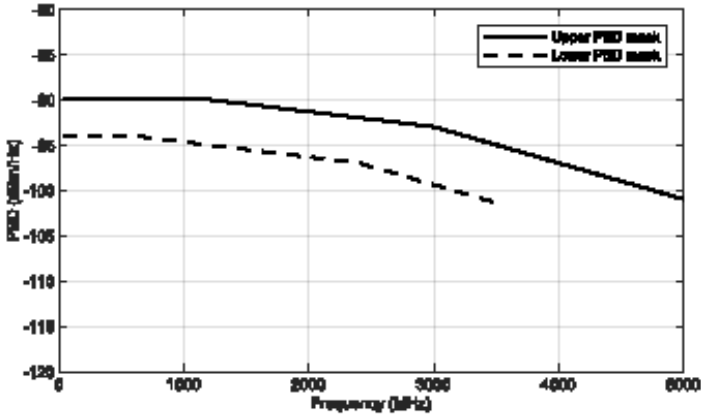


Figure 192-39—Transmitter Power Spectral Density for 7.5 Gb/s MAC at a rate
upper and lower masks

[Editing note for figure 192-39: change title 7.5 Gb/s to 5Gb/s associated with 1 Gb/s receive or 7.5 Gb/s associated with 100 Mb/s receive]

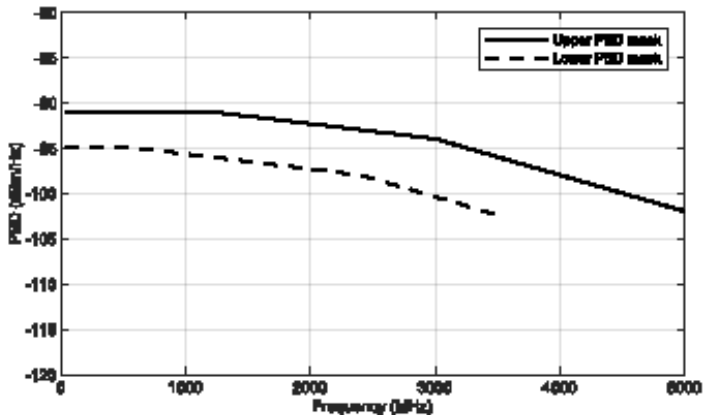


Figure 192-40—Transmitter Power Spectral Density for 10 Gb/s MAC data rate, upper and lower masks

[Editing note for figure 192-40: change title 10 Gb/s to 75Gb/s associated with 1 Gb/s receive or 10 Gb/s]

For the power spectral density of -V1, with single ended termination of 50 Ω load and test fixture 3 (see Figure 192-36), both upper and lower PSD Masks are lower by 3 dB from Equation (192-17), Equation (192-18), Figure 192-37, Figure 192-38, Figure 192-39 and Figure 192-40.

192.5.2.5 Transmitter peak output

The transmit differential signal at the -T1 MDI should be less than the peak-to-peak values specified in Table 192-24 when measured with a 100 Ω termination. The transmit signal at the -V1 MDI should be less than the peak-to-peak values specified in Table 192-24 when measured with a 50 Ω termination. The limits in this clause apply to all transmitted symbol sequences, including SEND_N, SEND_TS, and SEND_TA.

Table 192-24—Transmitter peak-to-peak output

Transmit MAC data rate	-T1 MDI peak-to-peak output (V)	-V1 MDI peak-to-peak output (V)
100 Mb/s	1.3	0.65
1 Gb/s	1.5	0.75
2.5 Gb/s	1.3	0.65
5G+1005-Gb/s	1.5	0.75

<u>5G+1000</u>	<u>1.5</u>	<u>0.75</u>	
~~7.5G+1007.5 Gb/s~~	1.5	0.75	
<u>7.5G+1000</u>	<u>1.7</u>	<u>0.85</u>	
10 Gb/s	1.7	0.85	

192.5.2.6 Transmitter clock frequency

When using a local timing reference, the symbol transmission rate shall be within the range $6 \times S \text{ GBd} \pm 100 \text{ ppm}$ with drift less than 1 ppm/sec.

When the Follower is using a recovered timing reference, the symbol transmission rate (scaled by S) shall be within $\pm 10 \text{ ppm}$ of the recovered clock.

192.5.3 Receiver electrical specifications

The PMA provides the Receive function specified in 192.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 192.7 or 192.8.

192.5.3.1 Receiver input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 192.5.2 and have passed through a link specified in 192.7 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link_status = OK.

Single-ended signals received at the MDI that were transmitted from a remote transmitter within the specifications of 192.5.2 and have passed through a link specified in 192.8 shall be received with a BER less than 10^{-12} after RS-FEC decoding, and sent to the XGMII after link_status = OK.

This specification can be verified by a frame error ratio less than 7.8×10^{-9} for 800 octet frames with minimum IPG or greater than 220-octet IPG.

192.5.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver’s tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 192–25. The minimum noise frequency is 10 MHz. The -T1 receive DUT is connected to the noise source through a directional coupler with a -T1 link segment (see 192.7) as shown in Figure 192–41. The -V1 receive DUT is connected to the noise source through a directional coupler with a -V1 link segment (see 192.8) as shown in Figure 192–42. The BER is expected to be less than 10^{-12} , and to satisfy this specification, the frame loss ratio is less than 10^{-9} for 125-octet packets measured at the MAC/PLS service interface.

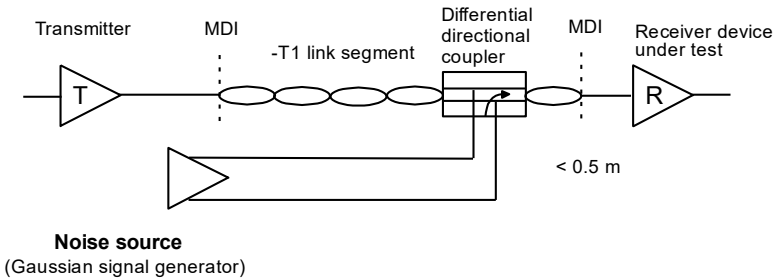


Figure 192–41—Broadband stationary noise rejection test setup, -T1

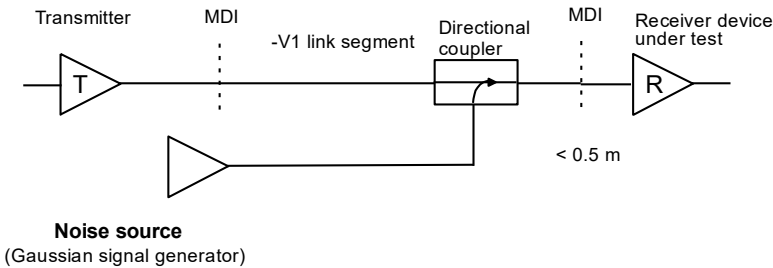


Figure 192–42—Broadband stationary noise rejection test setup, -V1

Table 192–25—Broadband stationary noise source, high speed data rate

Transmit MAC data rate	Noise bandwidth (MHz)	Added noise at MDI (dBm/Hz)	
		-T1	-V1
2.5 Gb/s	1750	–140	–143

~~5-Gb/s~~ 5G+100	3500	−144	−147
~~7.5-Gb/s~~ 5G+1000 7.5G+100	3500	−146	−149
7.5G+1000 10 Gb/s	3500	−148	−151

192.6 Management interface

MultiGBASE-A makes extensive use of the management functions that may be provided by the optional MDIO (see Clause 45).

192.7 Link segment characteristics, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. -T1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s or 1 Gb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

192.7.1 Link transmission parameters

The transmission characteristics for a -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

192.7.1.1 Insertion loss

The insertion loss of a -T1 link segment shall meet the values determined using Equation (192–19).

(192–19)

Insertion loss $(f) \leq 0.322 \sqrt{f} + 0.0019f + \frac{1}{\sqrt{f}}$ (dB)

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–19) is plotted in Figure 192–43, which is provided for information only.

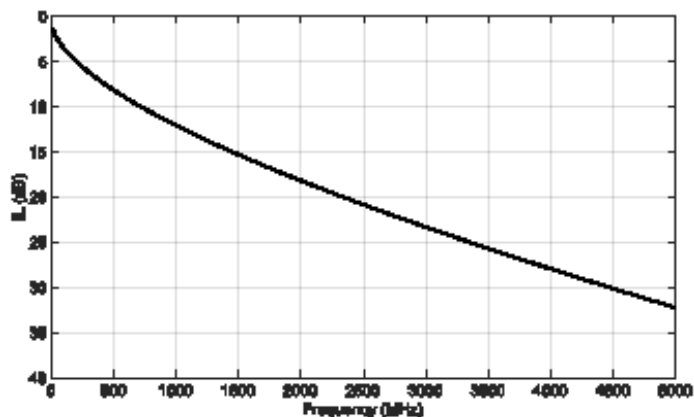


Figure 192–43—T1 link segment insertion loss

192.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of a -T1 link segment is 100 Ω.

192.7.1.3 Return loss

The return loss of a -T1 link segment shall meet the values determined using Equation (192–20).

(192–20)

$$RL(f) \geq \left\{ \begin{array}{ll} 12.5 & 10 \leq f < 500 \\ 12.5 - 3 \left(\frac{f-500}{1500} \right) & 500 \leq f < 2000 \\ 9.5 - 3 \left(\frac{f-2000}{2500} \right) & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{array} \right\} \quad (\text{dB})$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–20) is plotted in Figure 192–44, which is provided for information only.

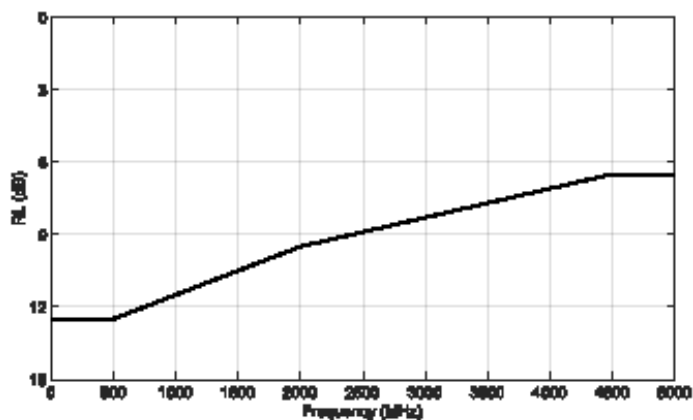


Figure 192–44—T1 link segment return loss

192.7.1.4 Coupling attenuation

The coupling attenuation of a -T1 link segment shall be as specified in 149.7.1.4.

192.7.1.5 Screening attenuation

The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5, where $F_{max} = 4000$ MHz.

192.7.1.6 Maximum link delay

The propagation delay of a -T1 link segment shall not exceed 160 ns for all frequencies between 10 MHz and 5 GHz.

192.7.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

192.7.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -T1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -T1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–21).

(192–21)

$$\text{PSANEXT}(f) = -10 \log_{10} \sum_{j=1}^m 10^{\frac{-\text{AN}(f)_j}{10}} \text{ dB}$$

where the function $\text{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -T1 link segment j (1 to m) for the disturbed -T1 link segment.

The PSANEXT loss between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (192–22).

(192–22)

$$\text{PSANEXT}(f) \geq 54 - 10 \log_{10} \left(\frac{f}{500} \right) \quad (\text{dB})$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–29) is plotted in Figure 192–45, which is provided for information only.

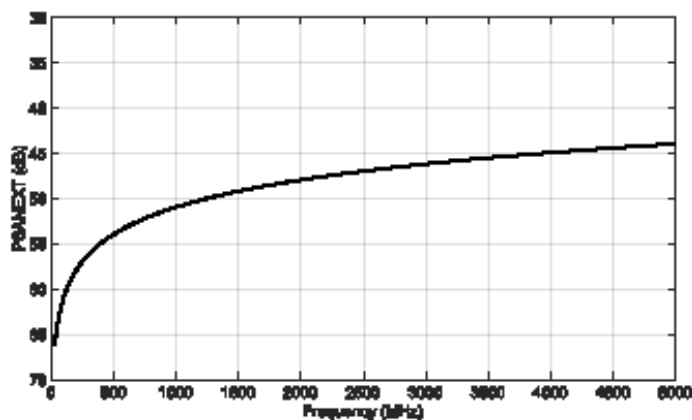


Figure 192–45—T1 link segment PSANEXT loss

192.7.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -T1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -T1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–23).

(192–23)

$$\text{PSAACRF}(f) = \left(-10 \log_{10} \sum_{j=1}^m 10^{\frac{-\text{AFEXT}_j(f)}{10}} \right) - \text{IL}_d(f) \quad \text{dB}$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$
 $\text{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -T1 link segment j (1 to m) to the disturbed -T1 link segment in dB
 $\text{IL}_d(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (192–24).

(192–24)

$$PSAACRF(f) \geq 51 - 9 \log_{10} \left(\frac{f}{300} \right) \quad (\text{dB})$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–31) is plotted in Figure 192–46, which is provided for information only.

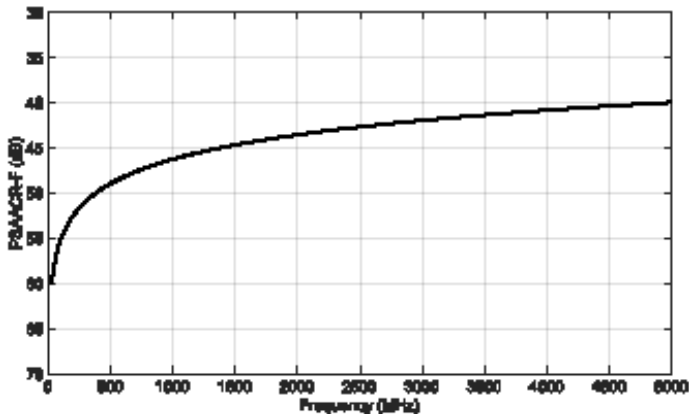


Figure 192–46—T1 link segment PSAACRF

192.8 Link segment characteristics, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial cable (-V1) that meet the requirements specified in this subclause. -V1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s or 1 Gb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

192.8.1 Link transmission parameters

The transmission characteristics for a -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

192.8.1.1 Insertion loss

The insertion loss of a -V1 link segment shall meet the values determined using Equation (192–25).

(192–25)

Insertion loss (f) ≤ 0.3 + 0.345 √ f + 0.000825 f + $\frac{0.48}{\sqrt{f}}$ (dB)

where

f is the frequency in MHz; 10 ≤ f ≤ 5000

Equation (192–25) is plotted in Figure 192–47, which is provided for information only.

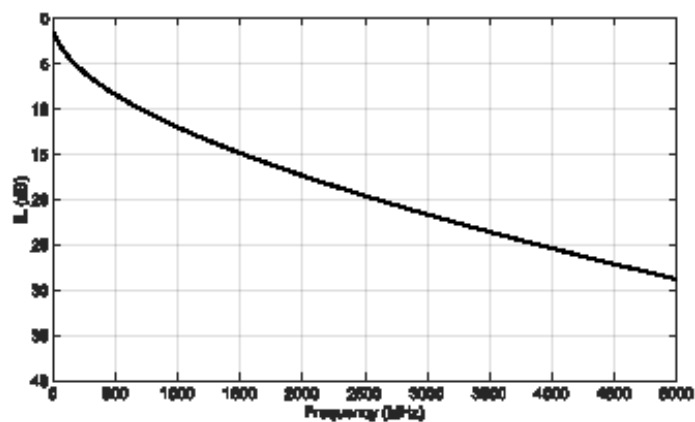


Figure 192–47—V1 link segment insertion loss

192.8.1.2 Single ended characteristic impedance

The nominal characteristic impedance of a -V1 link segment is 50 Ω.

192.8.1.3 Return loss

The return loss of a -V1 link segment shall meet the values determined using Equation (192–26).

(192–26)

$$RL(f) \geq \left\{ \begin{array}{ll} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left(\frac{f-500}{1500}\right) & 500 \leq f < 2000 \\ 9.5 - 3\left(\frac{f-2000}{2500}\right) & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{array} \right\} \quad (\text{dB})$$

where

f is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–26) is plotted in Figure 192–48, which is provided for information only.

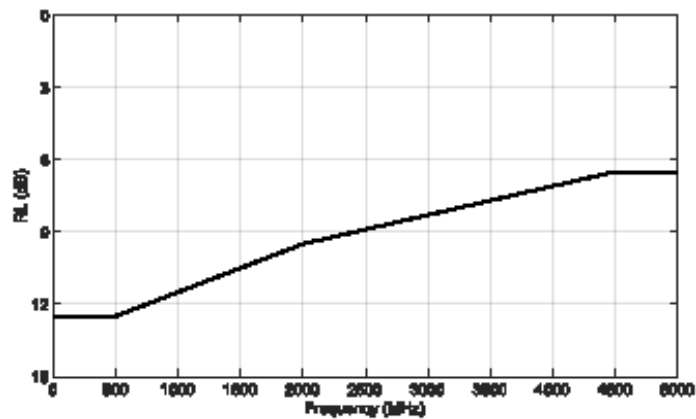


Figure 192–48—V1 link segment return loss

192.8.1.4 Coupling attenuation

Coupling attenuation is not defined for -V1 link segments.

192.8.1.5 Screening attenuation

The screening attenuation of a -V1 link segment shall meet the values determined using Equation (192–27). Screening attenuation is tested as specified in IEC 62153-4-7 using the triaxial tube-in-tube method.

(192–27)

$$\text{Screening attenuation}(f) \geq \left\{ \begin{array}{ll} 55 & 30 \leq f < 1000 \\ 50 & 1000 \leq f \leq 3000 \\ 45 & 3000 \leq f \leq 4000 \end{array} \right\} \text{ (dB)}$$

where

f is the frequency in MHz; $30 \leq f \leq 4000$

Equation (192–27) is plotted in Figure 192–49, which is provided for information only.

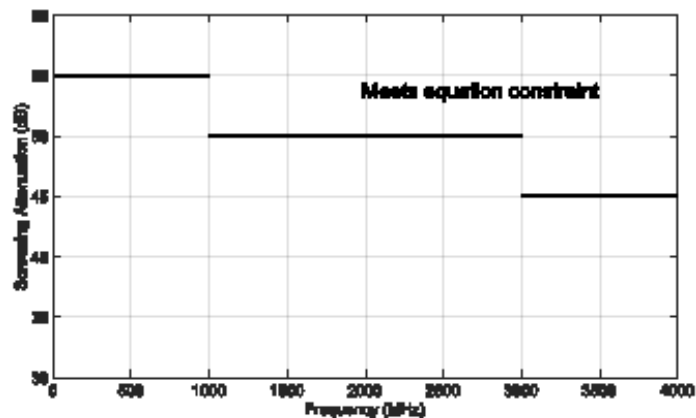


Figure 192–49—M link segment screening attenuation

192.8.1.6 Maximum link delay

The propagation delay of a -V1 link segment shall not exceed 160 ns for all frequencies between 10 MHz and 5 GHz.

192.8.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as alien crosstalk noise. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in [Annex 97B](#). These methodologies shall be applied with adaptation to unbalanced coaxial cabling and shall use a single 50 Ω termination to ground.

192.8.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -V1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -V1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–28).

(192–28)

$$\text{PSANEXT}(f) = -10 \log_{10} \sum_{j=1}^m 10^{\frac{-\text{AN}(f)_j}{10}} \text{ dB}$$

where the function $\text{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency f of the disturbing -V1 link segment j (1 to m) for the disturbed -V1 link segment.

The PSANEXT loss between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (192–29).

(192–29)

$$\text{PSANEXT}(f) \geq 54 - 10 \log_{10} \left(\frac{f}{500} \right) \quad (\text{dB})$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–29) is plotted in Figure 192–50, which is provided for information only.

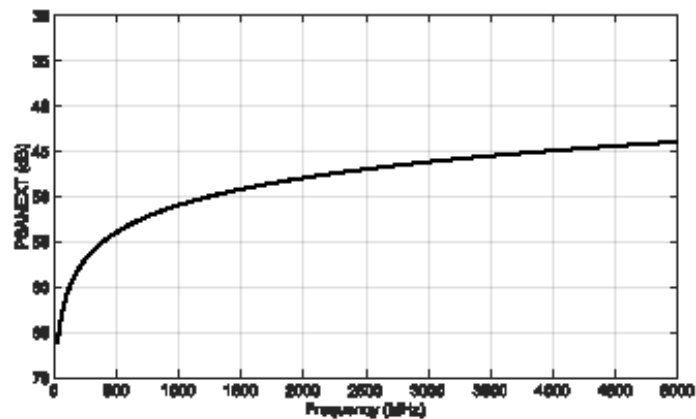


Figure 192–50—M link segment PWRNEXT loss

192.8.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -V1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -V1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–30).

(192–30)

$$\text{PSAACRF}(f) = \left(-10 \log_{10} \sum_{j=1}^m 10^{\frac{-\text{AFEXT}_j(f)}{10}} \right) - \text{IL}_d(f) \quad \text{dB}$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$
 $\text{AFEXT}_j(f)$ is the magnitude of the alien FEXT loss at frequency f from a disturbing -V1 link segment j (1 to m) to the disturbed -V1 link segment in dB
 $\text{IL}_d(f)$ is the measured insertion loss of the disturbed link segment at frequency f in dB

The PSAACRF between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (192–31).

(192–31)

$$\text{PSAACRF}(f) \geq 51 - 9 \log_{10} \left(\frac{f}{300} \right) \quad (\text{dB})$$

where

f is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–31) is plotted in Figure 192–51, which is provided for information only.

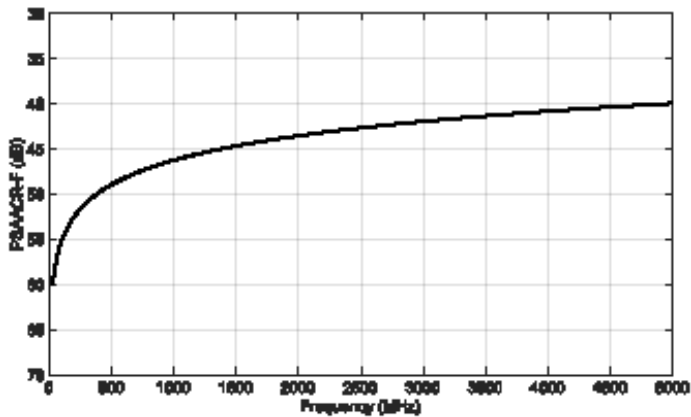


Figure 192–51—M link segment PMAACRF

192.9 MDI specification, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

192.9.1 MDI connectors

The -T1 MDI connectors are as specified in 149.8.1.

192.9.2 MDI electrical specification

The electrical requirements specified in 192.5.2 and 192.5.3 shall be met when the PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors.

192.9.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -T1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (192–32). For the -T1 MDI, a nominal differential characteristic impedance of 100 Ω is used.

(192–32)

$$MDI_Return_Loss(f) \geq \left\{ \begin{array}{ll} 18 + 20 \log_{10} \left(\frac{f}{50} \right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13 \log_{10} \left(\frac{f}{400} \right) & 400 \leq f < Fmax \end{array} \right\} \text{ (dB)}$$

where

f
 $Fmax$

is the frequency in MHz; $10 \leq f \leq Fmax$
= 3000 MHz for 100 Mb/s and 2.5 Gb/s data rates
= 4000 MHz for 1 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates

Equation (192–32) is plotted in Figure 192–52, which is provided for information only.

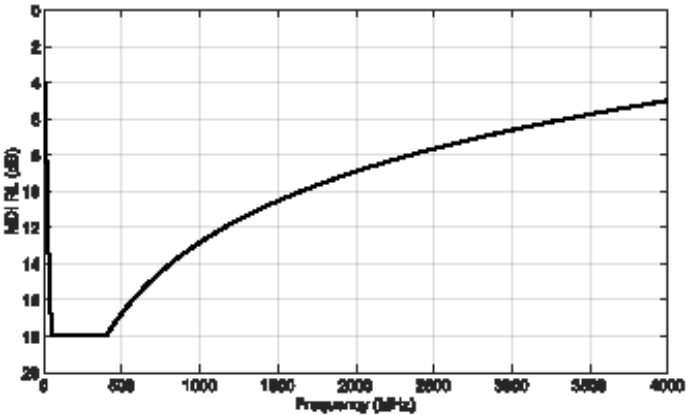


Figure 192–52—T1 MDI return loss using Equation (192–32)

192.9.3 MDI fault tolerance

The -T1 MDI fault tolerance shall comply with 96.8.3.

192.10 MDI specification, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial MDI (-V1) that meets the requirements specified in this subclause.

192.10.1 MDI connectors

The -V1 mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the -V1 mechanical interface is beyond the scope of this standard.

192.10.2 MDI electrical specifications

The electrical requirements specified in 192.5.2 and 192.5.3 shall be met when the PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable.

192.10.2.1 MDI return loss

The differential impedance at the -V1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -V1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (192–33). For the -V1 MDI, a nominal differential characteristic impedance of 50 Ω is used.

(192–33)

$$MDI_Return_Loss(f) \geq \begin{cases} 18 + 20 \log_{10} \left(\frac{f}{50} \right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13 \log_{10} \left(\frac{f}{400} \right) & 400 \leq f < Fmax \end{cases} \text{ (dB)}$$

where

f is the frequency in MHz; $10 \leq f \leq Fmax$
 $Fmax$ = 3000 MHz for 100 Mb/s and 2.5 Gb/s data rates
= 4000 MHz for 1 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates

Equation (192–33) is plotted in Figure 192–53, which is provided for information only.

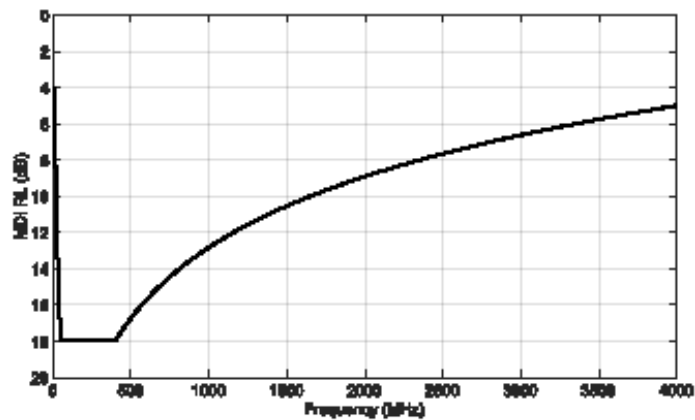


Figure 192–53—MDI return loss using Equation (192–33)

192.10.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 192–26, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

Table 192–26—Connection fault

Center conductor	Shield
No fault	Ground
MDI +	Ground
Ground	Ground
+50 V dc	Ground

192.11 Environmental specifications

192.11.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

192.11.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

192.11.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

- a) General loads: ISO 16750–1
- b) Electrical loads: ISO 16750–2, ISO 7637–2:2008, and ISO 8820–1
- c) Mechanical loads: ISO 16750–3, ASTM D4728, and ISO 12103–1
- d) Climatic loads: ISO 16750–4, IEC 60068–2–1, IEC 60068–2–27, IEC 60068–2–30, IEC 60068–2–38, IEC 60068–2–52, IEC 60068–2–64, and IEC 60068–2–78
- e) Chemical loads: ISO 16750–5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

192.11.3 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

- a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21
- b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21
- c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3
- d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

192.12 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (see [Clause 31](#) and [Annex 31B](#)) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 192–27. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

Table 192–27—Delay constraints

Transmit MAC data rate	Maximum delay (BT)	Maximum delay (pause_quanta)	Maximum delay (ns)
100 Mb/s	1 536	3	15 360
~~1 Gb/s~~	~~8 704~~	~~17~~	~~8 704~~
2.5 Gb/s	5 120	10	2 048
~~5G+1005-Gb/s~~	10 240	20	2 048
~~5G+1000~~	~~15 360~~	~~30~~	~~3 072~~
~~7.5G+1007.5-Gb/s~~	15 360	30	2 048
~~7.5G+1000~~	~~30 480~~	~~40~~	~~4 096~~
10 Gb/s	20 480	40	2 048

192.13 Protocol implementation conformance statement (PICS) proforma for Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1²

192.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in [Clause 21](#).

192.13.2 Identification

192.13.2.1 Implementation identification

Supplier ¹	
Contact point for inquiries about the PICS ¹	
Implementation Name(s) and Version(s) ^{1,3}	
Other information necessary for full identification— e.g., name(s) and version(s) for machines and/or operating systems; System Name(s) ²	
NOTE 1—Required for all implementations. NOTE 2—May be completed as appropriate in meeting the requirements for the identification. NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model).	

²*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

192.13.2.1

192.13.2.2 Protocol summary

Identification of protocol standard	IEEE Std 802.3dm-202x, Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1
Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS	
Have any Exception items been required? No ☐ Yes ☐ (See Clause 21 ; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.)	

Date of Statement	
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192.13.2.2

192.13.3 Major capabilities/options

Item	Feature	Subclause	Value/Comment	Status	Support
*PHY-T1	MultiGBASE-AT1 capability	192.1.1	Supports MultiGBASE-AT1 operation	O	Yes ☐ No ☐
*PHY-V1	MultiGBASE-AV1 capability	192.1.1	Supports MultiGBASE-AV1 operation	O	Yes ☐ No ☐
*7.5GTX	7.5 Gb/s transmit MAC data rate	192.1.1	Supports 7.5 Gb/s mode of operation, PHY_S	O	Yes ☐ No ☐
*10GTX	10 Gb/s transmit MAC data rate	192.1.1	Supports 10 Gb/s mode of operation, PHY_S	O	Yes ☐ No ☐
*10GRX	10 Gb/s receive MAC data rate	192.1.1	Supports 10 Gb/s mode of operation, PHY_D	O	Yes ☐ No ☐
*INS-LS, T1	Installation/link segment, -T1	192.7	Items marked with INS-LS, T1 include installation and cabling specifications for link segments and are not applicable to a PHY manufacturer	O	Yes ☐ No ☐

*INS-LS, V1	Installation/link segment, -V1	192.8	Items marked with INS-LS, V1 include installation and cabling specifications for link segments and are not applicable to a PHY manufacturer	O	Yes [] No []
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192.13.3

192.13.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

192.13.4.1 PCS Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PCST1	PCS Reset	192.3.2.1	Meets requirements 192.3.2.1	M	Yes []
PCST2	Control and management interface restoration	192.3.2.1	Restored to operation within 10 ms from the setting of bit 3.2322.15	M	Yes []
PCST3	PCS Transmit compliance	192.3.2.2	Conforms to the PCS 64B/65B Transmit state diagram in Figure 192–22 and to the PCS Transmit bit ordering in Figure 192–5 and Figure 192–6	M	Yes []
PCST4	PMA_TXMODE.indication message SEND_Z value	192.3.2.2	PCS Transmit passes Z symbols at each symbol period to the PMA via the PMA_UNITDATA.request primitive	M	Yes []
PCST5	PMA_TXMODE.indication message SEND_TS or SEND_TA value	192.3.2.2	PCS Transmit generates the O_n sequence defined in 192.3.4 to the PMA via the PMA_UNITDATA.request primitive	M	Yes []
PCST6	PMA_TXMODE.indication message SEND_N value	192.3.2.2	The PCS is in the data mode of operation and the PCS Transmit function uses a 65B coding technique to generate code-groups that represent data or control	M	Yes []

PCST7	Idle /I/ insertion and deletion	192.3.2.2.7	Occurs in groups of four. /I/s may not be added while data is being received. The first four characters after a /T/ are not be deleted when deleting /I/s.	M	Yes []
PCST8	RS-FEC (LS) encoding	192.3.2.2.13	Takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and generates the six 8-bit parity symbols (48 bits total)	M	Yes []
PCST9	RS-FEC (HS) encoding	192.3.2.2.13	Takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and generates the six 8-bit parity symbols (48 bits total)	M	Yes []
PCST10	Transmitter interleaving depth, L	192.3.2.2.14	Round-robin interleaving scheme shown in Figure 192–8 is applied	M	Yes []
PCST11	Transmitter interleaving depth, L > 1	192.3.2.2.14	Predefined for each data rate and complies with Table 192–4	M	Yes []
PCST12	Superframe aggregation	192.3.2.2.14	HS_TX PCS Transmit aggregates L RS-FEC input frames into an interleaved RS-FEC input	M	Yes []
PCST13	Scrambled refresh header data bit	192.3.2.2.17	See Equation (192–4)	M	Yes []
PCST14	PRBS11 scrambler polynomial	192.3.2.2.18	The PRBS11 pattern generator produces the same result as the implementation shown in Figure 192–10	M	Yes []
PCST15	PRBS11 scrambler state rule	192.3.2.2.18	Scrambler state is never initialized to all zeros	M	Yes []
PCST16	PRBS11 scrambler continuity	192.3.2.2.18	Once started, during PMA training, the scrambler continues to run uninterrupted during the refresh headers of each frame	M	Yes []

PCST17	PRBS11 scrambler stop rule	192.3.2.2.18	Once started, during PMA training, the scrambler stops during the burst payload field and QUIET	M	Yes []
PCST18	PRBS33 scrambler polynomial, Leader	192.3.2.2.19	PCS Transmit uses Equation (192–9) as the transmitter scrambler generator polynomial superframe	M	Yes []
PCST19	PRBS33 scrambler polynomial, Follower	192.3.2.2.19	PCS Transmit uses Equation (192–10) as the transmitter scrambler generator polynomial superframe	M	Yes []
PCST20	PRBS33 scrambler state rule	192.3.2.2.19	Scrambler state is never initialized to all zeros	M	Yes []
PCST21	PRBS33 scrambler continuity	192.3.2.2.19	Once started, during PMA training, the scrambler continues to run uninterrupted during the payload of PMA training frames and data mode frames	M	Yes []
PCST22	PRBS33 scrambler stop rule	192.3.2.2.19	Once started, during PMA training, the scrambler stops during QUIET and refresh headers	M	Yes []
PCST23	Gray mapping (Tx) for PAM4	192.3.2.2.20	See 192.3.2.2.20	10GTX:M	Yes [] N/A []
PCST24	Gray mapping (Rx) for PAM4	192.3.2.2.20	See 192.3.2.2.20	10GRX:M	Yes []
PCST25	PAM4 (Tx)	192.3.2.2.21	See 192.3.2.2.21	10GTX:M	Yes []
PCST26	PAM3 (Tx)	192.3.2.2.22	See 192.3.2.2.22	7.5GTX: M	Yes []

192.13.4.1

192.13.4.2 PCS Receive

Item	Feature	Subclause	Value/Comment	Status	Support
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PCSR1	PCS Receive compliance	192.3.2.3	Conforms to the PCS 64B/65B Receive state diagram in Figure 192–23 and the PCS Receive bit ordering in Figure 192–12 for the LS_RX and Figure 192–13 for the HS_RX, including compliance with the associated state variable as specified in 192.3.5.1.2	M	Yes []
PCST2	Frame and block synchronization	192.3.2.3.1	The receiving PCS concatenates rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload according to its data mode (see 192.3.2.3.1)	M	Yes []
PCST3	Descrambler, Leader	192.3.2.3.2	The Leader PHY uses the receiver descrambler generator polynomial in Equation (192–10)	M	Yes []
PCST4	Descrambler, Follower	192.3.2.3.2	The Follower PHY shall uses the receiver descrambler generator polynomial in Equation (192–9)	M	Yes []
PCST5	RS-FEC parity bit integrity check	192.3.2.3.3	The PCS Receive function checks the integrity of the RS-FEC parity bits defined in 192.3.2.2.13	M	Yes []

192.13.4.2

192.13.4.3 Physical Coding Sublayer (PCS)

Item	Feature	Subclause	Value/Comment	Status	Support
PCS1	SEND_TS frequency	192.3.4	Uses a symmetric frame format and transmits at 3 GBd	M	Yes []
PCS2	33-bit scrambler operation	192.3.4	Once started at the beginning of the training payload of the first training burst, continues to run uninterrupted for each symbol during all subsequent payloads and maintains its last state during the QUIET period and refresh headers	M	Yes []

PCS3	Refresh header content	192.3.4.2	Composed of a leading sequence of zeros followed by four bytes of 0x01, followed by four bytes of 0xF0	M	Yes []
PCS4	Scrambler synchronization acquisition and reporting	192.3.4.4	The PCS acquires descrambler state synchronization to the PAM2 training sequence and reports success through scr_status, and continues to use the synchronized state in all subsequent bursts in both data and training modes	M	Yes []
PCS5	DECODE function rule	192.3.5.1.3	Decodes the block as specified in 192.3.2.2.4	M	Yes []
PCS6	ENCODE function rule	192.3.5.1.3	Encodes the block as specified in 192.3.2.2.4	M	Yes []
PCS7	PCS functions	192.3.5.2	Performs the functions of RFER monitor, Transmit, and Receive as shown in Figure 192–21, Figure 192–22, and Figure 192–23	M	Yes []

192.13.4.3

192.13.4.4 OAM

Item	Feature	Subclause	Value/Comment	Status	Support
OAM1	State diagram behavior	192.3.7.4	Conforms to Figure 192–25 and Figure 192–26	OAM:M	Yes [] N/A []
OAM2	HS_TX mode OAM frame structure, first bit	192.3.7.2.1	The first bit of the first OAM symbol (OAM<0>) is inserted in the first RS frame in the first superframe of the TDD burst	OAM:M	Yes [] N/A []
OAM3	HS_TX mode OAM frame structure, subsequent bits	192.3.7.2.1	One subsequent bit of OAM<0> is inserted into each of second through tenth RS FEC frames	OAM:M	Yes [] N/A []
OAM4	LS_TX mode OAM frame structure	192.3.7.2.1	The first symbol (OAM<0>) is inserted in the first ten bits of the OAM field of the RS frame so that one OAM symbols is carried in each TDD burst	OAM:M	Yes [] N/A []

OAM5	When OAM is not implemented	192.3.7.2.1	10-bit OAM field is set to all zeros	OAM:M	Yes [] N/A []
OAM6	OAM frame data	192.3.7.2.1	Reserved fields are set to zero	OAM:M	Yes [] N/A []
OAM7	MultiGBASE-A OAM Frame acceptance criteria	192.3.7.2.13	See 192.3.7.2.13	OAM:M	Yes [] N/A []
OAM8	mr_tx_received	192.3.7.4.3	Clear on read	OAM:M	Yes [] N/A []

192.13.4.4

192.13.4.5 Physical Medium Attachment (PMA)

192.13.4.5.1 PMA Reset

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	PMA Reset function	192.4.2.1	See 192.4.2.1	M	Yes []

192.13.4.5.1

192.13.4.5.2 PMA Transmit

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT1	PMA Transmit operation	192.4.2.2	Continuously transmits pulses modulated by the symbols given by tx_symb onto the MDI, followed by a QUIET period to complete a TDD cycle, when the PHY Control state diagram (see Figure 192–31) is not in the DISABLE_TRANSMITTER state	M	Yes []
PMAT2	PMA Transmit signal compliance	192.4.2.2	Complies with the electrical specifications given in 192.5.2	M	Yes []

PMAT3	Clock source, Leader	192.4.2.2	The transmit symbol clock TX_TCLK is sourced from a local clock source, while meeting the transmit jitter requirements of 192.5.2.3, when the management parameter config is LEADER	M	Yes []
PMAT4	Loop timing	192.4.2.2	The Leader-Follower relationship include loops timing	M	Yes []
PMAT5	Clock source, Follower	192.4.2.2	The transmit symbol clock TX_TCLK is sourced from the recovered clock of 192.4.2.6, while meeting the jitter requirements of 192.5.2.3, when the management parameter config is FOLLOWER	M	Yes []
PMAT6	Transmit fault function mapping	192.4.2.2	Mapped to the transmit fault bit, as specified in 45.2.1.7.4, if the MDIO interface is implemented	M	Yes []
PMAT7	Launch power disable	192.3.2.2.1	The average launch power of the transmitter is as specified in 192.5.2.4 when the PMA_transmit_disable variable is set to TRUE and the value of tx_symb is Z	M	Yes []

192.13.4.5.2

192.13.4.5.3 PMA Receive

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	PMA Receive	192.4.2.3	See 192.4.2.3	M	Yes []
PMAR2	Status constraint	192.4.2.3	The reception of Z symbols during the TDD QUIET period alone does not trigger setting loc_rcvr_status to NOT_OK	M	Yes []
PMAR3	Receive fault function mapping	192.4.2.3	Contributed to the receive fault bit specified in 45.2.1.7.5, if the MDIO interface is implemented	M	Yes []

192.13.4.5.3

192.13.4.5.4 PHY Control

Item	Feature	Subclause	Value/Comment	Status	Support
CNTRL	PHY control compliance	192.4.2.4	Complies with the state diagram in Figure 192–31	M	Yes []

192.13.4.5.4

192.13.4.5.5 Infield

Item	Feature	Subclause	Value/Comment	Status	Support
IF1	12-octet Infield fields	192.4.2.4	Include the fields in 192.4.2.4.2 through 192.4.2.4.8 as shown in Figure 192–28 and Figure 192–29	M	Yes []
IF2	Infield transmission	192.4.2.4	Transmit Infield at least 16 times with each change to octets 7 to 10 when PMA_state = 00	M	Yes []
IF3	Infield reserved bits	192.4.2.4.1	Unused values are set to zero on transmit and ignored when received by the link partner	M	Yes []
IF4	Infield start of frame delimiter	192.4.2.4.2	Uses the hexadecimal value 0xBBA700	M	Yes []

192.13.4.5.5

192.13.4.5.6 Message Field

Item	Feature	Subclause	Value/Comment	Status	Support
MF1	PMA state communication	192.4.2.4.4	Bits PMA_state<7:6> communicate the state of the transmitting transceiver to the link partner	M	Yes []

MF2	Training phase signal	192.4.2.4.4	Bits training_phase<4:3> communicate the training phase of the transmitting transceiver to the link partner	M	Yes []
MF3	Invalid value transmission	192.4.2.4.4	Values not listed in Table 192–13 for the Leader or Follower are not transmitted and ignored at the receiver	M	Yes []
MF4	Initial Message Field setting	192.4.2.4.4	The Message Field setting for the first transmitted PMA burst is the first row of Table 192–13 for the Leader, and the first or second row of Table 192–10 for the Follower	M	Yes []
MF5	Next Message Field	192.4.2.4.4	Is the same Message Field setting or the Message Field setting corresponding to a row below the current setting in Table 192–13	M	Yes []

192.13.4.5.6

192.13.4.5.7 PHY capability

Item	Feature	Subclause	Value/Comment	Status	Support
CAP1	OAM capability	192.4.2.4.5	Enabled only if both PHYs set the capability bit OAMen=1	O	Yes []
CAP2	OAM capability validity	192.4.2.4.5	Valid only when loc_rcvr_status<5> bit is one	O	Yes []

192.13.4.5.7

192.13.4.5.8 TDD delay counter

Item	Feature	Subclause	Value/Comment	Status	Support
DLY1	Delay counter rule	192.4.2.4.6	delay_count set to a value between 0 to 63 and the delay_count_valid bit set to one after the Leader detects the Follower TDD burst position and estimates the link segment delay	M	Yes []

DLY2	Delay count acceptance	192.4.2.4.6	The Follower accepts the received remote delay_count only when received remote delay_count_valid bit is set to one	M	Yes []
DLY3	Delay count storage	192.4.2.4.6	The Follower stores delay_count number	M	Yes []
DLY4	Delay acknowledgment	192.4.2.4.6	The Follower sends back its own delay_count field as acknowledgment of delay_count reception, and set its delay_count_valid to one	M	Yes []
DLY5	Negotiation success rule	192.4.2.4.6	The Leader or the Follower sets negotiation_done to OK when it finishes the exchange of delay count and the negotiated data rates	M	Yes []
DLY6	Follower burst adjustment	192.4.2.4.6	The Follower adjusts its transmit burst position according to the stored delay_count, starting from Asymmetric training and continuing through to the data mode	M	Yes []

192.13.4.5.8

192.13.4.5.9 Phase switch

Item	Feature	Subclause	Value/Comment	Status	Support
PS1	PhaseSwBC24 burst count	192.4.2.4.7	A minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state	M	Yes []

192.13.4.5.9

192.13.4.5.10 CRC16

Item	Feature	Subclause	Value/Comment	Status	Support
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CRC1	CRC16 Infield	192.4.2.4.9	Implements the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>	M	Yes []
CRC2	CRC16 verification	192.4.2.4.9	Produces the same result as the implementation shown in Figure 192–30	M	Yes []
CRC3	CRC16 initialization	192.4.2.4.9	The 16 delay elements in Figure 192–30 are initialized to zero	M	Yes []

192.13.4.5.10

192.13.4.5.11 Startup

Item	Feature	Subclause	Value/Comment	Status	Support
ST1	Startup sequence compliance	192.4.2.4.11	Complies with the state diagram description given in Figure 192–31	M	Yes []
ST2	TRAINING0 alignment	192.4.2.4.11	The first symbol of the Follower's transmit PMA training frame at the transmit MDI is aligned at 400 ± 1 transmit symbols after arrival of the last PMA training payload symbol from the Leader at the Follower input MDI	M	Yes []
ST3	Alignment maintenance	192.4.2.4.11	The Follower maintains alignment while in the TRAINING0 and COUNTDOWN0 (i.e., while tx_mode = SEND_TS) states	M	Yes []
ST4	TRAINING1 alignment	192.4.2.4.11	The Follower uses the Leader transmitted delay_count to align its transmit PMA training frame to be $17 \text{ ns} - \text{delay_count} \times 5.333 \text{ ns}$ ($\pm 5.333 \text{ ns}$) after the last PMA training payload symbol from the Leader appears on the Follower input MDI	M	Yes []

ST5	Alignment maintenance	192.4.2.4.11	The Follower maintains its alignment while tx_mode is SEND_TA or SEND_N	M	Yes []
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192.13.4.5.11

192.13.4.5.12 Link monitor

Item	Feature	Subclause	Value/Comment	Status	Support
LM1	Link Monitor function compliance	192.4.2.5	Complies with the state diagram of Figure 192-33	M	Yes []

192.13.4.5.12

192.13.4.5.13 Clock recovery

Item	Feature	Subclause	Value/Comment	Status	Support
CR1	Clock Recovery function	192.4.2.6	Provides a clock suitable for signal sampling so that the RFER indicated in 192.4.2.3 is achieved	M	Yes []

192.13.4.5.13

192.13.4.6 MDI signals

Item	Feature	Subclause	Value/Comment	Status	Support
MDIS1	MDI symbol response compliance	192.4.3.1	Complies with the electrical specifications given in 192.5.2	M	Yes []

192.13.4.6

192.13.4.7 Timers

Item	Feature	Subclause	Value/Comment	Status	Support
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TIM1	link_fail_timer expiration	192.4.4.2	Expires 97.5 ms $\pm$ 5 ms after being started	M	Yes []
TIM2	minwait_timer expiration	192.4.4.2	Expires 975 μ s $\pm$ 50 μ s after being started	M	Yes []
TIM3	tdd_watchdog_timer expiration	192.4.4.2	Expires 96 μ s $\pm$ 5 μ s after being started	M	Yes []

192.13.4.7

192.13.4.8 PMA electrical specifications

192.13.4.8.1 Test modes

Item	Feature	Subclause	Value/Comment	Status	Support
TM1	Test modes	192.5.1	Implemented in PHY to allow testing transmitter electrical requirements	M	Yes []
TM2	Enable test modes	192.5.1	Enable by setting control register, 1.2313.15:13 as described in 192.5.1 when MDIO implemented; enabling of test modes is provided otherwise when MDIO is not implemented	M	Yes []
TM3	Test mode operation	192.5.1	Test modes only change data symbols provided to the transmitter circuitry	M	Yes []
TM4	Test mode 1	192.5.1	When enabled, PHY provides access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5	M	Yes []
TM5	Test mode 2	192.5.1	When enabled, PHY transmits a continuous repeating pattern of $\{+1, -1\}$ symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference	M	Yes []

TM6	Test mode 4, PAM2 mode	192.5.1	When enabled, PHY transmits the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16). All PHYs support transmission of this signal at 3 GBd. PHYs that support 5 Gb/s, and 7.5 Gb/s, and 10 Gb/s transmit rates support transmission of this signal at 6 GBd.	M	Yes []
TM7	Test mode 4, PAM3 mode	192.5.1	When enabled, PHY transmits the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 7.5 Gb/s transmit rates support transmission of this signal at 6 GBd.	M	Yes []
TM8	Test mode 4, PAM4 mode	192.5.1	When enabled, PHY transmits the PCS scrambler generator polynomial per Equation (192–16). PHYs that support 10 Gb/s transmit rates support transmission of this signal at 6 GBd.	M	Yes []
TM9	Test mode 5	192.5.1	When enabled, PHY transmits continuously with no QUIET period or refresh header and with transmit signal level corresponding to the data mode of operation	M	Yes []
TM10	Test mode 6	192.5.1	When enabled, PHY transmits a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source	M	Yes []

192.13.4.8.1

192.13.4.8.2 Transmitter

Item	Feature	Subclause	Value/Comment	Status	Support
PMAT1	Coupling	192.5.2	Electrical input is ac-coupled	M	Yes []

PMAT2	Transmitter electrical specifications	192.5.2	Meets requirements of 192.5.2	M	Yes []
PMAT3	Transmitter output droop	192.5.2.1	Less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing, when measured in test mode 6 using transmitter test fixture 1 or test fixture 3	M	Yes []
PMAT4	Captured block length and sampling	192.5.2.2	At least 4000 transmitted symbols long and sampled with a minimum of 10x oversampling	M	Yes []
PMAT5	Transmitter peak distortion	192.5.2.2	Less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM4 transmitters, measured at a minimum of ten equally spaced phases of a single symbol period	M	Yes []
PMAT6	RMS jitter, Leader mode	192.5.2.3	Less than 1 ps when supporting 10 Gb/s, less than 1.5 ps when supporting 7.5 Gb/s, less than 2 ps when supporting 5 Gb/s, and less than 4 ps when supporting 2.5 Gb/s for jitter frequencies greater than 100 kHz, measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1	M	Yes []
PMAT7	Time Interval Error, Leader mode	192.5.2.3	Less than 10 ps when supporting 10 Gb/s, less than 15 ps when supporting 7.5 Gb/s, less than 20 ps when supporting 5 Gb/s, and less than 40 ps when supporting 2.5 Gb/s, measured in test mode 1 using test fixture 2 over a period of 100 ms	M	Yes []
PMAT8	RMS jitter, Follower mode	192.5.2.3	Less than 1 ps when supporting 10 Gb/s, less than 1.5 ps when supporting 7.5 Gb/s, less than 2 ps when supporting 5 Gb/s, and less than 4 ps when supporting 2.5 Gb/s for jitter frequencies greater than 1 MHz, measured in test mode 1	M	Yes []

PMAT9	Time Interval Error, Follower mode	192.5.2.3	Less than 15 ps when supporting 10 Gb/s, less than 22.5 ps when supporting 7.5 Gb/s, less than 30 ps when supporting 5 Gb/s, and less than 60 ps when supporting 2.5 Gb/s, measured in test mode 1 over 50 overlapping periods of 10 ms	M	Yes []
PMAT1	Transmitter power levels	192.5.2.4	In the range of values specified in Table 192–22 when using the PSD measurement test fixture	M	Yes []
PMAT1	MDI transmit signal	192.5.2.4	Nominally zero and less than -36 dBm for frequencies greater 10 MHz	M	Yes []
PMAT1	Transmitter power spectral density, -T1	192.5.2.4	Between the upper mask specified in Equation (192–17) and the lower mask specified in Equation (192–18), measured into a 100 Ω differential load using test fixture 1	*PHY-T1:M	Yes [] N/A []
PMAT1	Symbol transmission rate	192.5.2.6	Within the range of $6 \times S \text{ GBd} \pm 100 \text{ ppm}$ with drift less than 1 ppm/sec	M	Yes []
PMAT1	Recovered symbol rate	192.5.2.6	Within $\pm 10 \text{ ppm}$ of the recovered clock used by the Follower	M	Yes []

192.13.4.8.2

192.13.4.8.3 Receiver

Item	Feature	Subclause	Value/Comment	Status	Support
PMAR1	Bit error rate, -T1	192.5.3.1	Less than 10^{-12} after RS-FEC decoding	*PHY-T1:M	Yes [] N/A []
PMAR2	Bit error rate, -V1	192.5.3.1	Less than 10^{-12} after RS-FEC decoding	*PHY-V1:M	Yes [] N/A []

192.13.4.8.3

192.13.4.9 Link segment

192.13.4.9.1 Link segment characteristics, -T1

Item	Feature	Subclause	Value/Comment	Status	Support
LST1	Insertion loss, -T1	192.7.1.1	Meets requirements of 192.7.1.1	INS-LS, T1:M	Yes [☐ N/A [☐
LST2	Return loss, -T1	192.7.1.3	Meets requirements of 192.7.1.3	INS-LS, T1:M	Yes [☐ N/A [☐
LST3	Coupling attenuation, -T1	192.7.1.4	Meets requirements of 192.7.1.4	INS-LS, T1:M	Yes [☐ N/A [☐
LST4	Screening attenuation, -T1	192.7.1.5	Meets requirements of 192.7.1.5	INS-LS, T1:M	Yes [☐ N/A [☐
LST5	Propagation delay, -T1	192.7.1.6	Not more than 160 ns for all frequencies between 10 MHz and 5 GHz	INS-LS, T1:M	Yes [☐ N/A [☐
LST6	PSANEXT loss, -T1	192.7.2.1	Meets requirements of 192.7.2.1	INS-LS, T1:M	Yes [☐ N/A [☐
LST7	PSAACRF, -T1	192.7.2.2	Meets requirements of 192.7.2.2	INS-LS, T1:M	Yes [☐ N/A [☐

192.13.4.9.1

192.13.4.9.2 Link segment characteristics, -V1

Item	Feature	Subclause	Value/Comment	Status	Support
LSV1	Insertion loss, -V1	192.8.1.1	Meets requirements of 192.8.1.1	INS-LS, V1:M	Yes [☐ N/A [☐
LSV2	Return loss, -V1	192.8.1.3	Meets requirements of 192.8.1.3	INS-LS, V1:M	Yes [☐ N/A [☐
LST3	Screening attenuation, -V1	192.8.1.5	Measured in accordance with ISO 19642-11 and meets requirements of 192.8.1.5	INS-LS, V1:M	Yes [☐ N/A [☐

LST4	Propagation delay, -V1	192.8.1.6	Not more than 160 ns for all frequencies between 10 MHz and 5 GHz	INS-LS, V1:M	Yes [] N/A []
LST5	Coupling parameter test methodologies, -V1	192.8.2	Applied with adaptation to unbalanced coaxial cabling and using a 50 Ω termination to ground	INS-LS, V1:M	Yes [] N/A []
LST6	PSANEXT loss, -V1	192.8.2.1	Meets requirements of 192.8.2.1	INS-LS, V1:M	Yes [] N/A []
LST7	PSAACRF, -V1	192.8.2.2	Meets requirements of 192.8.2.2	INS-LS, V1:M	Yes [] N/A []

192.13.4.9.2

192.13.4.10 MDI

192.13.4.10.1 MDI specification, -T1

Item	Feature	Subclause	Value/Comment	Status	Support
MDIT1	Electrical requirements, -T1	192.9.2	Electrical requirements are for when a PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors	*PHY-T1:M	Yes [] N/A []
MDIT2	Return loss, -T1	192.9.2.1	For each transmitter/receiver, measured with a nominal impedance of 50 Ω	*PHY-T1:M	Yes [] N/A []
MDIT3	Fault tolerance, -T1	192.9.3	Meets requirements of 96.8.3	*PHY-T1:M	Yes [] N/A []

192.13.4.10.1

192.13.4.10.2 MDI specification, -V1

Item	Feature	Subclause	Value/Comment	Status	Support
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MDIV1	Electrical requirements, -V1	192.10.2	Electrical requirement are for when a PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable	*PHY-V1:M	Yes [] N/A []
MDIV2	Return loss, -V1	192.10.2.1	For each transmitter/receiver, measured with a nominal impedance of 50 Ω	*PHY-V1:M	Yes [] N/A []
MDIT3	Fault tolerance, -V1	192.10.3	MDI coaxial cable interface withstands, without damage, 50 V dc with the source current limited to 150 mA. Normal operation resumes after all short circuits are removed. Single MDI conductor withstands, without damage, high-voltage transient noises and ESD per application requirements.	*PHY-V1:M	Yes [] N/A []

192.13.4.10.2

192.13.4.11 Delay constraints

Item	Feature	Subclause	Value/Comment	Status	Support
DC1	Delay constraints	192.12	Complies with Table 192–27	M	Yes []

192.13.4.11