Timing Recovery Considerations for Differential Manchester Encoded (DME) ACT Upstream Channel

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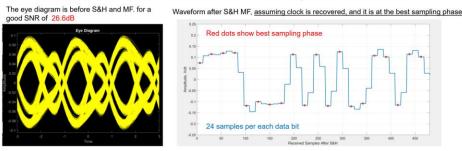
Why DME Timing Recovery Matters

- There has been some confusion on timing recovery with Differential Manchester Encoded (DME) data
- DME or Bi-Phase Encoding has been used in numerous digital communications systems including:
 - IEEE 802.3 Clause 98
 - IEEE 802.3 Clause 147
 - 802.5 (Token Ring)
 - AES3
 - SMPTE 12M (with the moniker 'Biphase Mark Code')
- This presentation will show robust low-complexity joint data reception and timing recovery for the DME upstream channel for the technology with the moniker 'ACT' is feasible without an equalizer

Background

- A. Chini and M. Tazebay's DME presentation [1] raised concerns about:
 - data dependent jitter (DJ)
 - extracting phase with the DME signal without an equalizer or preamble
 - Phase ambiguity/CDR Delay (?) "What if crystal" less [sic] camera clock shifts to the next symbol?"
- While there is DJ, it is not an issue
 - Due to the characteristics of DME an equalizer for any ACT channel for proper reception of symbols and timing recovery
- ACT-DME phase can be extracted and tracked with a comparator receiver without an equalizer or preamble

ACT-DME, Before and After S&H MF, Upstream Receiver

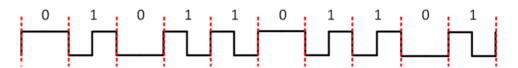


- Note the signal distortion and the data dependent jitter in the eye diagram.
- The best sampling phase shown is obtained with manual phase search. The distorted and jittery waveforms before MF mus be used to extract the sampling clock phase.
- · How well is the clock sampling phase extracted from the distorted received signal? (not a burst with a preamble)
- The Clock frequency tracking circuit, given large jitter before MF? Does it reach 1ps downstream clock accuracy?
- · What if crystal less camera clock shifts to the next symbol? (wrong Manchester phase does not happen in FDD or

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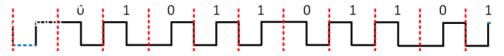
Differential Manchester Encoding (DME) Overview

- Differential Manchester Encoding (DME) has been proposed for ACT+GMSLE low speed upstream direction.
 - Robust and used for 802.3 Clause 98, Clause 146, etc.
 - Encoding rule:
 - 0: {1 1 } {-1 -1}
 - 1: {1 -1} {-1 1} (transition mid symbol)
 - Transition at symbol boundary (self-clocking)
 - Note that unlike NRZ, the maximum run length of symbols without a transition is '1' because there is always a transition at a symbol boundary



Differential Detection

 Instead of symbol-by-symbol detection, shift detection interval by ½ symbol period and differentially detect vs. previous symbol [2]



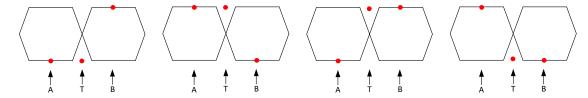
- If current symbol is in phase with previous symbol, detect '1'. If out of phase with previous symbol, detect zero.
- Phase ambiguity exists
 - Differential detection rule also works (with less signal margin) with normal offset (1/2 symbol period from differential)
- Differential detection symbol distance improves resistance to droop and resistance to noise.
 Refer to [2] & [3] for more information

Timing Recovery Methods

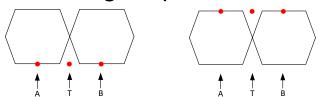
- Timing recovery methods include: [4, p.638]
 - Preamble correlation
 - Golay Sequence in Clause 98 is an example
 - Transition or Zero Crossing Methods
 - Gardner Timing Recovery
 - Quantized Zero Crossing Detection (QZCD) (so-called 'Bang Bang' Phase Detector)
 - Maximum Likelihood (ML) approximations
 - Early/Late Matched Filter correlation
 - harris Band Edge
 - Minimum variance methods
- The conceptual timing recovery shown in this presentation is one possible implementation of QZCD for DME

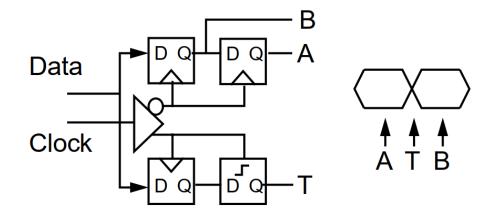
Quantized Zero Crossing (Bang Bang) with NRZ

- The Alexander [5] phase detector is shown at right from Rick Walker's presentation [6].
- The data is 2x oversampled at ½ UI intervals. If transition, depending on value of 'T' give a coarse action of 'early' or 'late' to the PI filter which controls the VCO.



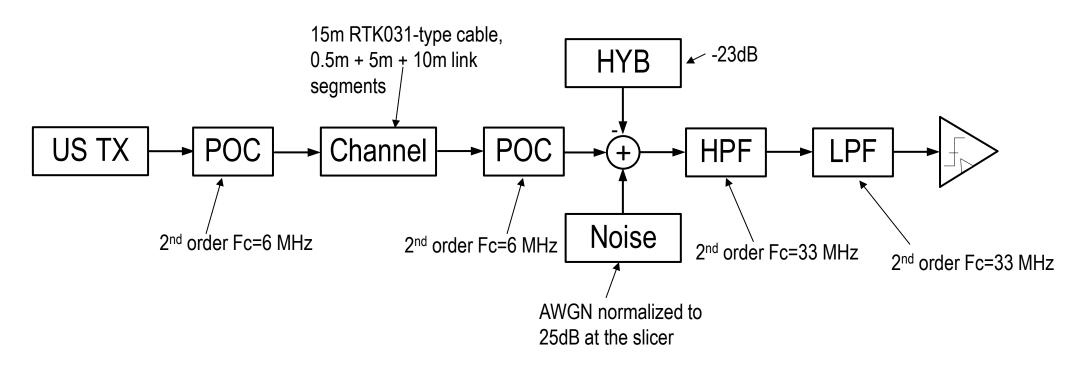
 Note that if there are long strings of ones or zeros, which will occur without a line coding with guaranteed transitions, a 'hold' signal to the VCO is required when there are long sequences of no transitions





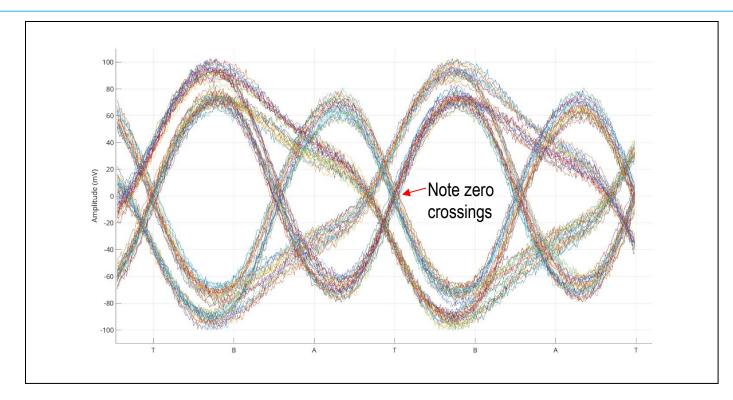
St	A	Т	В	UP	DWN	Action
0	0	0	0	0	0	Hold
1	0	0	1	0	1	Early
2	0	1	0	1	1	Hold/Err
3	0	1	1	1	0	Late
4	1	0	0	1	0	Late
5	1	0	1	1	1	Hold/Err
6	1	1	0	0	1	Early
7	1	1	1	0	0	Hold

DME System Conditions



- The system conditions are shown, above
- Represent expected values for ACT
- Exact values are not critical for the operation of the CDR

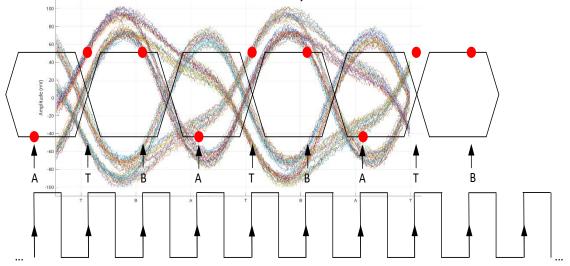
DME Received Waveform



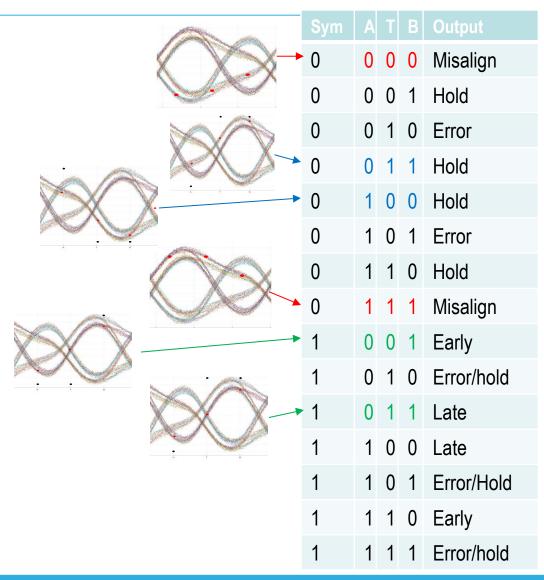
- Differentiall decoded '1' shows clean zero crossing in middle of UI
- Differentially decoded '0' shows significant zero crossing distortion (DJ)

DME Quantized Zero Crossing Detection

From the Alexander PD, a DME PD can be derived



- Sample at 1/3 UI intervals (3x OSR)
 - Timing decision and symbol detection from 3 samples
 - 1.5x OSR is also possible, but not shown
- Pattern match to filter which transitions are used to update control loop to remove DJ from timing decisions
 - Differential symbol == '1', update
 - Differential symbol == '0', hold
- Pattern match to filter the absence of transitions in a UI to detect and correct for ½ symbol period offset



Summary

- A conceptual implementation of a particular quantized zerocrossing phase detector for DME for the ACT channel was introduced
- This implementation is low complexity, requiring only 4 flip-flops and is not affected by ACT channel data dependent jitter
- The conceptual implementation extracts the phase of the received DME symbols without an equalizer or preamble
- Phase ambiguity present in decoding DME is detected and resolved
- This is only one conceptual implementation; it may be further optimized by an implementer, or a different implementation or timing recovery method may be used
- DME is a robust self-clocking modulation technique and can be used for ACT Upstream channel without an equalizer or a preamble

References

- [1] "DME Receiver Performance and EMC Comparison for ACT versus TDD" A. Chini, M. Tazebay DME Receiver Performance and EMC Comparison for ACT versus TDD
- [2] "Proposed Preamble: Synchronization and Harness Defect Detection" J. Cordaro, pp 19-21 https://www.ieee802.org/3/cg/public/adhoc/cordaro_3cg_06_0418.pdf
- [3] "IEEE 802.3da RX Model Proposal" P. Beruto https://www.ieee802.org/3/da/public/0722/beruto_3da_20220711_rx_model.pdf
- [4] B. Sklar and f. harris, "Digital Communications", 3rd ed. Upper Saddle River, NJ, USA: Pearson, p. 637, 2021.
- [5] Alexander, "Clock recovery from random binary signals," Electronics Letters, vol. 11, no. 22, pp. 541–542, October 1975
- [6] Walker, R. C.: Designing Bang-Bang PLLs for Clock and Data Recovery in Serial Data Transmission Systems, "Phase-Locking in High-Performance Systems", edited by: Razavi, B., IEEE Press, Wiley-Interscience, pp. 34–45, 2003