# IEEE P802.3dm™/D2.0

*[Markup highlight legend:*
*Green indicates changes for supporting 1 Gb/s LS in addition to those for adding a 7.5 Gb/s HS rate]*

# Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet

Prepared by the

**LAN/MAN Standards Committee**
of the
**IEEE Computer Society**

This draft is an amendment of IEEE Std 802.3-2022 as amended by IEEE Std 802.3yy-20xx. The purpose of the amendment is to add Physical Layer (PHY) specifications and management parameters for 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation in one direction and 100 Mb/s operation in the other direction on automotive cabling in an automotive environment. Draft D2.0 is prepared for initial Working Group ballot. This draft expires 6 months after the date of publication or when the next version is published, whichever comes first.

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**Abstract:** This amendment to IEEE Std 802.3-2022 adds Physical Layer (PHY) specifications and management parameters for 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation in one direction, and 100 Mb/s and 1 Gb/s operation in the other direction on automotive cabling in an automotive environment.

**Keywords:** automotive Ethernet, 100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V1, IEEE 802.3dm™

***Editor's Note (to be removed prior to publication):***

This front matter is provided for comment only. Front matter is not part of a published standard and is therefore, not part of the draft standard. You are invited to review and comment on it as it will be included in the published standard after approval.

…

# Introduction

**This introduction is not part of IEEE Std 802.3dm-20xx, IEEE Draft Standard for Ethernet. Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet.**

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. "Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications" was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The title was changed to Standard for Ethernet with the 2012 Revision.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2022 and are not maintained as separate documents.

At the date of IEEE Std 802.3dm-202x publication, IEEE Std 802.3 was composed of the following documents:

IEEE Std 802.3-2022

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber.

Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s Physical Layer specifications.

Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional Physical Layer specifications.

IEEE Std 802.3dd™-2022

Amendment 1—This amendment includes editorial and technical corrections, refinements, and clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the standard.

IEEE Std 802.3cs™-2022

Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network (ODN) through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive wavelength router that determines the channels used by the ODN. This standard specifies the Super-PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction.

IEEE Std 802.3db™-2022

Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling.

IEEE Std 802.3ck™-2022

Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and Annex 163B. This amendment includes Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling.

IEEE Std 802.3de™-2022

Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time Synchronization Service Interface (TSSI).

IEEE Std 802.3cx™-2023

Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data delay measurement point, and dynamic reporting of path data delay variation.

IEEE Std 802.3cz™-2023

Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and management parameters for optical automotive Ethernet using graded-index glass optical fiber.

IEEE Std 802.3cy™-2023

Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and Annex 165A. This amendment adds Physical Layer specifications and management parameters for operation at 25 Gb/s over a single balanced pair of conductors.

IEEE Std 802.3df™-2024

Amendment 9—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 through Clause 173, Annex 172A, and Annex 173A. This amendment includes Physical Layer specifications and management parameters for 400 Gb/s and 800 Gb/s operation.

IEEE Std 802.3-2022/Cor 1-2024

Corrigendum 1—This corrigendum includes changes to IEEE Std 802.3-2022 to correct the MDI return loss specifications in Clause 149 and Clause 165.

IEEE Std 802.3da™-2026

Amendment 10—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 188 through Clause 189. This amendment adds Physical Layer specifications and management parameters for enhancement of multidrop 10 Mb/s operation based on the 10BASE-T1S PHY specified in Clause 147 of IEEE Std 802.3-2022, and specifies optional provision of power over single balanced pair mixing segments. Additionally, this amendment includes additions and changes to Clause 148 to automatically allocate node IDs (Dynamic PLCA).

IEEE Std 802.3dk™-202x

Amendment 11—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 168. This amendment adds Physical Layer specifications and management parameters for 100 Gb/s Ethernet optical interfaces for bidirectional operation over a single strand of single-mode fiber.

IEEE Std 802.3dg™-202x

Amendment 12—This amendment to IEEE Std 802.3-2022 specifies additions and appropriate modifications to add 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation, and associated optional provision of power, over a single balanced pair of conductors.

IEEE Std 802.3dm™-20xx

This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 200. This amendment adds Physical Layer specifications and management parameters for operation at 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation in one direction and 100 Mb/s and 1 Gb/s operation in the other direction over a single balanced pair of conductors, or over a single coaxial cable. When 1 Gb/s is enabled, only 7.5 Gb/s and 5 Gb/s are supported in the opposite direction.

Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after approval of those enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

# Draft Standard for Ethernet Amendment: Physical Layer Specifications and Management Parameters for Asymmetrical Electrical Automotive Ethernet



NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

*TO BE REMOVED PRIOR TO FINAL PUBLICATION: Reviewers and the publication editor should note that editing instructions have been written to minimize the probability of changes being lost at publication from other IEEE 802.3 amendment projects running in parallel that modified the same text and tables.*

## 1. Introduction

### 1.3 Normative references

***Insert the following references in alphanumeric order:***

ISO 19642–11:2023, Road vehicles—Automotive cables—Part 11: Dimensions and requirements for coaxial RF cables with a specified analogue bandwidth up to 6 GHz (20 GHz).

## 1.4 Definitions

***Insert the following new definitions after 1.4.46 100 Gb/s Parallel Physical Interface (CPPI):***

**1.4.46a 100M+10GBASE-T1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 10 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191.)

**1.4.46b 100M+10GBASE-V1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 10 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191.)

**1.4.46c 100M+2.5GBASE-T1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 2.5 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191.)

**1.4.46d 100M+2.5GBASE-V1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 2.5 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191.)

**1.4.46e 100M+5GBASE-T1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 5 Gb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191.)

**1.4.46f 100M+5GBASE-V1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 100 Mb/s and reception at 5 Gb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191.)

**1.4.46g 100M+MultiGBASE:** PHYs that belong to the set of specific asymmetric PHYs that transmit at 100 Mb/s and receive at speeds in excess of 1000 Mb/s, with concurrent transmission in both directions, including 100M+2.5GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-T1, 100M+5GBASE-V1, 100M+10GBASE-T1, and 100M+10GBASE-V1. (See IEEE Std 802.3, Clause 191.)

**1.4.46g 1G+MultiGBASE: [Note to Editor:** Add new 1G+MultiGBASE definition that reflects the resolution to a D2.0 comment on 1.4.46g.]

***Insert the following new definitions after 1.4.62 10BROAD36:***

**1.4.62a 10G+100MBASE-T1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 10 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191.)

**1.4.62b 10G+100MBASE-V1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 10 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191.)

***Change 1.4.88 as follows:***

**1.4.88 10 Gigabit Media Independent Interface (XGMII):** The interface between the Reconciliation Sublayer (RS) and the Physical Coding Sublayer (PCS) for 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s operation (including asymmetric PHYs with 100 Mb/s in the reverse direction). (See IEEE Std 802.3, Clause 46.)

***Insert the following new definitions after 1.4.95 1G-EPON:***

**1.4.95a 2.5G+100MBASE-T1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 2.5 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191.)

**1.4.95b 2.5G+100MBASE-V1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 2.5 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191.)

***Insert the following new definitions after 1.4.178 50G-EPON:***

**1.4.178a 5G+100MBASE-T1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 5 Gb/s and reception at 100 Mb/s over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 191.)

**1.4.178b 5G+100MBASE-V1:** IEEE 802.3 Physical Layer specification for an asymmetric Ethernet full duplex point-to-point link supporting transmission at 5 Gb/s and reception at 100 Mb/s over a single unbalanced coaxial cable. (See IEEE Std 802.3, Clause 191.)

***Change 1.4.249 as follows:***

**1.4.249 coaxial cable interface:** The electrical and mechanical interface to the ~~shared~~ coaxial cable medium either contained within or connected to the Medium Attachment Unit (MAU). Also known as the Medium Dependent Interface (MDI).

***Insert the following new definitions after 1.4.405c* Multidrop Power Sourcing Equipment (MPSE*) (as modified by IEEE Std 802.3da-2026):***

**1.4.249a MultiG+100MBASE:** PHYs that belong to the set of specific asymmetric PHYs that transmit at speeds in excess of 1000 Mb/s and receive at 100 Mb/s, with concurrent transmission in both directions, including 2.5G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-T1, 5G+100MBASE-V1, 10G+100MBASE-T1, and 10G+100MBASE-V1. (See IEEE Std 802.3, Clause 191.)

**1.4.249a MultiG+1GBASE [Note to Editor:** Add new MultiG+1GBASE definition that reflects the resolution to a D2.0 comment on 1.4.249a.]

**1.4.405b MultiGBASE-A**: PHYs that belong to the set of specific asymmetric PHYs at speeds in excess of 1000 Mb/s in one direction and less than or equal to 1000 Mb/s in the other direction, including MultiGBASE-AT1 and MultiGBASE-AV1. (See IEEE Std 802.3, Clause 191.)

**1.4.405c MultiGBASE-AT1**: IEEE 802.3 Physical Layer specification for an asymmetric rate Ethernet full duplex point-to-point link operating at 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s or 1 Gb/s in the other direction over a single shielded balanced pair of conductors. (See IEEE Std 802.3, Clause 192.)

**1.4.405d MultiGBASE-AV1**: IEEE 802.3 Physical Layer specification for an asymmetric rate Ethernet full duplex point-to-point link operating at 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s in one direction and 100 Mb/s or 1 Gb/s in the other direction over a single coaxial conductor. (See IEEE Std 802.3, Clause 192.)

## 1.5 Abbreviations

***Insert the following new abbreviations into the list, in alphanumeric order:***

| | |
|---|---|
| ACT | Asymmetric Concurrent Transmission |
| TDD | Time Division Duplex |

# 30. Management

## 30.3 Layer management for DTEs

### 30.3.2 PHY device managed object class

#### 30.3.2.1 PHY device attributes

#### 30.3.2.1.2 aPhyType

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "2.5GBASE-T1" as follows:***

| | |
|---|---|
| 2.5G+100MBASE-T1/V1 | Clause 191 2.5 Gb/s PAM2 transmit, 100 Mb/s DME receive |
| 100M+2.5GBASE-T1/V1 | Clause 191 100 Mb/s DME transmit, 2.5 Gb/s PAM2 receive |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "5GBASE-T1" as follows:***

| | |
|---|---|
| 5G+100MBASE-T1/V1 | Clause 191 5 Gb/s PAM2, 100 Mb/s DME receive |
| 100M+5GBASE-T1/V1 | Clause 191 100 Mb/s DME transmit, 5 Gb/s PAM2 receive |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "10GBASE-T1" as follows:***

| | |
|---|---|
| 10G+100MBASE-T1/V1 | Clause 191 10 Gb/s PAM4, 100 Mb/s DME receive |
| 100M+10GBASE-T1/V1 | Clause 191 100 Mb/s DME transmit, 10 Gb/s PAM4 receive |

***Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for "400GBASE-R" as follows:***

| | |
|---|---|
| MultiGBASE-A | Clause 192 MultiG PAM2, PAM3, or PAM4 HS_PATH, 100 Mb/s or 1 Gb/s PAM2 LS_PATH |

#### 30.3.2.1.3 aPhyTypeList

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "2.5GBASE-T1" as follows:***

| | |
|---|---|
| 2.5G+100MBASE-T1/V1 | Clause 191 2.5 Gb/s PAM2 transmit, 100 Mb/s DME receive |
| 100M+2.5GBASE-T1/V1 | Clause 191 100 Mb/s DME transmit, 2.5 Gb/s PAM2 receive |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "5GBASE-T1" as follows:***

| | |
|---|---|
| 5G+100MBASE-T1/V1 | Clause 191 5 Gb/s PAM2, 100 Mb/s DME receive |
| 100M+5GBASE-T1/V1 | Clause 191 100 Mb/s DME transmit, 5 Gb/s PAM2 receive |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "10GBASE-T1" as follows:***

| | |
|---|---|
| 10G+100MBASE-T1/V1 | Clause 191 10 Gb/s PAM4, 100 Mb/s DME receive |
| 100M+10GBASE-T1/V1 | Clause 191 100 Mb/s DME transmit, 10 Gb/s PAM4 receive |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for "400GBASE-R" as follows:***

| | |
|---|---|
| MultiGBASE-A PAM2 LS_PATH | Clause 192 MultiG PAM2, PAM3, or PAM4 HS_PATH, 100 Mb/s or 1 Gb/s |

## 30.5 Layer management for medium attachment units (MAUs)

### 30.5.1 MAU managed object class

#### 30.5.1.1 MAU attributes

#### 30.5.1.1.2 aMAUType

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "2.5GBASE-T1" as follows:***

| | |
|---|---|
| 2.5G+100MBASE-T1 | Single balanced pair of conductors PHY as specified in Clause 191 |
| 100M+2.5GBASE-T1 | Single balanced pair of conductors PHY as specified in Clause 191 |
| 2.5G+100MBASE-V1 | Coaxial Cable PHY as specified in Clause 191 |
| 100M+2.5GBASE-V1 | Coaxial Cable PHY as specified in Clause 191 |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "5GBASE-T1" as follows:***

| | |
|---|---|
| 5G+100MBASE-T1 | Single balanced pair of conductors PHY as specified in Clause 191 |
| 100M+5GBASE-T1 | Single balanced pair of conductors PHY as specified in Clause 191 |
| 5G+100MBASE-V1 | Coaxial Cable PHY as specified in Clause 191 |
| 100M+5GBASE-V1 | Coaxial Cable PHY as specified in Clause 191 |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "10GBASE-T1" as follows:***

| | |
|---|---|
| 10G+100MBASE-T1 | Single balanced pair of conductors PHY as specified in Clause 191 |
| 100M+10GBASE-T1 | Single balanced pair of conductors PHY as specified in Clause 191 |

| | |
|---|---|
| 10G+100MBASE-V1 | Coaxial Cable PHY as specified in Clause 191 |
| 100M+10GBASE-V1 | Coaxial Cable PHY as specified in Clause 191 |

***Insert the following new entries in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for "802.9a" as follows:***

| | |
|---|---|
| MultiGBASE-AT1 | Single balanced pair of conductors PHY as specified in Clause 192 |
| MultiGBASE-AV1 | Coaxial Cable PHY as specified in Clause 192 |

## 30.6 Management for link Auto-Negotiation

### 30.6.1 Auto-Negotiation managed object class

### 30.6.1.1 Auto-Negotiation attributes

#### 30.6.1.1.5 aAutoNegLocalTechnologyAbility

***Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "2.5GBASE-T1" as follows:***

| | |
|---|---|
| 2.5G+100MBASE-T1 | 2.5G+100MBASE-T1 as specified in Clause 191 |
| 100M+2.5GBASE-T1 | 100M+2.5GBASE-T1 as specified in Clause 191 |
| 2.5G+100MBASE-V1 | 2.5G+100MBASE-V1 as specified in Clause 191 |
| 100M+2.5GBASE-V1 | 100M+2.5GBASE-V1 as specified in Clause 191 |

***Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "5GBASE-T1" as follows:***

| | |
|---|---|
| 5G+100MBASE-T1 | 5G+100MBASE-T1 as specified in Clause 191 |
| 100M+5GBASE-T1 | 100M+5GBASE-T1 as specified in Clause 191 |
| 5G+100MBASE-V1 | 5G+100MBASE-V1 as specified in Clause 191 |
| 100M+5GBASE-V1 | 100M+5GBASE-V1 as specified in Clause 191 |

***Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for "10GBASE-T1" as follows:***

| | |
|---|---|
| 10G+100MBASE-T1 | 10G+100MBASE-T1 as specified in Clause 191 |
| 100M+10GBASE-T1 | 100M+10GBASE-T1 as specified in Clause 191 |
| 10G+100MBASE-V1 | 10G+100MBASE-V1 as specified in Clause 191 |
| 100M+10GBASE-V1 | 100M+10GBASE-V1 as specified in Clause 191 |

# 45. Management Data Input/Output (MDIO) Interface

## 45.2 MDIO Interface Registers

### 45.2.1 PMA/PMD registers

***Change the reserved row for 1.77 through 1.79 in Table 45-3 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, and IEEE Std 802.3dj-20xx) and change the reserved row for 1.2318 through 1.2400 (as modified by IEEE Std 802.3dj-20xx) as follows (unchanged rows not shown):***

**Table 45–3—PMA/PMD registers**

| Register address | Register name | Subclause |
|---|---|---|
| … | | |
| 1.77 | Asymmetrical BASE-T1/V1 PMA/PMD extended ability | 45.2.1.60f |
| 1.~~77~~78 through 1.79 | Reserved | |
| … | | |
| 1.2318 | MultiGBASE-A PMA rate ability | 45.2.1.250a |
| 1.2319 | MultiGBASE-A PMA rate negotiation | 45.2.1.250b |
| 1.2320 | MultiGBASE-A PMA link partner rate negotiation | 45.2.1.250c |
| 1.2321 through 1.2400<br>~~1.2318 through 1.2400~~ | | |

…

### 45.2.1.6 PMA/PMD control 2 register (Register 1.7)

***Change Table 45-7 (as modified by IEEE Std 802.3cz-2023, IEEE Std 802.3df-2024, IEEE Std 802.3dk-2026, and IEEE Std 802.3dj-20xx) as follows (unchanged table rows and most unchanged bit description lines not shown):***

**Table 45–7—PMA/PMD control 2 register bit definitions**

| Bit(s) | Name | Description | R/W[1] |
|---|---|---|---|
| … | | | |
| 1.7.7:0 | PMA/PMD type selection | 7 6 5 4 3 2 1 0<br>…<br>0 0 1 1 1 1 0 1 = BASE-T1/V1 PMA/PMD[2]<br>… | R/W |
| … | | | |

### 45.2.1.7 PMA/PMD status 2 register (Register 1.8)

#### 45.2.1.7.4 Transmit fault (1.8.11)

***Insert new rows in Table 45-9 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows (unchanged rows not shown):***

**Table 45–9—Transmit fault description location**

| PMA/PMD | Description location |
|---|---|
| … | |

[1]R/W = Read/Write, RO = Read only.
[2]If BASE-T1/V1 is selected, bits 1.2100.~~3~~4:0 are used to differentiate which BASE-T1/V1 PMA/PMD is selected.

| | |
|---|---|
| 2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1 | 191.5.2.2 |
| 100M+2.5GBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-V1, 100M+10GBASE-V1 | 191.5.2.2 |
| … | |

### 45.2.1.7.5 Receive fault (1.8.10)

***Insert new rows in Table 45-10 immediately after row for 2.5GBASE-T1, 5GBASE-T1, 10GBASE-T1 as follows and insert a new row at the end of the table(unchanged rows not shown):***

**Table 45–10—Receive fault description location**

| PMA/PMD | Description location |
|---|---|
| … | |
| 2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1 | 191.5.2.3 |
| 100M+2.5GBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-V1, 100M+10GBASE-V1 | 191.5.2.3 |
| … | |
| MultiGBASE-AT1, MultiGBASE-AV1 | 192.4.2.3 |

### 45.2.1.10 PMA/PMD extended ability register (Register 1.11)

***Change the row for 1.11.11 in Table 45-19 as follows (unchanged rows not shown.):***

**Table 45–14—PMA/PMD Extended Ability register bit definitions**

| Bit(s) | Name | Description | R/W[3] |
|---|---|---|---|
| | | | |
| 1.11.11 | BASE-T1/V1 extended abilities | 1 = PMA/PMD has BASE-T1/V1 extended abilities listed in register 1.18<br>0 = PMA/PMD does not have BASE-T1/V1 extended ab-ilities | RO |
| … | | | |

***Change the title of 45.2.10.5 and the text as follows:***

### 45.2.1.10.5 BASE-T1/V1 extended abilities (1.11.11)

When read as a one, bit 1.11.11 indicates that the PMA/PMD has BASE-T1/V1 extended abilities listed in register 1.18. When read as a zero, bit 1.11.11 indicates that the PMA/PMD does not have BASE-T1/V1 extended abilities.

***Change the title of the following subsection as shown:***

### 45.2.1.16 BASE-T1/V1 PMA/PMD extended ability register (1.18)

***Change the title of the Table 45-19 and change row 2 and insert new row 3 (as modified by IEEE Std 802.3cy-2023, IEEE Std 802.3da-2026, and IEEE Std 802.3dg-202x) as follows (unchanged rows not shown)***

**Table 45–19—BASE-T1/V1 PMA/PMD extended ability register bit definitions**

| Bit(s) | Name | Description | R/W[4] |
|---|---|---|---|
| 1.18.15:12 ~~7~~ | Reserved | Value always 0 | RO |
| 1.18.11 | MultiGBASE-AT1/AV1 ability | 1 = PMA/PMD is able to perform MultiGBASE-AT1/AV1<br>0 = PMA/PMD is not able to perform MultiGBASE- | RO |

[3]RO = Read only.
[4]RO = Read only.

| | | | |
|---|---|---|---|
| | | AT1/AV1 | |
| 1.18.10 | MultiG+100M/ 100M+MultiGBASE-T1/V1 ability | 1 = PMA/PMD is able to perform MultiG+100M/100M+MultiGBASE-V1 ability<br>0 = PMA/PMD is able to perform MultiG+100M/100M+MultiGBASE-T1 | RO |
| 1.18.xx | MultiG+1G/ 1G+MultiGBASE-T1/V1 ability | 1 = PMA/PMD is able to perform MultiG+1G/ 1G +MultiGBASE-V1 ability<br>0 = PMA/PMD is able to perform MultiG+1G/ 1G +MultiGBASE-T1 | RO |
| … | | | |

***Insert 45.2.1.16.aaaa before 45.2.1.16.aaa (as inserted by IEEE Std 802.3dg-202x) as follows:***

### 45.2.1.16.aaaa MultiGBASE-AT1/AV1 ability (1.18.11)

When read as a one, bit 1.18.11 indicates that the PMA/PMD is able to operate as a MultiGBASE-AT1/AV1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.11 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AT1/AV1 PMA/PMD type as indicated in register 1.77.

### 45.2.1.16.aaab MultiG+100M/100M+MultiGBASE-T1/V1 ability (1.18.10)

When read as a one, bit 1.18.10 indicates that the PMA/PMD is able to operate as a MultiG+100M/100M+MultiGBASE-V1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.10 indicates that the PMA/PMD is able to operate as a MultiG+100M/100M+MultiGBASE-T1 PMA/PMD type as indicated in register 1.77.

### 45.2.1.16.aaab MultiG+1G/1G+MultiGBASE-T1/V1 ability (1.18.xx)

When read as a one, bit 1.18.xx indicates that the PMA/PMD is able to operate as a MultiG+1G/1G+MultiGBASE-V1 PMA/PMD type as indicated in register 1.77. When read as a zero, bit 1.18.xx indicates that the PMA/PMD is able to operate as a MultiG+1G/1G+MultiGBASE-T1 PMA/PMD type as indicated in register 1.77.

***Insert 45.2.1.60f after 45.2.1.60e (as inserted by IEEE Std 802.3df-202x) as follows:***

### 45.2.1.60f Asymmetric PMA/PMD extended ability register (Register 1.77)

The assignment of bits in the Asymmetric PMA/PMD extended ability register is shown in Table 45–58f.

**Table 45–58f—Asymmetric PMA/PMD extended ability register bit definitions**

| Bit(s) | Name | Description | R/W[5] |
|---|---|---|---|

[5]R/W = Read/Write, RO = Read only

| | | | |
|---|---|---|---|
| 1.77.15:14 | Reserved | Value always 0 | RO |
| 1.77.13 | MultiGBASE-AV1 ability | 1 = PMA/PMD is able to perform MultiGBASE-AV1<br>0 = PMA/PMD is not able to perform MultiGBASE-AV1 | RO |
| 1.77.13 | MultiGBASE-AT1 ability | 1 = PMA/PMD is able to perform MultiGBASE-AT1<br>0 = PMA/PMD is not able to perform MultiGBASE-AT1 | RO |
| 1.77.11 | 10G+100MBASE-V1 ability | 1 = PMA/PMD is able to perform 10G+100MBASE-V1<br>0 = PMA/PMD is not able to perform 10G+100MBASE-V1 | RO |
| 1.77.10 | 100M+10GBASE-V1 ability | 1 = PMA/PMD is able to perform 100M+10GBASE-V1<br>0 = PMA/PMD is not able to perform 100M+10GBASE-V1 | RO |
| 1.77.9 | 10G+100MBASE-T1 ability | 1 = PMA/PMD is able to perform 10G+100MBASE-T1<br>0 = PMA/PMD is not able to perform 10G+100MBASE-T1 | RO |
| 1.77.8 | 100M+10GBASE-T1 ability | 1 = PMA/PMD is able to perform 100M+10GBASE-T1<br>0 = PMA/PMD is not able to perform 100M+10GBASE-T1 | RO |
| 1.77.7 | 5G+100MBASE-V1 ability | 1 = PMA/PMD is able to perform 5G+100MBASE-V1<br>0 = PMA/PMD is not able to perform 5G+100MBASE-V1 | RO |
| 1.77.6 | 100M+5GBASE-V1 ability | 1 = PMA/PMD is able to perform 100M+5GBASE-V1<br>0 = PMA/PMD is not able to perform 100M+5GBASE-V1 | RO |
| 1.77.5 | 5G+100MBASE-T1 ability | 1 = PMA/PMD is able to perform 5G+100MBASE-T1<br>0 = PMA/PMD is not able to perform 5G+100MBASE-T1 | RO |
| 1.77.4 | 100M+5GBASE-T1 ability | 1 = PMA/PMD is able to perform 100M+5GBASE-T1<br>0 = PMA/PMD is not able to perform 100M+5GBASE-T1 | RO |
| 1.77.3 | 2.5G+100MBASE-V1 ability | 1 = PMA/PMD is able to perform 2.5G+100MBASE-V1<br>0 = PMA/PMD is not able to perform 2.5G+100MBASE-V1 | RO |
| 1.77.2 | 100M+2.5GBASE-V1 ability | 1 = PMA/PMD is able to perform 100M+2.5GBASE-V1<br>0 = PMA/PMD is not able to perform 100M+2.5GBASE-V1 | RO |

| | | | |
|---|---|---|---|
| 1.77.1 | 2.5G+100MBASE-T1 ability | 1 = PMA/PMD is able to perform 2.5G+100MBASE-T1<br>0 = PMA/PMD is not able to perform 2.5G+100MBASE-T1 | RO |
| 1.77.0 | 100M+2.5GBASE-T1 ability | 1 = PMA/PMD is able to perform 100M+2.5GBASE-T1<br>0 = PMA/PMD is not able to perform 100M+2.5GBASE-T1 | RO |

#### 45.2.1.60f.1 MultiGBASE-AV1 (1.77.13)

When read as a one, bit 1.77.13 indicates that the PMA/PMD is able to operate as a MultiGBASE-AV1 PMA/PMD type.

When read as a zero, bit 1.77.13 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AV1 PMA/PMD type.

#### 45.2.1.60f.2 MultiGBASE-AT1 (1.77.12)

When read as a one, bit 1.77.12 indicates that the PMA/PMD is able to operate as a MultiGBASE-AT1 PMA/PMD type.

When read as a zero, bit 1.77.12 indicates that the PMA/PMD is not able to operate as a MultiGBASE-AT1 PMA/PMD type.

#### 45.2.1.60f.3 10G+100MBASE-V1 (1.77.11)

When read as a one, bit 1.77.11 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.11 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-V1 PMA/PMD type.

#### 45.2.1.60f.4 100M+10GBASE-V1 (1.77.10)

When read as a one, bit 1.77.10 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.10 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-V1 PMA/PMD type.

#### 45.2.1.60f.5 10G+100MBASE-T1 (1.77.9)

When read as a one, bit 1.77.9 indicates that the PMA/PMD is able to operate as a 10G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.9 indicates that the PMA/PMD is not able to operate as a 10G+100MBASE-T1 PMA/PMD type.

#### 45.2.1.60f.6 100M+10GBASE-T1 (1.77.8)

When read as a one, bit 1.77.8 indicates that the PMA/PMD is able to operate as a 100M+10GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.8 indicates that the PMA/PMD is not able to operate as a 100M+10GBASE-T1 PMA/PMD type.

#### 45.2.1.60f.7 5G+100MBASE-V1 (1.77.7)

When read as a one, bit 1.77.7 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.7 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-V1 PMA/PMD type.

#### 45.2.1.60f.8 100M+5GBASE-V1 (1.77.6)

When read as a one, bit 1.77.6 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.6 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-V1 PMA/PMD type.

#### 45.2.1.60f.9 5G+100MBASE-T1 (1.77.5)

When read as a one, bit 1.77.5 indicates that the PMA/PMD is able to operate as a 5G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.5 indicates that the PMA/PMD is not able to operate as a 5G+100MBASE-T1 PMA/PMD type.

#### 45.2.1.60f.10 100M+5GBASE-T1 (1.77.4)

When read as a one, bit 1.77.4 indicates that the PMA/PMD is able to operate as a 100M+5GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.4 indicates that the PMA/PMD is not able to operate as a 100M+5GBASE-T1 PMA/PMD type.

#### 45.2.1.60f.11 2.5G+100MBASE-V1 (1.77.3)

When read as a one, bit 1.77.3 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.3 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-V1 PMA/PMD type.

#### 45.2.1.60f.12 100M+2.5GBASE-V1 (1.77.2)

When read as a one, bit 1.77.2 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-V1 PMA/PMD type.

When read as a zero, bit 1.77.2 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-V1 PMA/PMD type.

#### 45.2.1.60f.13 2.5G+100MBASE-T1 (1.77.1)

When read as a one, bit 1.77.1 indicates that the PMA/PMD is able to operate as a 2.5G+100MBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.1 indicates that the PMA/PMD is not able to operate as a 2.5G+100MBASE-T1 PMA/PMD type.

#### 45.2.1.60f.14 100M+2.5GBASE-T1 (1.77.0)

When read as a one, bit 1.77.0 indicates that the PMA/PMD is able to operate as a 100M+2.5GBASE-T1 PMA/PMD type.

When read as a zero, bit 1.77.0 indicates that the PMA/PMD is not able to operate as a 100M+2.5GBASE-T1 PMA/PMD type.

***Change the title of the following subsection as shown:***

#### 45.2.1.214 BASE-T1/V1 PMA/PMD control register (Register 1.2100)

***Change the title of the following table as shown. Replace the rows for bits 1.2100.13:4 and 1.2100.3:0 in Table 45–178 (as modified by IEEE Std 802.3cy-2023 and IEEE Std 802.3da-2026) as follows (unchanged rows not shown):***

**Table 45–178—BASE-T1/V1 PMA/PMD control register bit definitions**

| Bit(s) | Name | Description | R/W[6] |
|---|---|---|---|
| … | | | |
| 1.2100.13:5 | Reserved | Value always 0 | RO |

[6]R/W = Read/Write, RO = Read only

| | | | |
|---|---|---|---|
| 1.2100.4:0 | Type Selection | 4 3 2 1 0<br>1 1 1 1 1 = MultiGBASE-AV1<br>1 1 1 1 0 = MultiGBASE-AT1<br>1 1 1 0 x = Reserved<br>1 1 0 1 1 = 10G+100MBASE-V1<br>1 1 0 1 0 = 100M+10GBASE-V1<br>1 1 0 0 1 = 10G+100MBASE-T1<br>1 1 0 0 0 = 100M+10GBASE-T1<br>1 0 1 1 1 = 5G+100MBASE-V1<br>1 0 1 1 0 = 100M+5GBASE-V1<br>1 0 1 0 1 = 5G+100MBASE-T1<br>1 0 1 0 0 = 100M+5GBASE-T1<br>1 0 0 1 1 = 2.5G+100MBASE-V1<br>1 0 0 1 0 = 100M+2.5GBASE-V1<br>1 0 0 0 1 = 2.5G+100MBASE-T1<br>1 0 0 0 0 = 100M+2.5GBASE-T1<br>0 1 1 x x = Reserved<br>0 1 0 1 x = Reserved<br>0 1 0 0 1 = Reserved<br>0 1 0 0 0 = 10BASE-T1M<br>0 0 1 1 1 = 25GBASE-T1<br>0 0 1 1 0 = 10GBASE-T1<br>0 0 1 0 1 = 5GBASE-T1<br>0 0 1 0 0 = 2.5GBASE-T1<br>0 0 0 1 1 = 10BASE-T1S<br>0 0 0 1 0 = 10BASE-T1L<br>0 0 0 0 1 = 1000BASE-T1<br>0 0 0 0 0 = 100BASE-T1 | R/W |

***Change the subclause title and first sentence of 45.2.1.214.2 (as modified by IEEE Std 802.3da-2026) as follows:***

### 45.2.1.214.2 Type selection (1.2100.4:0) ~~(1.2100.3:0)~~

Bits 1.2100.4:0 ~~1.2100.3:0~~ are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to zero, or if Auto-Negotiation is not implemented.

***Insert the following new subclauses and tables after 45.2.1.250 and before 45.2.1.251 (as inserted by IEEE Std 802.3dj-202x) as follows:***

### 45.2.1.250a MultiGBASE-A PMA rate ability (Register 1.2318)

The assignment of bits in the MultiGBASE-A PMA rate ability register is shown in Table 45–212a.

**Table 45–212a—MultiGBASE-A PMA rate ability register bit definitions**

| Bit(s) | Name | Description | R/W[7] |
|---|---|---|---|

[7]RO = Read only.

| | | | |
|---|---|---|---|
| 1.2318.15 | MultiGBASE-A PHY_D 10 Gb/s RX ability | 1 = PHY has MultiGBASE-A PHY_D 10 Gb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_D 10 Gb/s RX ability | RO |
| 1.2318.14 | MultiGBASE-A PHY_D 7.5 Gb/s RX ability | 1 = PHY has MultiGBASE-A PHY_D 7.5 Gb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_D 7.5 Gb/s RX ability | RO |
| 1.2318.13 | MultiGBASE-A PHY_D 5 Gb/s RX ability | 1 = PHY has MultiGBASE-A PHY_D 5 Gb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_D 5 Gb/s RX ability | RO |
| 1.2318.12 | MultiGBASE-A PHY_D 2.5 Gb/s RX ability | 1 = PHY has MultiGBASE-A PHY_D 2.5 Gb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_D 2.5 Gb/s RX ability | RO |
| 1.2318.11 | MultiGBASE-A PHY_D 1 Gb/s TX ability | 1 = PHY has MultiGBASE-A PHY_D 1 Gb/s TX ability<br>0 = PHY does not have MultiGBASE-A PHY_D 1 Gb/s TX ability | RO |
| 1.2318.10:9 | Reserved | Value always 0 | RO |
| 1.2318.8 | MultiGBASE-A PHY_D 100 Mb/s TX ability | 1 = PHY has MultiGBASE-A PHY_D 100 Mb/s TX ability<br>0 = PHY does not have MultiGBASE-A PHY_D 100 Mb/s TX ability | RO |
| 1.2318.7 | MultiGBASE-A PHY_S 10 Gb/s TX ability | 1 = PHY has MultiGBASE-A PHY_S 10 Gb/s TX ability<br>0 = PHY does not have MultiGBASE-A PHY_S 10 Gb/s TX ability | RO |
| 1.2318.6 | MultiGBASE-A PHY_S 7.5 Gb/s TX ability | 1 = PHY has MultiGBASE-A PHY_S 7.5 Gb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_S 7.5 Gb/s RX ability | RO |
| 1.2318.5 | MultiGBASE-A PHY_S 5 Gb/s TX ability | 1 = PHY has MultiGBASE-A PHY_S 5Gb/s TX ability<br>0 = PHY does not have MultiGBASE-A PHY_S 5Gb/s TX ability | RO |
| 1.2318.4 | MultiGBASE-A PHY_S 2.5 Gb/s TX ability | 1 = PHY has MultiGBASE-A PHY_S 2.5Gb/s TX ability<br>0 = PHY does not have MultiGBASE-A PHY_S 2.5Gb/s TX ability | RO |
| 1.2318.3:2 | Reserved | Value always 0 | RO |
| 1.2318.3:1 | MultiGBASE-A PHY_S 1 Gb/s RX ability | 1 = PHY has MultiGBASE-A PHY_S 1 Gb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_S 1 Gb/s RX ability | RO |
| 1.2318.0 | MultiGBASE-A PHY_S 100 Mb/s RX ability | 1 = PHY has MultiGBASE-A PHY_S 100 Mb/s RX ability<br>0 = PHY does not have MultiGBASE-A PHY_S 100 Mb/s RX ability | RO |

#### 45.2.1.250a.1 MultiGBASE-A PHY_D 10 Gb/s RX ability (1.2318.15)

When read as a one, bit 1.2318.15 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 10 Gb/s. When read as a zero, bit 1.2318.15 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 10 Gb/s.

#### 45.2.1.250a.3 MultiGBASE-A PHY_D 7.5 Gb/s RX ability (1.2318.14)

When read as a one, bit 1.2318.14 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 7.5 Gb/s. When read as a zero, bit 1.2318.14 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 7.5 Gb/s.

*[Note to Editor: Renumber the 45.2.1.250a subclauses appropriately]*

#### 45.2.1.250a.2 MultiGBASE-A PHY_D 5 Gb/s RX ability (1.2318.13)

When read as a one, bit 1.2318.13 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 5 Gb/s. When read as a zero, bit 1.2318.13 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 5 Gb/s.

#### 45.2.1.250a.3 MultiGBASE-A PHY_D 2.5 Gb/s RX ability (1.2318.12)

When read as a one, bit 1.2318.12 indicates that the PHY supports operating in PHY_D mode at a receive data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.12 indicates that the PHY does not support operating in PHY_D mode at a receive data rate of 2.5 Gb/s.

#### 45.2.1.250a.4 MultiGBASE-A PHY_D 1 Gb/s TX ability (1.2318.11)

When read as a one, bit 1.2318.11 indicates that the PHY supports operating in PHY_D mode at a transmit data rate of 1 Gb/s. When read as a zero, bit 1.2318.11 indicates that the PHY does not support operating in PHY_D mode at a transmit data rate of 1 Gb/s.

#### 45.2.1.250a.4 MultiGBASE-A PHY_D 100 Mb/s TX ability (1.2318.8)

When read as a one, bit 1.2318.8 indicates that the PHY supports operating in PHY_D mode at a transmit data rate of 100 Mb/s. When read as a zero, bit 1.2318.8 indicates that the PHY does not support operating in PHY_D mode at a transmit data rate of 100 Mb/s.

#### 45.2.1.250a.5 MultiGBASE-A PHY_S 10 Gb/s TX ability (1.2318.7)

When read as a one, bit 1.2318.7 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 10 Gb/s. When read as a zero, bit 1.2318.7 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 10 Gb/s.

#### 45.2.1.250a.5 MultiGBASE-A PHY_S 7.5 Gb/s TX ability (1.2318.6)

#### 45.2.1.250a.6 When read as a one, bit 1.2318.6 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 7.5 Gb/s. When read as a zero, bit 1.2318.6 indicates that the PHY

**does not support operating in PHY_S mode at a transmit data rate of 7.5 Gb/s.MultiGBASE-A PHY_S 5 Gb/s TX ability (1.2318.5)**

When read as a one, bit 1.2318.5 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 5 Gb/s. When read as a zero, bit 1.2318.5 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 5 Gb/s.

### 45.2.1.250a.7 MultiGBASE-A PHY_S 2.5 Gb/s TX ability (1.2318.4)

When read as a one, bit 1.2318.4 indicates that the PHY supports operating in PHY_S mode at a transmit data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.4 indicates that the PHY does not support operating in PHY_S mode at a transmit data rate of 2.5 Gb/s.

### 45.2.1.250a.4 MultiGBASE-A PHY_S 1 Gb/s RX ability (1.2318.1)

When read as a one, bit 1.2318.1 indicates that the PHY supports operating in PHY_S mode at a receive data rate of 1 Gb/s. When read as a zero, bit 1.2318.1 indicates that the PHY does not support operating in PHY_S mode at a receive data rate of 1 Gb/s.

### 45.2.1.250a.8 MultiGBASE-A PHY_S 100 Mb/s RX ability (1.2318.0)

When read as a one, bit 1.2318.0 indicates that the PHY supports operating in PHY_S mode at a receive data rate of 100 Mb/s. When read as a zero, bit 1.2318.0 indicates that the PHY does not support operating in PHY_S mode at a receive data rate of 100 Mb/s.

### 45.2.1.250b MultiGBASE-A PMA rate negotiation (Register 1.2319)

The assignment of bits in the MultiGBASE-A PMA supported rates register is shown in Table 45–212a.

**Table 45–212b—MultiGBASE-A PMA rate negotiation register bit definitions**

| Bit(s) | Name | Description | R/W[8] |
|---|---|---|---|
| 1.2319.15:6 | Reserved | Value always 0 | RO |
| 1.2319.5:4 | Negotiated PHY_D Transmit rate | 5 4<br>0 0 = Negotiation in progress<br>0 1 = 100 Mb/s PHY_D TX<br>1 0 = 1 Gb/s PHY_D TX<br>1 1 = Reserved | R/W |
| 1.2319.3:1 | Negotiated PHY_S Transmit rate | 3 2 1<br>0 0 0 = Negotiation in progress<br>0 0 1 = 2.5 Gb/s PHY_S TX<br>0 1 0 = 5 Gb/s PHY_S TX<br>0 1 1 = 7.5 Gb/s PHY_S TX<br>1 0 0 = 10 Gb/s PHY_S TX<br>1 0 1 = Reserved<br>1 1 x = Reserved | R/W |

[8]RO = Read only, R/W = Read/Write.

| | | | |
|---|---|---|---|
| 1.2319.0 | Negotiated Direction | 1 = PHY_D requested of FOLLOWER<br>0 = PHY_S requested of FOLLOWER | R/W |

#### 45.2.1.250b.1 Negotiated PHY_D Transmit rate (1.2319.5:4)

When bits 1.2319:5:4 are 00 negotiation of the PHY_D transmit rate is in progress. When bits 1.2319:5:4 are 01 rate negotiation has selected a PHY_D transmit rate as described in Table 45–212b and the LEADER will request the FOLLOWER operate accordingly through Infofield exchange. The same PHY_S receive rate is selected.

#### 45.2.1.250b.2 Negotiated PHY_S Transmit rate (1.2319.3:1)

When bits 1.2319:3:1 are 000 negotiation of the PHY_S transmit rate is in progress. When bits 1.2319:5:4 are not 000 rate negotiation has selected a PHY_S transmit rate as described in Table 45–212b and the LEADER will request the FOLLOWER operate accordingly through Infofield exchange. The same PHY_D receive rate is selected.

#### 45.2.1.250b.3 Negotiated Direction (1.2319.0)

When bit 1.2319.0 is 1 the LEADER will operate in PHY_S mode and requests the FOLLOWER operate in PHY_D mode. When bit 1.2319.0 is 0 the LEADER will operate in PHY_D mode and requests the FOLLOWER operate in PHY_S mode

#### 45.2.1.250c MultiGBASE-A PMA link partner rate negotiation (Register 1.2320)

The assignment of bits in the MultiGBASE-A PMA link partner rate negotiation register is shown in Table 45–212c.

**Table 45–212c—MultiGBASE-A PMA link partner rate negotiation register bit definitions**

| Bit(s) | Name | Description | R/W[9] |
|---|---|---|---|
| 1.2320.15 | Link partner PHY_D 10 Gb/s RX ability | 1 = Link partner has MultiGBASE-A PHY_D 10 Gb/s RX ability<br>0 = Link partner does not have MultiGBASE-A PHY_D 10 Gb/s RX ability | RO |
| 1.2320.14 | Link partner PHY_D 7.5 Gb/s RX ability | 1 = Link partner has MultiGBASE-A PHY_D 7.5 Gb/s RX ability<br>0 = Link partner does not have MultiGBASE-A PHY_D 7.5 Gb/s RX ability | RO |
| 1.2320.13 | Link partner PHY_D 5 Gb/s RX ability | 1 = Link partner has MultiGBASE-A PHY_D 5 Gb/s RX ability<br>0 = Link partner does not have MultiGBASE-A PHY_D 5 Gb/s RX ability | RO |

[9]RO = Read only.

| | | | |
|---|---|---|---|
| 1.2320.12 | Link partner PHY_D 2.5 Gb/s RX ability | 1 = Link partner has MultiGBASE-A PHY_D 2.5 Gb/s RX ability<br>0 = Link partner does not have MultiGBASE-A PHY_D 2.5 Gb/s RX ability | RO |
| 1.2320.11:10 | Reserved | Value always 0 | RO |
| 1.2320.9 | Link partner PHY_D 1 Gb/s TX ability | 1 = Link partner has MultiGBASE-A PHY_D 1 Gb/s TX ability<br>0 = Link partner does not have MultiGBASE-A PHY_D 1 Gb/s TX ability | RO |
| 1.2320.8 | Link partner PHY_D 100 Mb/s TX ability | 1 = Link partner has MultiGBASE-A PHY_D 100 Mb/s TX ability<br>0 = Link partner does not have MultiGBASE-A PHY_D 100 Mb/s TX ability | RO |
| 1.2320.7 | Link partner PHY_S 10 Gb/s TX ability | 1 = Link partner has MultiGBASE-A PHY_S 10 Gb/s TX ability<br>0 = Link partner does not have MultiGBASE-A PHY_S 10 Gb/s TX ability | RO |
| 1.2320.6 | Link partner PHY_S 7.5 Gb/s TX ability | 1 = Link partner has MultiGBASE-A PHY_S 7.5 Gb/s TX ability<br>0 = Link partner does not have MultiGBASE-A PHY_S 7.5 Gb/s Tx ability | RO |
| 1.2320.5 | Link partner PHY_S 5 Gb/s TX ability | 1 = Link partner has MultiGBASE-A PHY_S 5Gb/s TX ability<br>0 = Link partner does not have MultiGBASE-A PHY_S 5Gb/s TX ability | RO |
| 1.2320.4 | Link partner PHY_S 2.5 Gb/s TX ability | 1 = Link partner has MultiGBASE-A PHY_S 2.5Gb/s TX ability<br>0 = Link partner does not have MultiGBASE-A PHY_S 2.5Gb/s TX ability | RO |
| 1.2320.3:2 | Reserved | Value always 0 | RO |
| 1.2320.3:1 | Link partner PHY_S 1 Gb/s RX ability | 1 = Link partner has MultiGBASE-A PHY_S 1 Gb/s RX ability<br>0 = Link partner does not have MultiGBASE-A PHY_S 1 Gb/s RX ability | RO |
| 1.2320.0 | Link partner PHY_S 100 Mb/s RX ability | 1 = Link partner has MultiGBASE-A PHY_S 100 Mb/s RX ability<br>0 = Link partner does not have MultiGBASE-A PHY_S 100 Mb/s RX ability | RO |

#### 45.2.1.250c.1 Link partner PHY_D 10 Gb/s RX ability (1.2320.15)

When read as a one, bit 1.2318.15 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 10 Gb/s. When read as a zero, bit 1.2318.15 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 10 Gb/s.

#### 45.2.1.250c.2 Link partner PHY_D 7.5 Gb/s RX ability (1.2320.14)

When read as a one, bit 1.2320.14 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 7.5 Gb/s. When read as a zero, bit 1.2320.14 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 7.5 Gb/s.

#### 45.2.1.250c.2 *[Note to Editor: Renumber the 45.2.1.250c subclauses appropriately]*Link partner PHY_D 5 Gb/s RX ability (1.2320.13)

When read as a one, bit 1.2318.13 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 5 Gb/s. When read as a zero, bit 1.2318.13 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 5 Gb/s.

#### 45.2.1.250c.3 Link partner PHY_D 2.5 Gb/s RX ability (1.2320.12)

When read as a one, bit 1.2318.12 indicates that the link partner supports operating in PHY_D mode at a receive data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.12 indicates that the link partner does not support operating in PHY_D mode at a receive data rate of 2.5 Gb/s.

#### 45.2.1.250c.4 Link partner PHY_D 1 Gb/s TX ability (1.2320.9)

When read as a one, bit 1.2320.9 indicates that the link partner supports operating in PHY_D mode at a transmit data rate of 1 Gb/s. When read as a zero, bit 1.2320.9 indicates that the link partner does not support operating in PHY_D mode at a transmit data rate of 1 Gb/s.

#### 45.2.1.250c.4 Link partner PHY_D 100 Mb/s TX ability (1.2318.8)

When read as a one, bit 1.2318.8 indicates that the link partner supports operating in PHY_D mode at a transmit data rate of 100 Mb/s. When read as a zero, bit 1.2318.8 indicates that the link partner does not support operating in PHY_D mode at a transmit data rate of 100 Mb/s.

#### 45.2.1.250c.5 Link partner PHY_S 10 Gb/s TX ability (1.2320.7)

When read as a one, bit 1.2318.7 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 10 Gb/s. When read as a zero, bit 1.2318.7 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 10 Gb/s.

#### 45.2.1.250c.5 Link partner PHY_S 7.5 Gb/s TX ability (1.2320.6)

When read as a one, bit 1.2320.6 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 7.5 Gb/s. When read as a zero, bit 1.2320.6 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 7.5 Gb/s.

#### 45.2.1.250c.6 Link partner PHY_S 5 Gb/s TX ability (1.2320.5)

When read as a one, bit 1.2318.5 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 5 Gb/s. When read as a zero, bit 1.2318.5 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 5 Gb/s.

#### 45.2.1.250c.7 Link partner PHY_S 2.5 Gb/s TX ability (1.2320.4)

When read as a one, bit 1.2318.4 indicates that the link partner supports operating in PHY_S mode at a transmit data rate of 2.5 Gb/s. When read as a zero, bit 1.2318.4 indicates that the link partner does not support operating in PHY_S mode at a transmit data rate of 2.5 Gb/s.

#### 45.2.1.250c.8 Link partner PHY_S 1 Gb/s RX ability (1.2320.1)

When read as a one, bit 1.2320.1 indicates that the link partner supports operating in PHY_S mode at a receive data rate of 1 Gb/s. When read as a zero, bit 1.2320.1 indicates that the link partner does not support operating in PHY_S mode at a receive data rate of 1 Gb/s.

#### 45.2.1.250c.8 Link partner PHY_S 100 Mb/s RX ability (1.2320.0)

When read as a one, bit 1.2318.0 indicates that the link partner supports operating in PHY_S mode at a receive data rate of 100 Mb/s. When read as a zero, bit 1.2318.0 indicates that the link partner does not support operating in PHY_S mode at a receive data rate of 100 Mb/s.

### 45.2.3 PCS registers

#### 45.2.3.87 MultiGBASE-T1 PCS status 2 register (Register 3.2324)

***Change the last sentence of 45.2.3.87.1 as follows:***

#### 45.2.3.87.1 Receive link status (3.2324.10)

When read as a one, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is in a fully operational state. When read as a zero, bit 3.2324.10 indicates that the MultiGBASE-T1 PCS is not fully operational. Bit 3.2324.10 is a reflection of the pcs_status variable defined in 149.3.8.1, 191.3.6.1, and 192.3.6.1.

#### 45.2.3.87.2 PCS high RFER (3.2324.9)

***Change the last sentence of 45.2.3.87.2 as follows:***

When read as a one, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS receiver is detecting 16 or more RS-FEC errored blocks within 88 RS-FEC frames. When read as a zero, bit 3.2324.9 indicates that the MultiGBASE-T1 PCS is detecting fewer than 16 RS-FEC errored blocks within 88 RS-FEC frames. Bit 3.2324.9 is a reflection of the state of the hi_rfer variable defined in 149.3.7.2.2, 191.3.5.1.2, and 192.3.5.1.2.

#### 45.2.3.87.3 PCS block lock (3.2324.8)

***Change the last sentence of 45.2.3.87.3 as follows:***

When read as a one, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has block lock. When read as a zero, bit 3.2324.8 indicates that the MultiGBASE-T1 PCS receiver has not achieved block lock. Bit 3.2324.8 is a reflection of the state of the block_lock variable defined in 149.3.8.1, 191.3.6.1, and 192.3.6.1.

#### 45.2.3.87.6 BER count (3.2324.5:0)

***Change the first sentence of 45.2.3.87.6 as follows:***

The BER counter formed by bits 3.2324.5:0 is a six bit counter as defined by RFER_count in 149.3.8.2, 191.3.6.2, and 192.3.6.2. These bits shall be reset to all zeros when the MultiGBASE-T1 PCS status 2 register is read by the

management function or upon execution of the MultiGBASE-T1 PCS reset. These bits shall be held at all ones in the case of overflow.

# 46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent -Interface (XGMII)

## 46.1 Overview

***Change the third paragraph of 46.1 as follows:***

The RS adapts the bit serial protocols of the MAC to the parallel encodings of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s (including asymmetric) PHYs. Though the XGMII is an optional interface, it is used extensively in this standard as a basis for specification. The 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s or 1 Gb/s in the reverse direction) Physical Coding Sublayers (PCS) are specified to the XGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XGMII were implemented.

***Change list item "a" in the fourth paragraph of 46.1 as follows:***

a) It is capable of supporting at least one of the following rates of operation: 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s or 1 Gb/s in the reverse direction).

### 46.1.1 Summary of major concepts

***Change list item "i" in 46.1.1 as follows:***

i) The XGMII is rate scalable and may support rates of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s or 1 Gb/s in the reverse direction).

### 46.1.2 Application

***Change the second paragraph of 46.1.2 as follows:***

This interface is used to provide media independence so that an identical media access controller may be used with all 2.5GBASE, ~~5GBASE, and 10GBASE~~, 100M+2.5GBASE, 2.5G+100MBASE, 5GBASE, 100M+5GBASE, 5G+100MBASE, 10GBASE, 100M+10GBASE, 10G+100MBASE, and MultiGBASE-A PHY types.

### 46.1.3 Rate of operation

***Change the first paragraph of 46.1.3 as follows:***

The XGMII supports MAC data rates of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s as defined within this clause. A compliant device may implement any subset of these rates in at least one direction. Symmetric ~~O~~operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35. The XGMII supports a MAC data rate of 100 Mb/s or 1 Gb/s in one direction, for asymmetric operation, when at least one of the specified multigigabit rates is used in the other direction.

## 46.3 XGMII functional specifications

### 46.3.1 Transmit

#### 46.3.1.1 TX_CLK (transmit clock)

***Change the second paragraph of 46.3.1.1 as follows:***

The TX_CLK frequency shall be 1/64 × $f_{MAC}$ ± 100 ppm, where $f_{MAC}$ is the frequency (in Hz) corresponding to the MAC's nominal transmit bit rate.

### 46.3.2 Receive

#### 46.3.2.1 RX_CLK (receive clock)

***Change the second paragraph of 46.3.1.1 as follows:***

The frequency of RX_CLK may be derived from the received data or the ~~it may be that of a~~ nominal clock (e.g., TX_CLK). When the received data rate at the PHY is within tolerance, the RX_CLK frequency shall be 1/64 × $f_{MAC}$ ± 100 ppm, where $f_{MAC}$ is the frequency (in Hz) corresponding to the MAC's nominal receive bit rate.

## 46.6 Protocol implementation conformance statement (PICS) proforma for Clause 46, Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)[10]

### 46.6.2 Identification

#### 46.6.2.3 Major capabilities/options

***Insert new row at end of table (unchanged rows not shown):***

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| … | | | | | |
| ASM | Support of Asymmetric Multigigabit PHYs | 46.1.2 | | O | Yes [ ]<br>No [ ] |

### 46.6.3 PICS proforma tables for Reconciliation Sublayer and 10 Gigabit Media Independent Interface

#### 46.6.3.1 General

***Change PICs items G1, G2, and G3, and insert new row G3a after row G3, as shown (unchanged rows not shown):***

[10]*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| G1 | PHY support of 10 Gb/s MAC data rate in at least one direction | 46.1.3 | Support MAC data rate of 10 Gb/s | PHY:O.1 | Yes [ ]<br>N/A [ ] |
| Gx | PHY support of 7.5 Gb/s to a 10 Gb/s MAC data rate in at least one direction | 46.1.3 | Support MAC data rate operation at 7.5 Gb/s | PHY:O.1 | Yes [ ]<br>N/A [ ] |
| G2 | PHY support of 5 Gb/s MAC data rate in at least one direction | 46.1.3 | Support MAC data rate of 5 Gb/s | PHY:O.1 | Yes [ ]<br>N/A [ ] |
| G3 | PHY support of 2.5 Gb/s MAC data rate in at least one direction | 46.1.3 | Support MAC data rate of 2.5 Gb/s | PHY:O.1 | Yes [ ]<br>N/A [ ] |
| G3a | Asymmetric support of 100 Mb/s | 46.1.3 | Support MAC data rate of 100 Mb/s in one direction when at least one of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s is supported in the other direction | ASM:M<br>PHY:O | Yes [ ]<br>N/A [ ] |
| Gy | Asymmetric support of 1 Gb/s | 46.1.3 | Support MAC data rate of 1 Gb/s in one direction when at least one of 5 Gb/s, or 7.5 Gb/s is supported in the other direction | ASM:M<br>PHY:O | Yes [ ]<br>N/A [ ] |
| … | | | | | |

*[Note to Editor: Renumber the items in this table appropriately]*

# 192. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

## 192.1 Overview

MultiGBASE-AT1 and MultiGBASE-AV1 PHYs use a time-division duplex (TDD) transmission structure between two active PHYs, in which one link partner transmits a burst while the other is silent. Each PHY may support multiple data rates. MultiGBASE-A PHYs use a common set of symbol rates across high speed and low speed implementations. They also use the same TDD cycle for all data rates (see 192.3) and the same base FEC with different shortening parameters for the high speed and low speed directions.

Each link partner transmits according to a TDD cycle consisting of the following three phases:

1) a PAM 2 modulated burst refresh header,
2) a PAM 2, PAM3, or PAM 4 modulated burst payload,
3) and a QUIET period during which no data is transmitted.

Bursts are aligned so that a PHY transmits its refresh header and burst payload during its link partner's QUIET period. The burst timing provides a gap between transmitted and received bursts to allow for signal propagation delay. Ethernet frames are encoded in 64/65B blocks and protected in RS-FEC frames (with interleaving at 5 Gb/s, 7.5 Gb/s, and 10 Gb/s data rates). The RS-FEC frames comprise the burst payload portion of the TDD cycle. Asymmetric data rates are achieved by asymmetric transmission times for the link partners, with one transmitting 25 RS-FEC superframes per burst and the other transmitting one RS-FEC frame per burst. See 192.3.4 for more detail on TDD bursts.

A MultiGBASE-A PHY may operate as the LEADER or the FOLLOWER. The LEADER-FOLLOWER relationship is predetermined via management control during initialization or via default hardware setup. The LEADER PHY uses a local clock to time its transmitter operations. The FOLLOWER PHY recovers the clock from the received signal and uses it to time its transmitter operations. The LEADER-FOLLOWER relationship is predetermined via management control during initialization or via default hardware setup.

### 192.1.1 Nomenclature

The MultiGBASE-AT1 and MultiGBASE-AV1 PHYs described in this clause represent two distinct PHY types that share the same PCS and PMA specifications subject to frequency scaling. In order to efficiently describe the two PHYs, the following nomenclature is used.

| | |
|---|---|
| HS_PATH | PHY_S HS_TX to PHY_D HS_RX |
| HS_RX | High speed receiver |
| HS_TX | High speed transmitter |
| LS_PATH | PHY_D LS_TX to PHY_S LS_RX |
| LS_RX | Low speed receiver |
| LS_TX | Low speed transmitter |
| *N_r* | Number of symbols transmitted in the refresh header of a TDD burst |
| *N_p* | Number of symbols transmitted in the payload of a TDD burst |
| *N_z* | Number of transmit symbol periods during which the TDD burst is QUIET |
| PHY_D | LS_TX, HS_RX mode of operation (high speed XGMII destination) |
| PHY_S | HS_TX, LS_RX mode of operation (high speed XGMII source) |

When talking about the asymmetric PHY communicating on a shielded, balanced, pair of conductors, use:

MultiGBASE-AT1

When talking about the asymmetric PHY communicating on a coaxial cable, use:

MultiGBASE-AV1

When talking about all PHYs, regardless of transmit bit rate or cable type, use:

MultiGBASE-A

The six modes of operation and MAC data rate combinations for each of the two PHY types are shown in Table 192–1.

**Table 192–1—PHY/PMD type definitions**

| PHY name | Medium interface | Mode of operation | Transmit MAC data rate | Receive MAC data rate |
|---|---|---|---|---|
| MultiGBASE-AT1 | Differential (balanced) | PHY_D | 100 Mb/s | 2.5 Gb/s |
| | | | 100 Mb/s | 5 Gb/s |
| | | | 100 Mb/s | 10 Gb/s |
| | | | 1 Gb/s | 5 Gb/s |
| | | | 1 Gb/s | 7.5 Gb/s |
| | | PHY_S | 2.5 Gb/s | 100 Mb/s |
| | | | 5 Gb/s | 100 Mb/s |
| | | | 10 Gb/s | 100 Mb/s |
| | | | 5 Gb/s | 1 Gb/s |
| | | | 7.5 Gb/s | 1 Gb/s |
| MultiGBASE-AV1 | Single-ended (unbalanced) | PHY_D | 100 Mb/s | 2.5 Gb/s |
| | | | 100 Mb/s | 5 Gb/s |
| | | | 100 Mb/s | 10 Gb/s |
| | | | 1 Gb/s | 5 Gb/s |
| | | | 1 Gb/s | 7.5 Gb/s |

| | | | | |
|---|---|---|---|---|
| | | PHY_S | 2.5 Gb/s | 100 Mb/s |
| | | | 5 Gb/s | 100 Mb/s |
| | | | 10 Gb/s | 100 Mb/s |
| | | | 5 Gb/s | 1 Gb/s |
| | | | 7.5 Gb/s | 1 Gb/s |

The following shorthand nomenclature, without the full PHY name, is used to describe the MDI, link segment, test mode, and other specifications that are medium dependent:

-T1 represents a single shielded balanced pair of conductors (i.e., differential)
-V1 represents a single coaxial cable (i.e., unbalanced)

Additionally, for parameters that scale with the PHY's supported MAC data rate, the parameter *S* is used for scaling as shown in Table 192–2.

**Table 192–2—Scaling parameters**

| Transmit MAC data rate | *S* |
|---|---|
| 100 Mb/s | 0.5 |
| 1 Gb/s | 1 |
| 2.5 Gb/s | 0.5 |
| 5 Gb/s | 1 |
| 7.5 Gb/s | 1 |
| 10 Gb/s | 1 |

### 192.1.2 Relationship of MultiGBASE-A to other standards

The relationship between a MultiGBASE-A PHY, the ISO Open Systems Interconnection (OSI) Reference Model, and the IEEE 802.3 Ethernet Model is shown in Figure 192–1. The PHY sublayers (shown shaded) in Figure 192–1 connect one Clause 4 Media Access Control (MAC) layer to the medium. The XGMII is defined in Clause 46.

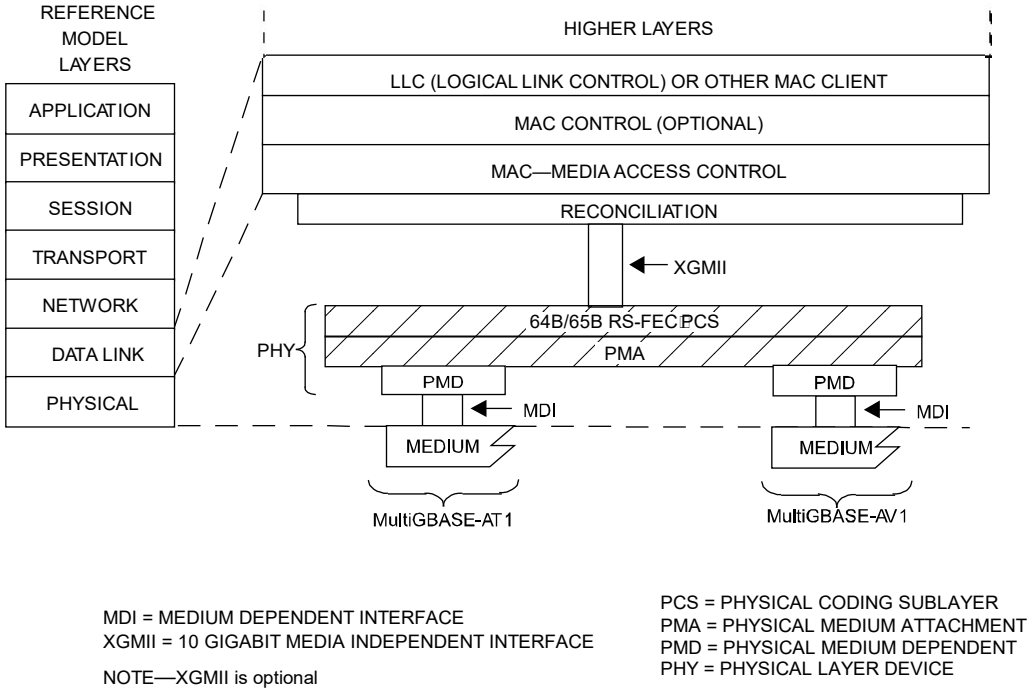
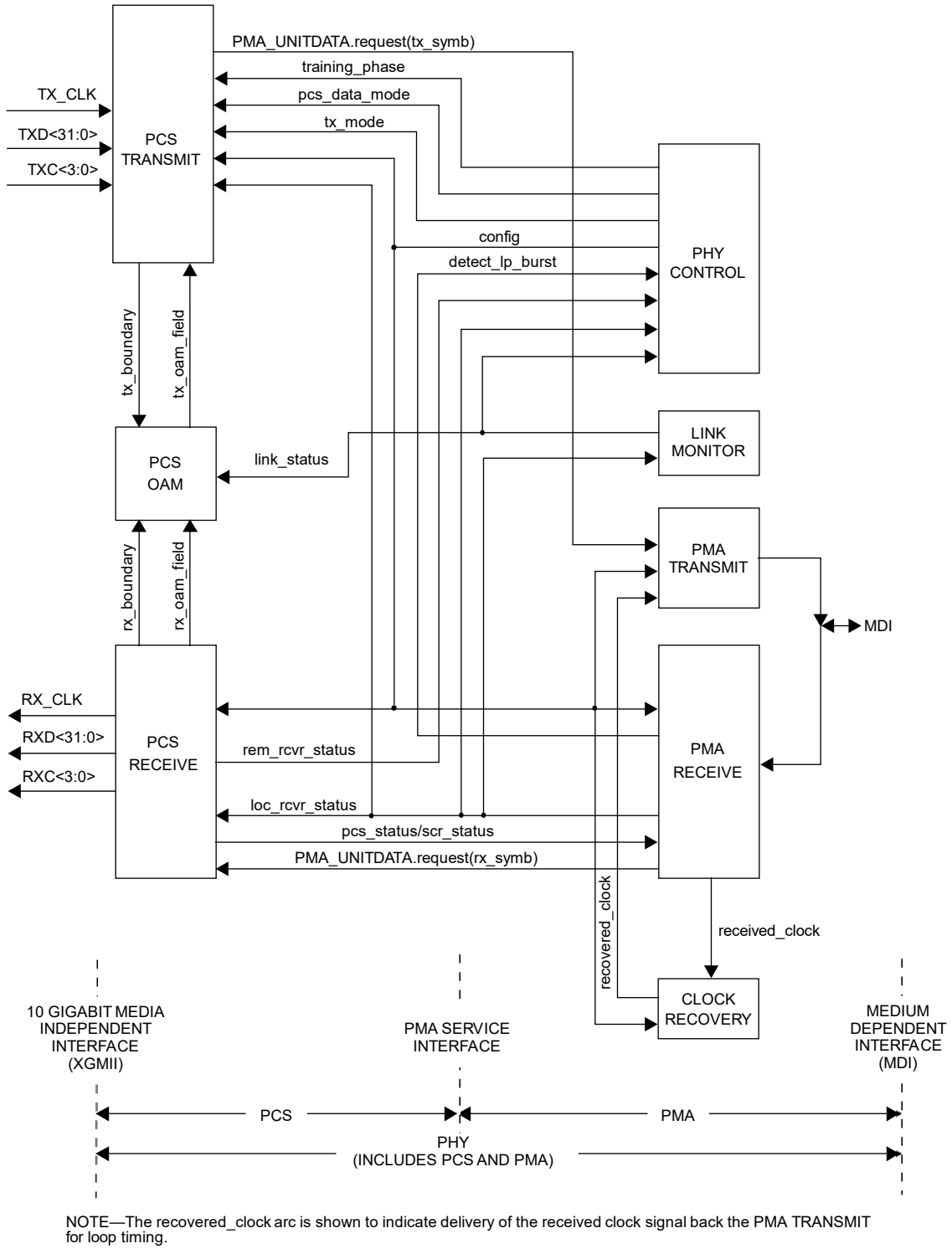



**Figure 192–1—Relationship of MultiGBASE-A PHYs to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet Model**

### 192.1.3 Operation of MultiGBASE-A

The MultiGBASE-A functional block diagram is shown in Figure 192–2.




NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

**Figure 192–2—Functional block diagram**

### 192.1.3.1 Physical Coding Sublayer (PCS) in PHY_S mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the data mode of operation (see 192.2.1.9), the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in data mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 1-bit OAM field is appended to form a 976-bit block. A number, L (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 3 for 7.5 Gb/s, L = 4 for 10 Gb/s), of these 976-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC(128,122,8) and the round-robin interleaving as described in 192.3.2.2.15. The RS-FEC output superframe consists of L × 1024 bits. The duration of the superframe is 1024 / 3 ns.

NOTE—Duration = L × 1024 bits / bits per symbol / baud rate. For 10 Gb/s, Duration = 4 × 1024 / 2 / 6 GBd; for 7.5 Gb/s when associated with 100 Mb/s LS, Duration= 3 × 1024 / 1.5 / 6 GBd, for 7.5 Gb/s when associated with 1 Gb/s LS, Duration= 3 × 1024 / 2 / 6 GBd; for 5 Gb/s when associated with 100 Mb/s LS, Duration = 2 × 1024 / 1 / 6 GBd; for 5 Gb/s when associated with 1 Gb/s LS, Duration = 2 × 1024 / 1.5 / 6 GBd; for 2.5 Gb/s, Duration= 1 × 1024 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the HS_TX payload. The PCS Transmit functions are described in 192.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}\langle 65 \times i + j \rangle = \text{tx\_coded}_i\langle j \rangle$$

where $i$ = 0 to 14, $j$ = 0 to 64, and $\text{tx\_coded}_i$<64:0> is the $i^{th}$ 64B/65B block where $\text{tx\_coded}_0$<64:0> is the first block transmitted.

In the training mode (see 192.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 192.3. The interface to the PMA is an abstract message-passing interface specified in 192.4.

### 192.1.3.2 Physical Coding Sublayer (PCS) in PHY_D mode

The PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, with the Physical Medium Attachment (PMA) sublayer.

In addition to the data mode of operation (see 192.2.1.9), the PCS supports a training mode. Furthermore, the PCS contains a management interface.

In the transmit direction, in data mode, the PCS receives eight XGMII data octets provided by two consecutive transfers on the XGMII service interface on TXD<31:0> and groups them into 64-bit blocks with the 64-bit block boundaries aligned with the boundary of the two XGMII transfers. Each group of eight octets along with the data/control indications is transcoded into a 65-bit block. These 65-bit blocks are then aggregated into groups of 15 blocks. The contents of each group are contained in a vector tx_group15x65B.

Next, a 17-bit OAM field is appended to form a 992-bit block. Each of these 992-bit blocks is formed into an RS-FEC input frame, then encoded by the RS-FEC(130,124,8). The RS-FEC output frame consists of 1040 bits. The duration of the frame is 1040 / 3 ns.

NOTE—Duration = 1040 bits / bits per symbol / baud rate = 1040 / 1 / 3 GBd.

Finally these bits are exclusive OR'd with a degree 33 scrambler to create the LS_TX payload. The PCS Transmit functions are described in 192.3.2.2.

tx_group15x65B<974:0> is defined as:

$$\text{tx\_group15x65B}<65 \times i + j> = \text{tx\_coded}_i<j>$$

where $i$ = 0 to 14, $j$ = 0 to 64, and tx_coded$_i$<64:0> is the $i^{th}$ 64B/65B block where tx_coded0<64:0> is the first block transmitted.

In the training mode (see 192.4.2.4), the PCS transmits and receives PAM2 training frames to synchronize to the PHY frame and exchanges OAM capabilities.

Details of the PCS functions and state diagrams are covered in 192.3. The interface to the PMA is an abstract message-passing interface specified in 192.4.

### 192.1.3.3 Physical Medium Attachment (PMA) sublayer

The PMA couples messages from the PCS service interface onto a single balanced pair of conductors (-T1) or a single coaxial cable (-V1) via the Medium Dependent Interface (MDI) and provides the link management and PHY Control functions. The PMA provides communications at 6 × *S* GBd. See Table 192–2 for the definition of *S*.

The PMA PHY Control function generates signals that control the PCS and PMA sublayer operations. PHY Control is enabled and provides the startup functions required for successful operation. It determines whether the PHY operates in a disabled state, a training state, or a data state where MAC frames can be exchanged between the link partners.

The Link Monitor determines the status of the underlying link and communicates this status to other functional blocks. A failure of the receive link causes the data mode operation to stop and startup functions to restart.

PMA functions and state diagrams are specified in 192.4 and 192.5. The electrical parameters of the PMA (i.e., test modes and electrical specifications for the transmitter and receiver) are specified in 192.5.

### 192.1.4 LS_PATH signaling

LS_PATH signaling is performed by the LS_TX PCS generating continuous symbols that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The symbols consist of PAM2 symbols within a burst and Z symbols between bursts. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling in opposite directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for signal inversion.

The PHY may operate in two basic modes: the data mode or the training mode.

In both data mode and training mode, the LS_TX PCS generates a continuous stream of symbols that are transferred to the PMA during the payload (see Figure 192–26). The Z symbols are transmitted at the same symbol rate.

### 192.1.5 HS_PATH signaling

HS_PATH signaling is performed by the HS_TX PCS generating continuous symbols that the PMA transmits over a single balanced pair of conductors (-T1) or a single coaxial cable (-V1). The symbols consist of PAM2, PAM3 or PAM4 symbols within a burst and Z symbols between bursts. The refresh headers use PAM2 regardless of the MAC data rate. The modulation used by 5 Gb/s and 7.5 Gb/s for the HS_PATH depends on whether the corresponding LS_PATH operates at 100 Mb/s or 1 Gb/s. The HS_PATH modulation are shown in Table 192-yy. The signaling scheme achieves a number of objectives including:

a) Forward error correction (FEC) coded symbol mapping for data.
b) Algorithmic mapping from TXD<31:0> and TXC<3:0> to PAM2 symbols in the 2.5 Gb/s and 5 Gb/s transmit path, PAM4 symbols in the 7.5 Gb/s transmit path when using a 1 Gb/s LS transmit path, and PAM4 symbols in the 10 Gb/s transmit path.
c) Algorithmic mapping from the received signal on the MDI port to RXD<31:0> and RXC<3:0>.
d) Uncorrelated symbols in the transmitted symbol stream.
e) No correlation between symbol streams traveling in opposite directions.
f) Block framing and other control signals.
g) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.
h) Ability to automatically detect and correct for signal inversion.

Table 192-yy – PAM encoding for the HS_PATH

| HS_PATH Rate | HS_PATH Modulation when ls_rate = 100 Mb/s | HS_PATH Modulation when ls_rate = 1 Gb/s |
|---|---|---|
| 2.5 Gb/s | PAM2 | N/A |
| 5 Gb/s | PAM2 | PAM3 |
| 7.5 G/s | PAM3 | PAM4 |
| 10 Gb/s | PAM4 | N/A |

The PHY may operate in two basic modes: the data mode or the training mode.

In both data and training modes, the HS_TX PCS generates a continuous stream of symbols that are transferred to the PMA during the payload (see Figure 192–26). The Z symbols are transmitted at the same symbol rate.

### 192.1.6 Interfaces

All MultiGBASE-A PHY implementations are compatible at the XGMII, if implemented. Implementation of the XGMII is optional. All MultiGBASE-AT1 PHY implementations are compatible at the -T1 MDI. All MultiGBASE-AV1 PHY implementations are compatible at the -V1 MDI. The MDI for a single balanced pair of conductors (-T1) and a single coaxial cable (-V1) are different. Designers are free to implement circuitry within the PCS and PMA in an application-dependent manner provided that the MDI and XGMII (if the XGMII is implemented) specifications are met. System operation from the perspective of signals at the MDI and management objects are identical whether the XGMII is implemented or not.

### 192.1.7 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of state diagrams as described in 21.5, along with the extensions described in 145.2.5.2. State diagram timers follow the conventions of 14.2.3.2. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

Default initializations, unless specified, are left to the implementer.

## 192.2 Service primitives and interfaces

MultiGBASE-A transfers data and control information across the following three service interfaces:

a) 10 Gigabit Media Independent Interface (XGMII)
b) PMA service interface
c) Medium Dependent Interface (MDI)

The XGMII is specified in Clause 46. The PMA service interface is defined in 192.2.1. The -T1 MDI is defined in 192.9. The -V1 MDI is defined in 192.10.

### 192.2.1 PMA service interface

MultiGBASE-A uses the following service primitives to exchange symbol vectors, status indications, and control signals across the service interfaces:

PMA_TXMODE.indication(tx_mode)
PMA_CONFIG.indication(config)
PMA_UNITDATA.request(tx_symb)
PMA_UNITDATA.indication(rx_symb)
PMA_SCRSTATUS.request(scr_status)
PMA_PCSSTATUS.request(pcs_status)
PMA_RXSTATUS.indication(loc_rcvr_status)
PMA_REMRXSTATUS.request(rem_rcvr_status)
PMA_PCSDATAMODE.indication(pcs_data_mode)

The use of these primitives is shown in Figure 192–3. Connections from the management interface (signals MDC and MDIO) to the sublayers are pervasive and are not shown in Figure 192–3.

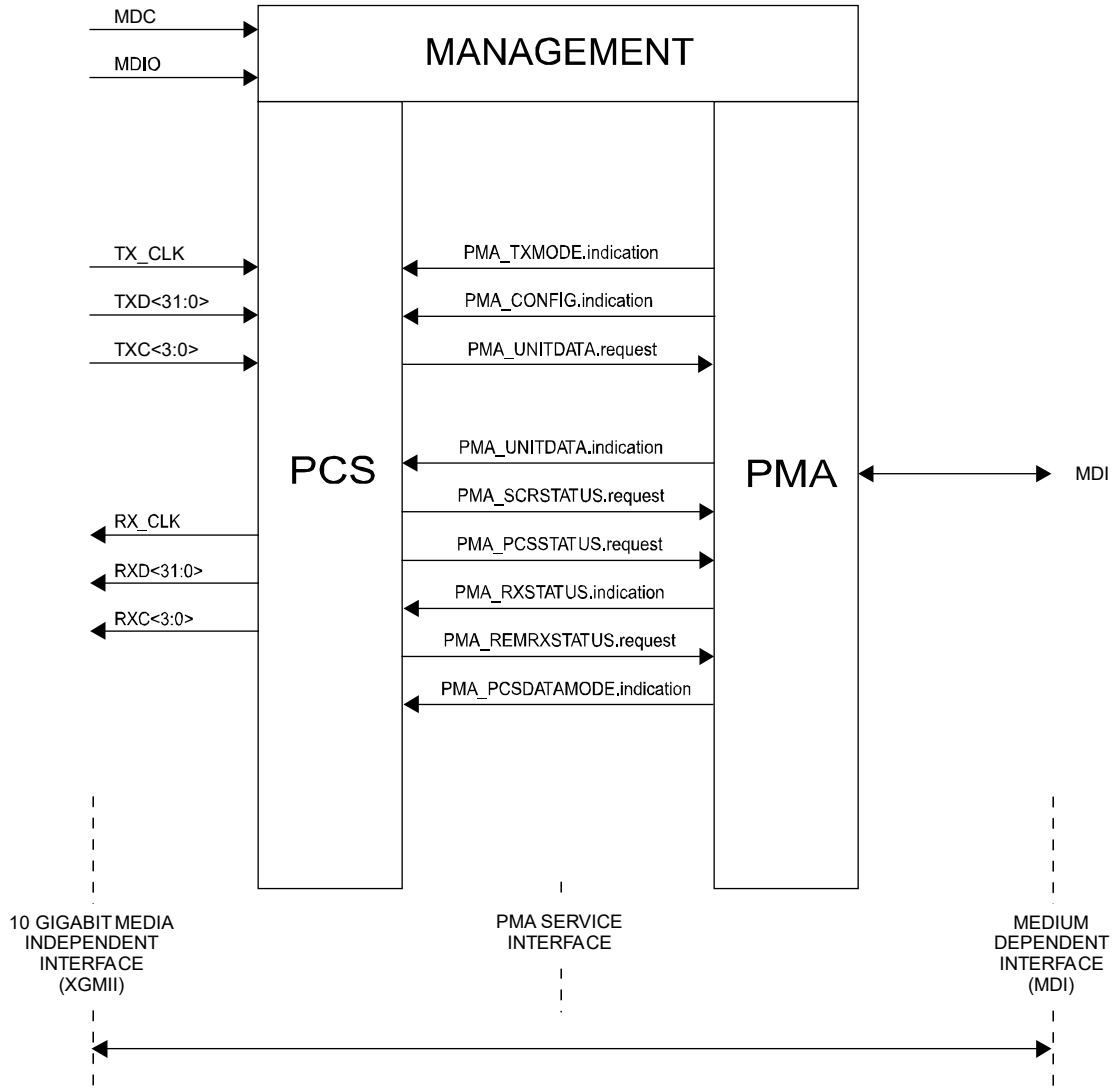



**Figure 192–3—MultiGBASE-A service interface**

#### 192.2.1.1 PMA_TXMODE.indication

The transmitter in a MultiGBASE-A link normally sends over the MDI symbols that represent an XGMII data stream with framing, scrambling and encoding of data, control information, or idles.

#### 192.2.1.1.1 Semantics of the primitive

PMA_TXMODE.indication(tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of symbols the PCS should be transmitting. The parameter tx_mode can take on one of the following values of the form:

SEND_N This value is continuously asserted during transmission of sequences of symbols representing the TDD bursting (including QUIET periods) of an XGMII data stream in the data mode.

SEND_TS This value is continuously asserted in case transmission of sequences of symbols representing the TDD symmetric training mode is to take place. LS_TX and HS_TX send at 3 GBd with PAM2 TDD training frames.

SEND_TA This value is continuously asserted in case transmission of sequences of symbols representing the TDD asymmetric training mode is to take place. LS_TX sends at 3 GBd with PAM2 TDD training frames. HS_TX sends at 3 GBd or 6 GBd with PAM2 TDD training frames.

SEND_Z This value is continuously asserted in case continuous transmission of Z symbols is required. See 192.5.2.4 for the encoding of Z.

#### 192.2.1.1.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages to indicate a change in tx_mode.

#### 192.2.1.1.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 192.3.2.2.

### 192.2.1.2 PMA_CONFIG.indication

PMA_CONFIG FOLLOWER-LEADER configuration is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

#### 192.2.1.2.1 Semantics of the primitive

PMA_CONFIG.indication(config)

PMA_CONFIG.indication specifies to the PHY functions via the parameter config whether the PHY operates as the LEADER or FOLLOWER. The parameter config can take on one of the following two values of the form:

LEADER This value is continuously asserted when the PHY operates as the LEADER.

FOLLOWER
This value is continuously asserted when the PHY operates as the FOLLOWER.

#### 192.2.1.2.2 When generated

PMA generates PMA_CONFIG.indication messages to indicate a change in configuration.

#### 192.2.1.2.3 Effect of receipt

PCS and PMA perform their functions in the LEADER or FOLLOWER configuration according to the value of the parameter config.

#### 192.2.1.3 PMA_UNITDATA.request

This primitive defines the transfer of symbols in the form of the tx_symb parameter from the PCS to the PMA. The symbols are obtained in the PCS Transmit function using the encoding rules defined in 192.3.2.2 to represent XGMII data and control streams or other sequences.

##### 192.2.1.3.1 Semantics of the primitive

PMA_UNITDATA.request(tx_symb)

The PMA_UNITDATA.request primitive conveys the value of the symbol to be transmitted over the MDI via the tx_symb parameter. The tx_symb may take on one of the following values:

{–1, –1/3, +1/3, +1} when PAM4 symbols are to be transmitted in the data mode of HS_PATH for the following two cases:
1) 10 Gb/s transmit payload in data mode when LS_PATH operates at 100 Mb/s, and
2) 7.5 Gb/s transmit payload in data mode when LS_PATH operates at 1 Gb/s.

{-1, 0, +1} when PAM3 symbols are to be transmitted in the data mode of HS_PATH for the following two cases:
1) 7.5 Gb/s transmit payload when LS_PATH operates at 100 Mb/s, and
2) .5 Gb/s transmit payload in data mode when LS_PATH operates at 1 Gb/s.

{–1, +1} in data and training modes for all refresh header, 1 Gb/s, 2.5 Gb/s mode, and 5 Gb/s mode data payloads.

Z when Z symbols are to be transmitted (see 192.5.2.4) in the following two cases:
1) when PMA_TXMODE.indication is SEND_Z during PMA training, and
2) during the QUIET period in each TDD cycle.

##### 192.2.1.3.2 When generated

The PCS generates PMA_UNITDATA.request(tx_symb) synchronously with every transmit clock cycle.

##### 192.2.1.3.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated symbols processed to conform to 192.5.2.

#### 192.2.1.4 PMA_UNITDATA.indication

This primitive defines the transfer of symbols in the form of the rx_symb parameter from the PMA to the PCS.

##### 192.2.1.4.1 Semantics of the primitive

PMA_UNITDATA.indication(rx_symb)

During reception, the PMA_UNITDATA.indication conveys to the PCS via the parameter rx_symb the value of symbols detected on the MDI during each cycle of the recovered clock. The rx_symb may take on the same values defined for tx_symb in 192.2.1.3.1.

#### 192.2.1.4.2 When generated

The PMA generates PMA_UNITDATA.indication(rx_symb) messages synchronously for every symbol received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive, as governed by the recovered clock, is 3 GHz for 100 Mb/s and 2.5 Gb/s receive modes and 6 GHz for 1 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s receive modes.

#### 192.2.1.4.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

### 192.2.1.5 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the PCS descrambler has achieved synchronization.

#### 192.2.1.5.1 Semantics of the primitive

PMA_SCRSTATUS.request(scr_status)

The scr_status parameter can take on one of two values of the form:

| | |
|---|---|
| OK | The PCS descrambler has achieved synchronization. |
| NOT_OK | The PCS descrambler is not synchronized. |

#### 192.2.1.5.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages to indicate a change in scr_status.

#### 192.2.1.5.3 Effect of receipt

The effect of receipt of this primitive is specified in 192.4.2.3 and 192.4.2.4.

### 192.2.1.6 PMA_PCSSTATUS.request

This primitive is generated by PCS Receive to indicate the fully operational state of the PCS for the local PHY. The parameter pcs_status conveys to the PMA Receive function the information that the PCS is operating reliably in the data mode.

#### 192.2.1.6.1 Semantics of the primitive

PMA_PCSSTATUS.request(pcs_status)

The pcs_status parameter can take on one of two values of the form:

| | |
|---|---|
| OK | The PCS is operating reliably in the data mode. |
| NOT_OK | The PCS is not operating reliably in the data mode. |

#### 192.2.1.6.2 When generated

PCS Receive generates PMA_PCSSTATUS.request messages to indicate a change in pcs_status.

#### 192.2.1.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 192.4.2.3 and 192.4.4.1.

#### 192.2.1.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criteria for setting the parameter loc_rcvr_status is left to the implementer. For example, it can be based on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol stream.

##### 192.2.1.7.1 Semantics of the primitive

PMA_RXSTATUS.indication(loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values of the form:

OK This value is asserted and remains true during reliable operation of the receive link for the local PHY.

NOT_OK This value is asserted whenever operation of the link for the local PHY is unreliable.

##### 192.2.1.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages to indicate a change in loc_rcvr_status on the basis of signals received at the MDI.

##### 192.2.1.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–3, 192.3.2.3, 192.4.2.4, and 192.5.

#### 192.2.1.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The parameter rem_rcvr_status is set to the value received in the loc_rcvr_status bit in the Infofield from the remote PHY. The rem_rcvr_status is set to NOT_OK if the PCS has not decoded a valid Infofield from the remote PHY.

##### 192.2.1.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request(rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values of the form:

OK The receive link for the remote PHY is operating reliably.

NOT_OK Reliable operation of the receive link for the remote PHY is not detected.

##### 192.2.1.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request message to indicate a change in rem_rcvr_status based on the PCS decoding the loc_rcvr_status bit in Infofield messages received from the remote PHY during training.

##### 192.2.1.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 192–26.

#### 192.2.1.9 PMA_PCSDATAMODE.indication

This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states. The pcs_data_mode variable is generated by the PMA PHY Control function. It is passed to the PCS Control function via the PMA_PCSDATAMODE.indication primitive.

##### 192.2.1.9.1 Semantics of the primitive

PMA_PCSDATAMODE.indication(pcs_data_mode)

The pcs_data_mode parameter can take on one of two values of the form:

| | |
|---|---|
| TRUE | The PCS is transmitting and receiving data from the XGMII. |
| FALSE | The PCS is in a training or test mode. |

##### 192.2.1.9.2 When generated

The PMA PHY Control function generates PMA_PCSDATAMODE.indication messages continuously.

##### 192.2.1.9.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its transmit function as described in 192.3.2.2.

## 192.3 Physical Coding Sublayer (PCS) functions

### 192.3.1 PCS service interface (XGMII)

The PCS service interface allows the PCS to transfer information to and from a PCS client. The PCS service interface is precisely defined as the 10 Gigabit Media Independent Interface (XGMII) in Clause 46.

### 192.3.2 PCS functions

The PCS comprises one PCS Reset function and two simultaneous and asynchronous operating functions. The PCS operating functions are PCS Transmit and PCS Receive. All operating functions start immediately after the successful completion of the PCS Reset function.

The PCS reference diagram (see Figure 192–4) shows how the two operating functions relate to the messages of the PCS-PMA interface. Connections from the management interface (signals MDC and MDIO) to other layers are pervasive and are not shown in Figure 192–4.

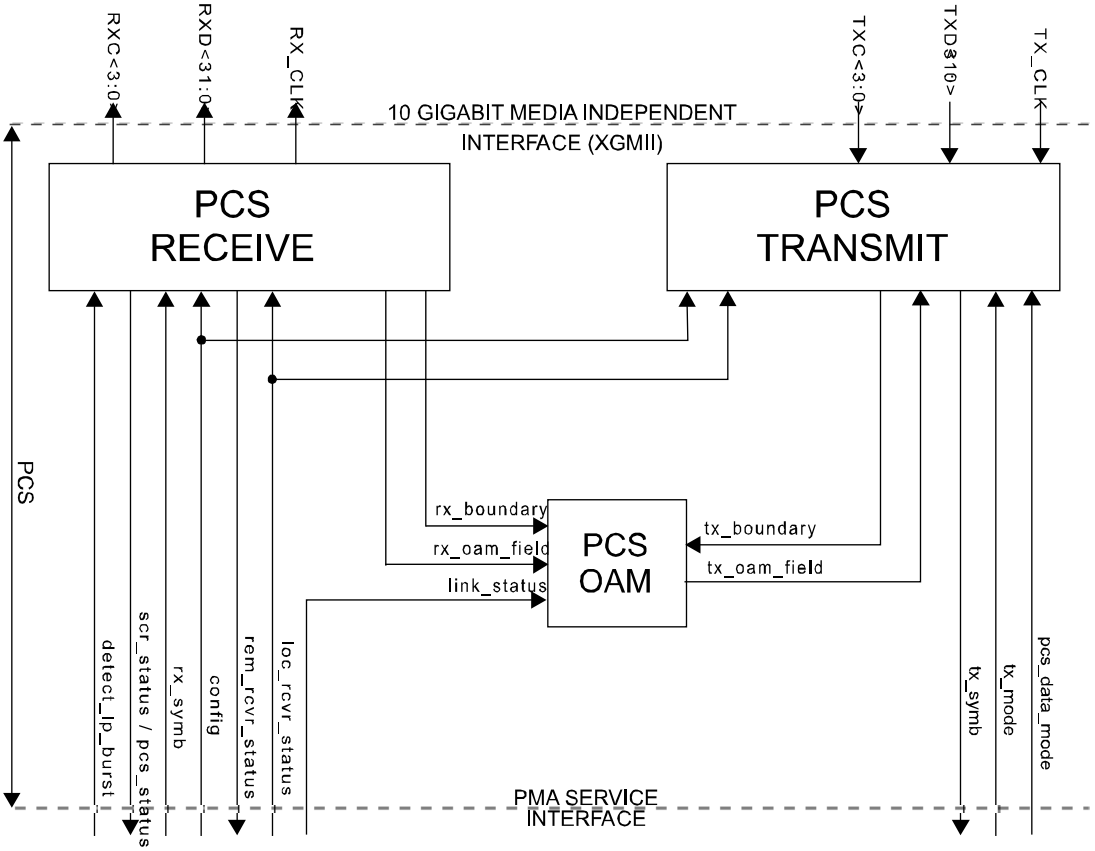



**Figure 192–4—PCS reference diagram**

### 192.3.2.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of following conditions occur:

a) Power on (see 192.3.5.1.2)
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset = TRUE while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

The control and management interface shall be restored to operation within 10 ms from the setting of bit 3.2322.15.

### 192.3.2.2 PCS Transmit function

The LS_TX PCS Transmit function is shown in Figure 192–5 and the HS_TX PCS Transmit function is shown in Figure 192–6. The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 192–20 and to the PCS Transmit bit ordering (see Figure 192–5 and Figure 192–6).

When communicating with the XGMII, the PCS uses a four octet-wide, synchronous data path, with packet delimiting being provided by transmit control signals and receive control signals.

Alignment of pairs of XGMII transfers to 64B/65B blocks is performed in the PCS. The PMA sublayer operates independently of PCS block, RS-FEC frames, and higher-layer packet boundaries. The PCS provides the functions necessary to map packets between the XGMII format and the PMA service interface format. In each TDD cycle, the transmit PCS generates a sequence of PAM symbols followed by a sequence of Z symbols representing the QUIET period to the transmit PMA. The transmit QUIET period allows the receive PMA to receive a burst during each TDD cycle.

For LS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the LS_TX PCS Transmit process take 1 group of 15 65B blocks and append a 17-bit OAM field to it, shown in Figure 192–5. This forms the input to the RS-FEC(130,124) encoder, which adds 48 parity bits. The resulting 1040 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. Transmit data-units are sent to the LS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For HS_TX, after mapping the XGMII transfers to 64B/65B blocks, the subsequent functions of the HS_TX PCS Transmit process take L groups of 15 65B blocks and append a 1-bit OAM field to each group. This forms the input to an L-interleaved RS-FEC(128,122) superframe which adds L × 48 parity bits, shown in Figure 192–6. 25 such superframes are formed for one data payload. L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s and 1Gb/s, L = 3 for 7.5 Gb/s, and L = 4 for 10 Gb/s. The resulting L × 1024 × 25 bits are then scrambled. For 1 Gb/s, 2.5 Gb/s and 5 Gb/s, these bits are then mapped, one at a time, into PAM2 symbols. For 7.5 Gb/s and 5 Gb/s when used with 1 Gb/s LS, these bits are then mapped, three at a time, into PAM3 symbols. For 10 Gb/s and 7.5 Gb/s when used with 1 Gb/s LS, these bits are then mapped, two at a time, into PAM4 symbols. Transmit data-units are sent to the HS_TX PMA service interface via the PMA_UNITDATA.request primitive.

For both LS_TX and HS_TX, each set of transmit data-units forming the payload of a TDD burst are preceded by a PAM-2 mapped refresh header sequence of $N\_r$ symbols and followed by a sequence of $N\_z$ Z symbols to complete the TDD cycle. In each symbol period of a TDD burst, when communicating with the PMA, the PCS Transmit generates a PAM2, PAM3, or PAM4 symbol that is transferred to the PMA via the PMA_UNITDATA.request primitive. Between TDD bursts, the PCS Transmit transfers Z symbols to the PMA via the PMA_UNITDATA.request primitive. The symbol period, $T$, is 1000 / (6 × $S$) ps. See Table 192–2 for the definition of $S$.

The operation of the PCS Transmit function is controlled by the PMA_TXMODE.indication message received from the PMA PHY Control function. During training, PMA_TXMODE.indication has values SEND_Z, SEND_TS, and SEND_TA before transitioning to SEND_N for data mode.

If a PMA_TXMODE.indication message has the value SEND_Z, PCS Transmit shall pass Z symbols at each symbol period to the PMA via the PMA_UNITDATA.request primitive.

If a PMA_TXMODE.indication message has the value SEND_TS or SEND_TA, PCS Transmit shall generate a sequence ($O_n$) defined in 192.3.4 to the PMA via the PMA_UNITDATA.request primitive. These symbols are used for training mode and only transmit the values {–1, +1}.

During training mode, an Infofield is transmitted at regular intervals containing messages for startup operation. By this mechanism, a PHY indicates the status of its own receiver to the link partner and makes request for remote transmitter settings (see 192.4.2.4).

If a PMA_TXMODE.indication message has the value SEND_N, the PCS is in the data mode of operation and the PCS Transmit function shall use a 65B coding technique to generate code-groups that represent data or control. For LS_TX PCS, during transmission, the 15 blocks of 65B encoded bits are appended with a 17-bit OAM field to form the RS-FEC input frame. During data encoding, LS_TX PCS Transmit utilizes Reed-Solomon encoders to generate and append 48 parity check bits to form (130,124) RS-FEC frames for 100 Mb/s or (128, 122) RS-FEC frames for 1 Gb/s, which become the burst payload for one TDD cycle. For HS_TX PCS, during transmission, the 15 blocks of

65B encoded bits are appended with a 1-bit OAM field to form the RS-FEC input frame. During data encoding, HS_TX PCS Transmit utilizes L-interleaved (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 3 for 7.5 Gb/s, or L = 4 for 10 Gb/s) Reed-Solomon encoders to generate and append 48 parity check bits to form 1024-bit (128,122) RS-FEC frames that are interleaved into an L-interleaved RS-FEC superframe that is L × 1024 bits long. 25 consecutive RS-FEC superframes are concatenated to form the burst payload for one TDD cycle.

In all PCS bursts, a scrambled refresh header bit sequence is concatenated with the scrambled burst payload bit sequence and the bit sequences are mapped to PAM symbols appropriate to the transmit rate. These PAM symbols are then concatenated with the required number of Z symbols to complete a full TDD cycle of symbols, and then the process is repeated for each TDD cycle.

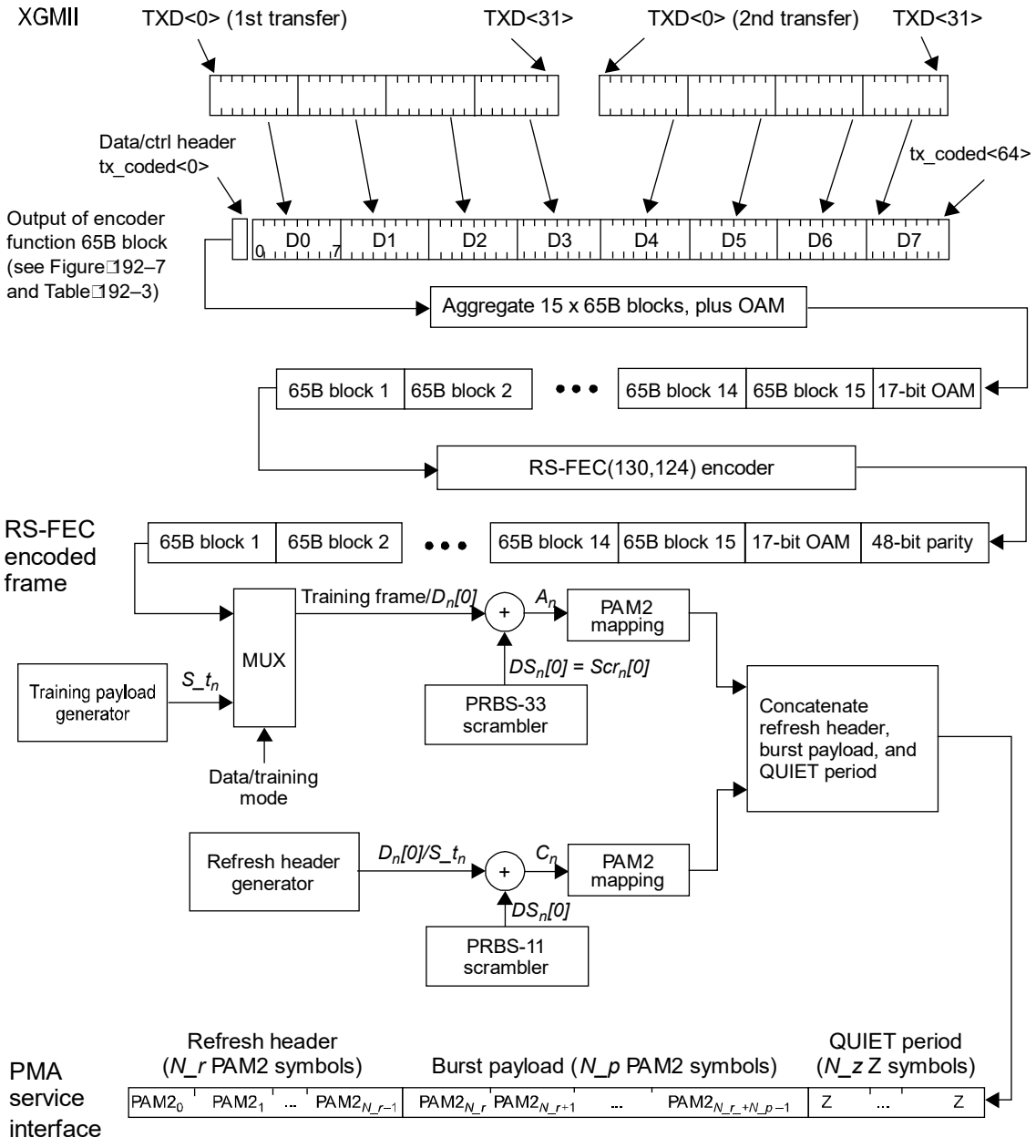
#### 192.3.2.2.1 Use of blocks

The PCS maps XGMII signals into 65-bit blocks inserted into an RS-FEC frame, and vice versa, using a 65B RS-FEC coding scheme. The PAM2/PAM4 PMA training frame synchronization allows establishment of RS-FEC frame and 65B boundaries by the PCS Synchronization process. Blocks and frames are unobservable and have no meaning outside the PCS. The PCS functions ENCODE and DECODE generate, manipulate, and interpret blocks and frames as provided by the rules in 192.3.2.2.4.

#### 192.3.2.2.2 65B RS-FEC transmission code

The PCS uses a transmission code to improve the transmission characteristics of information to be transferred across the link and to support transmission of control and data characters.

The relationship of block bit positions to XGMII, PMA, and other PCS constructs is shown in Figure 192–5 for LS_TX, Figure 192–6 for HS_TX, Figure 192–12 for LS_RX, and Figure 192–13 for HS_RX. These figures show the processing of a multiplicity of blocks containing 8 data octets. See 192.3.2.2.4 for information on how blocks containing control characters are mapped.




NOTE—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

**Figure 192–5—BS_TX PCS Transmit bit ordering**

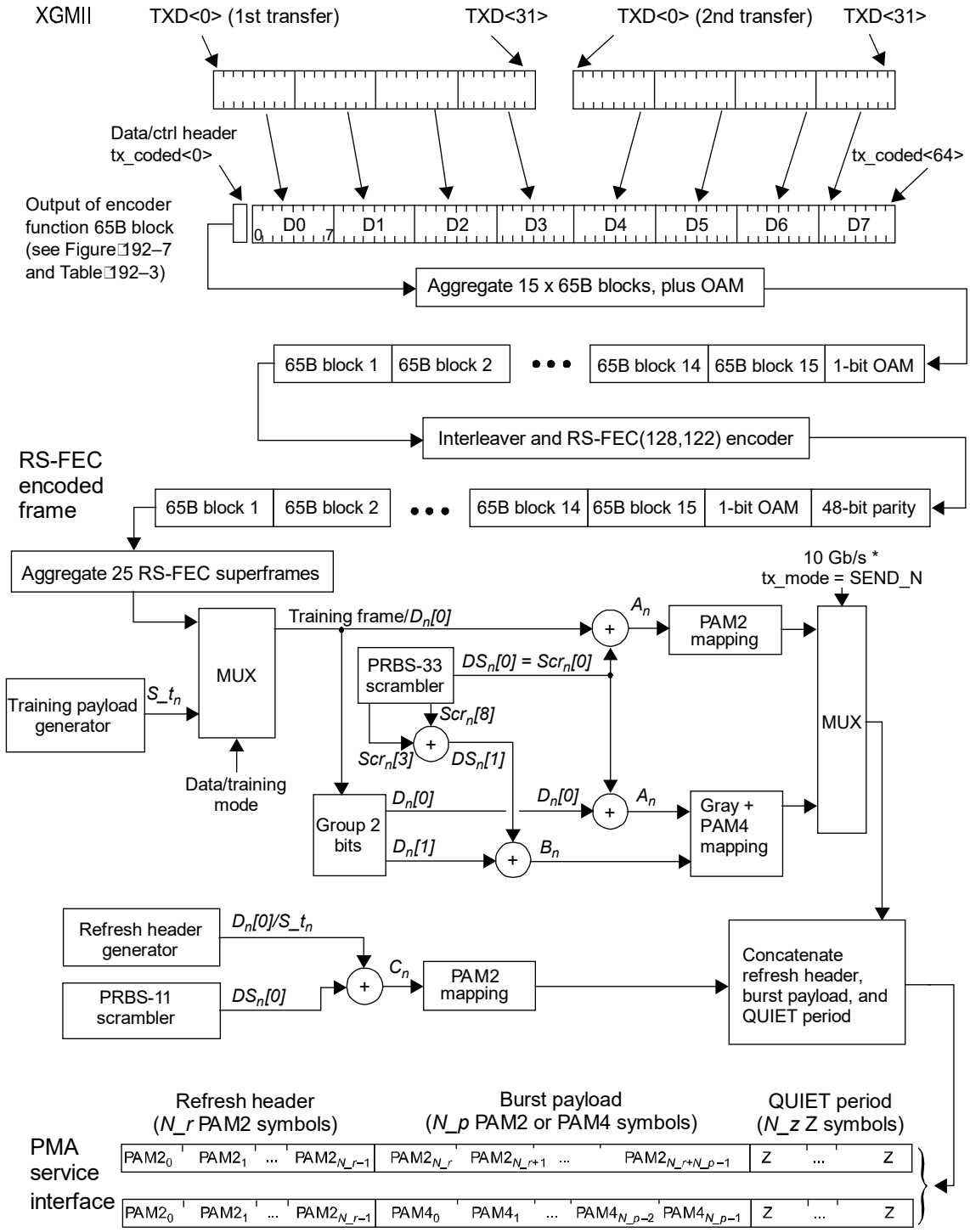
[Note to Editor: A separate version of the figure should be added for the 1 Gb/s LS. Putting both in the same figure could be confusing to the reader. The edits to current Figure 192-5 to create the 1 Gb/s version are as follows:

1. For the FEC, use an RS-FEC(128,122) encoder,

2. The output of the RS-FEC encoder is fifteen 65B blocks, 1 OAM bit and a 48-bit parity (i.e., similar to what's in Figure 192-6 with the same RS-FEC),

3. Similarly similar to Figure 192-6, add an aggregator block between the RS-FEC-encoded frame and the mux. Specifically, the aggregator block should be labeled “Aggregate 6 RS-FEC superframes”,

4. If the PMA service interface is retained in these figures, it should be re-drawn similar to Figure 192-6.]




NOTE 1—This figure shows the mapping from the XGMII to a 64B/65B block for a block containing eight data characters.

NOTE 2—Figure shown for $L = 1$.

NOTE 3—Either the PAM2 or PAM4 path and TDD frame at the PMA service interface is used. PAM4 path (and the lower TDD frame shown) is chosen if the bit rate is 10 Gb/s and tx_mode = SEND_N.

**Figure 192–6—BI_TX PCS Transmit bit ordering**

**192.3.2.2.3** [Note to Editor: In addition to the changes for adding 7.5 Gb/s HS with 100 Mb/s LS, further changes are required to 7.5Gb/s /PAM4, 5Gb/s /PAM3 and 1 Gbps /PAM2 for cases 1Gb/s LS path is selected. It is probably best to add these in a separate figure that can be prepared as a D2.1 comment.]

#### 192.3.2.2.3 Notation conventions

For values shown as binary, the leftmost bit is the first transmitted bit.

64B/65B encodes 8 data octets or control characters into a block. Blocks containing control characters also contain a block type field. Data octets are labeled D0 to D7. Control characters other than /O/, /S/, and /T/ are labeled C0 to C7. The control character for ordered set is labeled as O0 or O4 since it is only valid on the first octet of the XGMII. The control character for start is labeled as S0 or S4 for the same reason. The control character for terminate is labeled as T0 to T7.

The two XGMII transfers provide eight characters that are encoded into one 65-bit transmission block. The subscript in the above labels indicates the position of the character in the eight characters from the XGMII transfer(s).

Contents of block type fields, data octets, and control characters are shown as hexadecimal values. The LSB of the hexadecimal value represents the first transmitted bit. For instance, the block type field 0x1E is sent from left to right as 01111000. The bits of a transmitted or received block are labeled tx_coded<64:0> and rx_coded<64:0> where tx_coded<0> and rx_coded<0> represent the first transmitted bit. The value of the data/ctrl header is shown as a binary value. Binary values are shown with the first transmitted bit (the LSB) on the left.

#### 192.3.2.2.4 Block structure

Blocks consist of 65 bits. The first bit of a block is the data/ctrl header. Blocks are either data blocks or control blocks. The data/ctrl header is 0 for data blocks and 1 for control blocks. The remainder of the block contains the payload.

Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block. For control blocks containing a Start or Terminate character, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. Each control block contains eight characters.

The format of the blocks is shown in Figure 192–7. In the figure, the column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, $D_0$ through $D_7$ are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set

to one. The single bit fields (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt.

| **Input data** | data ctrl header | **Block payload** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Bit position:** / **Data block format:** | 0 | 1 | | | | | | | 64 |
| $D_0$ $D_1$ $D_2$ $D_3$/$D_4$ $D_5$ $D_6$ $D_7$ | 0 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ |
| **Control Block Formats:** | | Block | | | | | | | |
| $C_0$ $C_1$ $C_2$ $C_3$/$C_4$ $C_5$ $C_6$ $C_7$ | 1 | 0x1E | $C_0$ | $C_1$ | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $C_0$ $C_1$ $C_2$ $C_3$/$O_4$ $D_5$ $D_6$ $D_7$ | 1 | 0x2D | $C_0$ | $C_1$ | $C_2$ | $C_3$ | $O_4$ | $D_5$ | $D_6$ | $D_7$ |
| $C_0$ $C_1$ $C_2$ $C_3$/$S_4$ $D_5$ $D_6$ $D_7$ | 1 | 0x33 | $C_0$ | $C_1$ | $C_2$ | $C_3$ | | $D_5$ | $D_6$ | $D_7$ |
| $O_0$ $D_1$ $D_2$ $D_3$/$S_4$ $D_5$ $D_6$ $D_7$ | 1 | 0x66 | $D_1$ | $D_2$ | $D_3$ | $O_0$ | | $D_5$ | $D_6$ | $D_7$ |
| $O_0$ $D_1$ $D_2$ $D_3$/$O_4$ $D_5$ $D_6$ $D_7$ | 1 | 0x55 | $D_1$ | $D_2$ | $D_3$ | $O_0$ | $O_4$ | $D_5$ | $D_6$ | $D_7$ |
| $S_0$ $D_1$ $D_2$ $D_3$/$D_4$ $D_5$ $D_6$ $D_7$ | 1 | 0x78 | $D_1$ | $D_2$ | $D_3$ | $D_4$ | | $D_5$ | $D_6$ | $D_7$ |
| $O_0$ $D_1$ $D_2$ $D_3$/$C_4$ $C_5$ $C_6$ $C_7$ | 1 | 0x4B | $D_1$ | $D_2$ | $D_3$ | $O_0$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $T_0$ $C_1$ $C_2$ $C_3$/$C_4$ $C_5$ $C_6$ $C_7$ | 1 | 0x87 | | $C_1$ | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0$ $T_1$ $C_2$ $C_3$/$C_4$ $C_5$ $C_6$ $C_7$ | 1 | 0x99 | $D_0$ | | $C_2$ | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0$ $D_1$ $T_2$ $C_3$/$C_4$ $C_5$ $C_6$ $C_7$ | 1 | 0xAA | $D_0$ | $D_1$ | | $C_3$ | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0$ $D_1$ $D_2$ $T_3$/$C_4$ $C_5$ $C_6$ $C_7$ | 1 | 0xB4 | $D_0$ | $D_1$ | $D_2$ | | $C_4$ | $C_5$ | $C_6$ | $C_7$ |
| $D_0$ $D_1$ $D_2$ $D_3$/$T_4$ $C_5$ $C_6$ $C_7$ | 1 | 0xCC | $D_0$ | $D_1$ | $D_2$ | $D_3$ | | $C_5$ | $C_6$ | $C_7$ |
| $D_0$ $D_1$ $D_2$ $D_3$/$D_4$ $T_5$ $C_6$ $C_7$ | 1 | 0xD2 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | | $C_6$ | $C_7$ |
| $D_0$ $D_1$ $D_2$ $D_3$/$D_4$ $D_5$ $T_6$ $C_7$ | 1 | 0xE1 | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | | $C_7$ |
| $D_0$ $D_1$ $D_2$ $D_3$/$D_4$ $D_5$ $D_6$ $T_7$ | 1 | 0xFF | $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | |

**Figure 192–7—64B/65B block formats for MultiGBASE-A**

#### 192.3.2.2.5 Control codes

All control characters are supported by both the XGMII and the PCS. The representations of the control characters are the control codes. The XGMII encodes a control character into an octet (an eight-bit value). The PCS encodes the start and terminate control characters implicitly by the block type field. The PCS encodes the ordered set control codes using a combination of the block type field and a four-bit O code for each ordered set. The PCS encodes each of the other control characters into a seven-bit C code.

The control characters and their mappings to MultiGBASE-A control codes and XGMII control codes are specified in Table 192–3.

**Table 192–3—MultiGBASE-A control codes**

| Control character | Notation | XGMII control code | Control code | O code |
|---|---|---|---|---|
| idle | /I/ | 0x07 | 0x00 | — |
| start | /S/ | 0xFB | Encoded by block type field | — |
| terminate | /T/ | 0xFD | Encoded by block type field | — |
| error | /E/ | 0xFE | 0x1E | — |
| Sequence ordered set | /Q/ | 0x9C | Encoded by block type field plus O code | 0x0 |
| reserved0 | | 0x1C | 0x2D | reserved0 |
| reserved1 | | 0x3C | 0x33 | reserved1 |
| reserved2 | | 0x7C | 0x4B | reserved2 |

| | | | | |
|---|---|---|---|---|
| reserved3 | | 0xBC | 0x55 | reserved3 |
| reserved4 | | 0xDC | 0x66 | reserved4 |
| reserved5 | | 0xF7 | 0x78 | reserved5 |
| Signal ordered set[11] | /Fsig/ | 0x5C | Encoded by block type field plus O code | 0xF |

#### 192.3.2.2.6 Ordered sets

Ordered sets are used to extend the ability to send control and status information over the link such as remote fault and Local Fault status. Ordered sets consist of a control character followed by three data characters. Ordered sets always begin on the first octet of the XGMII. 2.5, 5, and 10 Gigabit Ethernet use one kind of ordered set: the sequence ordered set (see 46.3.4). The sequence ordered set control character is denoted /Q/. An additional ordered set, the signal ordered set, has been reserved and it begins with another control code. The four-bit O field encodes the control code. See Table 192–3 for the mappings.

#### 192.3.2.2.7 Idle (/I/)

Idle control characters (/I/) are transmitted when idle control characters are received from the XGMII. Idle characters may be added or deleted by the PCS to adapt between clock rates. /I/ insertion and deletion shall occur in groups of 4. /I/s may be added following idle or ordered sets. They shall not be added while data is being received. When deleting /I/s, the first four characters after a /T/ shall not be deleted.

#### 192.3.2.2.8 Start (/S/)

The start control character (/S/) indicates the start of a packet. This delimiter is only valid on the first octet of the XGMII (TXD<7:0> and RXD<7:0>). Receipt of an /S/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /S/ as the fifth or first character of the block. These are the only characters of a block on which a start can occur.

#### 192.3.2.2.9 Terminate (/T/)

The terminate control character (/T/) indicates the end of a packet. Since packets may be any length, the /T/ can occur on any octet of the XGMII interface and within any character of the block. The location of the /T/ in the block is implicitly encoded in the block type field. A valid end of packet occurs when a block containing a /T/ is followed by a control block that does not contain a /T/.

[11]Reserved for INCITS T11 Fibre Channel use.

#### 192.3.2.2.10 Ordered set (/O/)

The ordered set control characters (/O/) indicate the start of an ordered set. There are two kinds of ordered sets: the sequence ordered set and the signal ordered set, which is reserved. When it is necessary to designate the control character for the sequence ordered set specifically, /Q/ is used. /O/ is only valid on the first octet of the XGMII. Receipt of an /O/ on any other octet of TXD indicates an error. Block type field values implicitly encode an /O/ as the first or fifth character of the block. The 4-bit O code encodes the specific /O/ character for the ordered set.

#### 192.3.2.2.11 Error (/E/)

The /E/ is sent whenever an /E/ is received. The /E/ allows physical sublayers such as the PCS to propagate received errors. See R_BLOCK_TYPE and T_BLOCK_TYPE function definitions in 192.3.5.1.3 for further information.

#### 192.3.2.2.12 Transmit process

The LS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. For the 100 Mb/s LS_TX rate, 30 XGMII data transfers are encoded into an RS-FEC frame. It takes 1040 PMA_UNITDATA transfers to send an RS-FEC frame of data. For the 1 Gb/s LS_TX, it takes 360 PMA_UNITDATA transfers to send an RS-FEC frame of data.

The HS_TX PCS Transmit process generates blocks based upon the TXD and TXC signals received from the XGMII. L × 30 XGMII data transfers are encoded into an RS-FEC superframe. For 2.5 Gb/s and 5 Gb/s mode associated with 100 Mb/s LS, it takes L × 1024 PMA_UNITDATA PAM2 transfers to send an RS-FEC superframe of data. For 5 Gb/s mode associated with 1 Gb/s LS and 7.5 Gb/s mode associated with 100 Mb/s LS, it takes L × 2/3 × 1024 PMA_UNITDATA PAM3 transfers to send an RS-FEC superframe of data. For 10 Gb/s mode and 7. 5 Gb/s mode associated with 1 Gb/s LS, it takes L × 1024*0.5 PMA_UNITDATA PAM4 transfers to send an RS-FEC superframe of data. Where the XGMII and PMA sublayer data rates are not synchronized, the transmit process needs to insert idles, delete idles, or delete sequence ordered sets to adapt between the rates.

The transmit process generates blocks as specified in the PCS 64B/65B Transmit state diagram (see Figure 192–20). The contents of each block are contained in a vector tx_coded<64:0>, which is passed to the RS-FEC encoder and scrambler. The bit tx_coded<0> contains the data/ctrl header and the remainder of bits contain the block payload.

#### 192.3.2.2.13 RS-FEC framing and RS-FEC encoder

Fifteen of 65B blocks (tx_coded) are grouped together to form tx_group15x65B as described in 192.1.3.1. For LS_TX transmission, tx_group15x65B, followed by the 17-bit OAM/Reserved field and 48 parity bits, forms an RS-FEC frame of 1040 bits. See Figure 192–5 and 192.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 992-bit vector, consisting of tx_group15x65B, and the 17-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

For HS_TX transmission, tx_group15x65B, followed by the 1-bit OAM/Reserved field and 48 parity bits, forms an RS-FEC frame of 1024 bits. See Figure 192–6 and 192.3.2.2.16 for details on PCS bit ordering and RS-FEC encoding. The RS-FEC encoding takes the 976-bit vector, consisting of tx_group15x65B, and the 1-bit OAM_field, and shall generate the six 8-bit parity symbols (48 bits total).

#### 192.3.2.2.14 RS-FEC superframe and round-robin interleaving

The interleaving depth, L, of the transmitter shall be predefined for each data rate and comply with Table 192–4. When L = 1, there is no interleaving and the RS-FEC superframe is the same as the RS-FEC frame. When L > 1, the round-robin interleaving scheme shown in Figure 192–8 shall be applied.

**Table 192–4—Interleaving depth**

| Transmit MAC data rate | Interleaving depth, L |
|---|---|
| 100 Mb/s | 1 |
| 2.5 Gb/s | 1 |
| 1 Gb/s, | 2 |
| 5 Gb/s | 2 |
| 7.5 Gb/s | 3 |
| 10 Gb/s | 4 |

The HS_TX PCS Transmit shall aggregate L RS-FEC input frames into an interleaved RS-FEC input superframe. There are 976 × L bits, or 122 × L Reed-Solomon message symbols in total in the input superframe. The corresponding message symbols are as follows:

$$m_{122 \times L-1}, m_{122 \times L-2}, \ldots m_1, m_0$$

These message symbols are distributed to L RS-FEC encoders. When L > 1, each RS-FEC encoder receives one out of every L message symbols from the superframe. Otherwise, the RS-FEC encoder operates exactly the same as specified in 192.3.2.2.16.

### 192.3.2.2.15 RS-FEC recombine

The L encoded RS-FEC frames are combined into an interleaved RS-FEC superframe. The output symbols are as follows:

$$m_{122 \times L-1}, m_{122 \times L-2}, \ldots, m_1, m_0, p_{1,5}, \ldots, p_{L,5}, \ldots, p_{1,0}, \ldots, p_{L,0}$$

where $p_{i,r}$ is the $r^{th}$ parity symbol of the $i^{th}$ encoder.

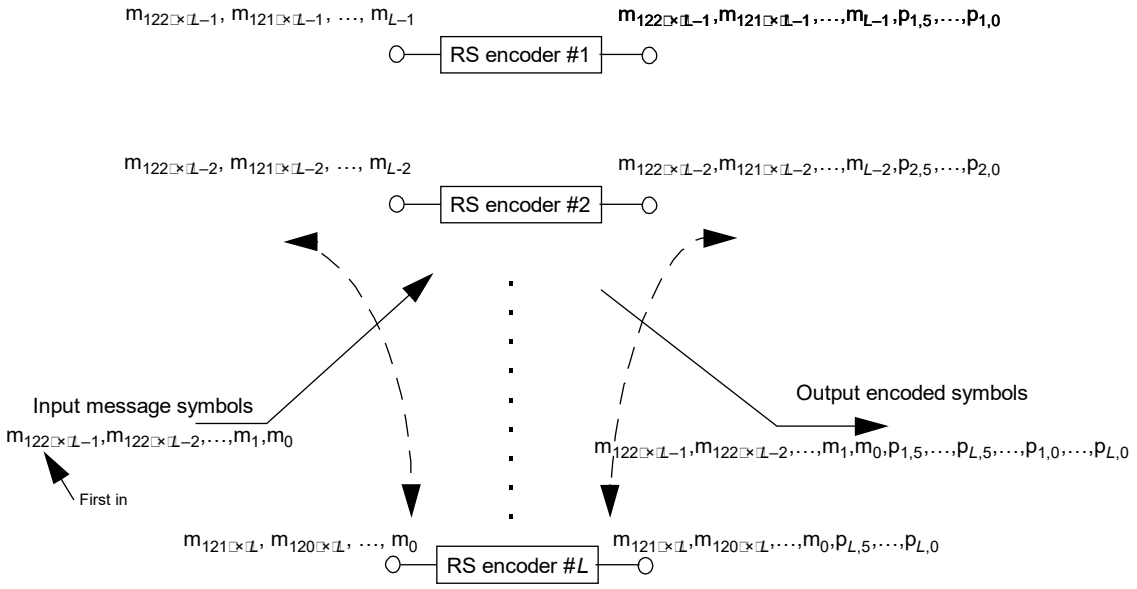



**Figure 192–8—Interleaving block diagram with interleaving depth *L***

### 192.3.2.2.16 Reed-Solomon encoder

The PCS sublayer employs a Reed-Solomon code operating over the Galois Field GF($2^8$) where the symbol size is 8 bits. For the LS_PATH, the encoder processes 124 8-bit RS-FEC message symbols to generate six 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. For the HS_PATH, the encoder processes 122 8-bit RS-FEC message symbols to generate six 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 128 8-bit RS-FEC symbols. For the purposes of this clause, the Reed-Solomon code, RS-FEC(*n*,*k*), is denoted as RS-FEC(130,124) for the LS_PATH and RS-FEC(128,122) for the HS_PATH.

The code is based on the generating polynomial shown in Equation (192–1).

(192–1)

$$g(x) = \prod_{j=0}^{n-k-1} (x - \alpha^j) = g_{n-k}x^{n-k} + g_{n-1-k}x^{n-1-k} + \ldots + g_3x^3 + g_2x^2 + g_1x + g_0$$

In Equation (192–1), $\alpha$ is a primitive element of the finite field defined by the primitive polynomial $0x11D = x^8 + x^4 + x^3 + x^2 + 1$.

Equation (192–2) defines the message polynomial $m(x)$ whose coefficients are the message symbols $m_{k-1}$ to $m_0$.

(192–2)

$$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1x^{n-k+1} + m_0x^{n-k}$$

Each message symbol $m_i$ is the bit vector ($m_{i,7}$, $m_{i,6}$, …, $m_{i,1}$, $m_{i,0}$), which is identified with the element of the finite field $m_{i,0}$ is the first bit transmitted. The message symbols are composed of the bits in tx_RSmessage<(8 × *k* – 1):0>.

For LS_TX, $m_{i,j}$ = tx_RSmessage<(123 – $i$) × 8 + $j$>, for $i$ = 0 to 123, and $i$ = 0 to 7.

tx_RSmessage<991:0> prior to RS-FEC(130,124) encoder is formed as follows:

tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<991:975> = OAM_field<16:0>.

For HS_TX, $m_{i,j}$ = tx_RSmessage<(121 – $i$) × 8 + $i$>, for $i$ = 0 to 121, and $i$ = 0 to 7.

tx_RSmessage<975:0> prior to RS-FEC(128,122) encoder is formed as follows for L = 1 (see 192.3.2.2.14):

tx_RSmessage<974:0> = tx_group15x65B<974:0>.
tx_RSmessage<975> = OAM_field<0>.

For L = 2 and L = 4, see both 192.3.2.2.14 and 192.3.2.2.15.

The first symbol input to the encoder is $m_{k-1}$.

Equation (192–3) defines the parity polynomial $p(x)$ whose coefficients are the message symbols $p_{n-k-1}$ to $p_0$.

(192–3)

$$p(x) = p_{n-k-1}x^{n-k-1} + p_{n-k-2}x^{n-k-2} + \ldots + p_2x^2 + p_1x + p_0$$

Each parity symbol $p_i$ is the bit vector ($p_{i,7}$, $p_{i,6}$, …, $p_{i,1}$, $p_{i,0}$), which is identified with the element of the finite field. $p_{i,0}$ is the first bit transmitted.

The parity polynomial is the remainder from the division of $m(x)$ by $g(x)$. This can be computed using the shift register implementation shown in Figure 192–9. The outputs of the delay elements are initialized to zero prior to the computation of the parity for a given message. After the last message symbol, $m_0$, is processed by the encoder, the outputs of the delay elements are the parity symbols for that message.

The codeword polynomial $c(x)$ is then the sum of $m(x)$ and $p(x)$ where the coefficient of the highest power of $x$ (e.g., $c_{n-1} = m_{k-1}$) is transmitted first and the coefficient of the lowest power of $x$ (e.g., $c_0 = p_0$) is transmitted last. The first bit transmitted from each symbol is bit 0.

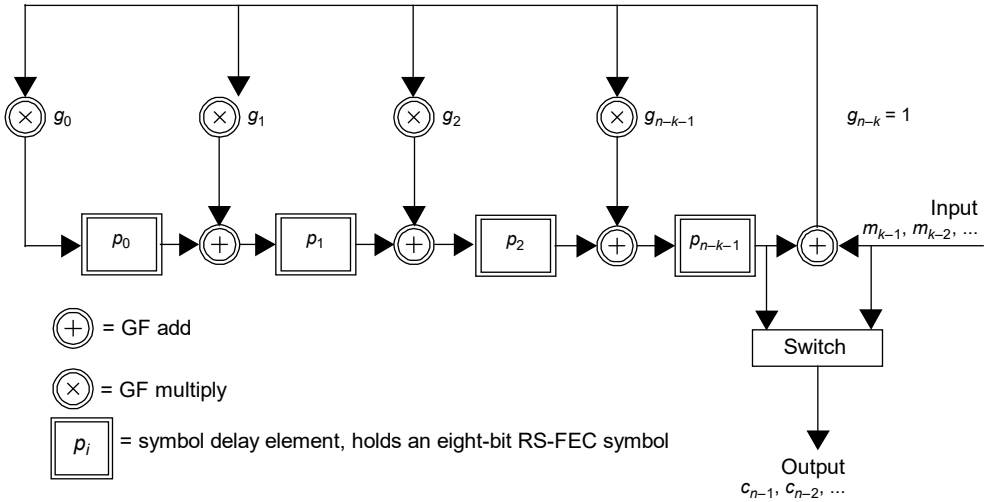



**Figure 192–9—Reed-Solomon encoder functional model**

The coefficients of the generator polynomial for the code are presented in Table 192–5

**Table 192–5—Coefficients of the generator polynomial $g_i$ (decimal)**

| *i* | RS-FEC(130,124) | RS-FEC(128,122) |
|---|---|---|
| 0 | 38 | 38 |
| 1 | 227 | 227 |
| 2 | 32 | 32 |
| 3 | 218 | 218 |
| 4 | 1 | 1 |
| 5 | 63 | 63 |
| 6 | 1 | 1 |

.

### 192.3.2.2.17 PCS scrambler

Different scramblers are used for the refresh header and for the burst payload (see 192.3.4). The scrambled refresh header data bit, $C_n$, shall be as in Equation (192–4). Refresh header data bits are mapped to PAM2 symbols for all data rates.

(192–4)

$$C_n = \begin{cases} DS_n[0] \oplus S\_t_n & \text{tx\_mode ! = SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad 0 \le n \le N\_r - 1$$

where

$DS_n[0]$ is produced using the scrambler defined in 192.3.2.2.18

For interfaces using PAM2 or PAM3 encoding (see Table 192-yy), the scrambled payload bits, $A_n$, are shown in Equation (192–5). Bit $DS_n[0]$ is produced using the scrambler defined in 192.3.2.2.19. It is applied as an additive scrambler sequence to incoming data bit Dn[0] (LSB) to generate the scrambled data bit, $A_n$.

(192–5)

$$A_n = \begin{cases} DS_n[0] \oplus S\_t_n & \text{tx\_mode ! = SEND\_N} \\ DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1$$

For 10 Gb/s interfaces and 7.5 Gb/s using PAM4 coding, the burst data bits of the interleaved RS-FEC superframe are grouped into pairs. Each pair of bits, $D_n[0]$ and $D_n[1]$, where $n$ is an index indicating the symbol number, is scrambled using an additive scrambler. For each pair of interleaved bits, two scrambler bits are generated from the PCS scrambler. The first least significant bit (LSB) is $DS_n[0]$ equal to $Scr_n[0]$. The second most significant (MSB) bit is $DS_n[1]$ equal to $Scr_n[3] \oplus Scr_n[8]$. Bits $DS_n[0]$ and $DS_n[1]$ in Equation (192–6) and Equation (192–7) are produced using the scrambler defined in 192.3.2.2.19. They are applied as additive scrambler sequences to incoming data bits $D_n[0]$ (LSB) and $D_n[1]$ (MSB) to generate two scrambled data bits $\{A_n, B_n\}$.

(192–6)

$$A_n = \begin{cases} DS_n[0] \oplus D_n[0] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1$$

(192–7)

$$B_n = \begin{cases} DS_n[1] \oplus D_n[1] & \text{tx\_mode = SEND\_N} \end{cases} \qquad N\_r \le n \le N\_r + N\_p - 1$$

### 192.3.2.2.18 PRBS11 scrambler polynomial

The refresh header specified in 192.3.4 is scrambled from the output of a pseudo-random bit sequence of order 11 (PRBS11) generator. The PRBS11 pattern generator shall produce the same result as the implementation shown in Figure 192–10. This implements the generator polynomial shown in Equation (192–8), which is the same as Equation (72–1).

(192–8)

$$G(x) = 1 + x^9 + x^{11}$$

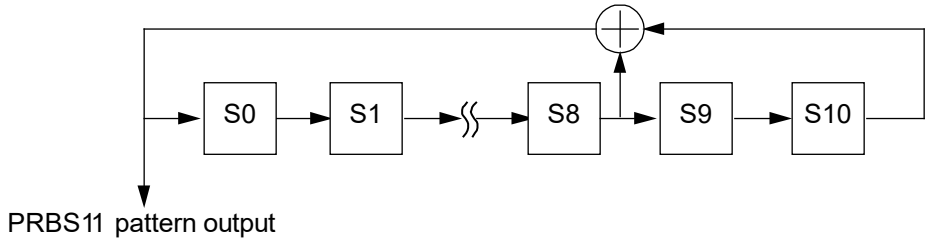



**Figure 192–10—PRBS11 pattern generator**

#### 192.3.2.2.19 PRBS33 scrambler polynomials

The PCS Transmit function employs additive scrambling. If the parameter config provided to the PCS by the PMA PHY Control function via the PMA_CONFIG.indication message assumes the value LEADER, PCS Transmit shall employ Equation (192–9) as the transmitter scrambler generator polynomial.

(192–9)

$$g_M(x) = 1 + x^{13} + x^{33}$$

If the PMA_CONFIG.indication message assumes the value FOLLOWER, PCS Transmit shall employ Equation (192–10) as the transmitter scrambler generator polynomial.

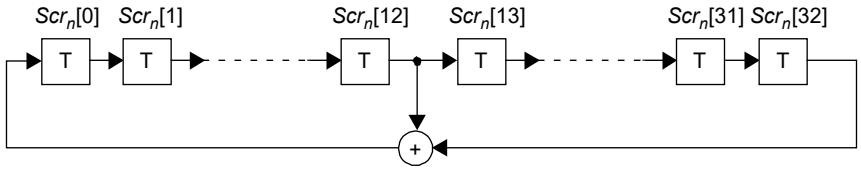
(192–10)

$$g_S(x) = 1 + x^{20} + x^{33}$$

An implementation of the LEADER PCS and FOLLOWER PCS transmitter scramblers by linear-feedback shift registers is shown in Figure 192–11. The bits stored in the shift register delay line at time *n* are denoted by $Scr_n[32:0]$. At each symbol period, the shift register is advanced by one bit, and one new bit represented by $Scr_n[0]$ is generated. The transmitter scrambler is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the 33-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case, shall the scrambler state be initialized to all zeros.

This scrambler, once started during PMA training, shall continue to run uninterrupted during the payload of PMA training frames and data mode frames and shall stop during QUIET and refresh headers.

PCS scrambler employed by the LEADER transmitter




PCS scrambler employed by the FOLLOWER transmitter

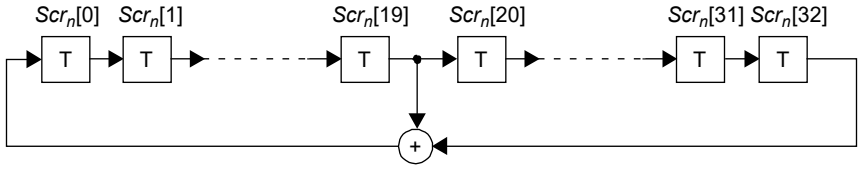



**Figure 192–11—Realization of PCS scramblers by linear feedback shift registers**

### 192.3.2.2.20 Gray mapping for PAM4 encoding

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall map consecutive pairs of bits, $\{A_n, B_n\}$, where $A_n$ is the bit arriving first, and $n$ is an index indicating the symbol number, to Gray-coded symbols, $G(n)$, with one of four levels as follows:

{0, 0} maps to 0,
{0, 1} maps to 1,
{1, 1} maps to 2, and
{1, 0} maps to 3.

When receiving at 10 Gb/s in the PAM4 transmission period, the PCS Receive process shall map Gray-coded symbols, $G(n)$, with one of four levels, to pairs of bits, $\{A_n, B_n\}$, where $A_n$ is considered to be the first bit as follows:

0 maps to {0, 0},
1 maps to {0, 1},
2 maps to {1, 1}, and
3 maps to {1, 0}.

#### 192.3.2.2.21 PAM4 encoding

When transmitting at 10 Gb/s in the PAM4 transmission period, the PCS Transmit process shall encode each Gray-coded symbol, $G(n)$, to one of four PAM4 levels as specified in this clause.

The PAM4 encoded symbols are denoted $M(n)$, where $n$ is an index indicating the symbol number.

Each consecutive Gray-coded symbol, $G(n)$, is mapped to one of four PAM4 levels and assigned to the PAM4 encoder output, $M(n)$.

Mapping from the Gray-coded symbol, $G(n)$, to a PAM4 encoded symbol, $M(n)$, is as follows:

0 maps to –1,
1 maps to –1/3,
2 maps to +1/3, and
3 maps to +1.

#### 192.3.2.2.22 PAM3 encoding

[Note to Editor: Renumber the clauses]

3B2T encoding is used to map a group of three consecutive bits into a consecutive pair of three-level (ternary) PAM3 symbols. When transmitting at 7.5 Gb/s or 5 Gb/s in the PAM3 transmission period (see Table 192-yy), the PCS Transmit process encodes each of the two PAM3 symbols in the pair T(n+1), T(n) into the appropriate PAM3 level.

The 3B2T mapping into PAM3 symbols is shown in Table 192-zz. B[0] is the first of the three bits received by the mapper (i.e., the LSB of the trio) and T[0] is the first PAM3 symbol of the pair to be transmitted.

**Table 192-zz – 3B2T mapping**

| Three-bit groups B[2], B[1], B[0] | PAM3 symbol pairs T[1], T[0] |
|---|---|
| 000 | -1,-1 |
| 001 | 0,-1 |
| 010 | -1,0 |
| 011 | -1,+1 |
| 100 | +1,0 |
| 101 | +1, -1 |
| 110 | +1,+1 |
| 111 | 0,+1 |

#### 192.3.2.2.22 PAM2 mapping

During the PAM2 transmission period, the PCS Transmit process sends out PAM2 symbols according to following mapping:

Input bit $S_n$ is mapped to the transmit symbol $T_n$ as follows: if $S_n = 0$, then $T_n = +1$, if $S_n = 1$, then $T_n = –1$.

### 192.3.2.3 PCS Receive function

The PCS Receive function shall conform to the PCS 64B/65B Receive state diagram in Figure 192–21 and the PCS Receive bit ordering in Figure 192–12 for the LS_RX and Figure 192–13 for the HS_RX, including compliance with the associated state variable as specified in 192.3.5.1.2.

The PCS Receive function accepts received symbols provided by the PMA Receive function via the parameter rx_symb. The PCS receiver uses knowledge of the encoding rules and PMA training alignment to correctly align the 65B RS-FEC frames. The received PAM2, PAM3 or PAM4 symbols are demapped and descrambling is performed.

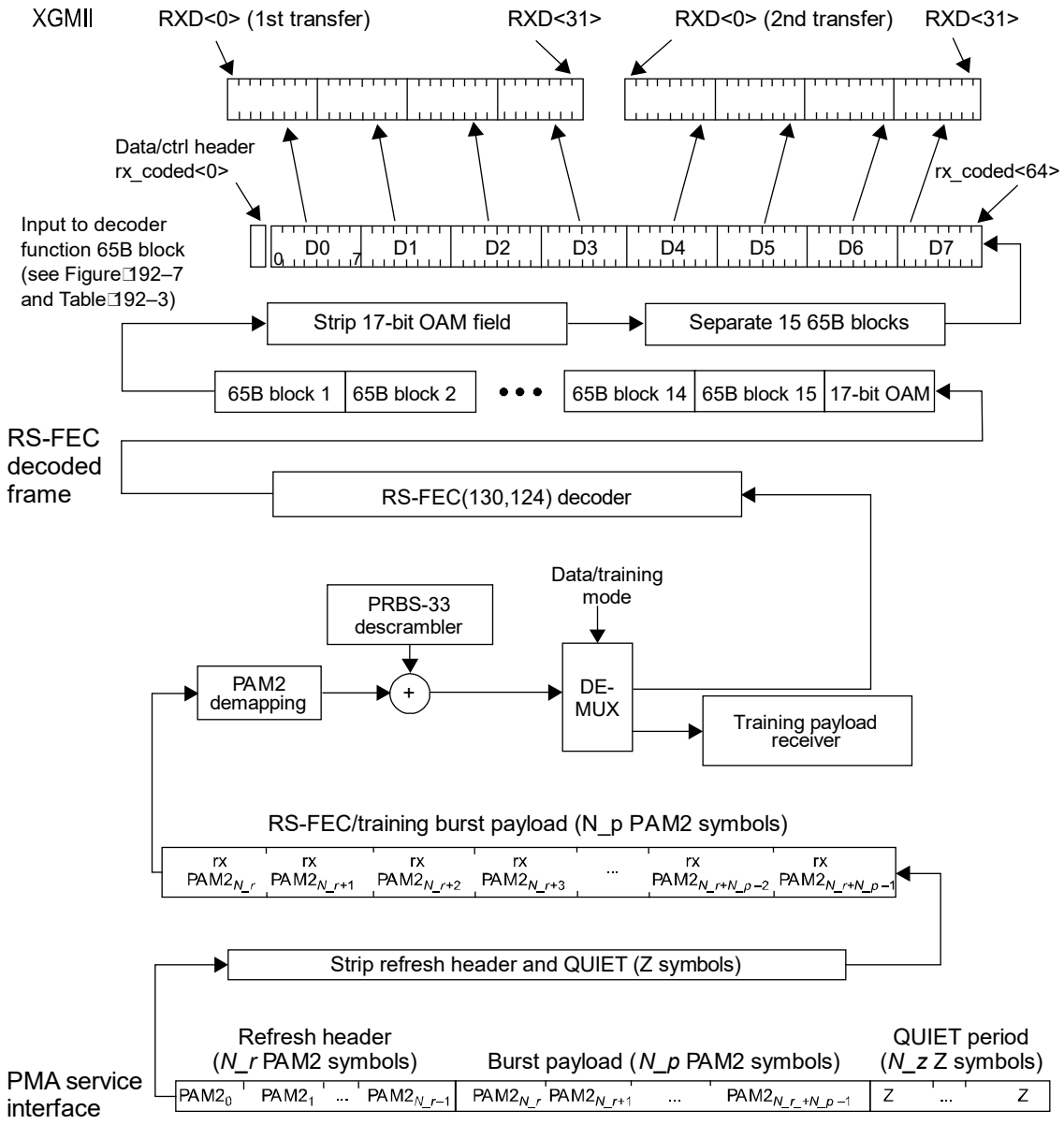
Following descrambling, the *L*-interleaved RS-FEC superframe is de-interleaved and the Reed-Solomon frames are decoded with Reed-Solomon error correction. Frames that cannot be corrected are marked with error symbols by the decoder. For 100 Mb/s LS_RX, the RS-FEC decoded frame is then separated into a 17-bit OAM field and 15 64B/65B blocks. For 1 Gb/s LS_RX, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks for 12 superframes with a 12-bit OAM field. For HS_RX, the RS-FEC decoded frame is then separated into a 1-bit OAM field and 15 64B/65B blocks. In each data payload, the 25 superframes can form a 25-bit OAM field for 2.5 Gb/s mode, a 50-bit OAM field for 5 Gb/s mode when associated with 100 Mb/s LS, a 54-bit OAM field for 5 Gb/s mode when associated with 1 Gb/s LS, a 75-bit OAM field for 7.5 Gb/s mode when associated with 100 Mb/s LS, a 78-bit OAM field for 7.5 Gb/s mode when associated with 1 Gb/s LS and a 100-bit OAM field for 10 Gb/s mode.

Groups of 15 64/65B blocks are then separated into individual 64/65B blocks. The PCS Receive function generates the 64B/65B block vector rx_coded <64:0>, which is then decoded to form the XGMII signals RXD<31:0> and RXC<3:0> as specified in the PCS 64B/65B Receive state diagram (see Figure 192–21). Two XGMII data transfers are decoded from each block. Because the received data stream is divided into TDD bursts with silence interspersed, the PCS receive function recombines separated bursts before passing to the XGMII. When the XGMII and PMA sublayer data rates are not frequency synchronized, the PCS receive process inserts idles, deletes idles, or deletes sequence ordered sets to adapt between rates.

During PMA training mode, PCS Receive checks the received PAM2 framing and signals the reliable acquisition of the descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK.

When the PCS Synchronization process has obtained synchronization, the RS-FEC frame error ratio (RFER) monitor process monitors the signal quality and asserts hi_rfer to indicate excessive RS-FEC frame errors. If 40 consecutive RS-FEC frame errors are detected, the block_lock flag is de-asserted. The block_lock flag is re-asserted upon detection of a valid RS-FEC frame. When block_lock is asserted and hi _rfer is de-asserted, the PCS Receive process continuously accepts blocks. The PCS Receive process monitors these blocks and generates RXD <31:0> and RXC <3:0> on the XGMII.

When the receiver is in training mode, the PCS Synchronization process continuously monitors PMA_RXSTATUS.indication(loc_rcvr_status). When loc_rcvr_status indicates OK, then the PCS Synchronization process accepts data-units via the PMA_UNITDATA.indication primitive. It attains frame and block synchronization based on the PMA training frames and conveys received blocks to the PCS Receive process when PHY Control is in PCS_TEST or PCS_DATA state. The PCS Synchronization process sets the block_lock flag to indicate whether the PCS has obtained synchronization. The PMA training frame includes a refresh header (see 192.3.4). It also includes training payload which has an Infofield, inserted in the $N\_inf^{th}$ bit of the training payload (see 192.3.4.3). When the PCS Synchronization process is synchronized to this pattern, block_lock is asserted.




NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

**Figure 192–12—1S_RX PCS Receive bit ordering**

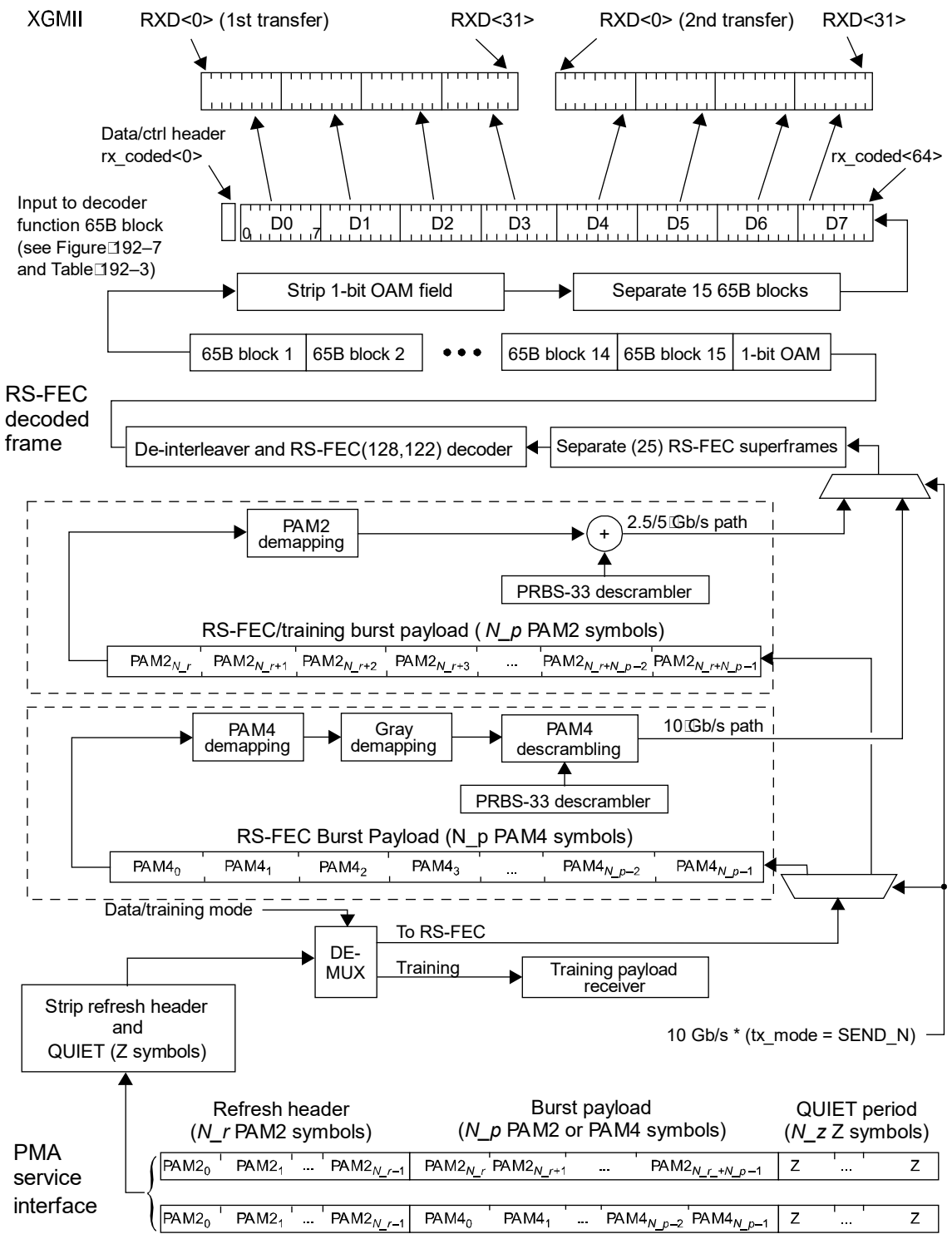
[Note to Editor: A separate version of the figure should be added for the 1 Gb/s LS. Putting both in the same figure could be confusing to the reader. The edits to current Figure 192-5 to create the 1 Gb/s version are as follows:

1. Replace "RS-FEC(130,124) decoder" with "De-interleaver and RS-FEC(128-122) decoder"

2. Add a "Separate (6) RS-FEC superframes" block ahead of the De-interleaver and RS-FEC decoder block

3. The output of the RS-FEC decoder is fifteen 65B blocks, 1 OAM bit and a 48-bit parity (i.e., similar to what's in Figure 192-13 with the same RS-FEC),

4. If the PMA service interface is retained in these figures, it should be re-drawn similar to Figure 192-13.]




NOTE 1—This figure shows the mapping from a 64B/65B block to the XGMII for a block containing eight data characters.

NOTE 2—Figure shown for $L = 1$.

NOTE 3—Either the PAM2 or PAM4 path and TDD frame at the PMA service interface is used. PAM4 path (and the lower TDD frame shown) is chosen if the bit rate is 10 Gb/s and tx_mode = SEND_N.

**Figure 192–13—SB_RX PCS Receive bit ordering**

[Note to Editor: It is probably best to add the changes associated with 1 Gb/s LS in a separate figure that can be prepared as a D2.1 comment.

#### 192.3.2.3.1 Frame and block synchronization

When operating in 100 Mb/s, 2.5 Gb/s, 5 Gb/s data mode, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from $PAM2_{N\_r}$ to $PAM2_{N\_r + N\_p - 1}$ (see Figure 192–12 for LS_RX or Figure 192–13 for HS_RX). When operating in 10 Gb/s data mode, the receiving PCS shall concatenate rx_symb values conveyed by the PMA_UNITDATA.indication during the burst payload in order from $PAM4_0$ to $PAM4_{N\_p-1}$ (see Figure 192–13).

The receiving PCS obtains block_lock to the PHY frames during training using synchronization sequence and Infofield provided in the training frames.

#### 192.3.2.3.2 PCS descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. The PCS descrambles the data stream and returns the proper sequence of symbols to the decoding process for generation of RXD<31:0> to the XGMII. For descrambling, the LEADER PHY shall employ the receiver descrambler generator polynomial per Equation (192–10) and the FOLLOWER PHY shall employ the receiver descrambler generator polynomial per Equation (192–9).

#### 192.3.2.3.3 Invalid blocks

A block is invalid if any of the following conditions exist:

a) The block type field contains a reserved value.
b) Any control character contains a value not in Table 192–3.
c) Any O code contains a value not in Table 192–3.
d) The block contains information from the payload of an invalid RS-FEC frame.

The PCS Receive function shall check the integrity of the RS-FEC parity bits defined in 192.3.2.2.13. If the check fails, the RS-FEC frame is invalid. The R_BLOCK_ TYPE of an invalid block is set to E.

### 192.3.3 Test-pattern generators

The test-pattern generator mode is provided for enabling joint testing of the local transmitter, channel, and remote receiver.

When the transmit PCS is operating in test-pattern mode, the input to the RS-FEC encoder (see Figure 192–5 or Figure 192–6) is set to zero and the initial condition of the PCS scrambler set to any non-zero value. This has the same effect as setting the input to the PCS scrambler to zero.

When the receiver PCS is operating in test-pattern mode, the received information is processed as shown in Figure 192–12 or Figure 192–13. In the absence of errors in PMA Receive, the descrambler output should be zeros. The output of the RS-FEC decoder should also be zeros, and may correct errors in the descrambler output. Any nonzero values at the output of the RS-FEC decoder are due to uncorrectable RS-FEC frames. This mode is further described as test mode 7 in 192.5.1.

### 192.3.4 PCS TDD signaling

The PCS generates symbols to be transmitted by the PMA in the form of TDD bursts. TDD burst structure depends on the value of tx_mode and the data rate of transmission. Each TDD burst is comprised of a refresh header and payload followed by a QUIET period. During startup, the PCS transmits TDD bursts in two different formats for the tx_mode values SEND_TS and SEND_TA, before finally switching to SEND_N. SEND_TS uses a symmetric frame format and shall transmit at 3 GBd. PHY data rate and direction may be negotiated during the SEND_TS phase. SEND_TA and SEND_N use an asymmetric frame format, and transmit at either 3 GBd or 6 GBd depending on the selected transmitter rate. QUIET periods (i.e., when the PCS inserts Z symbols) are introduced between TDD bursts. The duration of each QUIET period depends on the state of tx_mode.

The refresh header is a sequence of PAM2 symbols with length of *N_r* symbols. The refresh header bits are all zeros except for the final 64 bits (see 192.3.4.2).

An 11-bit scrambler (see 192.3.2.2.18) is used to scramble the refresh header. This scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

The burst payload is a sequence of symbols with length of *N_p* symbols.

The training payload data sequence bits are all zeros, with the exception of a 96-bit Infofield started at the $N\_inf^{th}$ symbol of the training payload (see Figure 192–14). The Infofield is used to exchange messages between link partners during startup. The training data sequence, $S\_t_n$, is defined in Equation (192–11). Training payloads are sent when tx_mode is SEND_TS or SEND_TA.

The data mode burst payload consists of RS-FEC superframes that are sent when tx_mode is SEND_N.

The 33-bit scrambler (see 192.3.2.2.19) is used to scramble the payload. Once started at the beginning of the training payload of the first training burst, this scrambler shall continue to run uninterrupted for each symbol during all subsequent payloads and shall maintain its last state during the QUIET period and refresh headers.

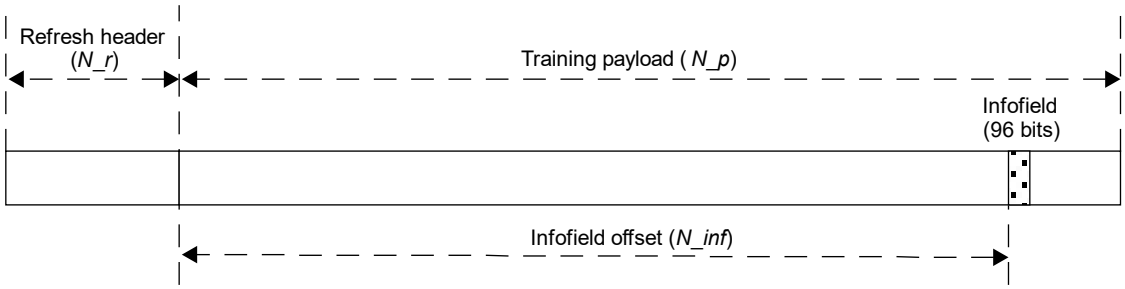
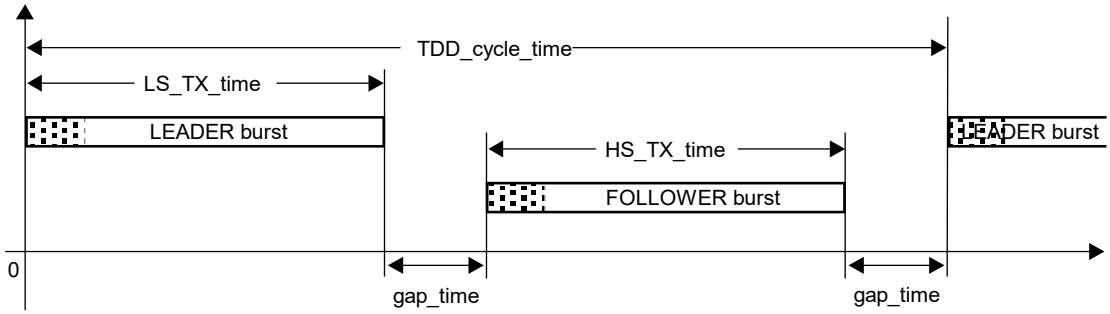



**Figure 192–14—PMA Training frame**

The timing diagram in Figure 192–15 shows the TDD cycle signaling and TDD frame structures assuming the LS_TX is configured as the LEADER and the HS_TX is configured as the FOLLOWER. Table 192–6 specifies the LS_TX and HS_TX transmit times in each TDD cycle.




NOTE 1—TDD_cycle_time is the nominal 9.6µs TDD cycle time.

NOTE 2—gap_time is the time between the start of QUIET at one MDI output and end of QUIET at the other MDI output. gap_time is a result of the alignment of the two ends, so is not specified.

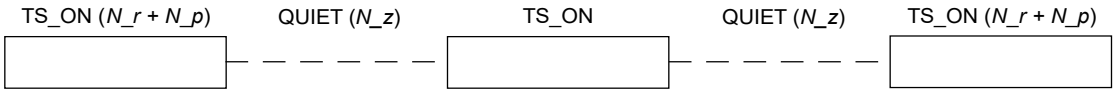
**Figure 192–15—FOLLOWER/LEADER TDD cycle illustration**

**Table 192–6—TDD cycle timing**

| tx_mode | LS_TX_time (ns) | HS_TX_time (ns) | Total gap_time per cycle (ns) | TDD cycle time (ns) |
|---|---|---|---|---|
| SEND_TS | 4480 | 4480 | 640 | 9600 |
| SEND_TA | 554.67 | 8693.33 | 352 | |
| SEND_N | | | | |

[Note to Editor: Update the table above to add SEND_TA and SEND_N values for the case when 1 Gb/s is selected. HS_TX_time is 6949.33 ns and LS_TX_time is 2298.66 ns.

The symmetric training burst timing and structure are shown in Figure 192–16. TS_ON indicates a symmetric training burst and QUIET (*N_z)* indicates the QUIET period between bursts when Z symbols are transmitted by the PHY




NOTE—The parameters for SEND_TS are used for *N_r*, *N_p*, and *N_z* (see Table 192–7, Table 192–8, and Table 192–9).

**Figure 192–16—Symmetric training timing and frame structure**

Figure 192–17 shows the LS_TX timing and frame structure for both the data mode and the asymmetric training modes. TA_ON indicates an asymmetric training burst and QUIET (*N_z)* indicates the QUIET period between bursts when Z symbols are transmitted by the PHY. The refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 192.3.4. Note that FEC is not used with the training payload.

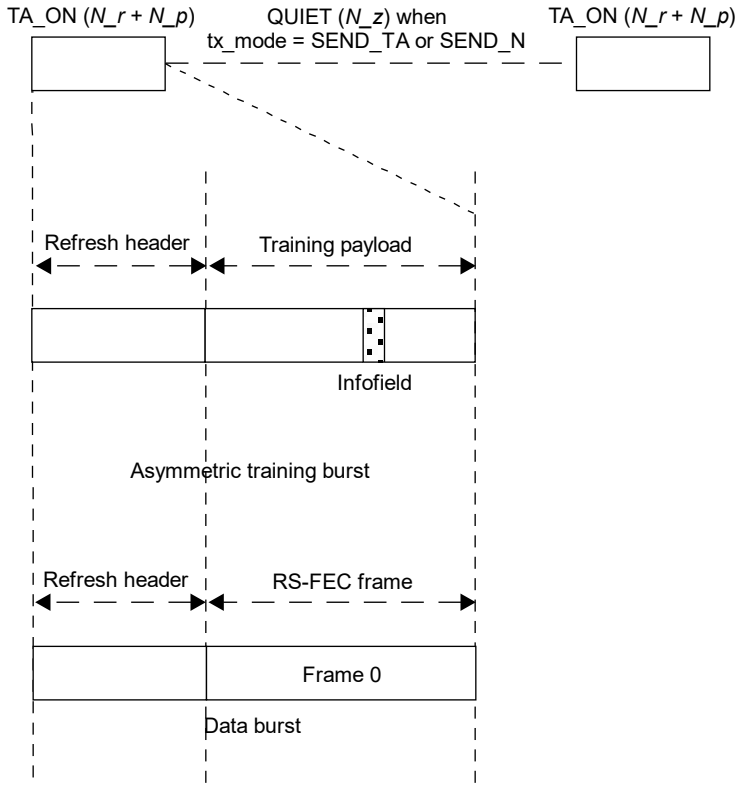



**Figure 192–17—Asymmetric training/Data Mode timing and frame structure—LS_TX**

Figure 192–18 shows the HS_TX timing and frame structure for both the data mode and the asymmetric training modes. As with the LS_TX direction, the refresh header at the beginning of the data mode burst is the same as the one defined for all training bursts in 192.3.4 and FEC is not used with the training payload.

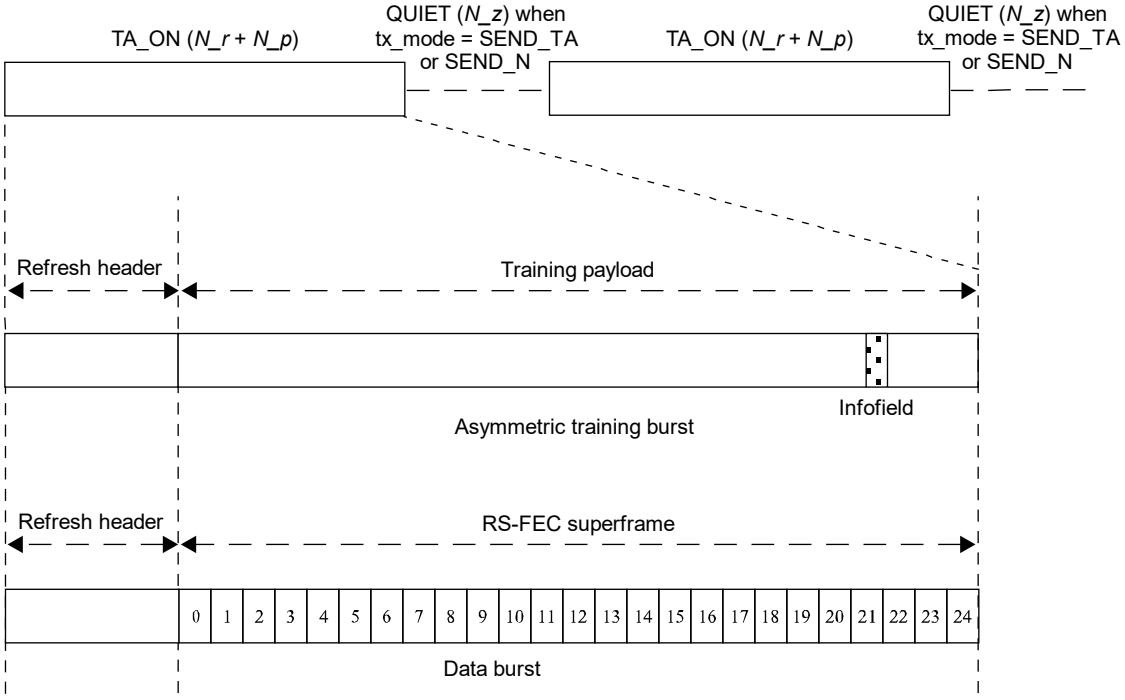
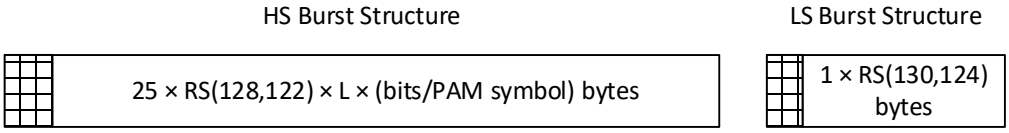



**Figure 192–18—Asymmetric training/Data Mode timing and frame structure—HS_TX**

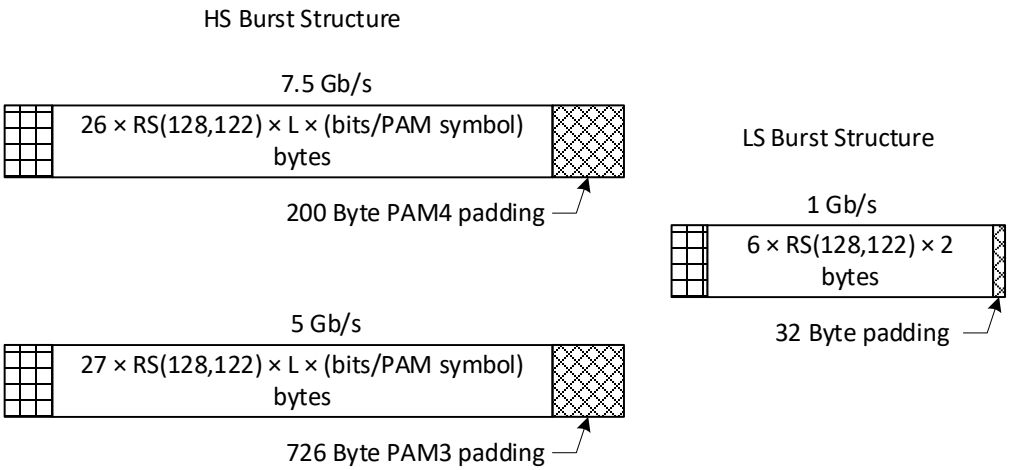
*[Note to Editor: Remove the 25-FEC superframe block structure from within the Data burst payload and add the following new figure:]*

The burst payload structures are illustrated in Figure 192-hh, with the data burst payload information summarized in Table 192-h. The data burst structures associated with 1 Gb/s LS include padding in the data burst payload area and

there is capacity remaining in the last RS-FEC block of the data payload area. The content of the unused RS-FEC block payload bits and the padding fields are user defined and outside the scope of IEEE 802.3.




***a) Burst structures with 100 Mb/s LS rate***




***b) Burst structures with 1 Gb/s LS rate***

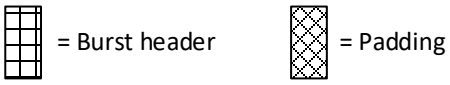



**Figure 192-hh – Illustration of the data burst payload structure**

**Table 192-hh - Table 192-hh – Data burst payload summary information**

| HS Payload | | | | | LS Payload | | | | |
|---|---|---|---|---|---|---|---|---|---|
| BPS | Baud | PAM | L | # symbols | BPS | Baud | PAM | L | # symbols |
| 2.5 G | 3 G | 2 | 1 | 25 600 | 100 M NOTE 1 | 3 | 2 | 1 | 1040 |
| 5 G | 6 G | 2 | 2 | 51 200 | | | | | |
| 7.5 G | | 3 | 3 | | | | | | |
| 10 G | | 4 | 4 | | | | | | |
| 5 G | 6 G | 3 | 2 | 40 736* | 1 G NOTE 2 | 6 | 2 | 2 | 12 544* |
| 7.5 G | | 4 | 3 | 40 736* | | | | | |
| * Including padding | | | | | | | | | |

### 192.3.4.1 Refresh header, payload, and QUIET period length

The lengths for refresh header (*N_r*) and payload (*N_p*) are described in Table 192–7, Table 192–8, and Table 192–9. The length of the QUIET period (*N_z*) in Table 192–7, Table 192–8, and Table 192–9 is the number of Z symbols sent to complete the TDD cycle

**Table 192–7—*N_r, N_p, and N_z* values for 100 Mb/s mode transmission**

| tx_mode | refresh header *N_r* (symbols) | payload *N_p* (symbols) | QUIET *N_z* (symbols) |
|---|---|---|---|
| SEND_TS | 560 | 12 880 | 15 360 |
| SEND_TA | 624 | 1040 | 27 136 |
| SEND_N | 624 | 1040 | 27 136 |
| NOTE—All symbols are sent at 3 GBd. | | | |

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**Table 192–7—*N_r, N_p, and N_z* values for 1 Gb/s mode transmission**

| tx_mode | refresh header *N_r* (symbols) | payload *N_p* (symbols) | QUIET *N_z* (symbols) |
|---|---|---|---|
| SEND_TS | 560 | 12 880 | 15 360 |
| SEND_TA | 1248 | 12 544 | 43 808 |
| SEND_N | 1248 | 12 544 | 43 808 |
| NOTE—All SEND_TS symbols are sent at 3 GBd, SEND_TA and SEND_N symbols during the burst payload are sent at 6 GBd. | | | |

**Table 192–7—*N_r, N_p, and N_z* values for 5 Gb/s+1 Gb/s and 7.5 Gb/s+1 Gb/s mode transmission**

| tx_mode | refresh header *N_r* (symbols) | payload *N_p* (symbols) | QUIET *N_z* (symbols) |
|---|---|---|---|
| SEND_TS | 560 | 12 880 | 15 360 |
| SEND_TA | 960 | 40 736 | 15 904 |

| | | | |
|---|---|---|---|
| SEND_N | 960 | 40 736 | 15 904 |
| NOTE—All SEND_TS symbols are sent at 3 GBd, SEND_TA and SEND_N symbols during the burst payload are sent at 6 GBd. | | | |

.

**Table 192–8—*N_r*, *N_p, and N_z* values for 2.5 Gb/s mode transmission**

| tx_mode | refresh header *N_r* (symbols) | payload *N_p* (symbols) | QUIET *N_z* (symbols) |
|---|---|---|---|
| SEND_TS | 560 | 12 880 | 15 360 |
| SEND_TA | 480 | 25 600 | 2720 |
| SEND_N | 480 | 25 600 | 2720 |
| NOTE—All symbols are sent at 3 GBd. | | | |

**Table 192–9—*N_r*, *N_p, and N_z* values for 5 Gb/s, 7.5 Gb/s, and 10 Gb/s mode transmission**

| tx_mode | refresh header *N_r* (symbols) | payload *N_p* (symbols) | QUIET *N_z* (symbols) |
|---|---|---|---|
| SEND_TS | 560 | 12 880 | 15 360 |
| SEND_TA | 960 | 51 200 | 5440 |
| SEND_N | 960 | 51 200 | 5440 |
| NOTE—SEND_TS symbols are sent at 3 GBd. SEND_TA and SEND_N symbols are sent at 6 GBd. | | | |

#### 192.3.4.2 Refresh header and payload data bits generation

The refresh header shall be composed of a leading sequence of zeros followed by four bytes of 0x01, followed by four bytes of 0xF0. The refresh header bits are scrambled with the PRBS11 scrambler defined in 192.3.2.2.18. The PRBS11 scrambler stops at the end of the refresh header and resumes at the beginning of the next refresh header.

*N_p* payload bits follow the refresh header in each burst. The payload bits are scrambled with the PRBS33 scrambler defined in 192.3.2.2.19.

The training frame contents are specified in Equation (192–11). *N_inf* is the bit position where Infofield starts within the training payload. The training frame starts at bit zero, with $0 \le n \le N\_r - 1$ consisting of the refresh header as shown in Equation (192–11). Per Equation (192–11), $S\_t_n$ is all zeros from the end of the refresh header to the beginning of the Infofield, followed by the 96-bit Infofield, then followed by all zeros from the end of the Infofield to the end of the training payload, which is the end of the training frame.

(192–11)

$$S\_t_n = \begin{cases} refresh\_header(n) & 0 \le n \le N\_r - 1 \\ 0 & N\_r \le n \le N\_r + N\_inf - 1 \\ Infofield(n - [N\_r + N\_inf]) & N\_r + N\_inf \le n \le N\_r + N\_inf + 95 \\ 0 & N\_r + N\_inf + 96 \le n \le N\_r + N\_p - 1 \end{cases}$$

where

*N_inf* is equal to $N\_p - 256$

### 192.3.4.3 PAM mapping and generation of TDD bursts

Except when transmitting 10 Gb/s, 7.5 Gb/s or , or 5 Gb/s associated with 1 Gb/s LS, payload symbols and tx_mode is SEND_N, bits are encoded by the PAM2 mapper defined in 192.3.2.2.23. When transmitting 5 Gb/s payload symbols associated with 1 Gb/s LS, tx_mode is SEND_N bits are encoded by the PAM3 encoder defined in 192.3.2.2.22. When transmitting 10 Gb/s payload symbols, or 7.5 Gb/s associated with 1 Gb/s LS, and tx_mode is SEND_N, bits are encoded by the Gray-coded PAM4 encoder defined in 192.3.2.2.20 and 192.3.2.2.21. Z symbols are sent between each TDD burst frame to form the sequence $O_n$, as defined in Equation (192–12). The values of $O_n$ are then conveyed to the PMA for transmission via the parameter tx_symb of the PMA_UNITDATA.request primitive.

The transmit symbol $O_n$ is selected by TDD control logic. For each TDD cycle (specified in 192.3.4), the Transmit function will send out $T_n$ or Z symbols to the PMA, based on symbol time index *n*.

$$O_n = \begin{cases} T_n & 0 \le n \le N\_r + N\_p - 1 \\ \text{Z} & N\_r + N\_p \le n \le N\_TDD - 1 \end{cases}$$

(192–12)

where

*n* is the continuous symbol count modulo *N_TDD*
*N_TDD* is the number of symbols equivalent to a nominal 9.6 µs TDD cycle time

$T_n$ is the output of the PAM2, PAM3, or PAM4 Mapper as defined in Equation (192–13).

(192–13)

$$T_n = \begin{cases} PAM2\_Mapper(A_n) & !(\text{tx\_rate} = 10\ \text{Gb/s AND tx\_mode} = \text{SEND\_N}) \text{ OR} \\ & (0 \le n \le N\_r - 1) \\ PAM4\_Mapper(G_n) & (\text{tx\_rate} = 10\ \text{Gb/s AND tx\_mode} = \text{SEND\_N}) \text{ AND} \\ & (N\_r \le n \le N\_r + N\_p - 1) \end{cases}$$

Note to Editor:
Change the PAM2_Mapper(An) conditions to be "!(tx_rate = 10 Gb/s AND tx_mode = SEND_N) OR

!(tx_rate = 7.5 Gb/s AND tx_mode = SEND_N) OR !(tx_rate = 5 Gbs AND LS rx_rate = 1 Gb/s AND SEND_N) OR …
Add row "PAM3_Mapper(An) conditions to be "(tx_rate = 7.5 Gb/s AND LS tx_rate = 100 Mb/s AND tx_mode = SEND_N) OR (tx_rate = 5 Gb/s AND rx_rate = 1 Gb/s AND tx_mode = SEND_N) OR (0<= n <= N_r-1)"
Change the PAM4_Mapper(Gn) conditions to be "tx_mode = SEND_N AND (tx_rate = 10 Gb/s OR tx_rate = 7/5 Gb/s AND rx_rate = 1 Gb/s) AND …

where

| | |
|---|---|
| *PAM2_Mapper* | is specified in 192.3.2.2.23 |
| *PAM3_Mapper* | is specified in 192.3.2.2.22 |
| *PAM4_Mapper* | is specified in 192.3.2.2.21 |
| tx_rate | is the selected transmit data rate |

#### 192.3.4.4 PCS descrambler polynomials

The PCS shall acquire descrambler state synchronization to the PAM2 training sequence and report success through scr_status, and continue to use the synchronized state in all subsequent bursts in both data and training modes. The FOLLOWER PCS employs the receiver descrambler generator polynomial per Equation (192–9) and the LEADER PCS employs the receiver descrambler generator polynomial per Equation (192–10).

### 192.3.5 PCS Detailed functions and state diagrams

#### 192.3.5.1 State diagram parameters

##### 192.3.5.1.1 Constants

EBLOCK_R<71:0>
72-bit vector to be sent to the XGMII interface containing /E/ in all the eight character locations.

EBLOCK_T<64:0>
65-bit vector to be sent to the RS-FEC encoder containing /E/ in all the eight character locations.

LBLOCK_R<71:0>
72-bit vector to be sent to the XGMII interface containing two Local Fault ordered sets. The Local Fault ordered set is defined in 46.3.4.

LBLOCK_T<64:0>
65-bit vector to be sent to the RS-FEC encoder containing two Local Fault ordered sets.

IBLOCK_R<71:0>
72-bit vector to be sent to the XGMII containing /I/ in all the eight character locations.

IBLOCK_T<64:0>
65-bit vector to be sent to the RS-FEC encoder containing /I/ in all the eight character locations.

RFER_CNT_LIMIT
TYPE: Integer
VALUE: 16
Number of Reed-Solomon frames with uncorrectable errors.

RFRX_CNT_LIMIT
TYPE: Integer

VALUE: 88
Number of Reed-Solomon frames received over bit error ratio interval.

UBLOCK_R<71:0>
72-bit vector to be sent to the XGMII containing two Link Interruption ordered sets. The Link Interruption ordered set is defined in 46.3.4.

#### 192.3.5.1.2 Variables

block_lock
Boolean variable that is set TRUE when receiver acquires block delineation.

hi_rfer
Boolean variable that is asserted TRUE when the rfer_cnt reaches 16 errors in one rfer_timer interval.

pcs_data_mode
Variable set by the PMA PHY Control function. See 192.4.4.1.

pcs_reset
Boolean variable that controls the resetting of the PCS. It is TRUE whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

rf_valid
Boolean indication that is set TRUE if received Reed-Solomon frame is valid. Reed-Solomon frame is valid if and only if all parity checks of the Reed-Solomon code are satisfied.

rs_fec_frame_done
A Boolean value. This variable is set TRUE when the final symbol of each RS-FEC frame is transmitted. It is set FALSE otherwise.

rx_coded<64:0>
Vector containing the input to the 64B/65B decoder. The format for this vector is shown in Figure 192–7. The leftmost bit in the figure is rx_coded<0> and the rightmost bit is rx_coded<64>.

rx_raw<71:0>
Vector containing two successive XGMII output transfers. RXC<3:0> for the first transfer are taken from rx_raw<3:0>. RXC<3:0> for the second transfer are taken from rx_raw<7:4>. RXD<31:0> for the first transfer are taken from rx_raw<39:8>. RXD<31:0> for the second transfer are taken from rx_raw<71:40>.

tx_coded<64:0>
Vector containing the output from the 64B/65B encoder. The format for this vector is shown in Figure 192–7. The leftmost bit in the figure is tx_coded<0> and the rightmost bit is tx_coded<64>.

tx_raw<71:0>
Vector containing two successive XGMII transfers. TXC<3:0> for the first transfer are placed in tx_raw<3:0>. TXC<3:0> for the second transfer are placed in tx_raw<7:4>. TXD<31:0> for the first transfer are placed in tx_raw<39:8>. TXD<31:0> for the second transfer are placed in tx_raw<71:40>.

#### 192.3.5.1.3 Functions

DECODE(rx_coded<64:0>)
In the PCS Receive process, this function takes as its argument 65-bit rx_coded<64:0> from the RS-FEC

decoder and decodes the 65B RS-FEC bit vector returning a vector rx_raw<71:0>, which is sent to the XGMII. The DECODE function shall decode the block based on code specified in 192.3.2.2.4.

ENCODE(tx_raw<71:0>)

Encodes the 72-bit vector received from the XGMII, returning 65-bit vector tx_coded. The ENCODE function shall encode the block as specified in 192.3.2.2.4.

R_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x1E and seven valid control characters other than /E/;

b) A block type field 0x2D or 0x4B, a valid O code, and four valid control characters;

c) A block type field of 0x55 and two valid O codes.

S; The vector contains a data/ctrl header of 1 and one of the following:

a) A block type field of 0x33 and four valid control characters;

b) A block type field of 0x66 and a valid O code;

c) A block type field of 0x78.

T; The vector contains a data/ctrl header of 1, a block type field of 0x87, 0x99, 0xAA, 0xB4, 0xCC, 0xD2, 0xE1 or 0xFF and all control characters are valid.

D; The vector contains a data/ctrl header of 0.

E; The vector does not meet the criteria for any other value.

A valid control character is one containing a control code specified in Table 192–3. A valid O code is one containing an O code specified in Table 192–3.

R_TYPE(rx_coded<64:0>)

Returns the R_BLOCK_TYPE of the rx_coded<64:0> bit vector.

R_TYPE_NEXT

Prescient end of packet check function. It returns the R_BLOCK_TYPE of the rx_coded vector immediately following the current rx_coded vector.

T_BLOCK_TYPE = {C, S, T, D, E}

Every case of the vector belongs to only one type.

Values: C; The vector contains one of the following:

a) Eight valid control characters other than /O/, /S/, /T/, /E/;

b) One valid ordered set and four valid control characters other than /O/, /S/, and /T/;

c) Two valid ordered sets.

S; The vector contains an /S/ in its first or fifth character. Any characters before the S character are valid control characters other than /O/, /S/ and /T/ or form a valid ordered set, and all characters following the /S/ are data characters.

T; The vector contains a /T/ in one of its characters, all characters before the /T/ are data characters, and all characters following the /T/ are valid control characters other than /O/, /S/ and /T/.

D; The vector contains eight data characters.

E; The vector does not meet the criteria for any other value.

A tx_raw character is a control character if its associated TXC bit is asserted. A valid control character is one containing an XGMII control code specified in Table 192–3. A valid ordered set consists of a valid /O/ character in the first or fifth characters and data characters in the three characters following the /O/. A valid /O/ is any character with a value for O code in Table 192–3.

T_TYPE(tx_raw<71:0>)

Returns the T_BLOCK_TYPE of the tx_raw<71:0> bit vector.

#### 192.3.5.1.4 Counters

rfer_cnt

Count up to a maximum of RFER_CNT_LIMIT of the number of invalid Reed-Solomon frames within the current RFRX_CNT_LIMIT Reed-Solomon frame period.

rfrx_cnt

Count number Reed-Solomon frames received during current period.

#### 192.3.5.1.5 Messages

RX_FRAME
: A signal sent to PCS Receive indicating that a full Reed-Solomon frame has been decoded and the variable rf_valid is updated.

### 192.3.5.2 State diagrams

The RFER monitor state diagram shown in Figure 192–19 monitors the received signal for high RS-FEC frame error ratio.

The PCS 64B/65B Transmit state diagram shown in Figure 192–20 controls the encoding of 65B transmitted blocks. It makes exactly one transition for each 65B transmit block processed. Though the state diagram sends Local Fault ordered sets when reset is asserted, the PCS scrambler and 65B RS-FEC are not guaranteed to be operational during reset. Thus, the Local Fault ordered sets are not guaranteed to appear on the PMA service interface.

The PCS 64B/65B Receive state diagram shown in Figure 192–21 controls the decoding of 65B received blocks. It makes exactly one transition for each receive block processed.

The PCS shall perform the functions of RFER monitor, Transmit, and Receive as specified in these state diagrams.

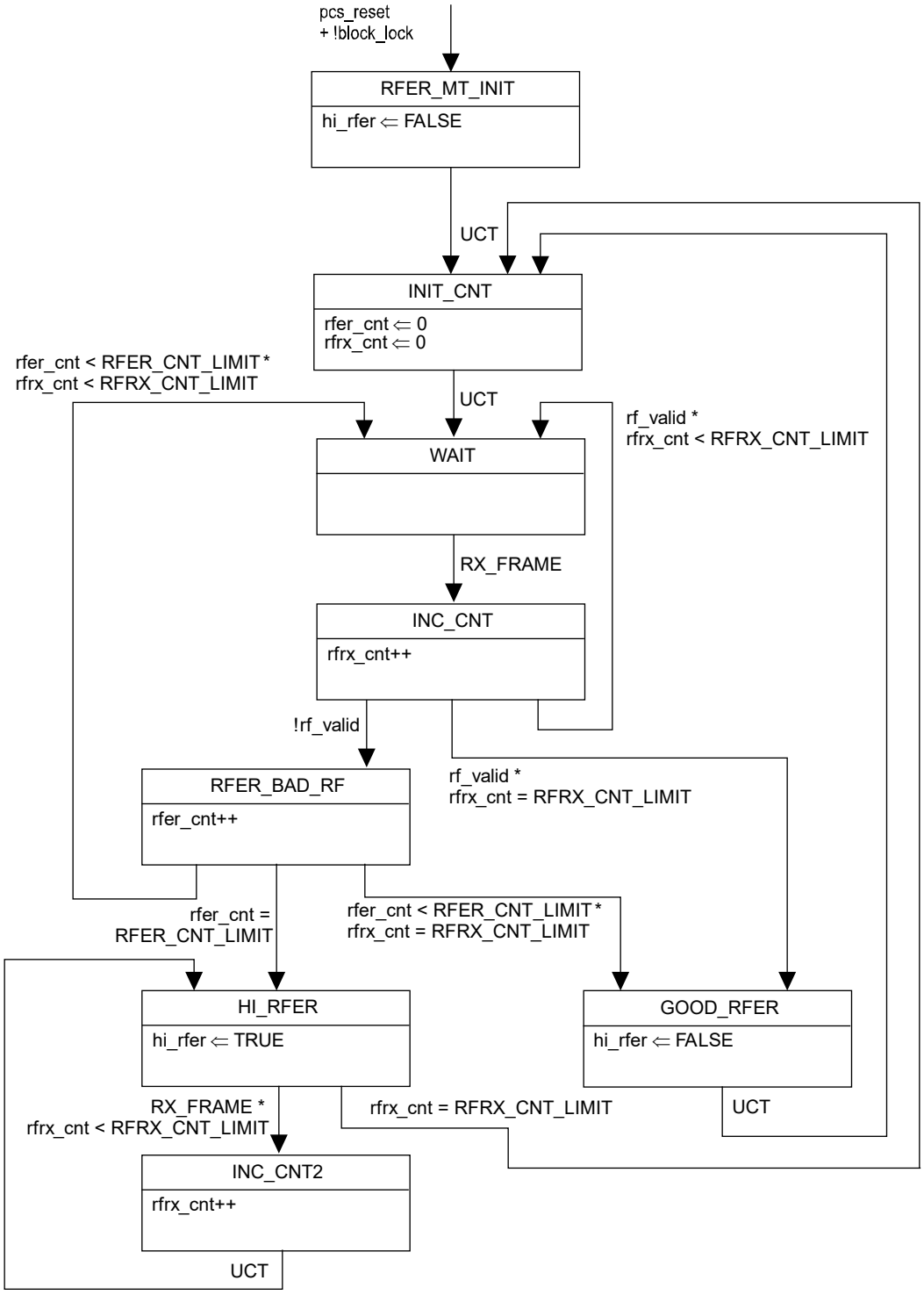



**Figure 192–19—RFER monitor block state diagram**

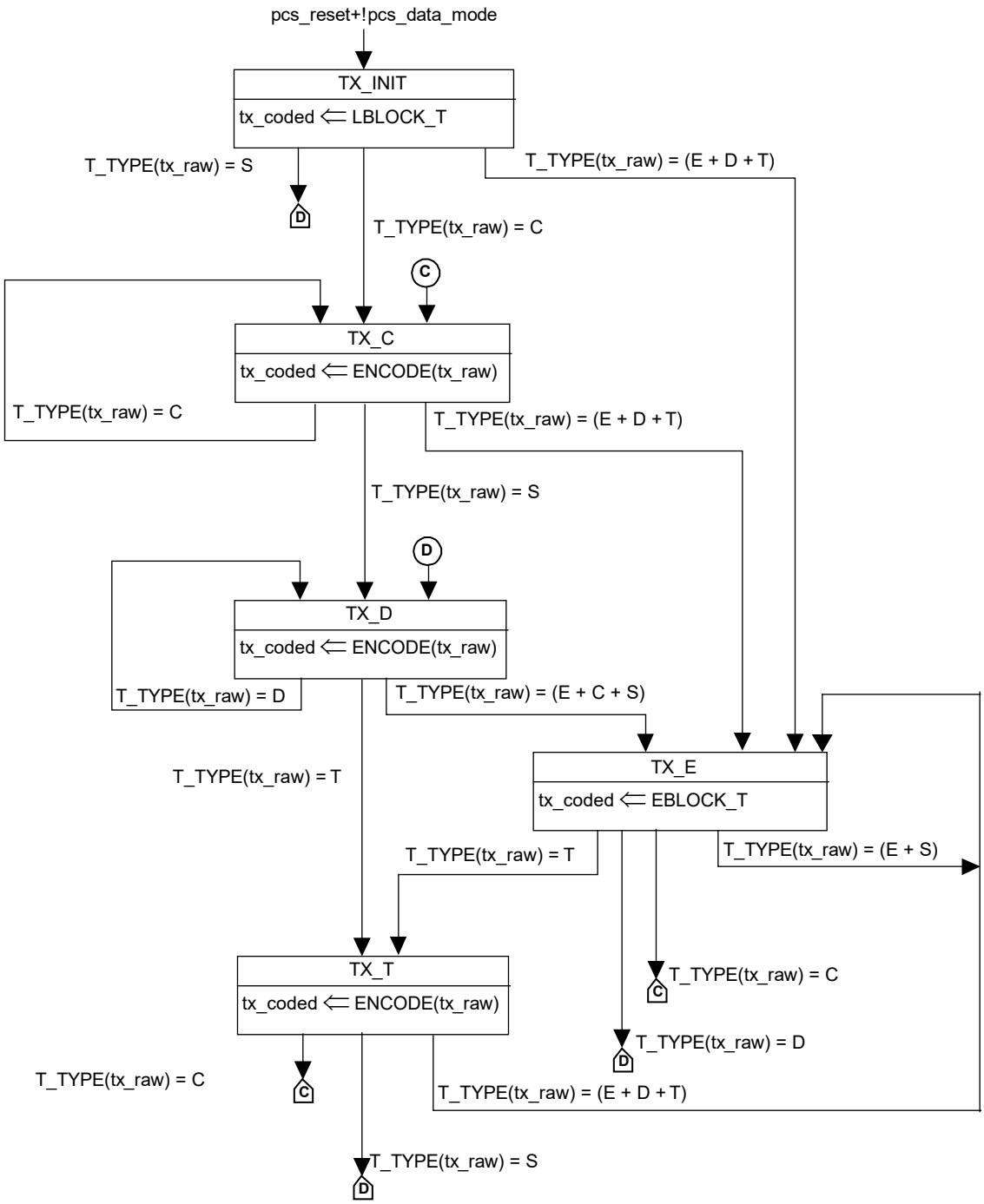



**Figure 192–20—PCS 64B/65B Transmit state diagram**

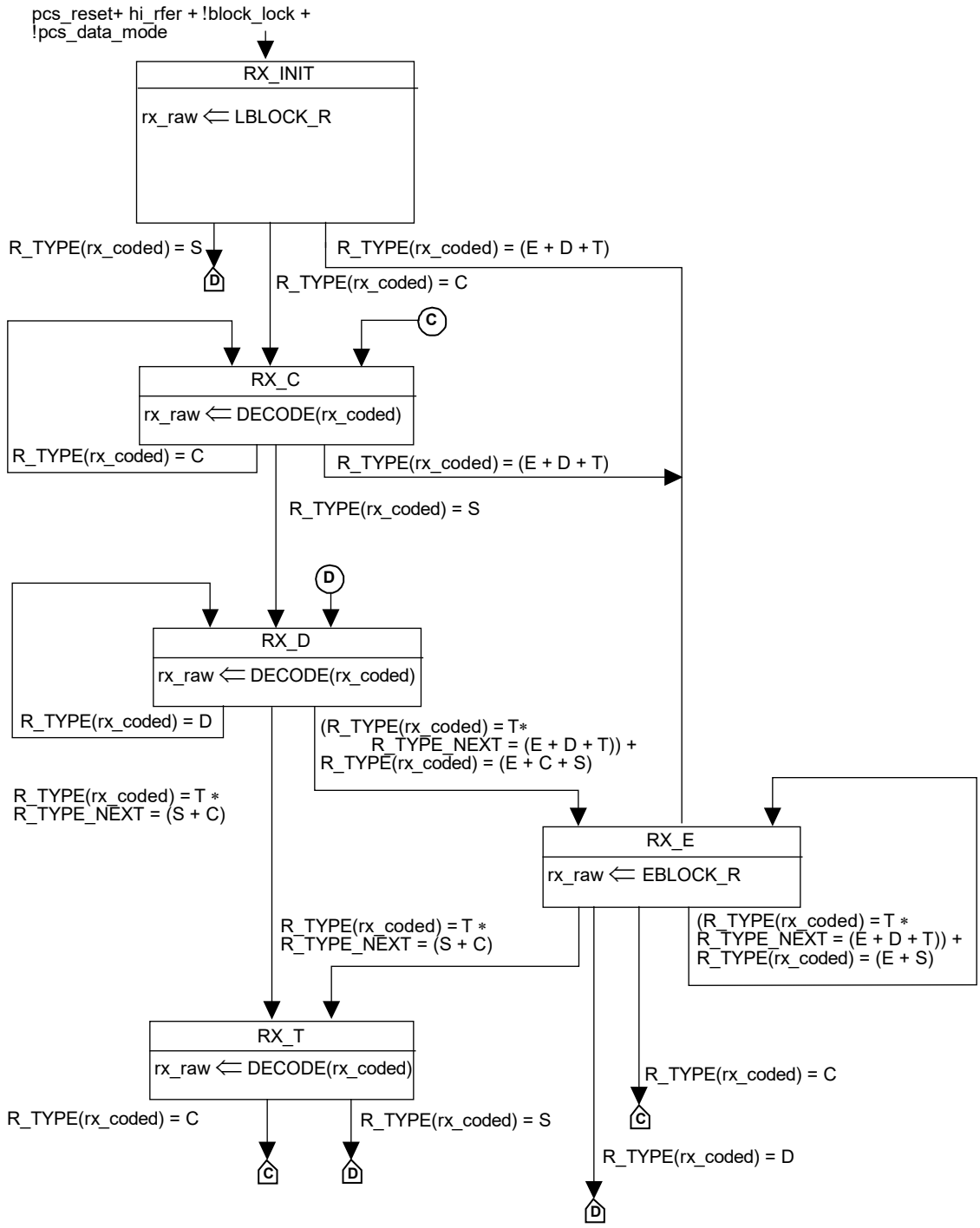



**Figure 192–21—PCS 64B/65B Receive state diagram**

#### 192.3.6 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access be provided.

##### 192.3.6.1 Status

pcs_status:
: Indicates whether the PCS is in a fully operational state. It is only TRUE if pcs_data_mode is TRUE, block_lock is TRUE, and hi_rfer is FALSE. This status is reflected in MDIO bit 3.2324.10. A latch low view of this status is reflected in MDIO 3.2323.2 and the inverse of this status is reflected in MDIO 3.2323.7.

block_lock:
: Indicates the state of the block_lock variable. This status is reflected in MDIO bit 3.2324.8. A latching low version of this status is reflected in MDIO bit 3.2324.6.

hi_rfer:
: Indicates the state of the hi_rfer variable. This status is reflected in MDIO bit 3.2324.9. A latching high version of this status is reflected in MDIO bit 3.2324.7.

##### 192.3.6.2 Counter

The following counter is reset to zero upon read and upon reset of the PCS. When it reaches all ones, it stops counting. Its purpose is to help monitor the quality of the link.

RFER_count:
: 6-bit counter that counts each time the RFER_BAD_RF of the RFER monitor state diagram (see Figure 192–19) is entered. This counter is reflected in MDIO register bits 3.2324.5:0. The counter is reset when register 3.2324 is read by management. Note that this counter counts a maximum of RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

#### 192.3.7 Operations, administration, and maintenance (OAM)

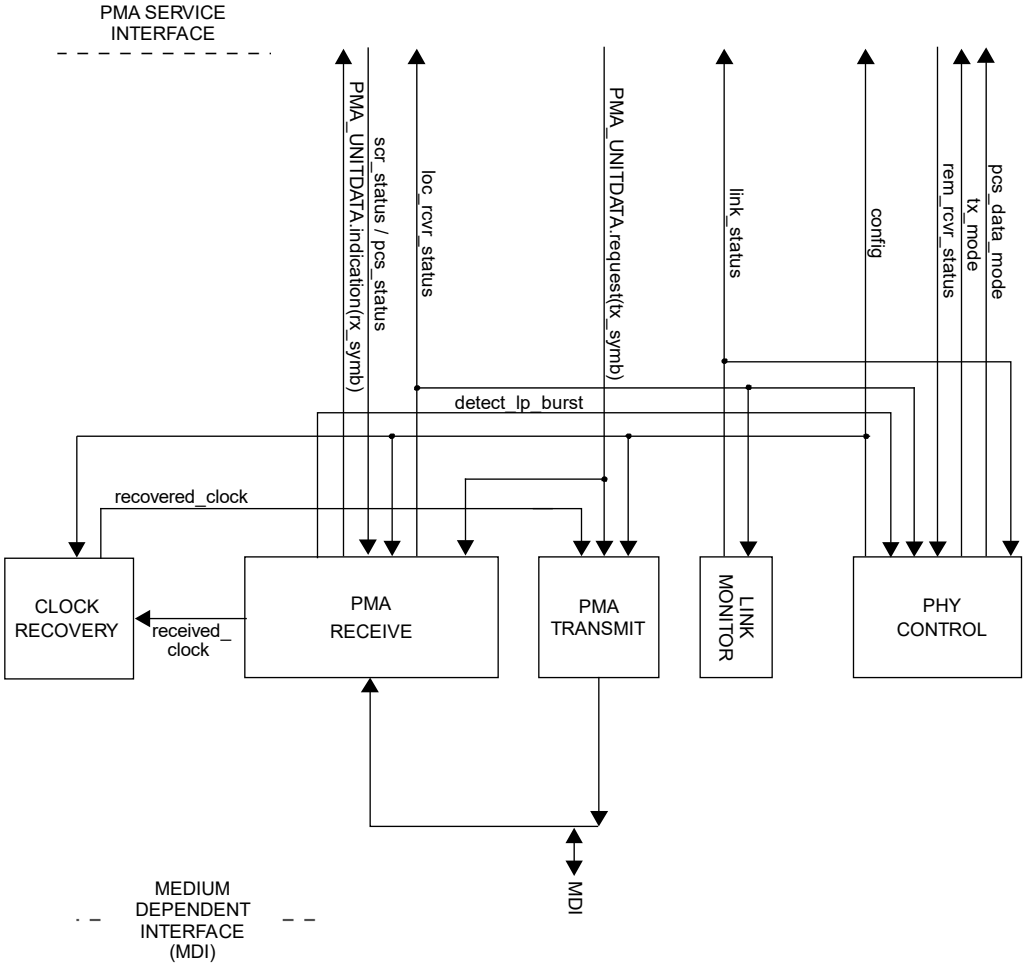
MultiGBASE-A operations, administration, and maintenance (OAM) is as specified for MultiGBASE-T1 PHYs in 149.3.9. OAM involves both HS_PATH and LS_PATH. The 10-bit symbols are inserted one per TDD burst into the OAM fields in the HS_PATH and LS_PATH. OAM bits after the first ten per burst are reserved.

### 192.4 Physical Medium Attachment (PMA) sublayer

#### 192.4.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 192.2.1 to the baseband medium specified in 192.7 or 192.8.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 192.9 or 192.10.




NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back the PMA TRANSMIT for loop timing.

**Figure 192–22—PMA reference diagram**

### 192.4.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram (see Figure 192–22) shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 192–22.

#### 192.4.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 192–26), if link partner has already exited DISABLE_TRANSMITTER state.

#### 192.4.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a two-level, three-level, or four-level modulated signal on the single balanced pair of conductors (-T1) or the single coaxial cable (-V1). When the PHY Control state diagram (see Figure 192–26) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI, followed by a QUIET period to complete a TDD cycle. The signals generated by PMA Transmit shall comply with the electrical specifications given in 192.5.2.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source the transmit symbol clock TX_TCLK from a local clock source while meeting the transmit jitter requirements of 192.5.2.3. The LEADER-FOLLOWER relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the recovered clock of 192.4.2.6 while meeting the jitter requirements of 192.5.2.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

##### 192.4.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to TRUE, this function shall cause the average launch power of the transmitter to be as specified in 192.5.2.4 when the value of tx_symb is Z.

#### 192.4.2.3 PMA Receive function

On a single balanced pair of conductors (-T1) or single coaxial cable (-V1), the PMA Receive function comprises a receiver for PAM4 signals when receiving 10 Gb/s or 7.5 Gb/s associated with a 1 Gb/s LS rate, for PAM3 signals when receiving when receiving 7.5 Gb/s associated with a 100 Mb/s LS rate or 5 Gb/s associated with a 1 Gb/s LS rate, and for PAM2 for all other signal rates.. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI and to present these sequences to the PCS Receive function. The PMA translates the signals received into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than $2 \times 10^{-10}$ after RS-FEC decoding, over a -T1 link segment meeting the requirements of 192.7 or a -V1 link segment meeting the requirements of 192.8.

To achieve the indicated performance, it is highly recommended that PMA Receive include the functions of signal equalization. No echo cancellation is needed due to the TDD nature of the duplexing method.

The PMA Receive generates the detect_lp_burst signal, which is set to TRUE when the PMA detects reception of PAM2 symbols at the start of a burst and set to FALSE when the PMA detects the QUIET portion of the burst.

The PMA Receive function uses the parameters pcs_status and scr_status, as well as the state of the equalization and estimation functions, to determine the quality of the receiver performance and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see Figure 192–26). Failing to receive link partner's consecutive TDD bursts could trigger deassertion of loc_rcvr_status. The reception of Z symbols during the TDD QUIET period alone shall not trigger setting loc_rcvr_status to NOT_OK. The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for signal inversions.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

### 192.4.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 192–26.

During PMA training (TRAINING and COUNTDOWN states in Figure 192–26), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the 96 bits starting after the *N_inf* th bit of the training payload specified in 192.3.4.3. The link partner is not required to decode every Infofield transmitted but is required to decode Infofields at a rate that enables the correct actions prior to the training phase transition.

The 12-octet Infofield shall include the fields in 192.4.2.4.2 through 192.4.2.4.8, also shown in Figure 192–23 and Figure 192–24. When PMA_state = 00, Infofield shall be transmitted at least 16 times with each change to octets 7 to 10.

PMA_state = 00

| octet 1 | octet 2 | octet 3 | octets 4/5/6 | octet 7 | octet 8 | octets 9/10 | octets 11/12 |
|---|---|---|---|---|---|---|---|
| 0xBB | 0xA7 | 0x00 | BC24 | Message | delay counter | PHY capability bits | CRC16 |

**Figure 192–23—Infofield TRAINING format**

PMA_state = 01

| octet 1 | octet 2 | octet 3 | octets 4/5/6 | octet 7 | octets 8/9/10 | octets 11/12 |
|---|---|---|---|---|---|---|
| 0xBB | 0xA7 | 0x00 | BC24 | Message | PhaseSwBC24 | CRC16 |

**Figure 192–24—Infofield COUNTDOWN format**

#### 192.4.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved ‹bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (i.e., the LSB of octet 1 is sent first).

#### 192.4.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0 > and so forth.

#### 192.4.2.4.3 PHY burst count (BC24)

The PHY burst count consists of 3 octets [Oct4<7:0>,Oct5<7:0>,Oct6,7:0>] and indicates the running count of PHY bursts sent LSB first. The BC24 continues to run uninterrupted for the duration of the link.

BC24 is defined to rollover to 0 after it reaches 16776959. BC24 could roll over in the case the LEADER has started long before the FOLLOWER sends the first responding burst.

#### 192.4.2.4.4 Message Field

The Message Field is one octet. For both the LEADER and FOLLOWER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, training_phase<4:3>, reserved<2:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6>=00 indicates TRAINING, and PMA_state<7:6>=01 indicates COUNTDOWN.

The two training_phase-indicator bits training_phase<4:3> shall communicate the training phase of the transmitting transceiver to the link partner. Training_phase<4:3> =00 indicates SYMMETRIC TRAINING and training_phase<4:3>=01 indicates ASYMMETRIC TRAINING.

All possible Message Field settings are listed in Table 192–10 for the LEADER or FOLLOWER. Any other values shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA burst shall be the first row of Table 192–10 for the LEADER, and the first or second row of Table 192–10 for the FOLLOWER. Moreover, for a given Message Fields setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5>=1 and set to 0 otherwise.

**Table 192–10—Infofield Message Field valid LEADER or FOLLOWER settings**

| PMA_state<7:6> | loc_rcvr_status<5> | training_phase<4:3> | reserved | reserved | reserved |
|---|---|---|---|---|---|
| 00 | 0 | 00 | 0 | 0 | 0 |

| | | | | | |
|---|---|---|---|---|---|
| 00 | 1 | 00 | 0 | 0 | 0 |
| 01 | 1 | 00 | 0 | 0 | 0 |
| 00[12] | 0 | 01 | 0 | 0 | 0 |
| 00 | 1 | 01 | 0 | 0 | 0 |
| 01 | 1 | 01 | 0 | 0 | 0 |

### 192.4.2.4.5 PHY capability bits

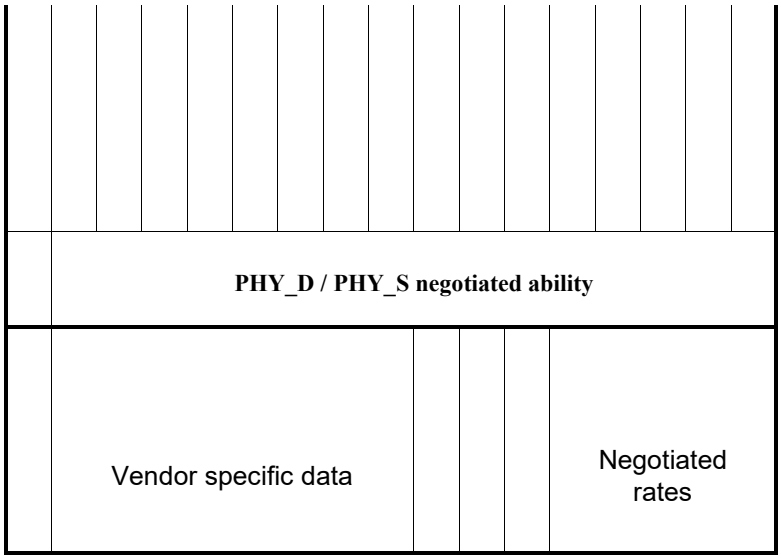
This multi-rate PHY supports bidirectional data transfer with 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, or 10 Gb/s point-to-point transmission or reception in one direction and 100 Mb/s or 1 Gb/s point-to-point reception or transmission in the other direction. The direction of asymmetry and high speed data rate are determined at link startup. The management control configures the LEADER to negotiate with the FOLLOWER to configure it for the desired high speed data rate that the FOLLOWER is expected to use. The PHY capability and negotiated rates of the Infofield are used to establish the FOLLOWER rate and check for misconfiguration.

When PMA_state<7:6> = 00, the Infofield [Oct9<7:0>,Oct10<7:0>] contains the PHY capability and negotiated ability bits. Each octet is sent LSB first. The field locations (see Table 192–11) carry different values depending on the value of the burst count (BC24) LSB. Table 192–12, Table 192–13, and Table 192–14 show the field encoding bits.

**Table 192–11—PHY capability and negotiated ability bits**

| | **octet 9** | | | | | | | | **octet 10** | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| | **PHY_D / PHY_S transmit and receive capability** | | | | | | | | | | | | | | | |
| | **Transmit capability** | | | | | | | | **Receive capability** | | | | | | | |
| | **LS rate** | | **HS rate** | | | | | | **LS rate** | | **HS rate** | | | | | |

[12]This row can be skipped if not applicable.




[Note to Editor: Since I can't edit the table imported from FrameMaker, the modified version of Table 192-11 is shown below:

| | Octet 9 | | | | | | | | Octet 10 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| BC24 LSB = 0 | PHY_D / PHY_S Transmit and Receive Capability | | | | | | | | | | | | | | | |
| | Transmit Capability | | | | | | | | Receive Capability | | | | | | | |
| | LS Rate | | HS Rate | | | | | | LS Rate | | HS Rate | | | | | |
| | 1 Gb/s | 100 Mb/s | Reserved | Reserved | 10 Gb/s | 7.5 Gb/s | 5 Gb/s | 2.5 Gb/s | 1 Gb/s | 100 Mb/s | Reserved | Reserved | 10 Gb/s | 7.5 Gb/s | 5 Gb/s | 2.5 Gb/s |
| BC24 LSB = 1 | PHY_D / PHY_S Negotiated Abilities | | | | | | | | | | | | | | | |
| | Vendor Specific Data | | | | | | | | Direction | OAMEn | R | Negotiated Rates | | | | |

End Note.]The transmit and receive capabilities depend on whether the PHY supports PHY_S, PHY_D, or both capabilities. For example, PHY_S sets its HS TX capability and LS RX capability, and PHY_D set its HS RX capability and LS TX capability. The capability bit field assignments are shown in Table 192–12. A one in a field bit indicates that the PHY has that capability and a zero indicates it does not. All zeros indicates that the field is not applicable to this PHY. For example, since a PHY that only supports PHY_S has no HS RX capability, it would set Oct10<7:2> to zero.

**Table 192–12—Rate field encoding**

| LS rate | HS rate |
|---|---|

| | | | |
|---|---|---|---|
| 00 | N/A | 000000 | N/A |
| 01 | 100 Mb/s | 000001 | 2.5 Gb/s |
| 10 | 1 Gb/s | 000010 | 5 Gb/s |
| 11 | Reserved | 000100 | 7.5 Gb/s |
| | | 001000 | 10 Gb/s |
| | | 010000 | Reserved |
| | | 100000 | Reserved |

The negotiated rates field encoding is shown in Table 192–13. The LEADER selects the negotiated rates based on either management configuration of register bits 1.2319<5:1> or selecting the highest mutually supported advertised rate. In the latter case, the LEADER optionally sends the all zeros negotiated rate code when it desires to see the FOLLOWER capabilities prior to determining the negotiated rates.

**Table 192–13—Negotiated rate field encoding**

| Code | LS rate | HS rate |
|---|---|---|
| 00000 | In progress | In progress |
| 00001 | 100 Mb/s | 2.5 Gb/s |
| 00010 | 100 Mb/s | 5 Gb/s |
| 00011 | 100 Mb/s | 7.5 Gb/s |
| 00100 | 100 Mb/s | 10 Gb/s |
| 00101 | 1 Gb/s | 5 Gb/s |
| 00110 | 1 Gb/s | 7.5 Gb/s |
| 00111 | Reserved | Reserved |
| 01xxx | Reserved | Reserved |
| 1xxxx | Reserved | Reserved |

The LEADER uses the direction bit to communicate the desired FOLLOWER PHY type as shown in Table 192–14.

**Table 192–14—Negotiated direction field encoding**

| Code | LEADER | FOLLOWER |
|---|---|---|
| 0 | PHY_D | PHY_S |
| 1 | PHY_S | PHY_D |

OAMEn: The optional OAM capability shall be enabled only if both PHYs set the capability bit OAMen=1.

The capability bit values shall be considered as valid only when loc_rcvr_status<5> bit is 1.

### 192.4.2.4.6 TDD delay counter

When PMA_state<7:6>=00, then Oct8<7:0> contains TDD delay counter sent LSB first. The format of TDD delay counter is Oct8<0> = Reserved, Oct8<1:6> = delay_count<5:0>, and Oct8<7> = delay_count_valid as shown in Table 192–15.

**Table 192–15—TDD delay counter**

| octet 8 | | | | | | | |
|---|---|---|---|---|---|---|---|
| **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
| | delay_count | | | | | | |

After the LEADER detects the FOLLOWER TDD burst position, it should estimate the link segment delay, then set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to 1. Each LSB unit represents 5.333 ns delay (16 symbols at 3 GBd).

The FOLLOWER shall accept the received remote delay_count only when received remote delay_count_valid bit is set to 1. The FOLLOWER shall store this delay_count number.

As acknowledgment of the reception of this delay_count, the FOLLOWER shall send back its received delay count in its own delay_count field and set its delay_count_valid to 1, so the LEADER can confirm the exchange of this information is completed. When the LEADER or the FOLLOWER finishes the exchange of delay count and the negotiated data rates, it shall set negotiation_done to OK. The PHY Control can then move to COUNTDOWN0 state, if loc_rcvr_status and rem_rcvr_status are both OK.

Starting from Asymmetric training and continuing through to the data mode, the FOLLOWER shall adjust its transmit burst position according to the stored delay_count.

#### 192.4.2.4.7 Phase switch PHY burst count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>] contains the phase switch burst count (PhaseSwBC24) sent LSB first. PhaseSwBC24 indicates the burst count when the LEADER transmitter switches from current training phase to the next training phase or Data mode. PhaseSwBC24 shall be a minimum of 16 and a maximum of 256 from the BC24 value sent in the first burst after entering a COUNTDOWN state.

Since phase switch is always initiated from the LEADER, the PhaseSwBC24 value of FOLLOWER Infofield will be ignored. The LEADER will exit a COUNTDOWN state after sending the last burst (BC24 = PhaseSwBC24 – 1), and receiving the last burst from the FOLLOWER. The FOLLOWER will exit a COUNTDOWN state after receiving the last burst (BC24 = PhaseSwBC24 – 1) from the LEADER and finishing sending the last burst of its own.

#### 192.4.2.4.8 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0> Oct10<7:0>)] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

#### 192.4.2.4.9 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 192–25. In Figure 192–25 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 192–25, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order shown, first S15, followed

by S14, and so on, until the final value S0.

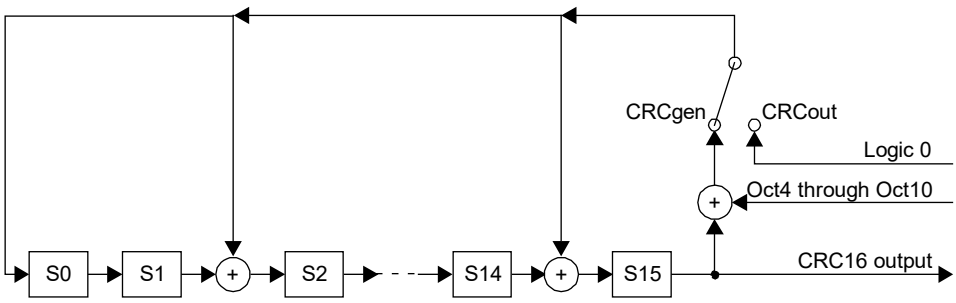



**Figure 192–25—CRC16**

#### 192.4.2.4.10 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 192–16. Mapping of MDIO status variables to PMA status variables is shown in Table 192–17.

**Table 192–16—MDIO/PMA control variable mapping**

| MDIO control variable | PMA register name | Register/bit number | PMA control variable |
|---|---|---|---|
| Reset | PMA/PMD control 1 register/ MultiGBASE-T1 PMA control register | 1.0.15 / 1.2309.15 | pma_reset |
| Transmit disable | MultiGBASE-T1 PMA control register | 1.2309.14 | PMA_transmit_disable |

**Table 192–17—MDIO/PMA status variable mapping**

| MDIO status variable | PMA register name | Register/bit number | PMA status variable |
|---|---|---|---|
| Receive fault | MultiGBASE-T1 PMA status register | 1.2310.1 | PMA_receive_fault |

#### 192.4.2.4.11 Startup sequence

The startup sequence shall comply with the state diagram description given in Figure 192–26. PMA_CONFIG is predetermined to be the LEADER or FOLLOWER via management control during initialization or via default hardware setup.

Upon entry to the TRAINING0 state, the first symbol of the FOLLOWER's transmit PMA training frame at the transmit MDI shall be aligned so that it is 400 ± 1 transmit symbols after the last PMA training payload symbol from the LEADER arrived at the FOLLOWER input MDI. The FOLLOWER shall maintain this alignment while in the TRAINING0 and COUNTDOWN0 (i.e., while tx_mode = SEND_TS) states. The PHY burst count communicated by

the FOLLOWER should match the PHY burst count communicated by the LEADER during the previous PMA training frame.

In the TRAINING0 state, PAM2 transmission is used and PHY capabilities and delay_count are exchanged using Infofields as specified in 192.4.2.4.5. The final negotiated data rate mode is determined by the LEADER. The LEADER and FOLLOWER transition from TRAINING0 state to COUNTDOWN0 state if loc_rcvr_status and rem_rcvr_status are both OK, and negotiation_done is OK.

At any COUNTDOWN or PCS_TEST state, if the local receiver status (indicated by loc_rcvr_status) transitions to NOT_OK, PHY Control returns to the SILENT state and attempts a retrain.

When entering the TRAINING1 state, the FOLLOWER shall use the LEADER transmitted delay_count to align its transmit PMA training frame to be 176 ns - delay_count × 5.333 ns (± 5.333 ns) after the last PMA training payload symbol from the LEADER appears on the FOLLOWER input MDI. The FOLLOWER shall maintain this alignment while tx_mode is SEND_TA or SEND_N.

The link_fail_inhibit_timer value is defined to be 97.5 ms, it is used to force a restart if the link up cannot be achieved within maximum allowed time.

The COUNTDOWN0 state synchronizes the link partner's transition from symmetric training TDD bursts (SEND_TS) to asymmetric training TDD bursts (SEND_TA) in the TRAINING1 state. The TRAINING1 state then waits until both local and remote receivers settle and signal that their status is OK, before transitioning to COUNTDOWN1. The PCS is tested after completion of COUNTDOWN1. If the link is reliable as indicated by block lock and the RS-FEC error rate, then the PHY Control transitions to PCS_DATA and begins transferring data.

#### 192.4.2.5 Link Monitor function

Link Monitor determines the status of the underlying receive link and communicates it via the variable link_status. Failure of the underlying receive link causes the PMA to set link_status to FAIL, which in turn causes the PMA's clients to stop exchanging frames and restart the link.

The Link Monitor function shall comply with the state diagram of Figure 192–28.

Upon power on reset, or release from power down, the PHY sets link_enable = DISABLE. During this period, link_status = FAIL is asserted. When the PHY link_enable is set to ENABLE, the Link Monitor state diagram begins monitoring the PMA. As soon as reliable transmission is achieved, with pcs_data_mode=TRUE, the variable link_status = OK is asserted, upon which further PHY operations can take place.

#### 192.4.2.6 Clock Recovery function

The Clock Recovery function shall provide a clock suitable for signal sampling so that the RFER indicated in 192.4.2.3 is achieved. The received clock signal is expected to be stable and ready for use when training has been completed. The received clock signal is supplied to the PMA Transmit function by received_clock for use when configured as the FOLLOWER.

### 192.4.3 MDI

Communication through the MDI is summarized in 192.4.3.1 and 192.4.3.2.

#### 192.4.3.1 MDI signals transmitted by the PHY

The symbols to be transmitted by the PMA are denoted by tx_symb. The transmit path uses PAM2 for all refresh headers and during RS-FEC frame transmission for 100 Mb/s, 2.5 Gb/s or 5 Gb/s when it is associated with 100 Mb/s LS. The transmit path uses PAM3 for 7.5 Gb/s when it is associated with 100 Mb/s LS or 5 Gb/s when it is associated

with 1 Gb/s LS. The transmit path uses PAM4 for the 10 Gb/s, and 7.5 Gb/s when it is associated with 1 Gb/s LS, RS-FEC frame transmission. PMA Transmit generates a pulse-amplitude modulated signal in the form shown in Equation (192–14).

(192–14)

$$s(t) = \sum_{n=0}^{\infty} a_n h_T(t - nT)$$

In Equation (192–14), $a_n$ is the PAM4 modulation symbol from the set {–1, –1/3, +1/3, +1}, the PAM3 modulation symbol from the set {-1, 0, +1}, or the PAM2 modulation symbol from the set {–1, +1} to be transmitted at time $nT$, and $h_T(t)$ denotes the system symbol response at the MDI. This symbol response shall comply with the electrical specifications given in 192.5.2.

#### 192.4.3.2 Signals received at the MDI

Signals received at the MDI can be expressed as pulse-amplitude modulated signals that are corrupted by noise as shown in Equation (192–15).

(192–15)

$$r(t) = \sum_{n=0}^{\infty} a_n h_R(t - nT) + w(t)$$

In Equation (192–15) $hR(t)$ denotes the symbol response of the overall impulse response between the transmit symbol source and the receive MDI and $w(t)$ represents the contribution of various noise sources. The receive signal is processed within the PMA Receive function to yield the received symbols rx_symb.

### 192.4.4 State variables

#### 192.4.4.1 State diagram variables

config
: See 192.2.1.2.

detect_lp_burst
: A Boolean variable indicating whether symbols (either PAM2, PAM3, or PAM4) of a TDD burst have been detected.
Values:
TRUE: TDD PAM2, PAM3, or PAM4 symbols are detected
FALSE: PMA detects the Z symbols after the PAM2/PAM3/PAM4 burst has ended (PMA could use timer timeout to terminate this detection signal).

link_enable
: This variable is set by management or default to enable or disable the PHY. It is set to disable the link upon power on reset or release from power down (see 192.4.2.5). Transition to ENABLE initiates PHY Control and the Link Monitor state diagram.
Values:
ENABLE: Enable operation of the PHY.
DISABLE: Disable the transmitter and await initiation of training.

link_status

The link_status parameter set by PMA Link Monitor state diagram.

Values:

OK: The Link Monitor function indicates that a valid MultiGBASE-A link is established. Reliable reception of signals transmitted from the remote PHY is possible.

FAIL: No valid link established.

loc_countdown_done

This variable is only used by the LEADER. It indicates that the LEADER has finished sending the last LEADER countdown Infofield and received the responding (last) Infofield from the FOLLOWER at the current TRAINING stage.

Values:

TRUE: The LEADER has sent its last burst (BC24 = PhaseSwBC24 – 1) and received the last burst from the FOLLOWER, as indicated by the received InfoField since the latest entry to a TRAINING state.

FALSE: The LEADER has not sent its last burst (BC24 = PhaseSwBC24 – 1) or has not received the last burst from the FOLLOWER, as indicated by the received InfoField since the latest entry to a TRAINING state.

loc_rcvr_status

See 192.2.1.7.

negotiation_done

During symmetric training phase, after loc_rcvr_status = OK, the LEADER and FOLLOWER exchange capabilities, delay_count and negotiated data rate, and then set the negotiation_done variable to OK.

Values:

OK: Negotiation is done, can move to COUNTDOWN0 state.

NOT_OK: Negotiation is not done, stay in TRAINING0 state.

pcs_data_mode

See 192.2.1.9.1.

pma_reset

Allows reset of all PMA functions. It is set by PMA Reset.

Values: ON or OFF.

PMA_state

Variable for the value transmitted in the PMA_state<7:6> of the Infofield by the local PHY.

Values:

00: TRAINING state.

01: COUNTDOWN state.

rem_countdown_done

This variable is only used by the FOLLOWER. It indicates that the FOLLOWER has finished receiving the last Infofield from the LEADER at the current TRAINING stage, and has sent at least one Infofield.

Values:

TRUE: The FOLLOWER has received the last burst (BC24 = PhaseSwBC24 – 1) sent by the LEADER and has sent at least one InfoField since the latest entry to a TRAINING state.

FALSE: The FOLLOWER has not received the last burst (BC24 = PhaseSwBC24 – 1) sent by the LEADER or has not sent at least one InfoField since the latest entry to a TRAINING state.

rem_rcvr_status

The status of the link partner's receiver indicated in the loc_rcvr_status received in the InfoField from the remote PHY. See 192.2.1.8.1.

training_active

A Boolean variable indicating whether the link_fail_inhibit_timer has started.

Values:

TRUE: The link_fail_inhibit_timer is running and the link is in a training phase.

FALSE: The link is not currently in a training phase.

training_phase

This variable indicates whether training is currently in the symmetric mode or the assymetric mode of training. It is transmitted to the link partner in the InfoField. See 192.4.2.4.4.

Values:

00: PHY Control is currently in either in a silent mode or a symmetric training phase.

01: PHY Control is currently in asymmetric training.

tx_mode

See 192.2.1.1.

### 192.4.4.2 Timers

All timers operate in the manner described in 14.2.3.2.

link_fail_inhibit_timer

A timer used to determine the maximum amount of time the PHY Control stays in the TRAINING, COUNTDOWN, and PCS_TEST states. The timer shall expire 97.5 ms ± 0.5 ms after being started.

minwait_timer

A timer used to determine the minimum amount of time the PHY Control stays in the SILENT, TRAINING1, and PCS_TEST states. The timer shall expire 975 μs ± 50 μs after being started.

tdd_watchdog_timer

A timer used to determine that the TDD signal has not been detected within the last ten TDD cycles. The timer shall expire 96 μs ± 5 μs after being started.

### 192.4.5 State diagrams

The PHY Control state diagram is shown in Figure 192–26 and Figure 192–27.

The Link Monitor state diagram is shown in Figure 192–28.

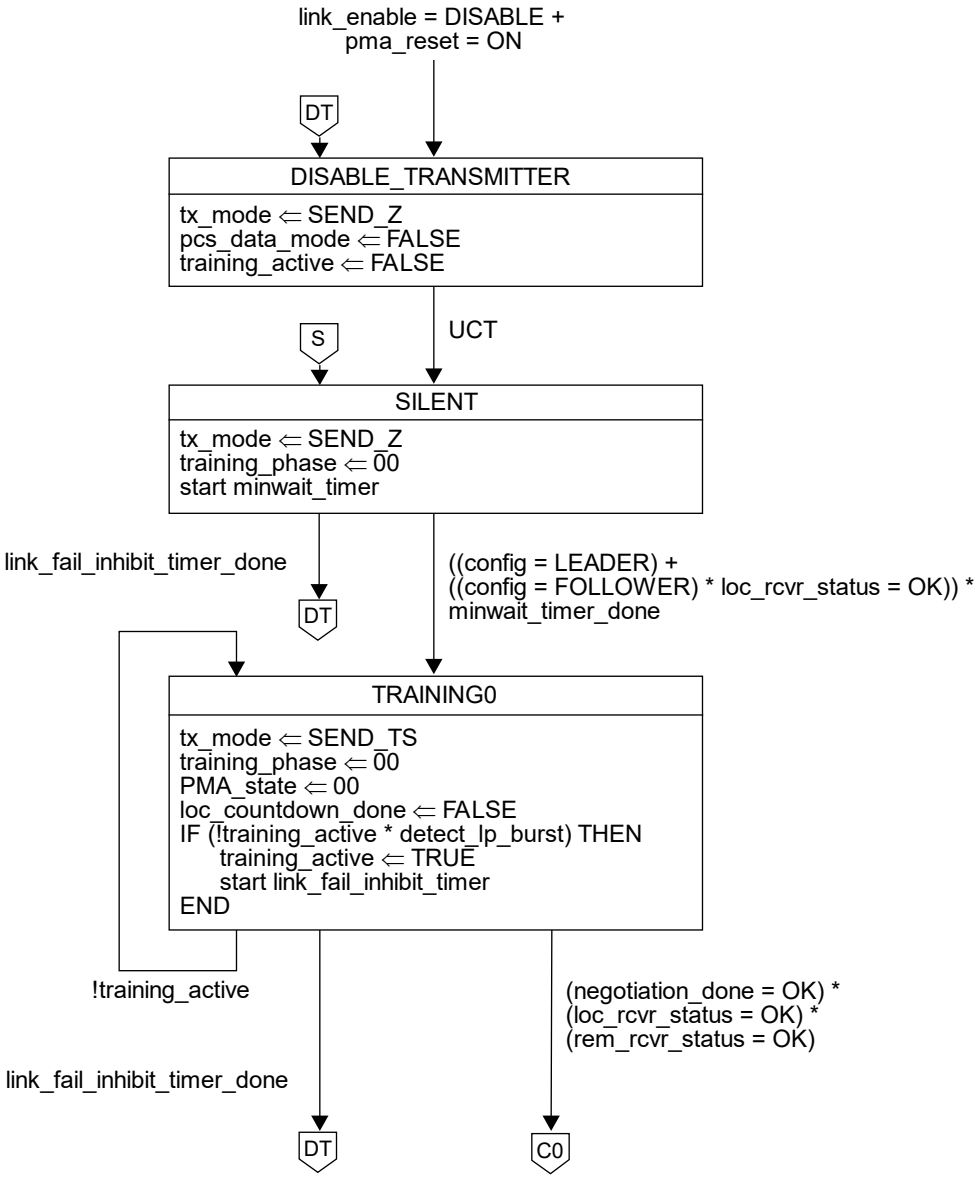



**Figure 192–26—PHY Control state diagram, part a**

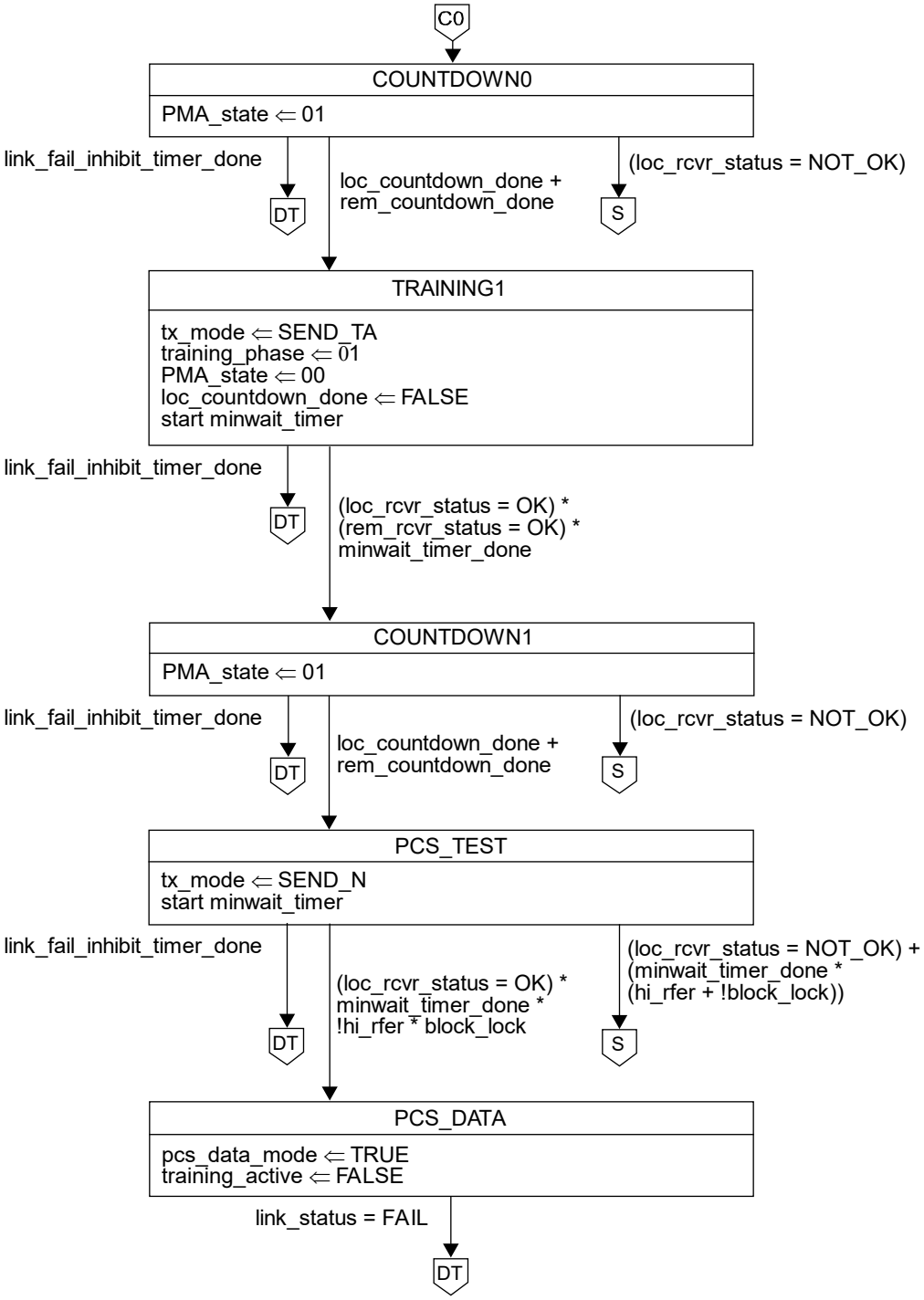



**Figure 192–27—PHY Control state diagram, part b**

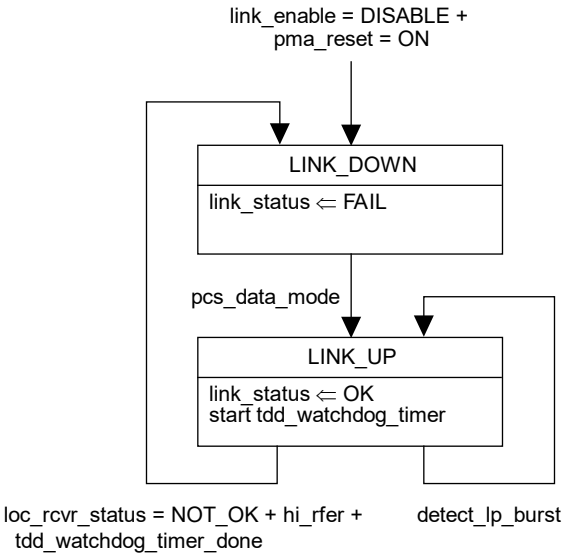



**Figure 192–28—Link Monitor state diagram**

## 192.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA and specifies PMA-to-MDI interface tests.

### 192.5.1 Test modes

The test modes described as follows shall be provided to allow for testing of the transmitter jitter, transmitter distortion, transmitter PSD, transmitter droop, and BER.

If MDIO is implemented, these test modes shall be enabled by setting a control register, 1.2313.15:13, as shown in Table 192–18. If MDIO is not implemented, then equivalent functionality shall be provided. The test modes shall only change the data symbols provided to the transmitter circuitry and do not alter the electrical and jitter characteristics of the transmitter and receiver from those of non-test mode operation.

**Table 192–18—MDIO management registers settings for test modes**

| Register value | Register description |
|---|---|
| 000 | Non-test mode operation |
| 001 | Test mode 1—Setting LEADER and FOLLOWER PHYs for transmit clock jitter test in linked mode |
| 010 | Test mode 2—Transmit MDI jitter test in LEADER mode |

| | |
|---|---|
| 011 | Test mode 3—Reserved |
| 100 | Test mode 4—Transmitter distortion test |
| 101 | Test mode 5—Continuous idle payload transmission (for the PSD Mask test) |
| 110 | Test mode 6—Transmitter droop test mode |
| 111 | Test mode 7—Data mode with zero data pattern (for BER monitoring) |

Test mode 1 enables testing of timing jitter on the LEADER and FOLLOWER transmitters. The LEADER and FOLLOWER PHYs are connected over a link segment defined in 192.7 or 192.8. When in this mode, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK_187.5. TX_TCLK_187.5 is equal to 187.5 MHz and is a divided version of TX_TCLK that times the transmitted symbols.

Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous repeating pattern of {+1, –1} symbols with the transmitted symbols timed by TX_TCLK derived from its local clock reference.

Test mode 4 is for transmitter distortion testing. When test mode 4 is enabled in PAM2 mode (i.e., 100 Mb/s, 2.5 Gb/s or 5 Gb/s when paired with 100 Mb/s LS), the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ (see Figure 192–5 and Figure 192–6). All PHYs shall support transmission of this signal at 3 GBd. PHYs that support 1 Gb/s, 5 Gb/s and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM3 mode (i.e., 5 Gb/s when paired with 1 Gb/s LS or 7.5 Gb/s when paired with 100 Mb/s), the PHY shall transmit the sequence of symbols generated by the PCS scrambler generator polynomial per Equation (192–16) such that An = Scrn[0] (see Figure 192–6). PHYs that support 7.5 Gb/s transmit rate shall support transmission of this signal at 6 GBd.

When test mode 4 is enabled in PAM4 mode (i.e., 10 Gb/s or 7.5 Gb/s when paired with 1 Gb/s LS), the PHY shall transmit the PCS scrambler generator polynomial per Equation (192–16) such that $A_n = Scr_n[0]$ and $B_n = Scr_n[3] \oplus Scr_n[8]$ (see Figure 192–6). PHYs that support 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd.

(192–16)

$g(x) = 1 + x^9 + x^{11}$ Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask and the transmit power level. When test mode 5 is enabled, the PHY shall transmit continuously with no QUIET period or refresh header and with transmit signal level corresponding to the data mode of operation. The PCS Transmit will encode data as when tx_mode = SEND_N, and as if continuously receiving idle control characters from the XGMII. The test applies to both the LEADER and FOLLOWER. The clock is sourced from a stable clock with 100 ppm accuracy for this test.

When test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {–1} symbols with the transmitted symbols timed from its local 3 GHz clock source.

Test mode 7 is for enabling measurement of the bit error ratio of the link including the RS-FEC encoder/decoder, transmit and receive analog front ends of the PHY, and a cable connecting two PHYs. This mode reuses the non-test mode with zero data pattern. Instead of encoding data received from the MAC, the input to the RS-FEC is all-zero message symbols and the continuous zero data pattern is encoded. On the receive side, after PCS FEC decoding processing, a zero data sequence is expected with no errors. Any block received with non-zero data bits is counted as an error and calculated in the RS-FEC block error ratio.

#### 192.5.1.1 Test fixtures

The following fixtures, or their equivalents, as shown in Figure 192–29, Figure 192–30, and Figure 192–31, in stated respective tests, are defined for measuring the transmitter specifications for data communication only.

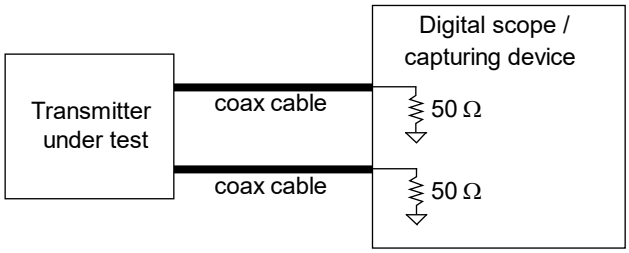



**Figure 192–29—Transmitter test fixture 1 for -T1 transmitter droop, transmitter linearity, power spectral density, transmit power level, and MDI jitter measurements**

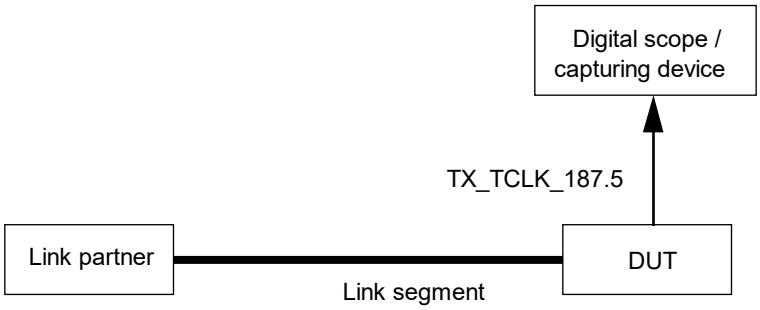



**Figure 192–30—Transmitter test fixture 2 for -T1 and -V1 LEADER and FOLLOWER clock jitter measurement**

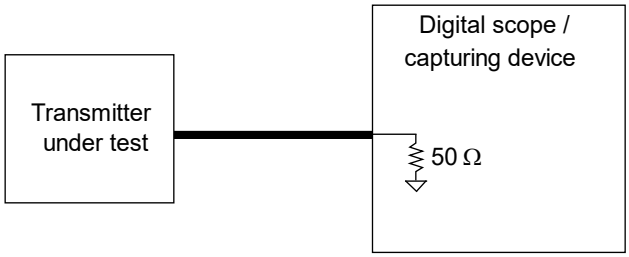



**Figure 192–31—Transmitter test fixture 3 for -V1 transmitter droop, transmitter linearity, power spectral density, transmit power level, and MDI jitter measurements**

### 192.5.2 Transmitter electrical specifications

The PMA provides the Transmit function specified in 192.4.2.2 in accordance with the electrical specifications of this clause. The electrical input shall be ac-coupled (i.e., it presents a high dc common-mode impedance at the MDI). There may be various methods for ac-coupling in actual implementations.

When a load is not specified, the transmitter shall meet the requirements of this clause with a 100 Ω resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 Ω resistive load connected to each single ended transmitter output when connected to a -V1 link. Transmitter electrical tests are specified with a load tolerance of ± 0.1%.

#### 192.5.2.1 Maximum output droop

With the transmitter in test mode 6 and using transmitter test fixture 1 (see Figure 192–29) or test fixture 3 (see Figure 192–31), the magnitude of both the positive and negative droop shall be less than 24%, measured with respect to an initial value at 2 ns after the zero crossing and a final value at 8 ns after the zero crossing.

#### 192.5.2.2 Transmitter distortion

Transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 1 (see Figure 192–29) or transmitter test fixture 3 (see Figure 192–31) as appropriate to the MDI.

The peak distortion is determined by sampling the signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with pseudo-code given below or an equivalent. The captured block of signal shall be at least 4000 transmitted symbols long and be sampled with the minimum 10x oversampling. The transmit baud rate may be reduced to 1 Gs/s by repeating the symbols using the same clock edge as in data mode of operation.

The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 20 mV when the peak signal level is normalized to 1 V for PAM2 transmitters and less than 15 mV for PAM3 or PAM4 transmitters.

```
% Post processing pseudo-code for transmitter distortion
clear
Ns=2^11-1; % Scrambler length
Nc=70; % Canceller length
Modulation=2; % Choices are 2 for PAM2, 3 for PAM3, and 4 for PAM4
```

```
% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
   scr(i)=mod(scr(i-11) + scr(i-9),2);
end

% Generate tm4 (test mode 4) for a given modulation
if Modulation==2
   tm4=2*scr-1;
elseif Modulation==3
tm4=ones(Ns,1);
map=[-1 -1;-1 0;0 -1;1 -1;0 1;-1 1;1 1;1 0];
scr3=[scr, circshift(scr,1), circshift(scr,2)];
data = 4*scr3(:,3)+ 2*scr3(:,2)+scr3(:,1);
for n=1:length(data)
tm4([2*n-1,2*n]) =map(data(n)+1,:);
end
elseif Modulation==4
   tm4=ones(Ns,1);
   map=[-1;-1/3;1;1/3];
   DS=[scr,mod(circshift(scr,3) + circshift(scr,8),2)];
   data = 2*DS(:,1)+DS(:,2);
   for n=1:length(DS)
   tm4(n) =map(data(n)+1);
   end
else
   disp('Error: The code supports either PAM2, PAM3 or PAM4')
   return
end

% Test mode4 matrix
for i=1:Nc
X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file

% Minimum of 4K TX symbols, 10X oversampling, high resolution capture
fid=fopen('TestMode4.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF at Nyquist
[A,B]=butter(1,1/10,'low');
tx=filter(A,B,tx);

% HPF (with this HPF, the 70-tap canceller residual linear error is 0.00
tx = filter([1,-1],[1,-0.98],tx);

% Select one period, 10x oversampling, a row vector
tx=tx((1:Ns*10)+2e3)'; % removes HPF transients

% Level normalization
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10
```

```
tx1=tx(n:10:end);
temp=xcorr(tx1,tm4); % Align data and test pattern
index=find(abs(temp)==max(abs(temp)));
X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);
coef=tx1/X; % Compute coefficients that minimize squared error in a cyclic block
err=tx1-coef*X; % Linear canceller
dist(n) = max(abs(err)); % Peak distortion
SNR(n)=std(tx)/std(err); % SNR
End

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist
```

#### 192.5.2.3 Transmitter timing jitter and jitter at the MDI

The following measurements are performed for a PHY in LEADER mode:

1) The RMS jitter for jitter frequencies greater than 100 kHz measured in test mode 2 using test fixture 1 for -T1 and test fixture 3 for -V1 shall be less than 1 ps when supporting 10 Gb/s, 2 ps when supporting 5 Gb/s/, and 4 ps when supporting 2.5 Gb/s.
2) Peak-to-peak of Time Interval Error measured in test mode 1 using test fixture 2 over a period of 100 µs shall be less than 10 ps when supporting 10 Gb/s, 20 ps when supporting 5 Gb/s, and 40 ps when supporting 2.5 Gb/s.

The following measurements are performed using test fixture 2 (see Figure 192–30) for a PHY in FOLLOWER mode:

1) The RMS jitter for jitter frequencies greater than 1 MHz measured in test mode 1 shall be less than 1 ps when supporting 10 Gb/s, 2 ps when supporting 5 Gb/s, and 4 ps when supporting 2.5 Gb/s.
2) Peak-to-peak of Time Interval Error over any period of 10 µs measured in test mode 1 over 50 overlapping periods of 10 µs each shall be less than 15 ps for 10 Gb/s, 30 ps for 5 Gb/s, and 60 ps for 2.5 Gb/s. The overlapping period of 5 µs is assumed.

#### 192.5.2.4 Transmitter power spectral density (PSD) and power level

Transmitter power spectral density (PSD) and power level measurements are performed in test mode 5. The measured transmit power shall be in the range specified in Table 192–19 when using the same test fixture as used for PSD measurement. When the value of tx_symb is Z, the transmit signal at the MDI is nominally zero and the transmit signal shall be less than -36 dBm for frequencies greater 10 MHz.

**Table 192–19—Power levels**

| Transmit MAC data rate | Differential (balanced) | | Single-ended (unbalanced) | |
|---|---|---|---|---|
| | Min (dBm) | Max (dBm) | Min (dBm) | Max (dBm) |
| 100 Mb/s | 0 | 2 | –3 | –1 |
| 1 Gb/s | 2 | 4 | –1 | 1 |
| 2.5 Gb/s | 0 | 2 | –3 | –1 |
| 5 Gb/s+100M | 2 | 4 | –1 | 1 |

| | | | | |
|---|---|---|---|---|
| 5 Gb/s+1G | 1 | 3 | -2 | 0 |
| 7.5 Gb/s+100M | 1 | 3 | -2 | 0 |
| 7.5 Gb/s+1G | 0 | 2 | –3 | –1 |
| 10 Gb/s | 0 | 2 | –3 | –1 |

The power spectral density of the transmitter of -T1, measured into a 100 Ω differential load using test fixture 1 (see Figure 192–29), shall be between the upper and lower masks specified in Equation (192–17) and Equation (192–18).

The upper and lower masks for each MAC data rate are shown in Figure 192–32, Figure 192–33, and Figure 192–34. See Table 192–2 for the definition of *S*. See Table 192–20 for the definition of PSD mask *K* factor.

**Table 192–20—PSD mask *K* factor**

| Transmit MAC data rate | *K* |
|---|---|
| 100 Mb/s | 0 |
| 1 Gb/s | 0 |
| 2.5 Gb/s | 0 |
| 5 Gb/s+100M | 0 |
| 5 Gb/s+1G | 1 |
| 7.5 Gb/s | 1 |
| 7.5 Gb/s+1G | 2 |
| 10 Gb/s | 2 |

(192–17)

$$UPSD(f) = \begin{cases} -89 - K & \text{dBm/Hz} \quad 40 < f \le 1200 \times S \\ -87 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 1200 \times S < f \le 3000 \times S \\ -80 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 3000 \times S < f \le 5000 \times S \end{cases}$$

(192–18)

$$LPSD(f) = \begin{cases} -93 - K & \text{dBm/Hz} \quad 40 < f \le 600 \times S \\ -92 - K - \dfrac{f}{600 \times S} & \text{dBm/Hz} \quad 600 \times S < f \le 2400 \times S \\ -86.4 - K - \dfrac{f}{250 \times S} & \text{dBm/Hz} \quad 2400 \times S < f \le 3500 \times S \end{cases}$$

where

$f$ is the frequency in MHz

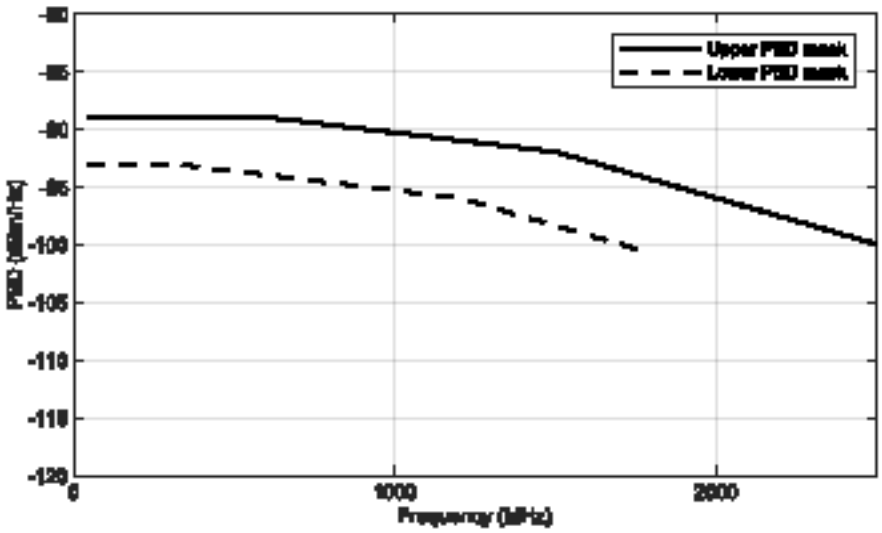



**Figure 192–32—Transmitter Power Spectral Density for 100 Mb/s and 250 Mb/s MAC data rates, upper and lower masks**

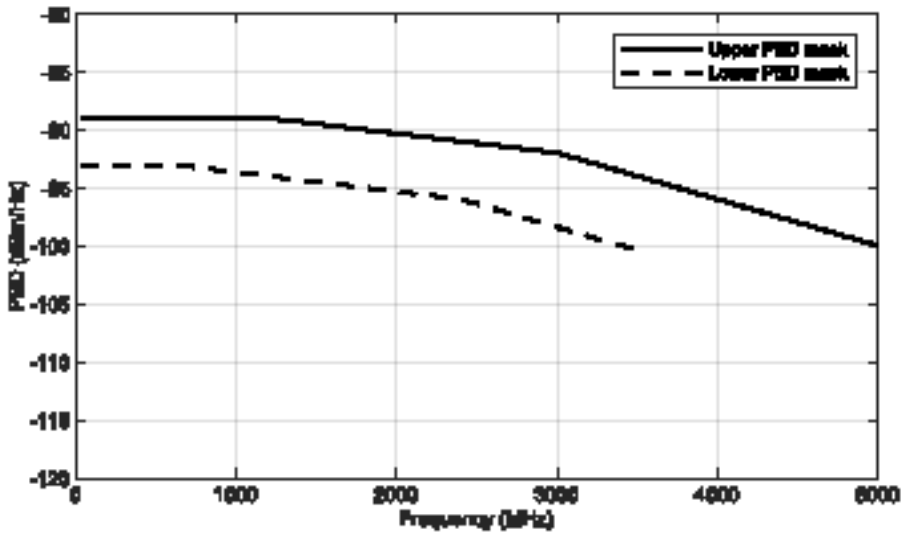



**Figure 192–33—Transmitter Power Spectral Density for 5 Gb/s MAC data rate, upper and lower masks**

*[Note to Editor: Add "1 Gb/s" to the caption of Figure 192-33.]*

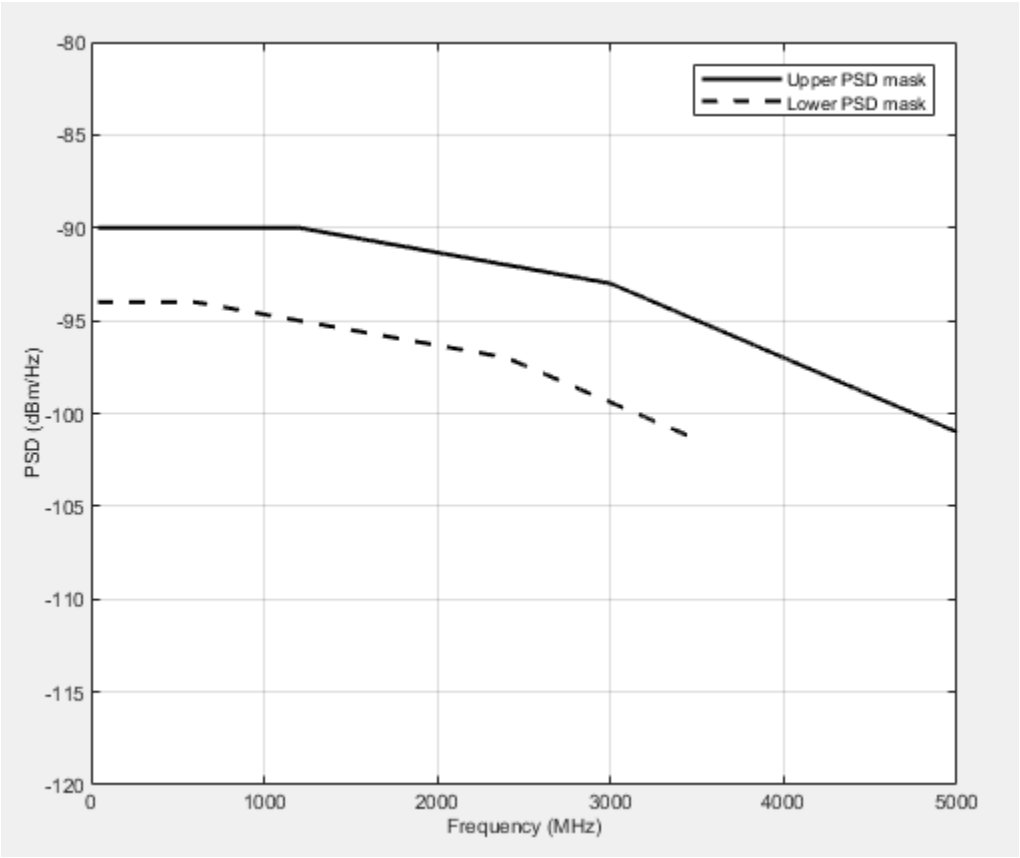



**Figure 192-xx – Transmit Power Spectral Density for 7.5 Gb/s MAC data rate, upper and lower masks**

[Note to Editor: This PSD plot for 7.5 Gb/s was generated using George's format with S=1 and K=1.]

[Note to Editor: This PSD plot applies to both 7.5 Gb/s and 5 Gb/s + 1 Gb/s LS.]

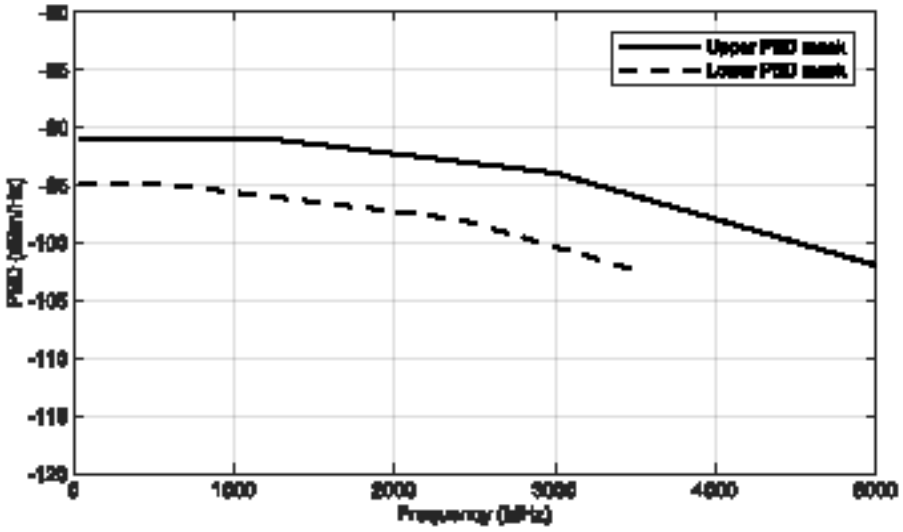



**Figure 192–34—Transmitter Power Spectral Density for 10 Gb/s MAC data rate, upper and lower masks**

[Note to Editor: This PSD plot applies to both 10 Gb/s and 7.5 Gb/s + 1 Gb/s LS.]

For the power spectral density of -V1, with single ended termination of 50 Ω load and test fixture 3 (see Figure 192–31), both upper and lower PSD Masks are lower by 3 dB from Equation (192–17), Equation (192–18), Figure 192–32, Figure 192–33, and Figure 192–33.

### 192.5.2.5 Transmitter peak output

The transmit differential signal at the -T1 MDI should be less than the peak-to-peak values specified in Table 192–21 when measured with a 100 Ω termination. The transmit signal at the -V1 MDI should be less than the peak-to-peak values specified in Table 192–21 when measured with a 50 Ω termination. The limits in this clause apply to all transmitted symbol sequences, including SEND_N, SEND_TS, and SEND_TA.

**Table 192–21—Transmitter peak-to-peak output**

| Transmit MAC data rate | -T1 MDI peak-to-peak output (V) | -V1 MDI peak-to-peak output (V) |
|---|---|---|
| 100 Mb/s | 1.3 | 0.65 |
| 1 Gb/s | 1.5 | 0.75 |
| 2.5 Gb/s | 1.3 | 0.65 |

| | | |
|---|---|---|
| 5 Gb/s+100M | 1.5 | 0.75 |
| 5 Gb/s+1G | 1.5 | 0.75 |
| 7.5 Gb/s+100M | 1.5 | 0.75 |
| 7.5 Gb/s+1G | 1.7 | 0.85 |
| 10 Gb/s | 1.7 | 0.85 |

#### 192.5.2.6 Transmitter clock frequency

When using a local timing reference, the symbol transmission rate shall be within the range $6 \times S$ GBd ± 100 ppm with drift less than 1 ppm/sec).

When the FOLLOWER is using a recovered timing reference, the symbol transmission rate (scaled by *S)* shall be within ± 10ppm of the recovered clock.

### 192.5.3 Receiver electrical specifications

The PMA provides the Receive function specified in 192.4.2.3 in accordance with the electrical specifications of this clause using cabling that is within the limits specified in 192.7 or 192.8.

#### 192.5.3.1 Receiver input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of 192.5.2 and have passed through a link specified in 192.7 shall be received with a BER less than $10^{-12}$ after RS-FEC decoding, and sent to the XGMII after link_status = OK.

Single-ended signals received at the MDI that were transmitted from a remote transmitter within the specifications of 192.5.2 and have passed through a link specified in 192.8 shall be received with a BER less than $10^{-12}$ after RS-FEC decoding, and sent to the XGMII after link_status = OK.

This specification can be verified by a frame error ratio less than $7.8 \times 10^{-9}$ for 800 octet frames with minimum IPG or greater than 220-octet IPG.

### 192.5.3.2 Broadband stationary noise rejection

This specification is provided to verify the receiver's tolerance to broadband stationary noise from a variety of sources. The test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwidths, and magnitudes shown in Table 192–22. The minimum noise frequency is 10 MHz. The -T1 receive DUT is connected to the noise source through a directional coupler with a -T1 link segment (see 192.7) as shown in Figure 192–35. The -V1 receive DUT is connected to the noise source through a directional coupler with a -V1 link segment (see 192.8) as shown in Figure 192–36. The BER is expected to be less than $10^{-12}$, and to satisfy this specification, the frame loss ratio is less than $10^{-9}$ for 125-octet packets measured at the MAC/PLS service interface.

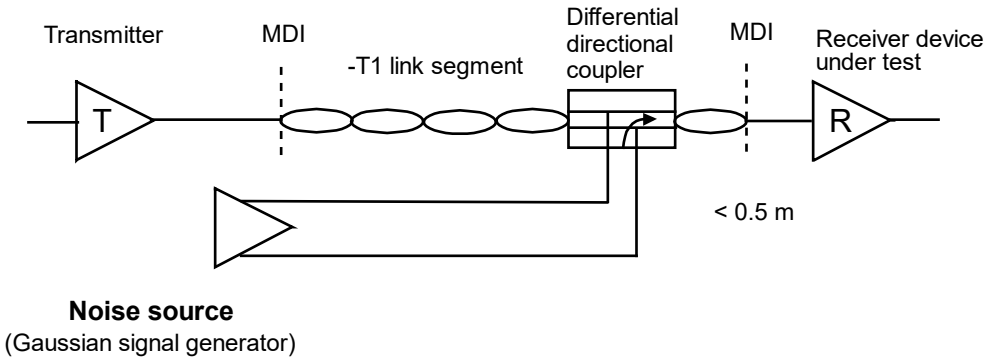



**Figure 192–35—Broadband stationary noise rejection test setup, -T1**

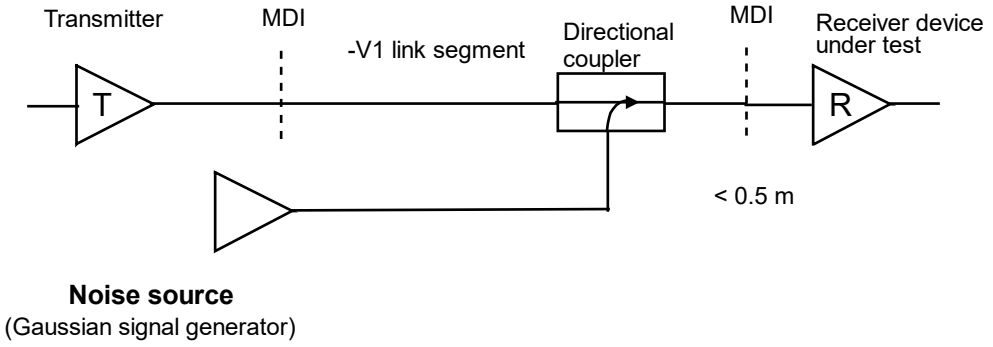



**Figure 192–36—Broadband stationary noise rejection test setup, -V1**

**Table 192–22—Broadband stationary noise source, high speed data rate**

| | | Added noise at MDI (dBm/Hz) | |
|---|---|---|---|
| **Transmit MAC data rate** | **Noise bandwidth (MHz)** | **-T1** | **-V1** |
| 2.5 Gb/s | 1750 | –140 | –143 |
| 5 Gb/s | 3500 | –144 | –147 |
| 7.5 Gb/s | 3500 | -146 | -149 |

| | | | |
|---|---|---|---|
| 10 Gb/s | 3500 | –148 | –151 |

## 192.6 Management interface

MultiGBASE-A makes extensive use of the management functions that may be provided by the optional MDIO (see Clause 45).

## 192.7 Link segment characteristics, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair of conductors (-T1) that meet the requirements specified in this subclause. -T1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s or 1 Gb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

### 192.7.1 Link transmission parameters

The transmission characteristics for a -T1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

#### 192.7.1.1 Insertion loss

The insertion loss of a -T1 link segment shall meet the values determined using Equation (192–19).

(192–19)

$$\text{Insertion loss}(f) \le 0.322\sqrt{f} + 0.0019f + \frac{1}{\sqrt{f}} \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $10 \le f \le 5000$

Equation (192–19) is plotted in Figure 192–37, which is provided for information only.

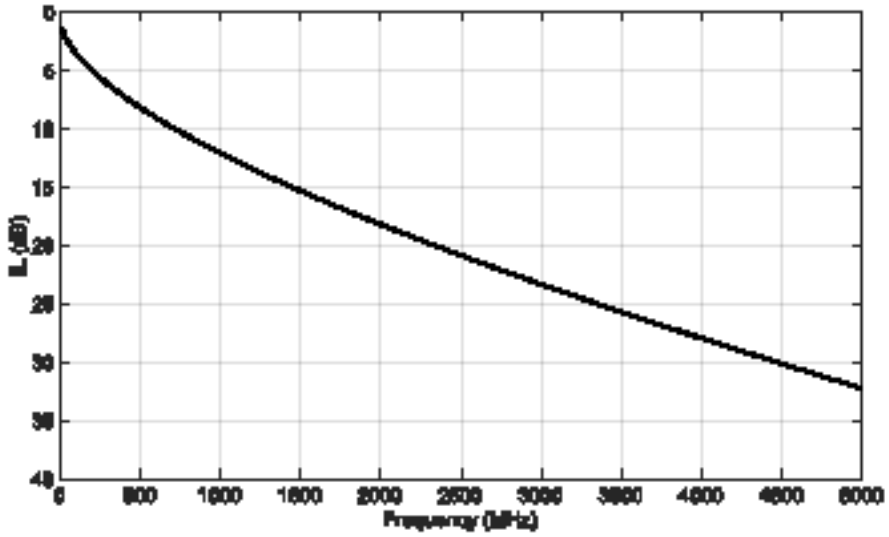



**Figure 192–37—T1 link segment insertion loss**

### 192.7.1.2 Differential characteristic impedance

The nominal differential characteristic impedance of a -T1 link segment is 100 Ω.

### 192.7.1.3 Return loss

The return loss of a -T1 link segment shall meet the values determined using Equation (192–20).

(192–20)

$$RL(f) \geq \begin{cases} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left\langle \frac{f-500}{1500} \right\rangle & 500 \leq f < 2000 \\ 9.5 - 3\left\langle \frac{f-2000}{2500} \right\rangle & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{cases} \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–20) is plotted in Figure 192–38, which is provided for information only.

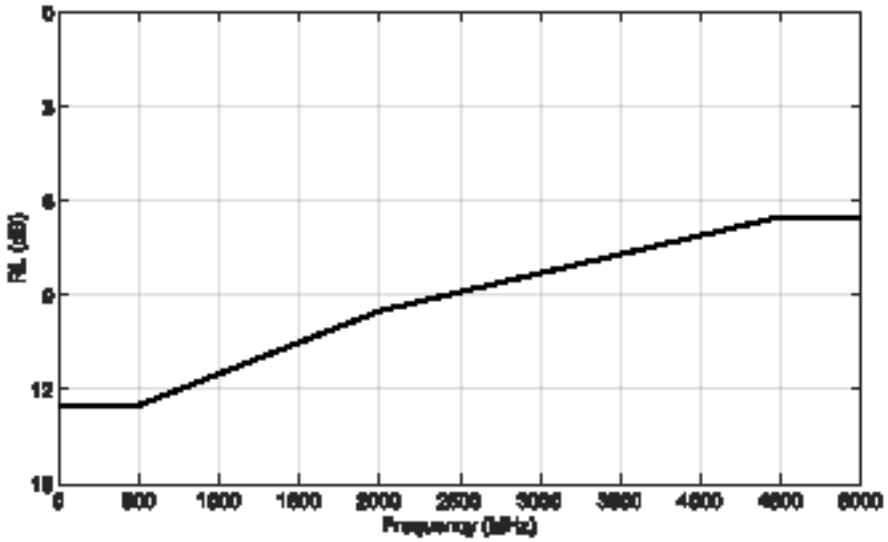



**Figure 192–38—T1 link segment return loss**

#### 192.7.1.4 Coupling attenuation

The coupling attenuation of a -T1 link segment shall be as specified in 149.7.1.4.

#### 192.7.1.5 Screening attenuation

The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5.

#### 192.7.1.6 Maximum link delay

The propagation delay of a -T1 link segment shall not exceed 160 ns for all frequencies between 3 MHz and 4 GHz.

### 192.7.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as *alien crosstalk noise*. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

#### 192.7.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -T1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -T1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–21).

(192–21)

$$\mathrm{PSANEXT(f)} = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN(f)_j}}{10}} \ \mathrm{dB}$$

where the function AN($f$)$_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency $f$ of the disturbing -T1 link segment $j$ (1 to $m$) for the disturbed -T1 link segment.

The PSANEXT loss between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (192–22).

(192–22)

$$\mathrm{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–29) is plotted in Figure 192–39, which is provided for information only.

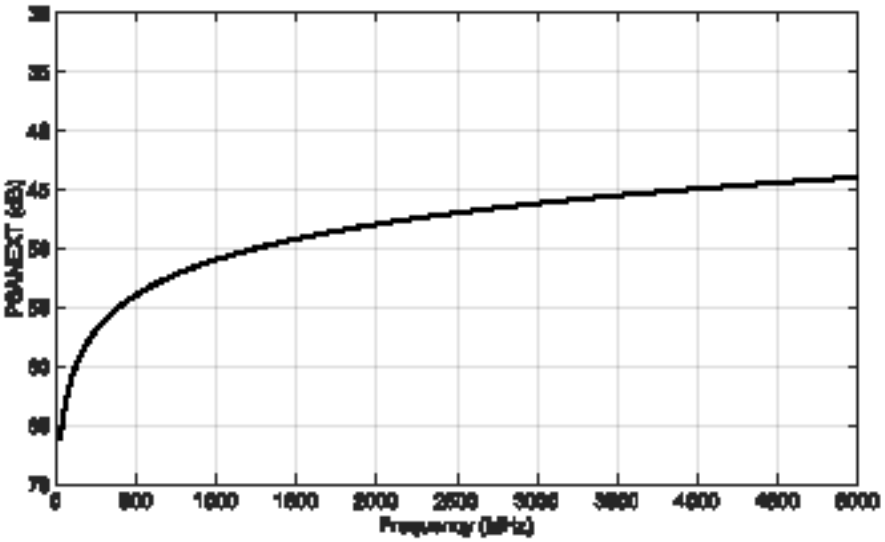



**Figure 192–39—T1 link segment PSANEXT loss**

### 192.7.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -T1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -T1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–23).

(192–23)

$$\mathrm{PSAACRF(f)} = \left(-10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AFEXT(f)}_j}{10}}\right) - \mathrm{IL_d(f)} \quad \mathrm{dB}$$

where

$f$ is the frequency in MHz; $30 \le f \le 5000$

$\mathrm{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency $f$ from a disturbing -T1 link segment $j$ (1 to $m$) to the disturbed -T1 link segment in dB

$\mathrm{IL_d}(f)$ is the measured insertion loss of the disturbed link segment at frequency $f$ in dB

The PSAACRF between a disturbed -T1 link segment and the disturbing -T1 link segments shall meet the values determined using Equation (192–24).

(192–24)

$$\text{PSAACRF}(f) \geq 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–31) is plotted in Figure 192–40, which is provided for information only.

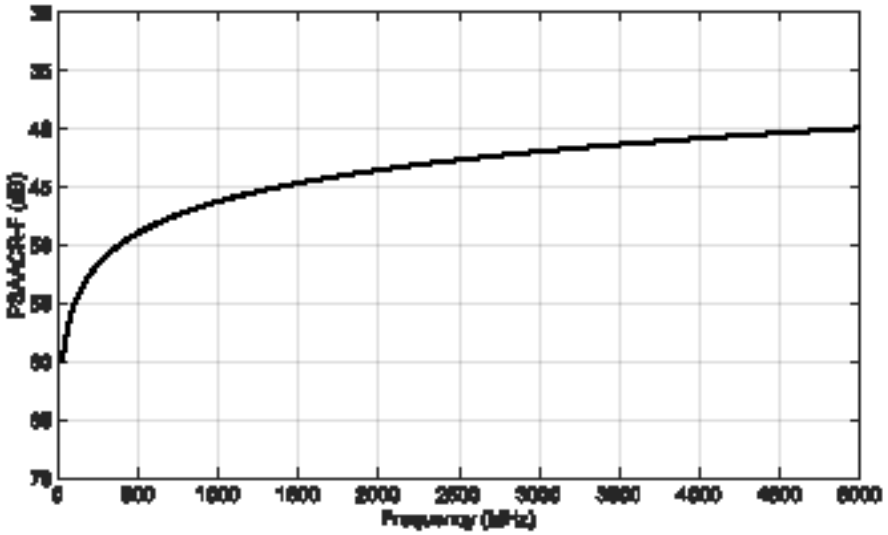



**Figure 192–40—T1 link segment PSAACRF**

## 192.8 Link segment characteristics, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial cable (-V1) that meet the requirements specified in this subclause. -V1 supports an effective MAC data rate of 2.5 Gb/s, 5 Gb/s, 7.5 Gb/s, and 10 Gb/s in one direction and, simultaneously, 100 Mb/s or 1 Gb/s in the other direction. Full duplex operation at the logical interface of XGMII is supported.

### 192.8.1 Link transmission parameters

The transmission characteristics for a -V1 link segment are specified to support operation over automotive temperature and electromagnetic conditions.

#### 192.8.1.1 Insertion loss

The insertion loss of a -V1 link segment shall meet the values determined using Equation (192–25).

(192–25)

$$\text{Insertion loss}(f) \leq 0.3 + 0.345\sqrt{f} + 0.000825f + \frac{0.48}{\sqrt{f}} \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–25) is plotted in Figure 192–41, which is provided for information only.

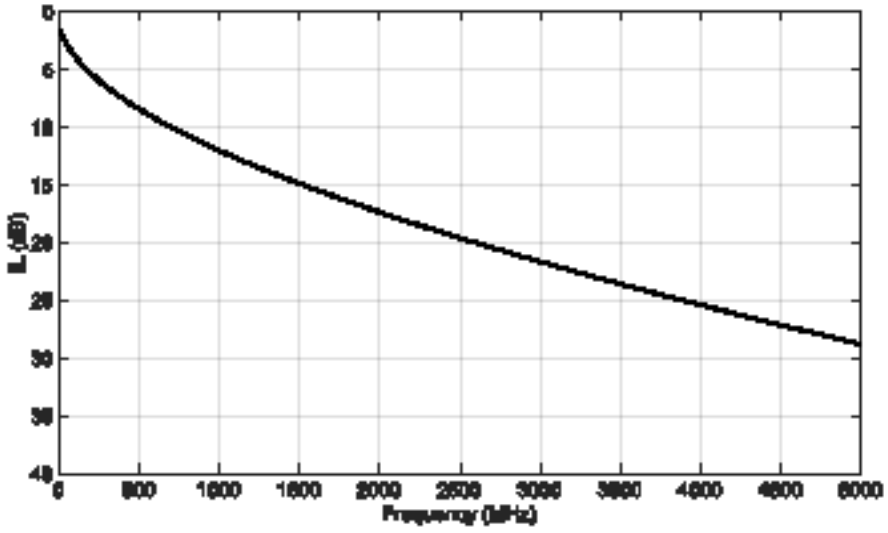



**Figure 192–41—V1 link segment insertion loss**

#### 192.8.1.2 Single ended characteristic impedance

The nominal characteristic impedance of a -V1 link segment is 50 Ω.

### 192.8.1.3 Return loss

The return loss of a -V1 link segment shall meet the values determined using Equation (192–26).

(192–26)

$$RL(f) \geq \begin{cases} 12.5 & 10 \leq f < 500 \\ 12.5 - 3\left\langle \frac{f-500}{1500} \right\rangle & 500 \leq f < 2000 \\ 9.5 - 3\left\langle \frac{f-2000}{2500} \right\rangle & 2000 \leq f < 4500 \\ 6.5 & 4500 \leq f \leq 5000 \end{cases} \text{ (dB)}$$

where

$f$ is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–26) is plotted in Figure 192–42, which is provided for information only.

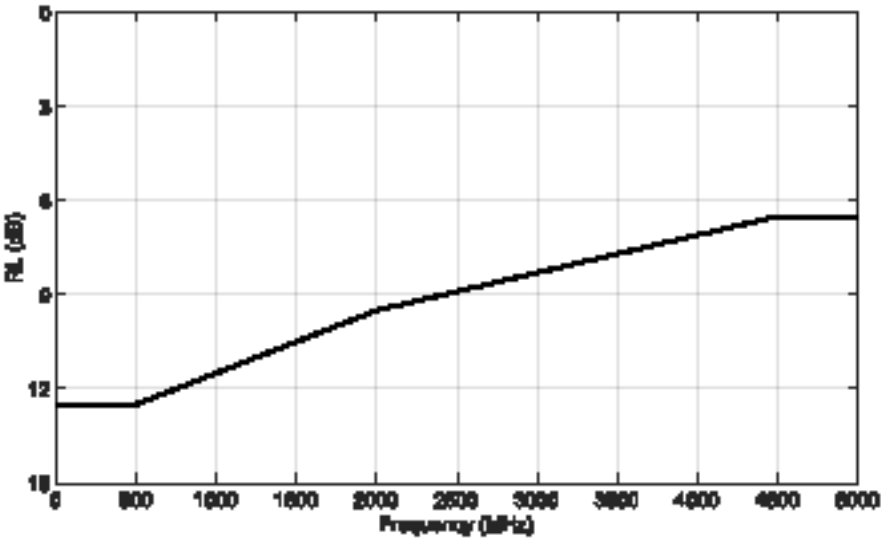



**Figure 192–42—V1 link segment return loss**

### 192.8.1.4 Coupling attenuation

Coupling attenuation is not defined for -V1 link segments.

#### 192.8.1.5 Screening attenuation

The screening attenuation of a -V1 link segment, measured in accordance with ISO 19642–11, shall meet the values determined using Equation (192–27). Additional screening attenuation test methodologies are defined in Annex 149A.

(192–27)

$$Screening\ attenuation(f) \geq \left\{ \begin{array}{ll} 64 & 10 \leq f < 3000 \\ 54 & 3000 \leq f \leq 5000 \end{array} \right\} \text{ (dB)}$$

where

$f$ is the frequency in MHz; $10 \leq f \leq 5000$

Equation (192–27) is plotted in Figure 192–43, which is provided for information only.

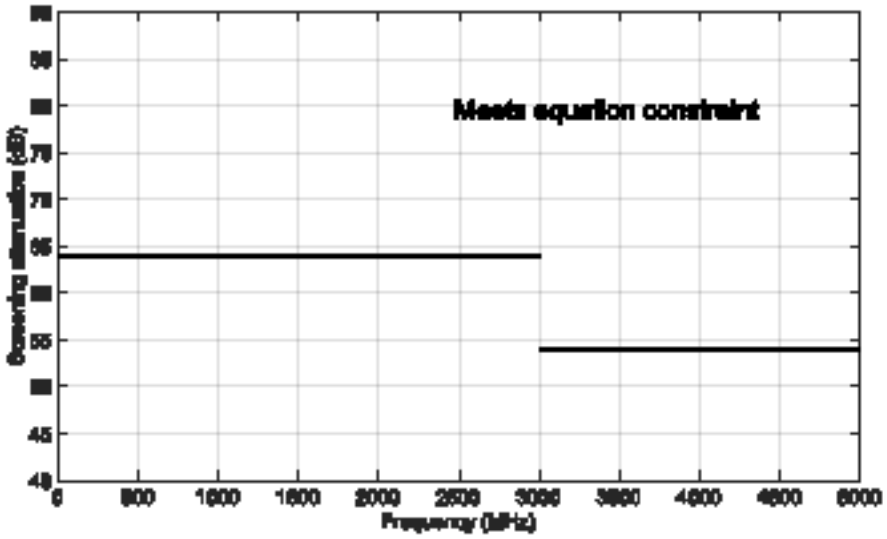



**Figure 192–43—V1 link segment screening attenuation**

#### 192.8.1.6 Maximum link delay

The propagation delay of a -V1 link segment shall not exceed 160 ns for all frequencies between 3 MHz and 4 GHz.

### 192.8.2 Coupling parameters between link segments

Noise coupled between the disturbed link segment and the disturbing link segment is referred to as alien crosstalk noise. Power sum alien near-end crosstalk (PSANEXT) loss and power sum alien attenuation to crosstalk ratio far-end (PSAACRF) are specified to limit the total alien NEXT and alien FEXT coupled between link segments. The test methodologies are specified in Annex 97B.

#### 192.8.2.1 Power sum alien near-end crosstalk (PSANEXT) loss

To ensure that the total alien NEXT loss coupled into a -V1 link segment is limited, multiple disturber alien NEXT loss is specified as the power sum of the individual alien NEXT loss disturbers.

PSANEXT loss is determined by summing the power of the individual -V1 alien NEXT loss values over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–28).

(192–28)

$$\mathrm{PSANEXT(f)} = -10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AN(f)_j}}{10}} \ \mathrm{dB}$$

where the function $\mathrm{AN}(f)_j$ represents the magnitude (expressed in dB) of the alien NEXT loss at frequency $f$ of the disturbing -V1 link segment $j$ (1 to $m$) for the disturbed -V1 link segment.

The PSANEXT loss between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (192–29).

(192–29)

$$\mathrm{PSANEXT}(f) \geq 54 - 10\log_{10}\left(\frac{f}{500}\right) \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $30 \leq f \leq 5000$

Equation (192–29) is plotted in Figure 192–44, which is provided for information only.

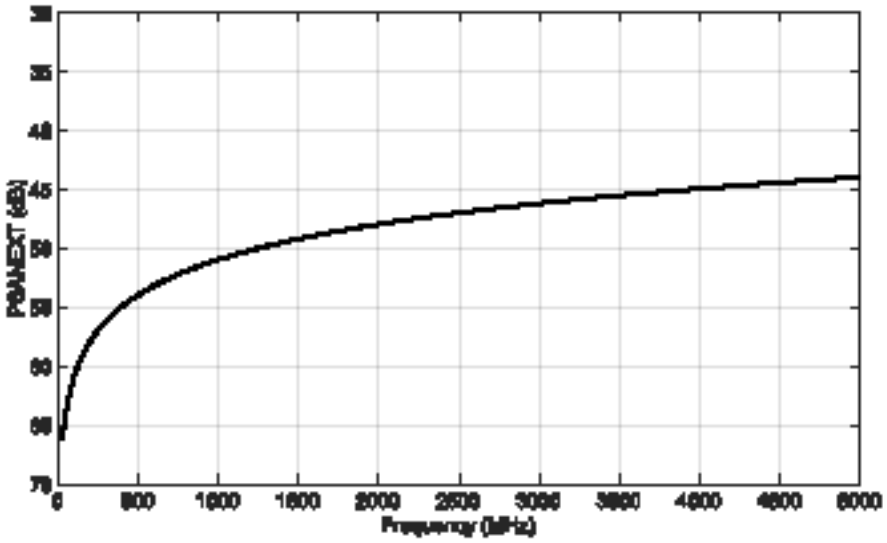



**Figure 192–44—V1 link segment PSANEXT loss**

### 192.8.2.2 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

To ensure that the total alien FEXT loss coupled into a -V1 link segment is limited, power sum AACRF is specified as the insertion loss of the disturbed link (in dB) subtracted from the multiple disturber alien FEXT loss of the individual disturbers.

Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) is determined by summing the power of the individual -V1 alien FEXT loss values and subtracting the insertion loss (in dB) of the disturbed link segment over the frequency range 30 MHz to 5000 MHz as follows in Equation (192–30).

(192–30)

$$\mathrm{PSAACRF(f)} = \left(-10\log_{10}\sum_{j=1}^{m} 10^{\frac{-\mathrm{AFEXT(f)}_j}{10}}\right) - \mathrm{IL_d(f)} \quad \mathrm{dB}$$

where

$f$ is the frequency in MHz; $30 \le f \le 5000$

$\mathrm{AFEXT}(f)_j$ is the magnitude of the alien FEXT loss at frequency $f$ from a disturbing -V1 link segment $j$ (1 to $m$) to the disturbed -V1 link segment in dB

$\mathrm{IL_d}(f)$ is the measured insertion loss of the disturbed link segment at frequency $f$ in dB

The PSAACRF between a disturbed -V1 link segment and the disturbing -V1 link segments shall meet the values determined using Equation (192–31).

(192–31)

$$\mathrm{PSAACRF}(f) \ge 51 - 9\log_{10}\left(\frac{f}{300}\right) \quad \text{(dB)}$$

where

$f$ is the frequency in MHz; $30 \le f \le 5000$

Equation (192–31) is plotted in Figure 192–45, which is provided for information only.

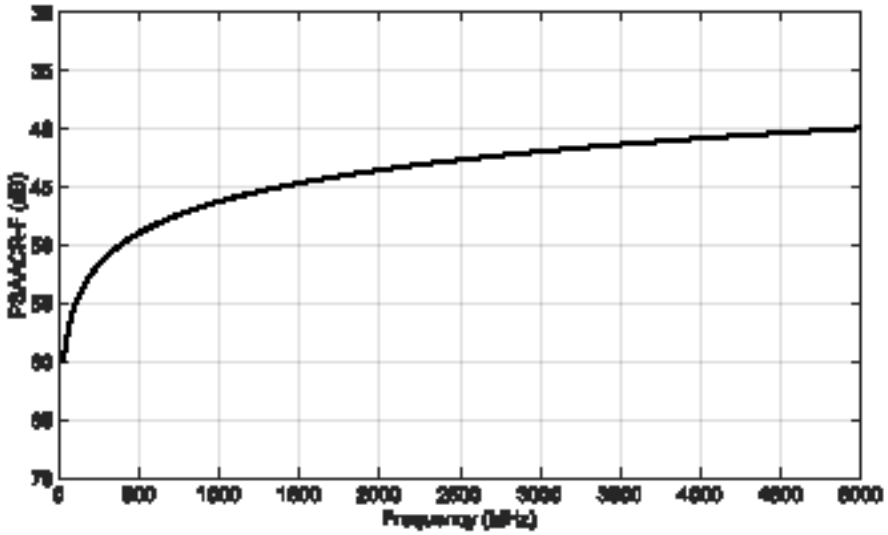


**Figure 192–45—M link segment PSAACRF**

## 192.9 MDI specification, -T1

MultiGBASE-AT1 is designed to operate over a single shielded balanced pair MDI (-T1) that meets the requirements specified in this subclause.

### 192.9.1 MDI connectors

The -T1 MDI connectors are as specified in 149.8.1.

### 192.9.2 MDI electrical specification

The electrical requirements specified in 192.5.2 and 192.5.3 shall be met when the PHY is connected to the -T1 MDI connector mated with a specified connector to a shielded balanced pair of conductors.

#### 192.9.2.1 MDI return loss

The differential impedance at the -T1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -T1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (192–32). For the -T1 PMD, a nominal differential characteristic is impedance of 100 Ω is used.

(192–32)

$$MDI\_Return\_Loss(f) \geq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)}$$

where

$f$ is the frequency in MHz; $10 \leq f \leq Fmax$
$Fmax$ = 3000 MHz for 100 Mb/s and 2.5 Gb/s data rate
= 4000 MHz for 1 Gb/s and 5 Gb/s data rate
= 4000 MHz for 7.5 Gb/s data rate
= 4000 MHz for 10 Gb/s data rate

Equation (192–32) is plotted in Figure 192–46, which is provided for information only.

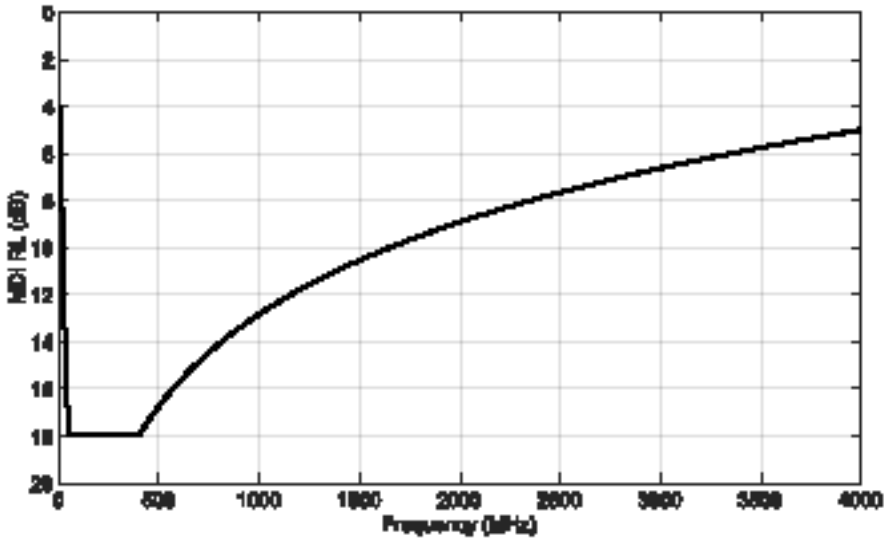



**Figure 192–46—T1 MDI return loss using Equation (192–32)**

#### 192.9.3 MDI fault tolerance

The -T1 MDI fault tolerance shall comply with 96.8.3.

## 192.10 MDI specification, -V1

MultiGBASE-AV1 is designed to operate over a single coaxial MDI (-V1) that meets the requirements specified in this subclause.

### 192.10.1 MDI connectors

The -V1 mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the -V1 mechanical interface is beyond the scope of this standard.

### 192.10.2 MDI electrical specifications

The electrical requirements specified in 192.5.2 and 192.5.3 shall be met when the PHY is connected to the -V1 MDI connector mated with a specified connector to a single coaxial cable.

#### 192.10.2.1 MDI return loss

The differential impedance at the -V1 MDI for each transmitter/receiver shall be such that any reflection due to signals incident upon the -V1 MDI from the cabling relative to the incident signal are per the relationship shown in Equation (192–33). For the -V1 PMD, a nominal differential characteristic is impedance of 50 Ω is used.

(192–33)

$$MDI\_Return\_Loss(f) \geq \begin{cases} 18 + 20\log_{10}\left(\frac{f}{50}\right) & 10 \leq f < 50 \\ 18 & 50 \leq f < 400 \\ 18 - 13\log_{10}\left(\frac{f}{400}\right) & 400 \leq f < Fmax \end{cases} \text{(dB)}$$

where

$f$ is the frequency in MHz; $10 \leq f \leq Fmax$

$Fmax$
= 3000 MHz for 100 Mb/s and 2.5 Gb/s data rate
= 4000 MHz for 1 Gb/s and 5 Gb/s data rate
= 4000 MHz for 7.5 Gb/s data rate
= 4000 MHz for 10 Gb/s data rate

Equation (192–33) is plotted in Figure 192–47, which is provided for information only.

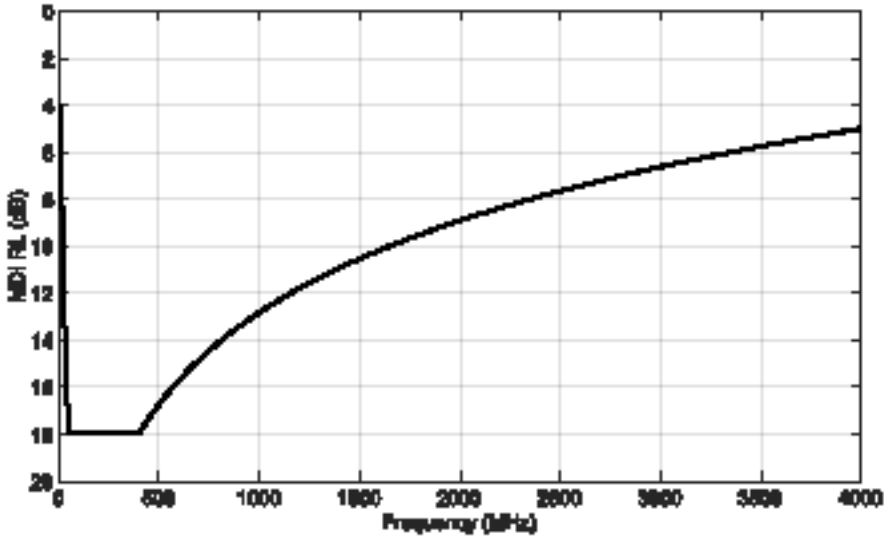



**Figure 192–47—MDI return loss using Equation (192–33)**

### 192.10.3 MDI fault tolerance

The coaxial cable interface of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of the center conductor to the shield, ground potential, or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 192–23, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed.

The single conductor of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

**Table 192–23—Connection fault**

| Center conductor | Shield |
|---|---|
| No fault | Ground |
| MDI + | Ground |
| Ground | Ground |
| +50 V dc | Ground |

## 192.11 Environmental specifications

### 192.11.1 General safety

All equipment subject to this clause is expected to conform to all applicable local, state, national, and application-specific standards.

### 192.11.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner.

#### 192.11.2.1 Environmental safety

All equipment subject to this clause, when used in the automotive environment, is expected to conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750–1
b) Electrical loads: ISO 16750–2, ISO 7637–2:2008, and ISO 8820–1
c) Mechanical loads: ISO 16750–3, ASTM D4728, and ISO 12103–1
d) Climatic loads: ISO 16750–4, IEC 60068–2–1, IEC 60068–2–27, IEC 60068–2–30, IEC 60068–2–38, IEC 60068–2–52, IEC 60068–2–64, and IEC 60068–2–78
e) Chemical loads: ISO 16750–5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial and industrial environments. The target automotive, industrial, or commercial environment(s) require careful analysis prior to implementation.

### 192.11.3 Electromagnetic compatibility

A system integrating a PHY intended for automotive applications is expected to comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements for the limitation of electromagnetic interference. When used in an automotive environment, the PHY is expected to meet the following motor vehicle EMC requirements:

a) Radiated/conducted emissions: CISPR 25, IEC 61967–1, IEC 61967–4, and IEC 61000–4–21
b) Radiated/conducted immunity: ISO 11452, IEC 62132–1, IEC 62132–4, and IEC 61000–4–21
c) Electrostatic discharge: ISO 10605, IEC 61000–4–2, and IEC 61000–4–3
d) Electrical disturbances: IEC 62215–3, ISO 7637–2, and ISO 7637–3

Exact test setup and test limit values may be adapted to each specific application.

## 192.12 Delay constraints

In full duplex mode, predictable operation of the MAC Control PAUSE operation (see Clause 31 and Annex 31B) also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices.

The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 192–24. Transmit data delay is measured from the input of a given unit of data at the XGMII to the presentation of the same unit of data by the PHY to the MDI. Receive data delay is measured from the input of a given unit of data at the MDI to the presentation of the same unit of data by the PHY to the XGMII.

NOTE—The physical medium interconnecting two PHYs introduces additional delay in a link.

**Table 192–24—Delay Limits**

| Transmit MAC data rate | Bit times | Pause quanta | Delay (ns) |
|---|---|---|---|
| LS path: 100 Mb/s | 1 536 | 3 | 15 360 |
| LS path: 1 Gb/s | 8 704 | 17 | 8 704 |
| 2.5 Gb/s | 5 120 | 10 | 2 048 |
| 5 Gb/s (+100 Mb/s) | 10 240 | 20 | 2 048 |
| 5 Gb/s (+1 Gb/s) | 15 360 | 30 | 3 072 |
| 7.5 Gb/s (+100 Mb/s) | 15 360 | 30 | 2 048 |
| 7.5 Gb/s (+1 Gb/s) | 30 480 | 40 | 4 096 |
| 10 Gb/s | 20 480 | 40 | 2 048 |

## 192.13 Protocol implementation conformance statement (PICS) proforma for Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1[13]

### 192.13.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

### 192.13.2 Identification

#### 192.13.2.1 Implementation identification

| | |
|---|---|
| Supplier[1] | |
| Contact point for inquiries about the PICS[1] | |
| Implementation Name(s) and Version(s)[1,3] | |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2] | |
| NOTE 1—Required for all implementations.<br>NOTE 2—May be completed as appropriate in meeting the requirements for the identification.<br>NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model). | |

#### 192.13.2.1

#### 192.13.2.2 Protocol summary

| | |
|---|---|
| Identification of protocol standard | IEEE Std 802.3xx-202x, Clause 192, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1 |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS | |
| Have any Exception items been required? No [ ] Yes [ ]<br>(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3xx-202x.) | |

[13] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

| | |
|---|---|
| Date of Statement | |

**192.13.2.2**

### 192.13.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| | | | | | Yes [ ]<br>No [ ] |
| | | | | | Yes [ ] |

**192.13.3**

### 192.13.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer, and baseband medium, type MultiGBASE-AT1 and MultiGBASE-AV1

#### 192.13.4.1 PMD functional specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| | | | | | Yes [ ] |
| | | | | | Yes [ ]<br>No [ ] |
| | | | | | Yes [ ]<br>No [ ]<br>N/A [ ] |

**192.13.4.1**

#### 192.13.4.2 Management functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| | | | | | Yes [ ]<br>N/A [ ] |
| | | | | | Yes [ ]<br>No [ ]<br>N/A [ ] |

**192.13.4.2**