

ACT Jitter Requirements for Camera PHY

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Introduction

- › Crystal-less operation at the camera is an important feature for 802.3dm PHYs
- › This presentation introduces jitter requirements that have the flexibility to allow crystal-less design on the camera side, yet tight enough to allow reliable link operation

Proposed Jitter Requirements

For the “camera side” clock follower PHY, the total RMS jitter shall be less than 6ps and the RMS jitter shall be less than 3ps for jitter frequencies greater than 100kHz. This requirement is verified in test mode 1.

Note: the term “camera side” should be replace with the appropriate 802.3dm nomenclature

Assumptions and Explanation

The proposed requirements are based on

- Measurements of real PLL, with 100kHz PLL bandwidth, showing that it can support this requirement, assuming that the input jitter is no more than 50ps RMS
- Experiments with ACT test chips in crystal-less configuration show that the link can operate reliably under these conditions

PLL Jitter Estimate

The output jitter from the PLL can be estimated as

$$J_{out} = J_{in} \sqrt{\frac{F_{pll}}{F_{signal}}} + J_{vco}$$

where

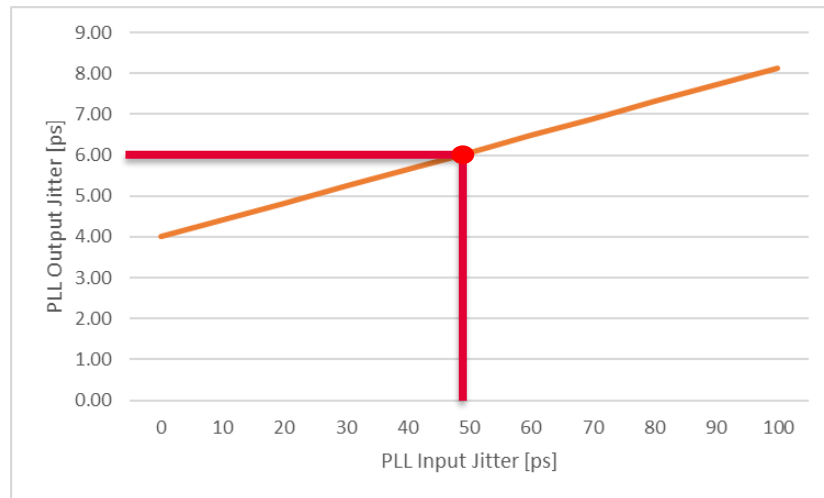
- › J_{in} is the input jitter into the PLL
- › J_{out} is the output jitter from the PLL
- › J_{vco} is the PLL VCO intrinsic jitter
- › F_{pll} is the PLL bandwidth
- › F_{signal} is the Nyquist frequency of the clock edge signal (half the edge rate)

PLL Jitter for ACT

For a 117MHz edge rate and 100kHz PLL bandwidth the slope becomes

$$h = \sqrt{\frac{F_{pll}}{F_{signal}}} = \sqrt{\frac{100kH}{58.5MHz}} = 0.041$$

The plot on the right shows example relationship between PLL input and output jitter, assuming PLL bandwidth of 100kHz, edge rate of 117MHz, and VCO jitter of 4ps.



Summary

- › Jitter requirements for ACT camera side PHY in clock follower (slave) mode was introduced
- › The proposed requirements were based on measured PLL characteristics and evaluation of ACT test chip in crystal-less operation



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