PIN-OPTIMIZED PHY INTERFACES • P802.3dq

Asymmetric 25GAUI: Two Paths Forward

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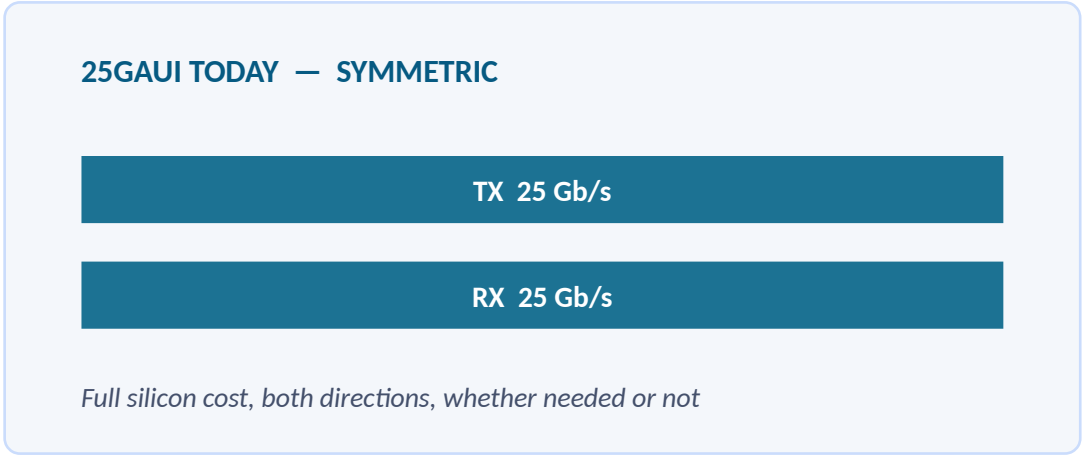
The Problem

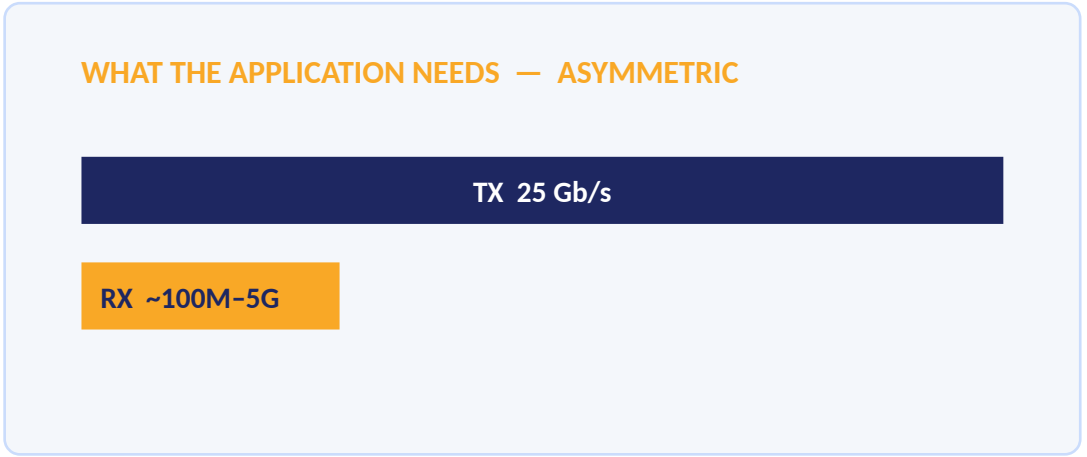
25GAUI is a fixed, symmetric interface — real traffic increasingly isn't

25GAUI defines a single lane running at 25 Gb/s in **both directions, all the time**.

Growing classes of endpoints — sensor and camera links, display links, zonal control links — need **high bandwidth one way and only a trickle the other** (e.g. video/point-cloud downstream, control & status upstream).

Because both directions must be provisioned for full 25G, 25GAUI pays the full SerDes power and complexity cost **in a direction the application doesn't need** — roughly a 250× rate mismatch (25G vs. ~100M) absorbed as if it were symmetric.





Why It Matters Now

Ethernet is losing asymmetric design wins to interfaces built for exactly this

MIPI D-PHY

High-Speed mode for payload plus separate Low-Power/control and Escape modes. Lean pin budget because it never provisions symmetric bandwidth it won't use.

eDP / DP

Main link is one-way by design; a bidirectional AUX channel handles control. Efficient because direction and rate match the use case.

25GAUI

Same silicon cost in both directions regardless of traffic shape — a structural disadvantage for sensor, camera, and display links.

The risk: as automotive and edge designs standardize on asymmetric links, a symmetric-only 25GAUI is progressively designed out of exactly the sockets 802.3dq is chartered to win back with pin- and cost-optimized interfaces.

Sources: VESA DisplayPort technical overview (bidirectional AUX channel); MIPI D-PHY specification (High-Speed / Low-Power / Escape modes).

Interface Comparison

Pin count and directionality — figures as compiled by presenter, to be confirmed against current specs

Interface	Signal Pins	Directionality	Notes
25GAUI (today)	4 (1 TX + 1 RX pair)	Symmetric, fixed 25G/25G	No native way to shed cost when upstream needs are minimal
MIPI D-PHY	10 / 12 (config-dependent)	Asymmetric by design	Pin count set by lane config, not by matching a symmetric ceiling
eDP / DP	10 main link + 2 AUX	One-way main link + light AUX	AUX carries control/status only — no full-rate return path

The pattern: MIPI and eDP/DP both spend their pin budget in proportion to actual traffic need. 25GAUI spends it on a fixed, symmetric ceiling — costing pins, power, and silicon area that go unused on links that are inherently one-way heavy.

Source: IEEE 802.3by (25G-AUI / 25GAUI origin, 2016).

Where This Fits in 802.3

dq has the logical vocabulary; dm has the closest precedent — at less than half the rate

P802.3dq — Pin-Optimized PHY Interfaces

Has: scalable logical interface, MDIO-over-pins, AN, EEE, GMII/XGMII compatibility.
Gap: current electrical objectives are capped at ≤100 Mb/s — no hook today for a 25G-class forward path.

P802.3dm — Asymmetrical Electrical Automotive Ethernet

Has: an already-adopted asymmetric architecture for automotive camera links — forward up to 10 Gb/s with a lower-rate reverse.
Gap: tops out at 10 Gb/s forward — doesn't yet reach the 25G class this proposal targets.

The gap: neither task force currently covers a 25G-class forward / low-rate reverse profile. This needs an explicit scope decision — extend dm's model to 25G, or have dq carry a rate-agnostic logical hook that either task force's electrical work can plug into.

Two Paths Forward

Two candidate directions for the reverse path — not mutually exclusive, but worth separating

OPTION A

Negotiated Rate-Adaptive PMA

Auto-negotiation selects a TX/RX rate pair per link; the SerDes reconfigures accordingly.

Strengths

- Maximum flexibility — supports many reverse-rate classes without new profiles
- Falls back to standard symmetric 25GAUI automatically for non-supporting peers
- One mechanism scales across future use cases

Trade-offs

- More complex PMA / AN state machine to specify and validate
- Longer path to a testable, interoperable spec

OPTION B

Fixed Low-Rate Reverse Profile

Defines one small, fixed reverse electrical mode (~100M–1G class) alongside the full 25G forward path.

Strengths

- Simpler to specify and validate — one defined mode, not a negotiation space
- Closer to precedent already adopted in dm
- Faster path to a testable spec and early interop

Trade-offs

- Less flexible — a new profile needed for each reverse-rate class
- May need revisiting as reverse bandwidth needs evolve

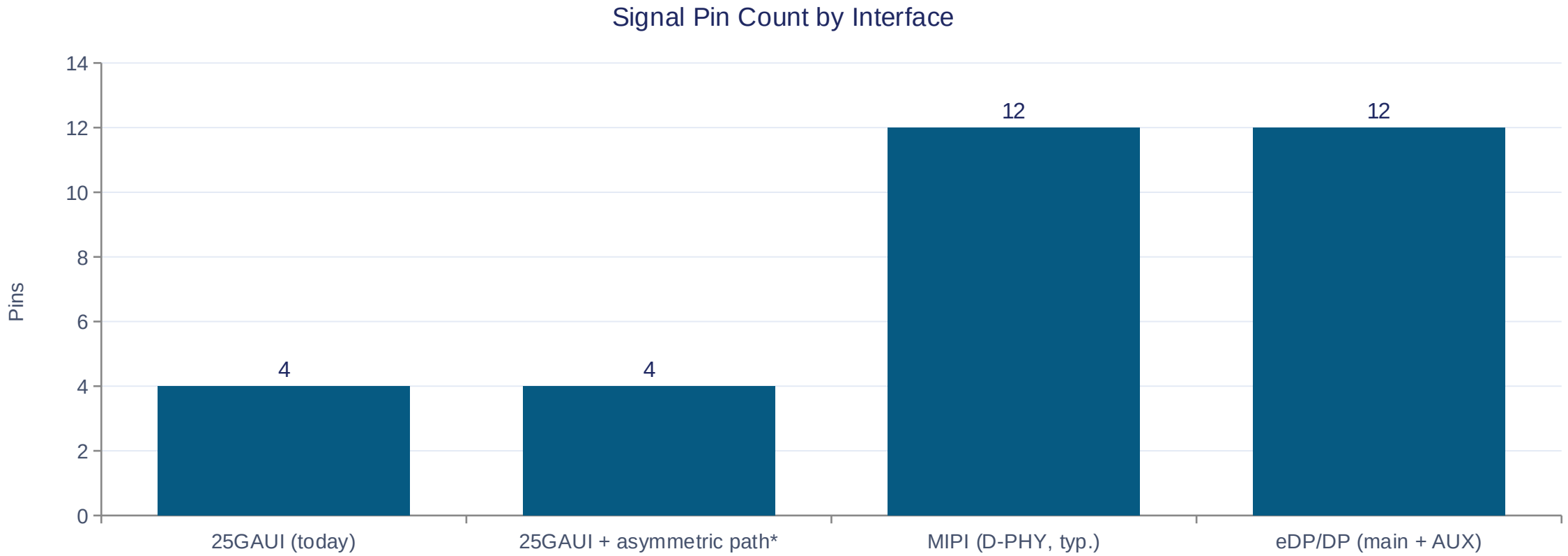
What Needs to Be Specified

A minimum viable profile — the same five items apply whichever path the group picks

1	**Independent direction rates**	A way for the MAC/PHY boundary to express forward and reverse rates separately, whether negotiated (A) or fixed (B).
2	**Low-rate reverse electrical option**	A defined lower-rate mode for the reverse SerDes path — negotiated range under Option A, single mode under Option B.
3	**Control + MDIO sideband mapping**	Map management, AN, and MDIO traffic onto the reverse path without assuming full 25G capability.
4	**Timestamps + status metadata**	Carry timestamp/control/status metadata across the rate mismatch without forcing a 25G reverse tax.
5	**AN / EEE / fault semantics**	Define idle, backpressure, and fault behavior cleanly across mismatched forward/reverse rates.

Competitive Positioning

Illustrative pin-count comparison — 25GAUI today vs. either asymmetric path



**Both Option A and Option B keep the existing 4-pin 25GAUI footprint — the gain is power/cost per link, not fewer pins. Shown alongside pin-count leaders for context.*

Call to Action

Suggested objective language

"Do not preclude a logical interface profile that supports independent transmit and receive data rates, including high-speed forward transport with a lower-rate reverse path, while preserving Ethernet frame, preamble, management, and timestamp semantics."

1. Confirm interest: does the group see value in an asymmetric-capable 25G-class interface for pin-optimized applications?
2. Decide the technical direction: negotiated rate-adaptive PMA (A), fixed low-rate reverse profile (B), or both in sequence?
3. Clarify scope ownership with 802.3dm liaison so a 25G extension doesn't duplicate or conflict with existing work.

Thank you — questions and discussion welcome.