Meeting Minutes: IEEE P802.3dq Pin-Optimized PHY Interface (POPI) Task Force

July 14, 2026
Interim

Prepared by George Zimmerman & Chad Jones

IEEE 802.3 Pin-Optimized PHY Interface (POPI) Study Group meeting was convened at 08:05 EDT, Tuesday, July 14, 2026, by Jason Potterf, IEEE 802.3 POPI Task Force Chair

All times are in EDT

Attendance is listed in Appendix A

Mr. Potterf reminded the group of the IEEE SA individual participation policy, and front matter and asked if everyone had reviewed the materials as was requested in the meeting announcement. There were affirmative responses, and no questions.

Presentation: POPI_Agenda_2026-07-14_v02.pdf
Presenter: Jason Potterf, Chair.

08:07 The Chair reviewed the agenda. Mr. Potterf turned to the presentation and reviewed the agenda. Mr. Potterf asked if there were any modifications to the agenda, none responded, and he noted that he considered the agenda approved.

The Chair then resumed the review of POPI_Agenda_2026-07-14_v02.pdf:

- Mr. Potterf asked if anyone was attending from the press including those who would run a public blog on this meeting – none responded. (08:09)
- Mr. Potterf noted that there should be no recording or photography without permission.

Mr. Potterf continued review of the presentation including access to the reflector and website, and ground rules.

Mr. Potterf advised the group of the IEEE meeting attendance tool and procedures.

08:11 Mr. Potterf reviewed the IEEE Structure and where to find the governing (IEEE-SA and below) rules and procedures documents.

IEEE Patent Policy, Mr. Potterf showed the patent slides and made the request for potentially essential patents at 08:12. None responded. Mr. Potterf completed reading the patent slides.

Mr. Potterf showed the IEEE-SA Copyright policy, Participant Behavior, Individual Process, “Fair and Equitable Consideration”, SA meeting rules, and the Ethics reporting line slides in the agenda deck and asked if there were any questions. No one responded.

Mr. Potterf reviewed the standards development process for IEEE and where this Task Force is in the process.

Mr. Potterf then advised the group that they had objectives and these had been approved by the Working Group, and he planned to discuss whether these needed addition or modification during the meeting.

Mr. Potterf reminded the group of upcoming meetings.

Future Meetings:

- September 2026 IEEE 802.3 Interim in Lisbon, Portugal
- POPI Meeting Timeslot (8 am Pacific US for 2 hours) on Tuesday ??, 2026

(Note – the presentation erroneously listed that the Lisbon, Portugal meeting was in July…)

PRESENTATIONS

08:19
Title: Symbol Encoding for POPI for 10/100M PHYs
URL: https://www.ieee802.org/3/dq/new/public/2026-07-14/Murray_3dq_01_07142026_v02.pdf
Presenters: Brian Murray, Jacobo Riesco – Analog Devices
Abstract: The presenter discussed potential approaches to encoding of signals on a 4-pin interface to support both single 10M or 100M PHYs and multi-port (Quad or Octal) PHYs, including higher speeds. The presentation began with a summary of previous presentations and focused on data encoding using 8B/9B encoding with scrambling, for 10Mb/s and 100 Mb/s operation. He discussed how this related to 8B/10B or 64B/65B encoding that were common. He additionally discussed latency, including interleaving, and how the proposed techniques achieved low latency.

Discussion: During discussion the presenter clarified that the 8B/9B encoding was only for PHY data rates less than 100 Mb/s and that he would stick with 64B/65B encoding at 1 Gb/s and higher if needed. He also explained that there were several unallocated control codes for future expandability. He also explained that, should the group wish, 8B/10B could be used in place of 8B/9B but with additional overhead.

(09:01)
The group consented to adjusting the order of presenters to better fit the flow, and Mr. Potterf’s presentation was hear next
9:03 The Chair asked George Zimmerman to chair the meeting while he presented.

09:04
Title: POPI SerDes Rate Survey
URL: https://www.ieee802.org/3/dq/new/public/2026-07-14/POPI_Potterf_SerDes_Staircase_2026-07-14_v01.pdf
Presenter: Jason Potterf – Cisco Systems
Abstract: The presenter discussed available SerDes rates using readily available IP for use with POPI. He then discussed how this related to numbers of ports and effective sideband channel bandwidth. He noted that the encodings presented did not anticipate Mr. Murray's presentation using 8B/9B, but could easily be adapted. He outlined existing SerDes rates scalable to multi-port at 10 Gb/s, and a methodology to expand as technology improved.

09:15 Discussion: General questions were asked and answered.

09:26
(At this point, Chad Jones assumed duties as recording secretary, and George Zimmerman returned Chair duties to Mr. Potterf.)

09:27
Title: Partitioning RS functions with POPI
URL: https://www.ieee802.org/3/dq/new/public/2026-07-14/zimmerman_3dq_01_0726.pdf
Presenter: George Zimmerman – CME Consulting
Abstract: The presenter described how several IEEE 802.3 RS functions that are tightly coupled to the PHY are often implemented on the PHY side of the xMII boundary. The presentation suggested that POPI could provide a cleaner architecture by defining MAC-side and PHY-side POPI RS layers that encode/decode primitives across the POPI physical interface, potentially using a macroframe structure for extensibility. The discussion focused on whether POPI can serve as a generic PCS abstraction layer, what PHY-side shim functions are needed, and which primitives should be generic versus application-specific.

09:41 Discussion: General questions were asked and answered.

10:03 Morning break

10:30 return from break
(At this point, George Zimmerman resumed duties as recording secretary)

Title: Asymmetric 25GAUI: Two Paths Forward
URL: https://www.ieee802.org/3/dq/new/public/2026-07-14/Houck_25GAUI_Rate_Adaptive_PMA-1.pdf
Presenter: TJ Houck - Infineon
Abstract: The presenter discussed the question of whether the transmit and receive directions of the interface should always use the same data rate. He clarified that it

wasn't a proposal to adopt a 25 Gb/s interface. He discussed existing non-Ethernet asymmetric interface solutions in the market that Ethernet should consider meeting to have competitive advantage. He offered a potential objective to support independent transmit and receive data rates.
(10:52)
Discussion: Questions were asked and answered. One participant suggested that deciding startup procedures might be important to consider in adding asymmetric interface rates.

Following discussion, two straw polls were offered by the presenter
Straw Poll 1
Should the 802.3dq scalable logical interfaces permit different MAC data rates in the transmit and receive directions?
Y: 15
N: 1
A: 4

Straw Poll 2
Should asymmetric operation be based on standardized transmit/receive rate profiles rather than arbitrary, independently selected transmit and receive rates?
Y: 14
N: 3
A: 6

The chair then returned to the POPI_Agenda_2026-07-14_v02.pdf and moved into a review of the updated objectives from the Munich meeting (slides 43-46). During discussion a proposed objective was added (to slide 46) to reflect the previous presentation.
Edits were made to the proposed objectives on slide 46 and those edits are shown in the revised version POPI_Agenda_2026-07-14_v03.pdf

(11:44 AM)
MOTION #1
Move to approve the objectives shown on slides 44, 45, and 46 of POPI_Agenda_2026-07-14_v03.pdf.
M: Jon Lewis
S: Luisma Torres
Technical (>=75%)
MOTION PASSES BY VOICE WITHOUT OBJECTION (11:47 AM)
The Chair then discussed possible contributions which would be useful for future discussion (slide 48)

Having exhausted the agenda, the meeting was adjourned at **11:48 AM EDT.**

Appendix A: Attendees at the IEEE P802.3dq Pin-Optimized PHY Interface (POPI) Task Force Meeting, July 14, 2026.

Name	Affiliation
Andrew Law	University of Strathclyde
Ariel Lasry	Qualcomm Technologies, Inc
Ben Mecklenburg	Huawei Technologies Duesseldorf GmbH
Brian Mowad	Cisco
Brian Murray	Analog Devices Inc.
Carlo Salata	Canova Tech
Chad Jones	Cisco Systems, Inc.
Christopher R Cole	Coherent Corp.
David Law	Hewlett Packard Enterprise
Eiichiro Oishi	Yazaki Corporation
Geoffrey Thompson	INDEPENDENT
George Zimmerman	CME Consulting; Analog Devices; Cisco; Eliyan; Infineon; OnSemi; Sony
Guy Hutchison	NXP Semiconductors
Gyudong Kim	Analog Devices Inc.
Hans Lackner	QoSCom GmbH
Heiko Strohmeier	Robert Bosch GmbH
Hideki Goto	Toyota Motor Corporation
Jae-Yong Chang	Keysight Technologies Inc
James Withey	Fluke Corporation
Jason Potterf	Cisco Systems, Inc.
Joerg Kock	NXP Semiconductors
Jon Lewis	Dell Technologies
Joseph Cordaro	Infineon Technologies
Karl Budweiser	BMW AG; BMW Group
Luisma Torres	KD
Markus Jochim	General Motors Company
Martin Gubow	Keysight Technologies
Masato Shiino	FURUKAWA ELECTRIC
Mehmet Tazebay	Broadcom Corporation
Michael Chandler-Page	Cirrus Logic
Natalie Wienckowski	IVN Solutions LLC; Ethernovia, Bosch
Nicholas Chimento	Analog Devices Inc.
Paul Vanderlaan	Panduit Corp.
Peter Jones	Cisco Systems, Inc.
Pusik Park	Korea Electronics Technology Institute (KETI); Korea Electronics Technology Institute (KETI); Korea Electronics Technology Institute (KETI); Korea Electronics Technology Institute (KETI)
Rich Boyer	Aptiv Signal and Power Solutions

Scott Muma	Microchip Technology, Inc.
Stephan Schreiner	Rosenberger
Terry Wei	Analog Devices Inc.
Tim Baggett	Microchip Technology, Inc.
Tingting Zhang	Huawei Technologies Co., Ltd
TJ Houck	Infineon Technologies
Valerie Maguire	Copperopolis (aff'l with CME Consulting and Cisco)
Xuebo Wang	Huawei
Yongbum Kim	General Motors Company
Yue Zhu	Huawei Technologies Co., Ltd
Yutao Wang	Rockwell Automation
Yuxuan Tan	Motorcomm