POPI SerDes Rate Survey

An Unauthoritative Look at Publicly Documented Options in the Market

Jason Potterf, Cisco

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SerDes Speed Impact on POPI

POPI has two basic objectives that are impacted by the SerDes IP market:

1. Define a scalable logical interface that can support arbitrary port speeds and counts while retaining as many of the features in our Feature Objectives as possible.

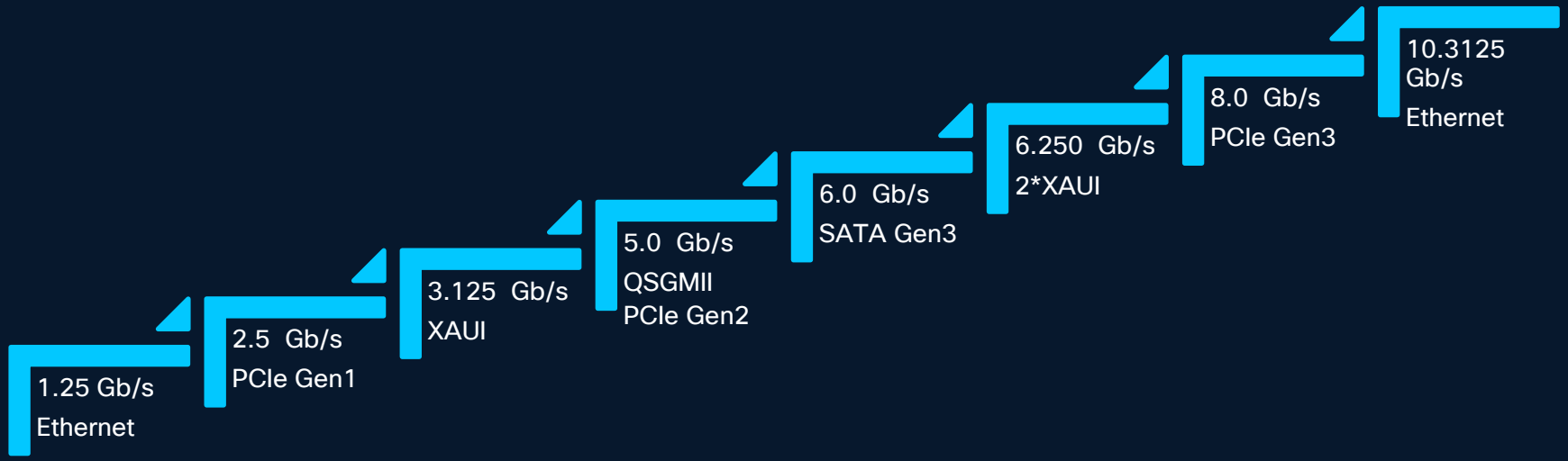
3. Define an electrical interface to provide connectivity to 8 ports using 6 or fewer pins, each port with MAC data rates up to 100 Mb/s.

   a) Provide eight-port connectivity with an electrical interface speed not to exceed 2 Gb/s.

To achieve these objectives, we need to define a SerDes rate “staircase” which includes:

- A step between 800 Mb/s and 2 Gb/s
- Additional steps at desirable port count and speed combinations
- Steps that are readily implementable using SerDes IP already in the market
- Compatibility with readily available FPGAs that include SerDes capabilities will help adoption

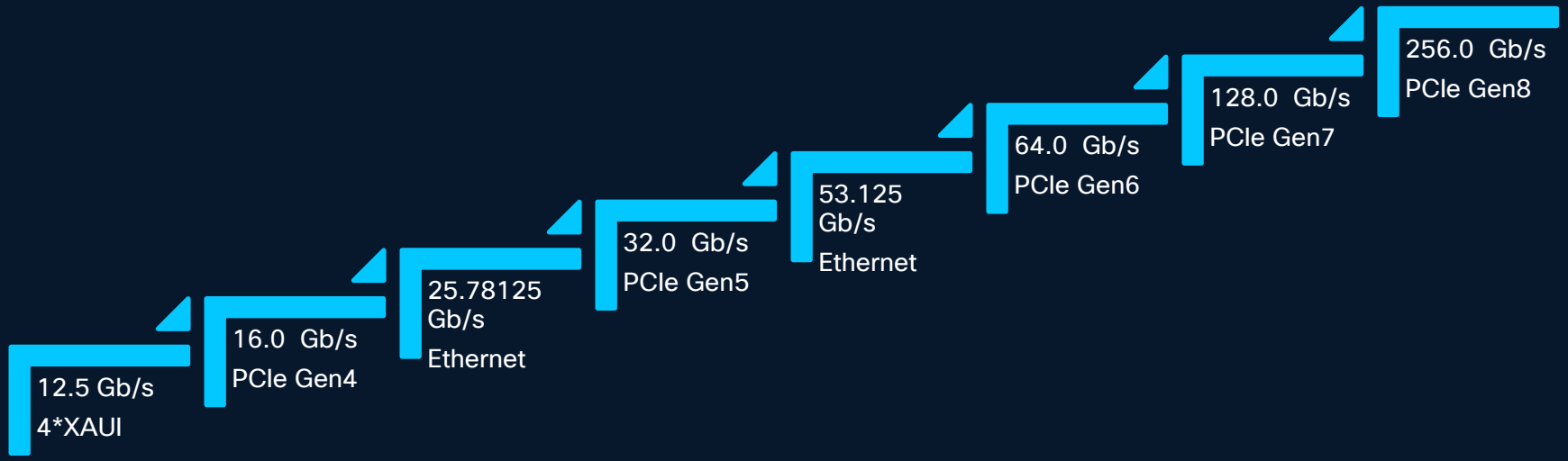
Available Rate Steps Up to 10 Gb/s



Port / Speed Table with Sideband Calculation, up to 10 Gb/s

Max Port Speed (Mb/s)	# of Ports	Sideband Ratio	PCS Input Rate (Mb/s)	Encoding	Encoding ratio	SerDes Rate (Gb/s)	Source	Sideband Effective Bandwidth	Sideband Bandwidth per Port
100	8	1.25	1,000	8b/10b	1.25	1.25	Eth	200	25
100	16	1.25	2,000	8b/10b	1.25	2.5	PCIe	400	25
1,000	2	1.25	2,500	8b/10b	1.25	3.125	Eth	500	250
1,000	4	1.0	4,000	8b/10b	1.25	5.0	Eth/ PCIe	-	-
1,000	4	1.2	4,800	8b/10b	1.25	6.0	SATA	800	200
1,000	4	1.25	5,000	8b/10b	1.25	6.250	~Eth	1,000	250
1,000	4	1.6	6,400	8b/10b	1.25	8.0	PCIe	2,400	600
1,000	8	1.03125	8,250	8b/10b	1.25	10.3125	Eth	250	31
1,000	8	1.25	10,000	64b/66b	1.03125	10.3125	Eth	2,000	250

Available Rate Steps Beyond 10 Gb/s



Example Port / Speed Table with Sideband Calculation

Max Port Speed (Mb/s)	# of Ports	Sideband Ratio	PCS Input Rate (Mb/s)	Encoding	Encoding ratio	SerDes Rate (Gb/s)	Source	Sideband Effective Bandwidth	Sideband Bandwidth per Port
1,000	8	1.515152	12,121	64b/66b	1.03125	12.500	~Eth	4,121	515
2,500	4	1.551515	15,515	64b/66b	1.03125	16.0	PCIe	5,515	1,379
2,500	8	1.25	25,000	64b/66b	1.03125	25.78125	Eth	5,000	625
5,000	4	1.551515	31,030	64b/66b	1.03125	32.0	PCIe	11,030	2,758
5,000	8	1.25	50,000	257/256b	1.0625	53.125	Eth	10,000	1,250
5,000	8	1.551515	62,061	64b/66b	1.03125	64.0	PCIe	22,061	2,758
10,000	8	1.551515	124,121	64b/66b	1.03125	128.0	PCIe	44,121	5,515
10,000	16	1.551515	248,242	64b/66b	1.03125	256.0	PCIe	88,242	5,515

Head to Head – Ethernet vs PCIe Rate Staircases

Max Port Speed (Mb/s)	# of Ports	Sideband Ratio	PCS Input Rate (Mb/s)	SerDes Rate (Gb/s)	Source
100	8	1.25	1,000	1.25	Eth
1,000	2	1.25	2,500	3.125	Eth
1,000	4	1.0	4,000	5.0	Eth
1,000	4	1.25	5,000	6.250	Eth
1,000	8	1.03125	8,250	10.3125	Eth
1,000	8	1.25	10,000	10.3125	Eth
1,000	8	1.515152	12,121	12.500	Eth
2,500	8	1.25	25,000	25.78125	Eth
5,000	8	1.25	50,000	53.125	Eth

Max Port Speed (Mb/s)	# of Ports	Sideband Ratio	PCS Input Rate (Mb/s)	SerDes Rate (Gb/s)	Source
100	8	N/A	N/A	N/A	PCIe
100	16	1.25	2,000	2.5	PCIe
1,000	4	1.0	4,000	5.0	PCIe
1,000	4	1.6	6,400	8.0	PCIe
2,500	4	1.551515	15,515	16.0	PCIe
5,000	4	1.551515	31,030	32.0	PCIe
5,000	8	1.551515	62,061	64.0	PCIe
10,000	8	1.551515	124,121	128.0	PCIe
10,000	16	1.551515	248,242	256.0	PCIe

Concluding Thoughts

- Ethernet Rate Compatible SerDes
  - Rates serve the low end well
  - Rate progression more irregular
  - More familiar to target implementers

- PCIe Rate Compatible SerDes
  - Rates serve the high end well
  - Rates provide more sideband on average
  - Doubling rate progression provides evenly spaced “stairs”
  - Unclear if SerDes are easily separable from PCIe-specific features

Questions and Discussion