PIN-OPTIMIZED PHY INTERFACES • P802.3dq

An Asymmetric Logical Profile for POPI

25 Gb/s one direction, 100 Mb/s the other — the case, the scope, and the open questions

TJ Houck | Infineon

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What July Established

An adopted objective and two straw polls — stated precisely

ADOPTED OBJECTIVE — JULY 2026

"Do not preclude a logical interface profile that supports independent transmit and receive data rates…"

This preserved the architectural option. It did not approve any rate pair, any profile, or a 25G electrical interface.

Straw poll 1 — permit independent TX/RX rates?

Y: 15 N: 1 A: 4

Support for the principle.

Straw poll 2 — standardized profiles over arbitrary rates?

Y: 14 N: 3 A: 6

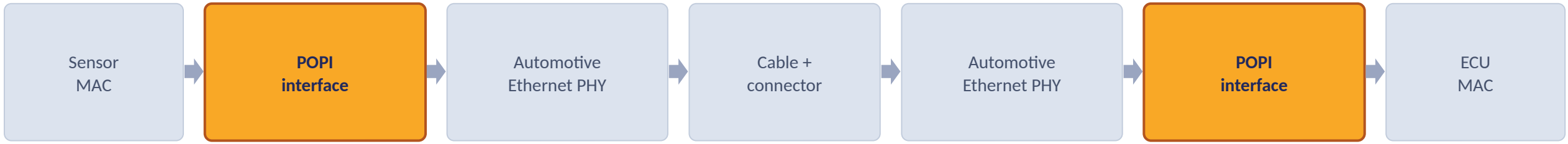
Preference for fixed profiles.

Where that leaves us. July established Task Force interest and preserved independent transmit and receive rates within the dq architecture. It did not select a profile. This contribution proposes a fixed asymmetric profile as the next technical baseline and asks the Task Force whether to develop it.

Scope: What dq Standardizes

P802.3dq defines interfaces between a MAC and a PHY. It does not define the media link.

PAR 5.2.b — "additions and modifications to IEEE Std 802.3 to add one or more new interfaces between a MAC and a PHY optimized for exposed interconnects."



This proposal applies here — and only here

What this means for the claims in this deck. The pin, power and area savings discussed here are savings at the MAC-PHY interface on each endpoint. Reaching the ECU over a cable additionally requires an automotive Ethernet PHY and a 25G-class media specification, neither of which is in dq scope. This contribution does not propose either. It proposes the logical profile that lets the MAC-PHY interface stop paying for a 25G receive path the application never uses.

Why This Is Needed

Ethernet is scaling in the vehicle but is absent from the sensor link

11 → 27

Ethernet sockets per vehicle, today to 2030

MIPI

Still predominant on camera and sensor links

Proprietary links

Asymmetric point-to-point serializers own the sensor connection

Why a symmetric interface cannot compete on these endpoints

Die area

A 25G-class receiver needs a full CDR plus adaptive equalization. On an endpoint whose return traffic is control and status, that path still consumes substantial area, potentially comparable to or greater than the transmitter.

Complexity

A symmetric interface retains a full-rate receive path, including its design and verification burden across process, voltage and temperature, even when the application does not use it.

Power

Each high-speed receiver instantiated is continuous dynamic power on every port. The full benefit of removing it is realized only if the receiver need not exist at all. See the startup discussion.

The competition already does this. MIPI's C-PHY specification states that operating data rates for a link can be asymmetrical, enabling implementers to optimize transfer rates to system needs. Asymmetric operation is a documented efficiency feature that the closest competitor on this link already ships.

Sources: OPEN Alliance automotive Ethernet market report, 2026 (average Ethernet sockets per vehicle, 11 today to 27 by 2030). MIPI Alliance C-PHY specification overview, mipi.org.

Power — Published References and an Estimate

A 25G-class SerDes lane is tens of milliwatts, not watts

Reference design	Node	Power	Efficiency	Source
56 Gb/s NRZ transceiver, short-reach	16nm FinFET	126 mW / lane	2.25 pJ/bit	ISSCC 2018 (Erett et al.)
Scaled to 25G-class equivalent	16nm FinFET	~55–60 mW / lane	~2.25 pJ/bit	Linear scale — estimate
25 Gb/s receiver, medium-reach	28nm CMOS	~150 mW (RX only)	5.99 pJ/bit	Published RX, CTLE + 5-tap DFE
28 Gb/s multi-standard, long-reach	28nm CMOS	560 mW / lane	20 pJ/bit	14-tap DFE, backplane-class

What asymmetry saves, by endpoint. The sensor endpoint eliminates or simplifies a 25G-class receive path. The aggregator endpoint simplifies a 25G-class transmit path. Receive is roughly 55 to 65 percent of lane power, so the sensor-side figure is on the order of **30 to 40 mW per port** in a short-reach 16nm design. This is an engineering estimate derived by linear scaling from a published 56G result. It is not a measured 25G number and should be treated as indicative of scale only.

Sources: Erett et al., ISSCC 2018, 56 Gb/s NRZ transceiver in 16nm FinFET. Published 25 Gb/s medium-reach receiver, 28nm CMOS, CTLE plus 5-tap DFE. Published 28 Gb/s multi-standard backplane SerDes, 28nm CMOS. Scaling to 25G-class is the presenter's estimate, not a measured result.

Proposed Profile and Orientations

One profile with technical grounding today, plus mirrored direction roles

Role	Transmit	Receive	Typical endpoint
High-rate transmit role	25 Gb/s	100 Mb/s	Camera, radar or lidar endpoint. Display sink-side driver
High-rate receive role	100 Mb/s	25 Gb/s	Zonal hub or ECU endpoint. Display source-side host

Proposed baseline — 25G / 100M

Return direction builds on 8B/9B symbol encoding with additive scrambling at 125 MBd, as proposed by Murray and Riesco for a 100M POPI interface in July 2026. That contribution already defines the encoding, idle codebook and sideband interleave at this rate.

Possible future profile — 25G / 1G

A 1 Gb/s return direction has been raised as a candidate, but no encoding for it has been contributed to dq. It would need its own proposal covering encoding, sideband capacity and signalling rate. It is listed here as a direction, not as part of the baseline being proposed today.

Draft Text: Rate Declaration at the MAC-PHY Boundary

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Expressing independent transmit and receive rates

x.y Asymmetric rate capability

A POPI interface may support independent configuration of the transmit data rate (TxDR) and receive data rate (RxDR) for a given port. TxDR and RxDR each take values from the asymmetric profile in use, and the pairing is determined by the configured role. For a high-rate transmit role TxDR is the high rate and RxDR is the low rate. For a high-rate receive role the assignment is reversed, such that the two link partners are complementary. When no asymmetric profile is in use, TxDR = RxDR as in existing operation.

What changes. The interface today assumes a single data rate per port. This adds the hook for two, bound to a defined profile and a role, rather than to an open rate space.

Open editorial questions. Which clause hosts this text, and whether the direction role is a configured parameter, a strap, or discovered at link-up. Both are for the Task Force and the assigned editor, not settled here.

Return-Direction Encoding

Building on the encoding already contributed to dq

Element	Definition	Origin
Symbol encoding	8B/9B, 512-code space	Murray and Riesco, July 2026
Scrambling	33-bit additive scrambler	Same contribution
Signalling rate	125 MBd for 100 Mb/s operation	Same contribution
Sideband capacity	12.5 Mb/s at one bit per symbol	Same contribution
Idle and control codes	32-entry idle codebook, randomized control codes	Same contribution

Why this matters for schedule. The return direction of the proposed profile operates at a rate for which dq already has a contributed, discussed encoding. This proposal does not ask the Task Force to invent a new low-rate encoding. It asks whether that existing work should be paired with a 25G-class forward direction as a defined asymmetric profile. That contribution identifies spare and unused code space in the 9B mapping that could be allocated for profile signalling.

Source: Murray and Riesco, Symbol Encoding for POPI for 10/100M PHYs, IEEE 802.3dq Task Force, July 2026.

Electrical Considerations

ILLUSTRATIVE DRAFT

What changes on the interface, and what does not

Parameter	Forward direction	Return direction
Signalling	25.78125 GBd NRZ, unchanged	125 MBd, NRZ
Differential pairs	1	1
New pins required	None	None
Equalization	As existing 25G-class AUI	Expected minimal, requirements to be defined

Two points to be precise about. First, this is an operating-mode change on an existing differential pair. The connector, pad count and forward-direction electrical specification are untouched. Second, a lower return rate does not extend the reach of the interface. The forward direction still sets the channel limit. The return direction benefit is area, complexity and power at the endpoint, not longer reach. Reusing the pins does not by itself establish electrical interoperability. Amplitude, termination, jitter, BER, AC-coupling behaviour, spectral characteristics and receiver lock at 125 MBd all remain to be defined.

Management and Profile Selection

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Advertising and selecting the profile

Parameter	Access	Function
ASYM_CAPABLE	Read only	Device supports an asymmetric profile
ASYM_ROLE	Read / write	Source or sink orientation for this port
PROFILE_SEL	Read / write	Selected profile, or none for symmetric operation
ASYM_FAULT	Read only, latching	Profile or role mismatch detected

On access method. Clause 45 management registers are accessed through MDIO. This proposal assumes the same, and additionally that these parameters are reachable through the in-band, error-checked management channel that dq is already defining in the POPI sideband. Vendors commonly expose equivalent registers over I^2C in their own devices, but that is an implementation choice rather than something this contribution should standardize. Register addresses are placeholders pending allocation.

Startup and the Two Device Classes

This is where the area saving is either realized or lost

Symmetric-capable device

Powers up symmetric, negotiates or is configured into an asymmetric profile, and falls back to symmetric on mismatch.

Benefit: dynamic power only.
The 25G receive path still exists, so area, verification and PVT burden remain.
Fully backward compatible.

Asymmetric-only endpoint

Has no 25G receive path at all. Cannot come up symmetric, so it needs a defined low-rate startup, a strap, or discovery.

Benefit: the full area, power and verification saving.
Cost: needs a startup mechanism that does not assume symmetric capability.
Not backward compatible with a symmetric-only partner.

The open question for the Task Force. A symmetric power-up default is the safe, compatible choice, but it preserves the receiver whose removal is the main argument for asymmetry. Defining a startup path for asymmetric-only endpoints is what converts a dynamic-power saving into an area saving. This contribution does not resolve it and asks for contributions on it.

Open Items and Risks

Stated plainly, with proposed handling

Item	Why it matters	Proposed handling
Startup for asymmetric-only endpoints	Determines whether the area saving is real	Solicit contributions. See previous slide
Backward compatibility	Symmetric-only partners must still link	Symmetric default for symmetric-capable devices
Local management carriage	PHY management, status and timestamps	dq in-band POPI sideband channel
Remote device control carriage	SPI, I^2C, GPIO as network traffic	Upper-layer mapping such as IEEE 1722 ACF
Media and PHY dependency	An Ethernet sensor link also needs a 25G-class PHY and media spec	Out of dq scope. Coordinate with the relevant project
Test and compliance	A new return-direction mode needs test points	Engage test and measurement vendors early
Relationship to 802.3dm	dm covers asymmetric automotive links to 10 Gb/s	dm is in recirculation ballot. Liaison note rather than overlap

Request to the Task Force

Does the Task Force support developing a fixed asymmetric logical profile for POPI with 25 Gb/s in one direction and 100 Mb/s in the other?

And, if so, does the group support:

1. Mirrored source and sink orientations, so both endpoints of a link are defined.
2. 8B/9B at 125 MBd as the initial return-direction encoding, building on the July contribution.
3. Contributions on startup, fault handling and electrical compliance, including the asymmetric-only endpoint case.

Why now. The next sensor generation crosses 10 Gb/s and selects a new PHY. Whether Ethernet is a candidate at that moment depends on the interface, the PHY and the media all being available. dq owns the first of those, and the return-direction encoding for this profile has already been contributed here.

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Backup

Competitive context and interface comparisons

Backup: Interface Comparison: C-PHY and a 25G-Class AUI

C-PHY signals over 3-wire trios. An AUI signals over differential pairs. Compare per unit.

	MIPI CSI-2 over C-PHY	25G-class AUI with asymmetric profile
Signaling unit	Trio — 3 wires, 3-phase encoded	Differential pair — 2 wires, NRZ
Effective capacity per unit	13.7 Gb/s per trio (6 Gsps × 2.28 b/sym)	25 Gb/s MAC rate per pair
Signalling rate	6 Gsps, 3-phase	25.78125 GBd NRZ
Units for ~26 Gb/s forward	2 trios	1 pair
Forward wires	6	2
Return path in that count	Not included	Second pair, at the profile rate

Read this as an interface comparison. Both are chip-to-chip interfaces, so the per-unit comparison is like for like. A trio provides 13.7 Gb/s of effective capacity over three wires, so roughly 26 Gb/s takes two trios and six wires. A differential pair carries a 25 Gb/s MAC rate over two wires at a 25.78125 GBd line rate, leaving a second pair for the return direction. Media reach is set by the PHY and cable, not by this interface.

Sources: MIPI C-PHY specification, symbol rates to 6 Gsps at 2.28 bits per symbol over the standard channel. IEEE Std 802.3 25G-AUI signalling at 25.78125 GBd NRZ.

Backup: The Next-Generation Sensor Decision Point

Not about re-spinning today's silicon. About what the next sensor generation selects.

The trigger. A 4-lane D-PHY v1.2 link tops out at 10 Gb/s. When a new image sensor, radar or lidar product needs more, its designers must choose a new PHY, and every option carries real cost.

Option	Configuration	Forward	Wires	What it costs
Stay: D-PHY v1.2	2.5 Gb/s × 4 lanes	10 Gb/s	10	Hard ceiling. The reason the decision arises
Step up: D-PHY v2.x	4.5 Gb/s × 4 lanes	18 Gb/s	10	Needs TX de-emphasis. Same wires for under 2× gain
Step up: D-PHY v3.x	9 Gb/s × 4 lanes	36 Gb/s	10	Requires RX CTLE. Short channel. Still 10 wires
Switch: C-PHY	6 Gsps × 2 trios	27.4 Gb/s	6	New 3-phase receiver architecture, a full redesign
25G-class AUI, asymmetric	**25.78 Gb/s forward**	**25.8 Gb/s**	**4**	**Return path included at the profile rate. IEEE interface**

Why this is the moment. A vendor crossing 10 Gb/s is already committing to new PHY silicon, so the switching cost is being paid either way. The question is what that investment buys. An Ethernet path exists only if the MAC-PHY interface, the PHY and the media spec are all available when the decision is made. This contribution addresses the first of those three.

Source: MIPI Alliance published PHY roadmap and specification pages. D-PHY v1.2 at 2.5 Gb/s per lane, v2.x at 4.5 Gb/s, v3.x at 9 Gb/s on the standard channel. C-PHY at 6 Gsps per trio.

Backup: Relationship to Ethernet at the Edge

Why an asymmetric profile matters for end-node sensors

802.3dm is defining asymmetric automotive links toward the sensor edge. An end node adopts Ethernet only if every layer fits its power and area budget, including the MAC-PHY interface. A symmetric 25G-class interface does not.

Management and low-speed control traffic the return direction must carry:

Station management

Register access, configuration and status for the PHY

Timestamps

Ingress and egress timestamps in the POPI sideband channel

Remote device control

SPI, I^2C and GPIO style functions, as network traffic

To be clear on layering. Two different mechanisms, at two different layers. The POPI sideband carries local MAC-to-PHY management, status and timestamp metadata. Remote control of a sensor device is Ethernet traffic carried across the network, for which IEEE 1722 ACF is one defined mapping. These are not alternatives to one another. What this proposal asserts is narrower and sufficient: none of this return traffic requires a 25 Gb/s receive path.