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Proposal for POPI Link Configuration and Low Power Operating Mode

Brian Murray
Jacobo Riesco

Introduction

- In a previous presentation in May the authors discussed the need for a low power mode and a means to configure the POPI link at power-up
- Low power mode
  - When the link is down standard MAC – PHY interfaces like GMII or RGMII will typically operate at a lower clock frequency to save power
  - It is desirable that POPI would support a low power mode when all the PHY links are down
- Link Configuration
  - Typically standard MAC – PHY interfaces like GMII or RGMII are configured on both sides to operate at a particular speed or the speed is selected based on the PHY link speed, including link down
  - POPI is intended to support a wide range of speeds and / or number of ports
    - POPI can be configured on both sides for a known speed / number of ports
    - But this requires pin configuration or software configuration (which requires POPI !)
  - It would be better to define a means to exchange POPI link configuration at power-up/reset to agree the signalling rate / number of ports
- This presentation expands on the May presentation to provide a more complete proposal for a POPI link configuration and low power operating mode

Default POPI Operation at Power-up and Reset

- It is envisaged that POPI will operate using single ended digital IO for lower speeds (< 1G) and SerDes for higher speeds (≥ 1G)
  - The lower and higher speed will use a very similar logical interface but have different signalling at the pins
- The first step is to define a default speed of operation of the POPI link at power-up/reset for the lower and higher speed POPI
  - This ensures that the MAC and PHY connect at a default known signalling rate at power-up
- We propose that the low speed POPI operates using 8B/9B encoding at a default speed of 12.5 MHz after power-up
  - Symbol alignment and scrambler lock follows the exact same procedure as for 8B/9B encoding
    - See Proposal for 8B/9B Symbol Encoding for POPI at rates of 10M to 200M, slide 13
  - After symbol alignment and scrambler lock is indicated on both sides - POPI is in a **Low Power Mode**
    - In this mode the MAC and PHY can send / receive Macro Frames
    - This gives the MAC a management interface to the PHY and allows the host S/W to configure the PHY ports
    - The MAC can send a configuration Macro Frame with POPI link configuration parameters to the PHY and the PHY acknowledges or rejects (the configuration)
    - The MAC can send a configuration Macro Frame to exit low power mode and enter active linking and the PHY acknowledges

Asymmetric POPI Rates

- POPI link configuration after power up enables asymmetric PHY rates
- Both lower and higher speed POPI operate as independent transmit / receive interfaces, loosely coupled
  - The lower speed POPI uses 8B/9B encoding with separate clock and data pins, so the MAC to PHY and PHY to MAC can operate at different speeds
  - The higher speed POPI using 64B/66B encoding and SerDes with sperate Tx and Rx differential pins can also have the MAC to PHY and PHY to MAC operate at different speeds
  - What is most important is that the speed of the up and down directions are configured by the MAC and acknowledged by the PHY in the symmetric low power mode
    - No obvious way to name the up / down directions
  - It is possible (maybe likely) that the lower of the up/down speed is lower than the lowest supported POPI rate
    - For example, a 100M up steam rate is a very low rate for a SerDes
    - In this case byte stuffing is used to align with the POPI rate

Link Configuration

- The following are a summary of the link configuration parameters to be sent from the MAC to the PHY
  - Noting, that the PHY must be capable of implementing the configuration
  - So there needs to be a mechanism for the PHY to acknowledge or reject
- Link configuration parameters – not exhaustive
  - Mode: 8B/9B or 64B/66B
  - Num of ports: at least 0-7, ideally up 32 or even higher
  - Higher speed sideband channel ratio: 1 to 16
  - Lower speed sideband bits: 1 to 4
  - Up stream PHY rate: 10M, 100M, 1G, 10G, 40G, 100G
  - Down stream PHY rate: 10M, 100M, 1G, 10G, 40G, 100G
  - PHY sub-rate: fraction (1/8 to 7/8)
- The actual POPI line rate is calculated from the above

Active Mode, Low Power Mode and Powerdown Mode

- POPI should support 4 modes of operation
  - Power-up mode:
    - This mode is entered after power-up/reset/wake; POPI achieves symbol alignment and scrambler lock
    - When both sides have indicated they have achieved scrambler lock POPI enters low power mode
  - Low Power mode:
    - In this mode, PHY linking is disabled and the MAC and PHY can send / receive Macro Frames
    - The MAC can configure the operation of each of the ports of the PHY, enabling/disabling ports
    - The MAC can configure the operation of the POPI link for speed/ports when linking is active
  - Active linking mode
    - POPI operates at the configured speed, PHY linking is enabled with port data and Macro Frames
    - POPI should also support using a fixed configuration for linking entered automatically after power-up, where pin configuration is required on the MAC and PHY side
  - Powerdown mode
    - In this mode POPI is powered down with no communication between MAC and PHY
    - Exit from this mode is via a wake signal or power-up/reset

Transition between POPI modes

- POPI always enters power-up mode after power-up/reset/wake and transitions to low power mode after scrambler lock on both sides
  - For higher speed POPI the MAC sends a configuration Macro Frame with PHY acknowledge to transition to low power mode
- POPI can transition from low power mode to active linking or powerdown mode
  - The MAC sends a configuration Macro Frame with PHY acknowledge to transition to either active linking (active) or powerdown mode (sleep)
  - The link is restarted at the agreed higher speed
- POPI can transition from active linking to low power mode
  - The MAC sends a configuration Macro Frame with PHY acknowledge to transition to low power mode (low power)
  - The link is restarted at the low power speed and PHY linking is disabled on all ports
- POPI can transition from powerdown mode to power-up mode
  - The MAC sends a wake signal or resets the PHY or power cycles the PHY to exit powerdown
  - POPI then transitions to low power mode after scrambler lock on both sides

Summary

- A proposal has been presented for POPI link configuration and low power operating modes
  - Link configuration parameters
  - Possible support for asymmetric speeds
  - Operating modes; power-up, low power mode, active linking, powerdown
  - Mechanism to transition between operating modes

Questions ?