Options for structure of the POPI draft amendment

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Overview

Problem statement

RS- interface clause structures

RS, AUI’s, and XS’s

Alternative Extender sublayer structure

POPI text structure and mapping

Discussion

Typical RS/Interface Clause structure

CLAUSE 22: MII

Overview

Functionals Specifications
- Architecture & Primitive definitions
- Signal definitions & encoding
- Management
- Timing

Electrical Specifications

Mechanical & interconnect specifications (cabling)

Special functions (e.g., EEE signalling)

CLAUSE 46: XGMII

Overview
- Rates
- Architecture
- Primitive definitions

Data Stream
- Encoding and format of bit streams
- Control symbols

Functional Specifications
- Transmit & Receive data formats
- Clocks and signaling

Special function signalling
- Faults, LPI, etc.

Electrical Characteristics

RS, AUI, and XS – formal 802.3 definitions

1.4.503 Reconciliation Sublayer (RS): A mapping function that reconciles the signals at the Media Independent Interface (MII) to the Media Access Control (MAC)-Physical Signaling Sublayer (PLS) service definitions. (See IEEE Std 802.3, Clause 22.)

XS – not in 1.4 – see clause 47: The purpose of the XGMII Extender, which is composed of an XGXS at the RS end (DTE XGXS), an XGXS at the PHY end (PHY XGXS) and a XAUI between them, is to extend the operational distance of the XGMII and to reduce the number of interface signals.

1.4.198 Attachment Unit Interface (AUI): In 10 Mb/s CSMA/CD, the interface between the Medium Attachment Unit (MAU) and the data terminal equipment (DTE) within a data station. Note that the AUI carries encoded signals and provides for duplex data transmission. (See IEEE Std 802.3, Clause 7 and Clause 8.)

RS, AUI, and XS – how they are used

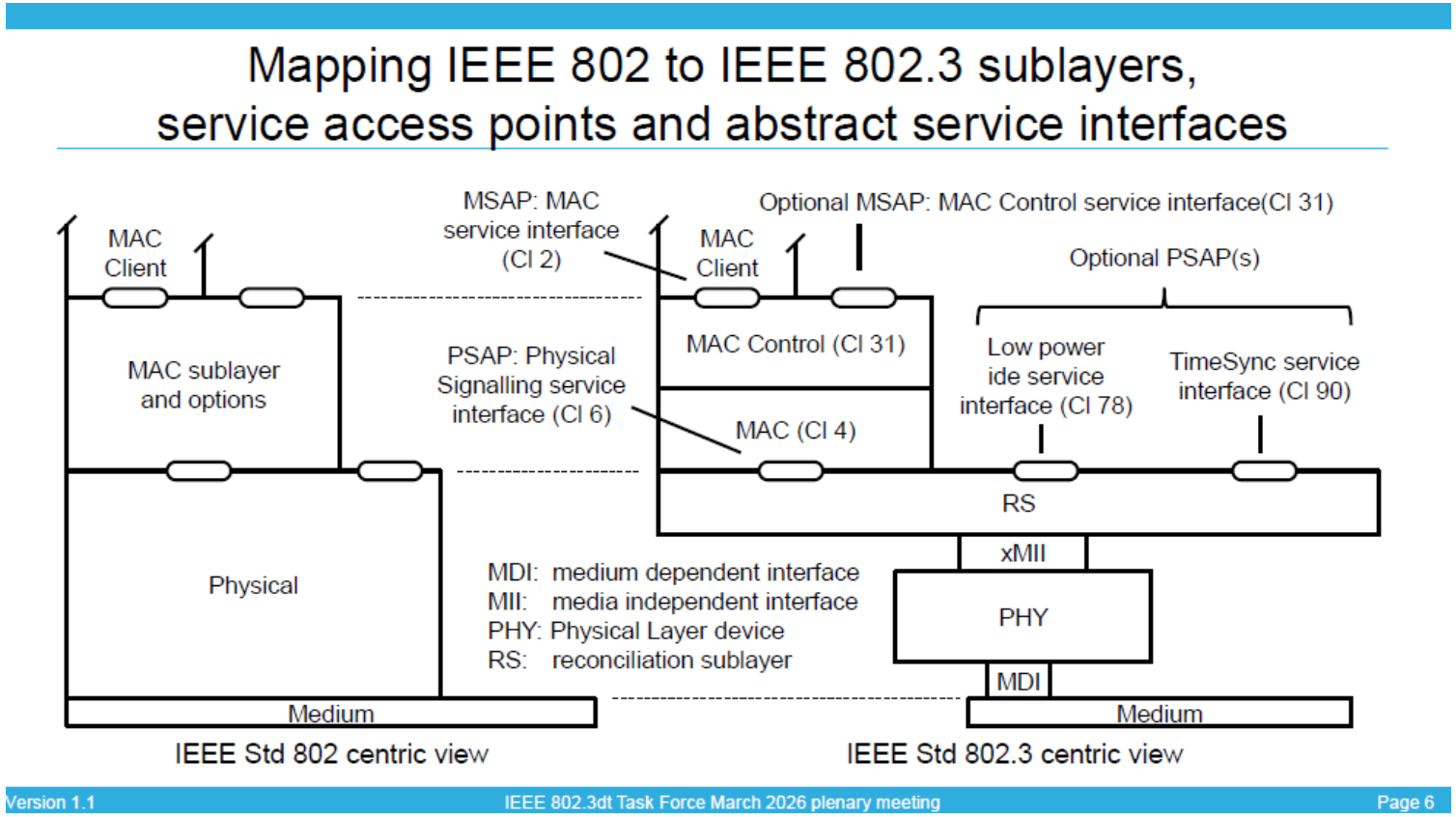
Reconciliation Sublayer (RS) : The RS sits directly **beneath the MAC layer and above the PHY**. It translates the abstract primitives and data streams coming from the MAC into the parallel, specific data paths of the xMII.

Attachment Unit Interface (AUI): The AUI is an electrical or physical interface specification that connects **different sublayers within the Physical Layer Device**. In higher-speed Ethernet standards (10GbE & beyond), AUI evolved into high-speed serial/lane electrical interfaces (e.g., XAUI, 200GAUI, 400GAUI) used to link chips or modules across a board.

3. Extender Sublayer (XS): The Extender Sublayer (e.g. XGXS, 200GXS, or 400GXS) is an optional functional block that **intercepts an xMII (like XGMII or CGMII) and reproduces it after transmission.** It re-encodes or compresses it so it can traverse an extended physical distance usually as a reduced-pin-count interface, with an XS on either end of the traversed distance.

RS definition may need to change:

Modern RS's merge in non-MAC clients (through optional PSAPs)



https://www.ieee802.org/3/dt/public/26_03/law_3dt_01a_2603.pdf

Alternative: Extender Sublayer-like structure (with an RS-twist)

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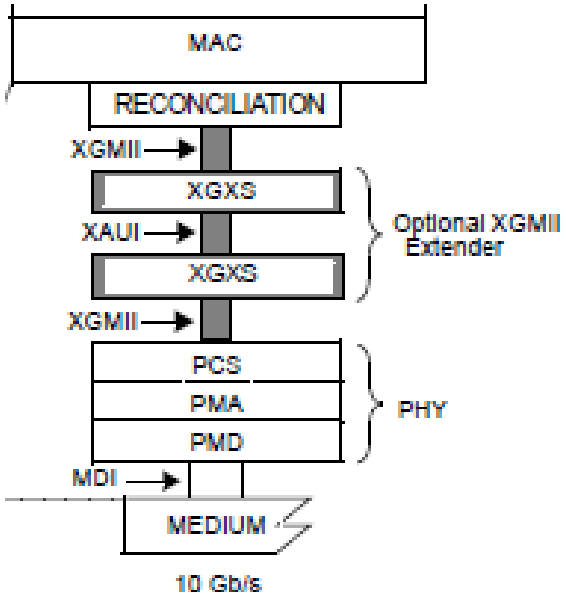
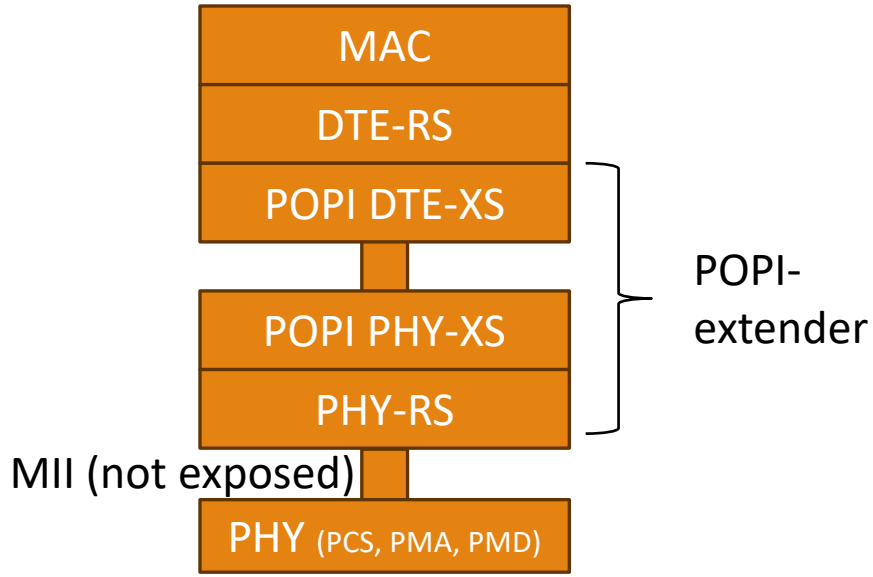
Extender Sublayer (XS): (Cl 47, 118, 171)

- Similar concept to POPI – pin reduced encodings for connection between device implementations
- Standardized encoding & electrical interface
- Mirror and borrow from PCS & PMA clauses



POPI could follow similar, but would need RS on the PHY side too to support PLCA, EEE, EMS

- Doesn't replicate MII on the MAC/DTE-RS side
- Creates MII "shim" (logically, not physically implemented) on PHY side for compatibility



Alternative Extender-based structure

Define POPI DTE-RS as the primitive architecture connecting to MAC

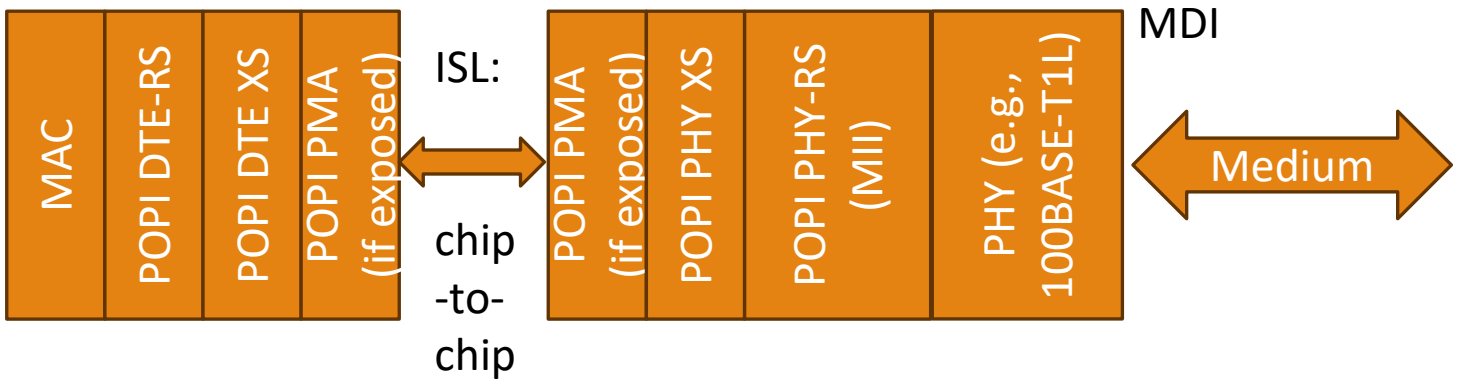
Define POPI PHY-RS as translation of primitives to the (logical) MII

Map the rest as though it were an extender, as an Inter-Sublayer Link

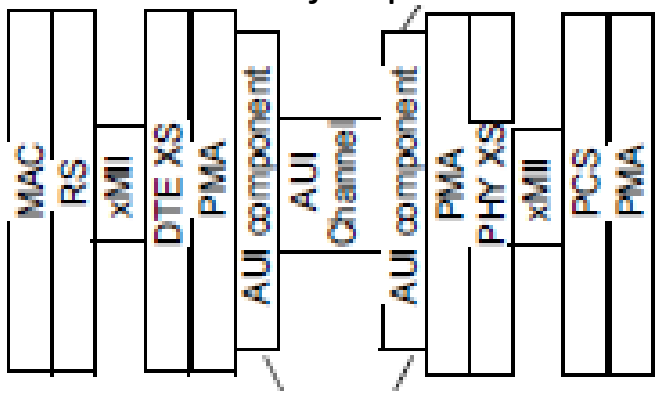
- See Clause 47, Clause 118, Annexes 120(B, C, D, E), 171, as well as 802.3dj, Annex 178B

Consider whether to do this as subclauses or separate clauses later

Allows us to also consider training of POPI PMA link, if needed similar to dj.



Excerpt from Fig 178B-2
IEEE P802.3dj D3p3



POPI Text Covers Several Unique Areas

- Architecture (RS, RS-splitting with an interface between)

Normal – but a change to the RS being only on the MAC side of the MII

- Logical interface definition
  - Primitives, translation

Normal stuff

- Out-of-Band signalling
  - Microframe format

Similar to PHY PCS-OAMs, but unique for an RS/PHY interface

- Encoding for the RS/PHY interface
  - General encoding of primitives, sequence ordered sets, etc.
  - High speed PCS encoding (e.g., 64/66B)
  - Low speed PCS (e.g., 8B/9B)

Pretty standard, except there are 2 different formats

- Electrical RS/PHY Interface specifications (for when it is exposed):
  - High speed electrical specifications (serdes speeds, levels, etc.)
  - Low speed electrical specifications

Unique in that there are 2 here, and we consider multiplexed ports

- Then there are the issues of which other clauses may need modification to accommodate POPI…

Uncertainty…

- Shim to translate PHY-side POPI to (unexposed) MII to mate with PHY clauses

This should be the most straightforward part of the architecture

Suggested Text Structure

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Overview

- Definition of one architecture, with interface between MAC/RS & RS/MII/PHY
- Rates - 2 POPI signaling formats – describe formats
- Describe DTE-RS, XS, POPI DTE-XS, POPI PHY-XS, and PHY-RS (not clear yet if DTE-XS and PHY-XS are the same)
- Primitive definitions (DTE-RS)

Data Stream definitions (XS – logical)

- PCS encodings (high speed & low speed separate)
- Micro frame structure – out of band signaling
- Separate if DTE-XS and PHY-XS are NOT the same

Electrical definitions (XS)

Transmit & Receive format (XS management)

- Multiplexing/Demultiplexing control – one per POPI-XS, not one per Port

Special functions (PHY-RS)

- Shims for PLCA, EEE, Time Sync, EMS, or future split RS functions

Murray presentations mostly map to POPI XS text

Slide	
Use a simple 4-pin interface with single ended IOs	Overview & Electrical Interface
Scrambling and 8B/9B encoding	POPI XS
Scrambler	POPI XS
Allocation of 9B codes	POPI XS – possibly both RS's
8B/9B encoding for Sequence Ordered Sets	POPI XS
Low Latency Data Requirement	Unclear at this time
Symbol Alignment and Scrambler Lock at Power-up	POPI XS
8B/9B Encoding for Multi-port PHYs	POPI XS, possibly also XS management

Initial Path to a Strawman

Identify which existing clauses need modification

- Clause 22 – RS for 10/100M; Clause 35 – RS for 1G; Clause 46 – RS for 10G; Clause 148 – RS for PLCA
- Clause 30 – Management objects
- Clause 45 – MDIO/MDC

Plan the addition of at least one new clause

- Suggest this new clause might contain three sections addressing 1) an overview, 2) the low-speed interface, and 3) the high-speed interface (TBD)
- Consider whether it is better to subdivide rates or functions into multiple clauses as it takes shape, but begin with one clause

Adopt baselines

- Identify content from contributions where the group feels we have good agreement
- Move to have content accepted as a baseline
- Assign volunteers to refine or develop new text based on the adopted baselines

Help your Editors

- Identify figures, state diagrams, and other baseline schematics that Editors can begin regenerating in FrameMaker as needed

Pass Clause 30 objects to YANG Open Source for an early look at YANG models

- If needed, updates to existing models to address missing configurations or to integrate new physical layers and features in Clause 30 will be handled by the YANG Open Source Project Ad Hoc led by Peter Jones



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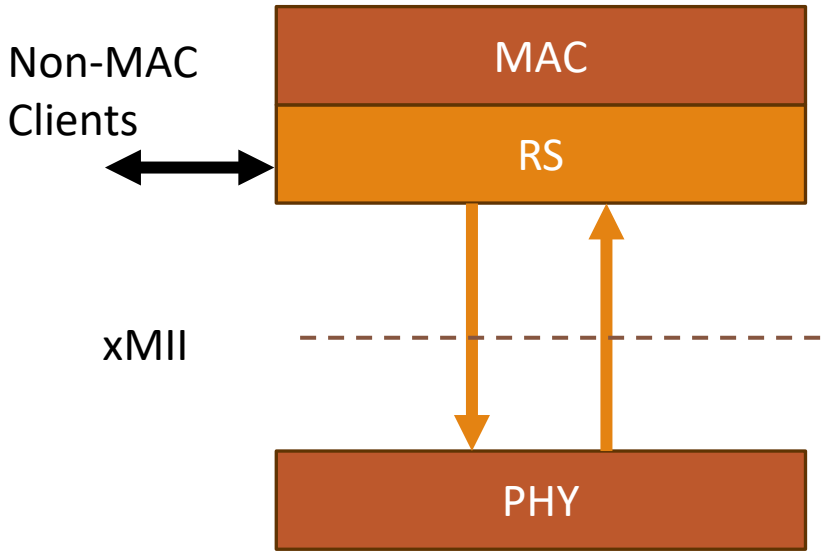
Discussion?
Thank you!

Summary of Differences

Feature	Reconciliation Sublayer (RS)	Attachment Unit Interface (AUI)	Extender Sublayer (XS)
Layer Location	Top of the Physical Layer (directly under the MAC)	An electrical connection/interface point within the PHY stack	An optional sublayer inserted around the MII/AUI boundary
Primary Job	Translates MAC signals to/from MII/xGMII format	Provides the physical electrical link/lanes between components	Re-maps and extends a Media Independent Interface across a longer/narrower link
Analogy	A translator/interpreter at the top of the desk	The copper or electrical wire/trace carrying the signal	An adapter/repeater package that lets the wire run farther

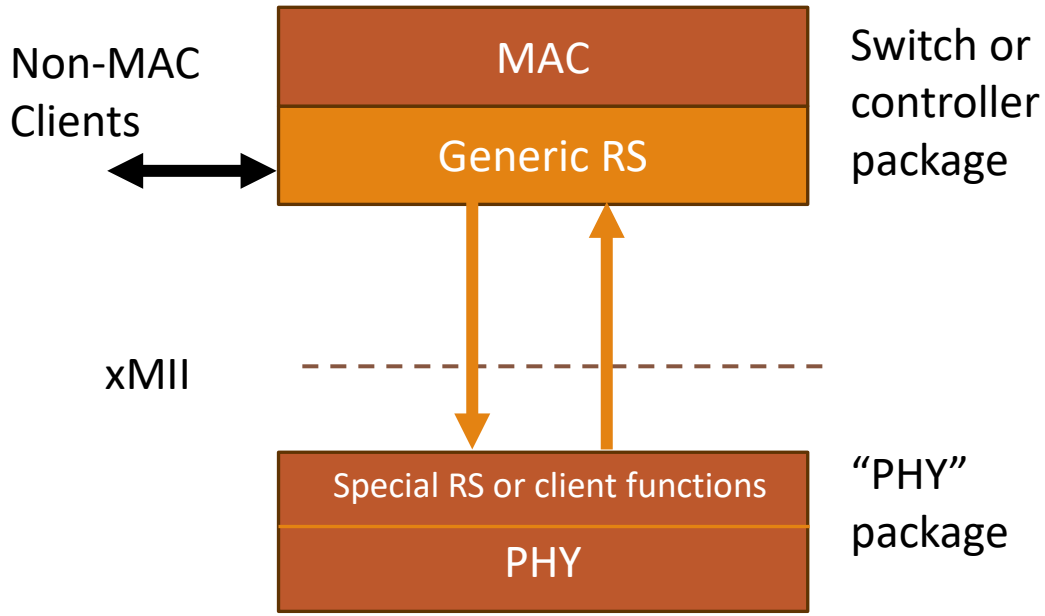
Usual architectural model vs. PHY implementation

Model in IEEE Std 802.3-2022



See, e.g., Figure 78-1, 90-1, or 148-1 & 148-2

Example implementation (EEE)



Special RS or client functions may include, for example, assertion of LPI, inserting timesync information, or handling PLCA state diagrams

Potential POPI “RS stack” architecture

