Basic Objectives

1. Define a scalable logical interface that can support arbitrary port speeds and counts while retaining as many of the features in our Feature Objectives as possible.
2. Define an electrical interface to provide connectivity to a single Ethernet port with 6 or fewer pins operating at MAC data rates up to 100 Mb/s.
   a) Provide single port connectivity without mandating clock recovery from the data.
3. Define an electrical interface to provide connectivity to 8 ports using 6 or fewer pins, each port with MAC data rates up to 100 Mb/s.
   a) Provide eight-port connectivity with an electrical interface speed not to exceed 2 Gbps.
4. Do not preclude compatibility between the logical interface and 802.3 PHY types that are specified with GMII or XGMII.

Feature Objectives

1. Provide an extensible communication channel for non-packet data that is carried on the POPI interface pins.
2. Support an error-checked MDIO management interface over the extensible communication channel for non-packet data.
3. Support Energy Efficient Ethernet (EEE).
4. Support half-duplex operation.
5. Support Clause 148 PLCA.
6. Support full-duplex operation.
7. Support auto-negotiation (e.g. Clause 28, Clause 98).

Compatibility Objectives

1. Preserve the Ethernet frame format and content
2. Preserve the preamble and SFD/SMD as presented to the POPI interface
3. Specify a logical and electrical interface between the Media Access Control (MAC)-Physical Signaling Sublayer (PLS) and the following Physical Coding Sublayers specified in:
    1. Clause 96 (100BASE-T1)
    2. Clause 97 (1000BASE-T1)
    3. Clause 146 (10BASE-T1L)
    4. Clause 147 (10BASE-T1S)
    5. Clause 148 (PLCA)
    6. Clause 188 (10BASE-T1M)
    7. Clause 190 (100BASE-T1L)
4. Do not preclude support for other existing PHYs specified in 802.3
5. Do not preclude the transmission of packet ingress / egress time data across the interface using in-band data.

POPI Termination Points

Figure 35–2 depicts a schematic view of the Reconciliation sublayer inputs and outputs, and demonstrates that the GMII management interface is controlled by the Station Management entity (STA).

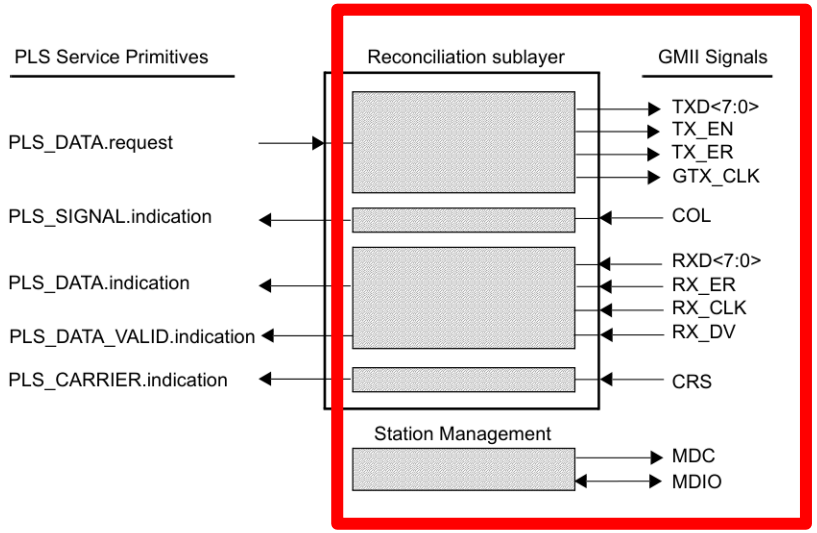

Figure 35–2—Reconciliation Sublayer (RS) inputs and outputs and STA connections to GMII

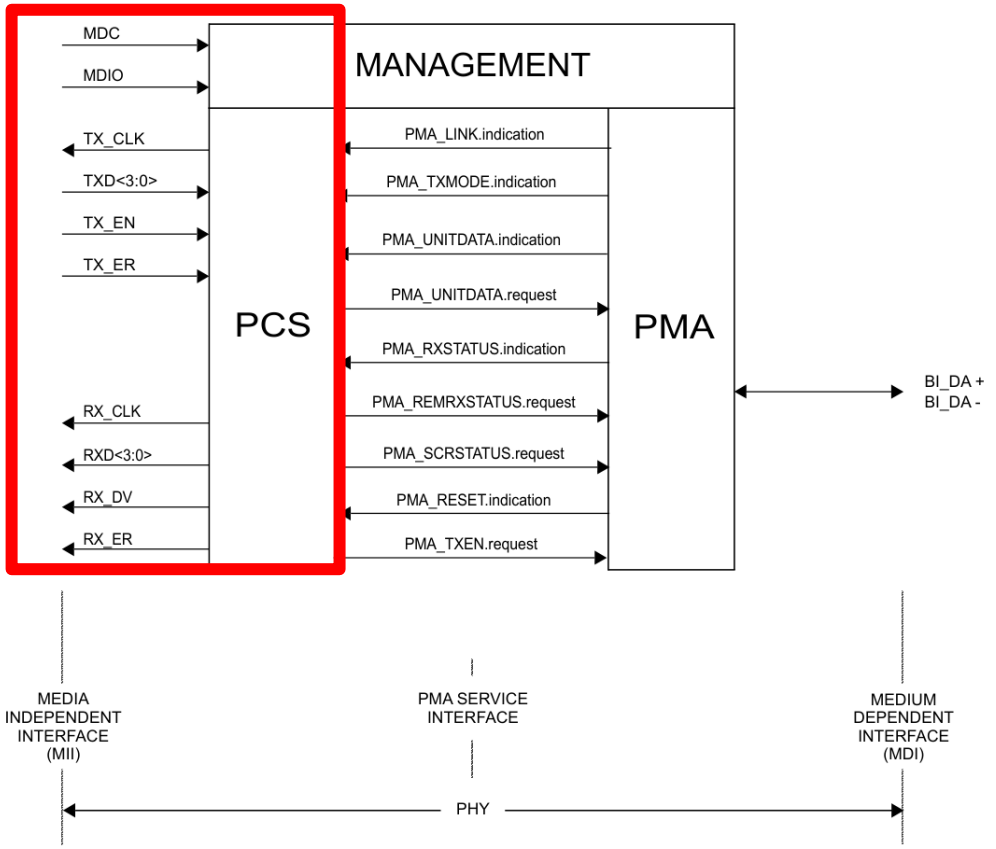

Figure 96–2—100BASE-T1 PHY interfaces