

POPI Sideband MicroFrame Format Proposal

Contribution to IEEE P802.3dq Pin-Optimized PHY Interface Task Force

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Baseline - MDIO

MDIO – Clause 22

- 64 bits per Management Frame
 - 32-bit Preamble (Optional)
 - 2-bit Start of Frame
 - 2-bit Operation Code
 - 5-bit PHY Address
 - 5-bit Register Address
 - 2-bit Turnaround Time
 - 16-bit Data

Table 22–12—Management frame format

	Management frame fields								
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE	
READ	1...1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z	
WRITE	1...1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z	

Key Observations

- Limited Address Space
 - $2^5=32$ PHYs
 - $2^5=32$ Registers
- Address in every transaction
- Multi-drop bus necessitates PHY Address

MDIO –Clause 45

- 64 bits per Management Frame
 - 32-bit Preamble (Optional)
 - 2-bit Start of Frame
 - 2-bit Operation Code
 - 5-bit Port Address
 - 5-bit Device Address
 - 2-bit Turnaround Time
 - 16-bit Address/Data

Table 45–426—Extensions to management frame format for indirect access

Frame	Management frame fields							IDLE
	PRE	ST	OP	PRTAD	DEVAD	TA	ADDRESS / DATA	
Address	1...1	00	00	PPPPP	EEEEEE	10	AAAAAAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	EEEEEE	10	DDDDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	EEEEEE	Z0	DDDDDDDDDDDDDDDDDD	Z
Post-read-increment-address	1...1	00	10	PPPPP	EEEEEE	Z0	DDDDDDDDDDDDDDDDDD	Z

Key Observations

- Same PHY Addressability
- Expanded Address Space for Each Port
 - $2^5=32$ Devices * 2^{16} Addresses
= 2^{21} (~ 2 Million) Registers
- Address in separate transaction

Achievable Clause 22 / Clause 45 Bandwidth

Worst-Case Bus Configuration

- 64 bits per Management Frame
- Management Data Clock (MDC)
 - Max 2.5 MHz per 802.3

Worst-Case Bandwidth @ 2.5 MHz

- 39,062.5 frames/s
- 625 kb/s

Best-Case Bus Configuration

- 32 bits per Management Frame
 - Enable Preamble Suppression
- Management Data Clock (MDC)
 - > 10 MHz seen in field

Best-Case Bus Transfer Rate @ 10 MHz

- 312,500 frames/s
- 5,000 kb/s

Common MDIO Data Flows

Payload Type	Typical Payload Length	Typical Transaction Frequency	Max Latency Tolerated
General MDIO Register Access	16 Bits	Bursty	Usually not latency sensitive
IEEE 1588 Timestamp Retrieval for Transmit	16 Bits - 16 Bytes	~10 Packets/s	On order of 10 ms for timestamp-related operations
IEEE 1588 Timestamp Retrieval for Receive	16 Bits - 16 Bytes	Every Packet Possible	On order of 10 ms for timestamp-related operations
Firmware Downloads	Kilobytes	Once at boot or upgrade	Affects power-loss recovery time
MACSEC (Re-)Key Exchange	256 Bits	On re-key, interval can range from seconds to minutes	Tight re-key timing budget must be met

Key Observations

- Timestamp retrieval drives MDIO latency
- MACSEC Re-Key Exchange drives bus speed

Problems to Solve

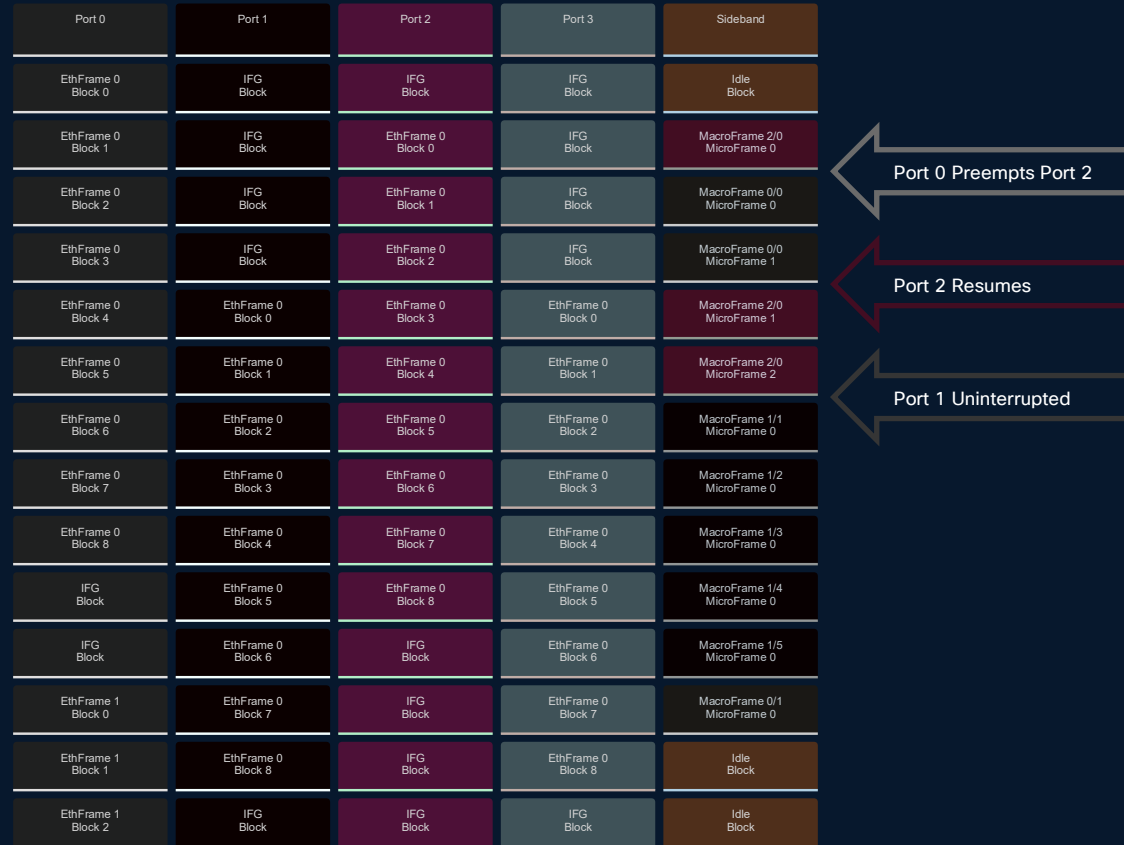
POPI Sideband Channel Challenges

- Challenging mix of data flows mirror Ethernet traffic
 - Long, speed sensitive flows want to be delivered as quickly as possible
 - Short, latency sensitive flows can't wait for the long transactions to finish
 - IP networking constructs can solve this, but are overly complicated for this application
 - No desire to design a QoS scheme
 - No desire to reinvent TCP
- Per-port traffic patterns vary within a four-port group that shares a sideband channel
 - One port should not starve adjacent ports
 - Strict striping/TDM schemes waste bandwidth

Proposed Solution

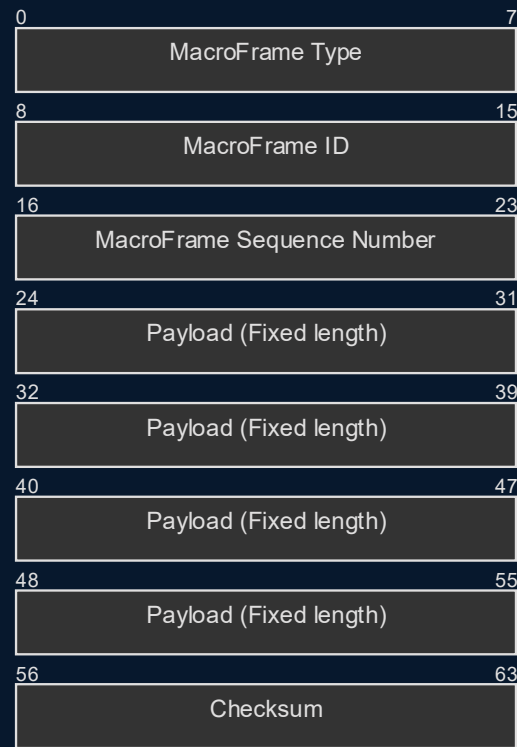
POPI Sideband MacroFrames / MicroFrames

- Sideband transmits larger MacroFrames as a sequence of fixed length 8-byte MicroFrames
- Microframes have enough information to rebuild the MacroFrame
- Supports MDIO Management Frames in a single MicroFrame
- Allows preemption within a single MicroFrame for a maximum latency of one 8-byte MicroFrame



POPI Sideband MacroFrames / MicroFrames - Revised

- 64 bits per MicroFrame, up to 256 MicroFrames per MacroFrame
- 8-bit MacroFrame Type
 - Basis for carrying unlimited diverse payload formats
- ~~• 2-bit Port Number - Removed as not all types address a single port~~
 - ~~• Assumes fixed 4:1 Port:Sideband ratio~~
- ~~• 6-bit MacroFrame ID~~
 - When combined with Port Number, provides primary key to reassemble a chain of MicroFrames to form a MacroFrame
- 8-bit MacroFrame Sequence Number
 - Ensures ordered delivery of MicroFrames
- 32-bit Payload
 - Payload defined by the MacroFrame Type
- 8-bit Checksum
 - Protect MicroFrame integrity



POPI Side Channel MicroFrame

Additional Benefits

- MacroFrames can be used to
 - Fragment a large transaction while ensuring context is maintained for reassembly
 - Create a “stream” of data to or from a particular endpoint in a PHY
- MicroFrames occupy the same worst-case footprint as an MDIO Management Frame but provide twice the payload, resulting in a net increase in available bandwidth
- In the worst-case 2.5 Mbit/s sideband configuration, which occurs at 25% of the bandwidth of a single 10 Mbit/s port, the proposed MicroFrame scheme provides performance that meets or exceeds the best-case 802.3 compliant MDIO bus
- ~~• The inclusion of a 2-bit port designator allows idle ports to cede sideband bandwidth to active ports, as opposed to a fixed per-port sideband data schedule~~
- MacroFrame Type ID can be extended within the Payload to create a virtually unlimited number of sub-types

Type Format Examples – MDIO Register Access

MacroFrame Type 1 – Clause 22 MDIO

Field Descriptions

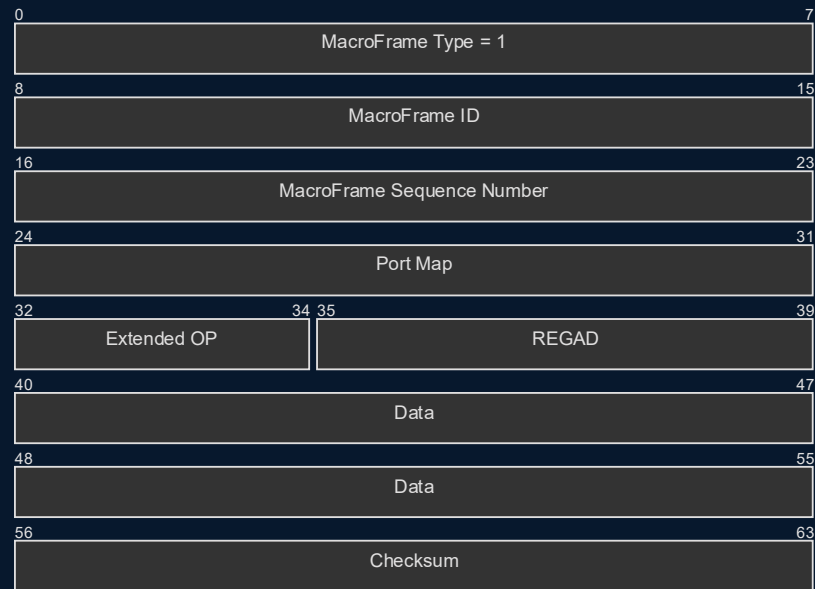
- **MacroFrame Type** - 1 to indicate MDIO Register Access Type
- **MacroFrame ID** - An ID number unique to this MacroFrame type that identifies this MDIO transaction
- **MacroFrame Sequence Number** - A sequence number, starting at zero, that provides ordering of the MicroFrames associated with this MacroFrame ID
- **REGAD** - As Defined in Clause 22.2.4.5.6

“The Register Address is five bits, allowing 32 individual registers to be addressed within each PHY. The first Register Address bit transmitted and received is the MSB of the address. The register accessed at Register Address zero <00000> shall be the control register defined in 22.2.4.1, and the register accessed at Register Address one <00001> shall be the status register defined in 22.2.4.2.”

- **Data** - As Defined in Clause 22.2.4.5.8

“The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.”

- **Checksum** - CRC8 of all preceding fields



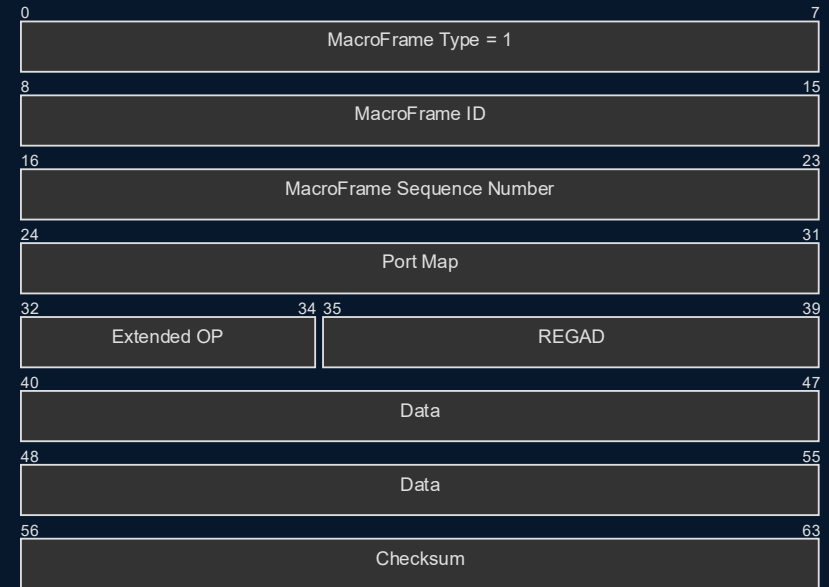
POPI Side Channel MicroFrame Type 1

MacroFrame Type 1 – Clause 22 MDIO

New Feature – New Read/Write Types

Extended OP – As Defined in Clause 22.2.4.5.4, but with extensions

- The operation code for a read transaction is <010>
- The operation code for a write transaction is <001>
- The operation code <101> indicates that the Data field contains the write mask to be used in conjunction with the following write operation
 - 1 – indicates that the corresponding register bit is to be modified
 - 0 – indicates that a register bit is to be preserved
- The operation code <110> indicates that the Data field contains the subscription mask to be used in conjunction with the following read operation
 - 1 – indicates that when the corresponding register bit changes, an unsolicited read result will be returned to the initiator of the operation
 - 0 – indicates that the corresponding register bit is masked from triggering an unsolicited read when it changes.



POPI Side Channel MicroFrame Type 1

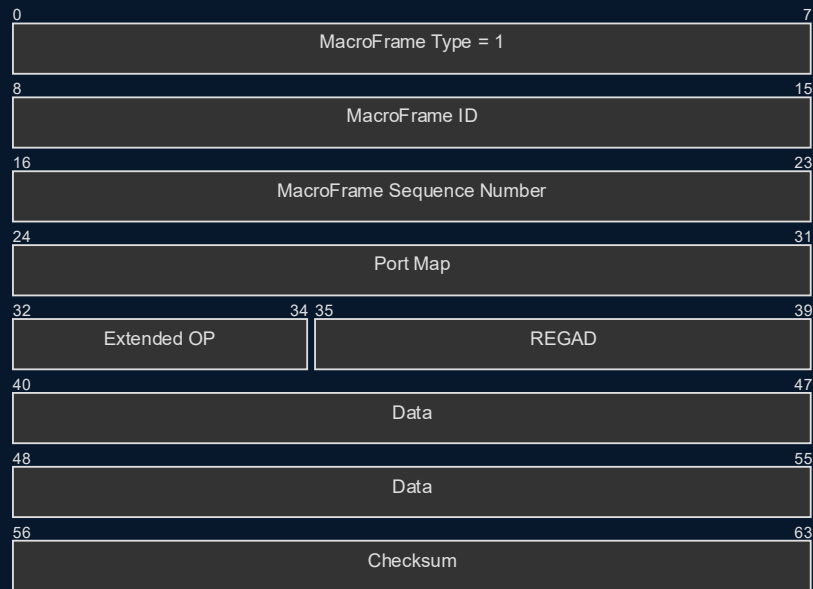
MacroFrame Type 1 – Clause 22 MDIO

New Feature – Broadcast / Multicast / Unicast Control

Port Map – NOT as Defined in Clause 22.2.4.5.5

Instead of a five-bit PHY Address, an 8-bit bit field is provided. PHY 0 shall observe bit 0, PHY 1 shall observe bit 1, etc. This approach enables broadcast and multicast MDIO writes, as well as batch reads that optimize bandwidth in the request direction.

- For Requests:
 - 1 – indicates that the corresponding PHY shall act on this transaction
 - 0 – indicates that the corresponding PHY shall not act on this transaction
 - Multiple bits may be set in the request frame.
- For Responses:
 - 1 – indicates that the corresponding PHY originated the response
 - 0 – indicates that the corresponding PHY did not respond.
 - Only one bit may be set in a response frame.

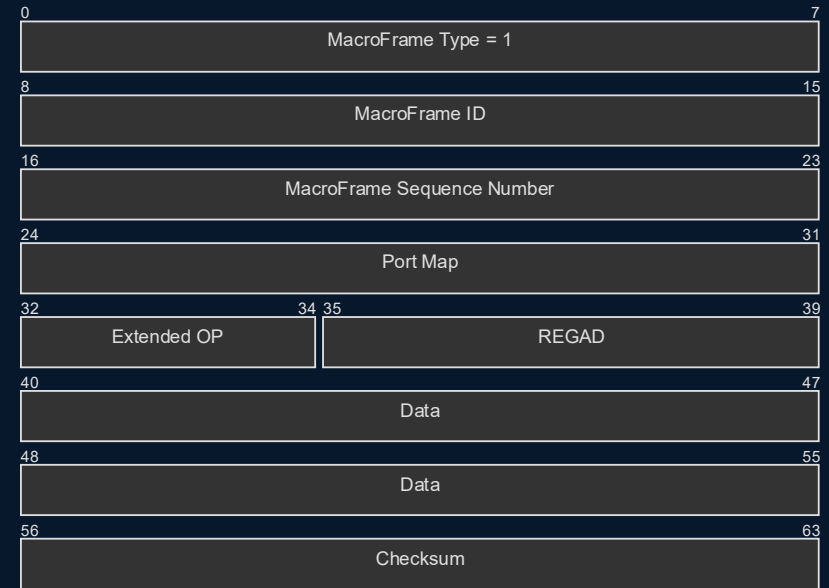


POPI Side Channel MicroFrame Type 1

MacroFrame Type 1 – Clause 22 MDIO

Operational Details

- Bi-Directional communication is allowed
 - PHY can initiate transactions into the POPI Interface
- Request transmitted in one sideband direction to initiate an MDIO transaction
- In the case of a read transaction, the response frame will arrive asynchronously via the opposing sideband channel
- The response shall be identical to the request frame, except:
 - MicroFrame Sequence Number shall be incremented
 - Port Map shall have only one bit set to one indicating which PHY is responding
 - Data field will be replaced with the response data
- **Open Questions:**
 - How should writes be handled? No Response, ACK, or implied read back of new contents?
 - How many port map bits should we reserve?



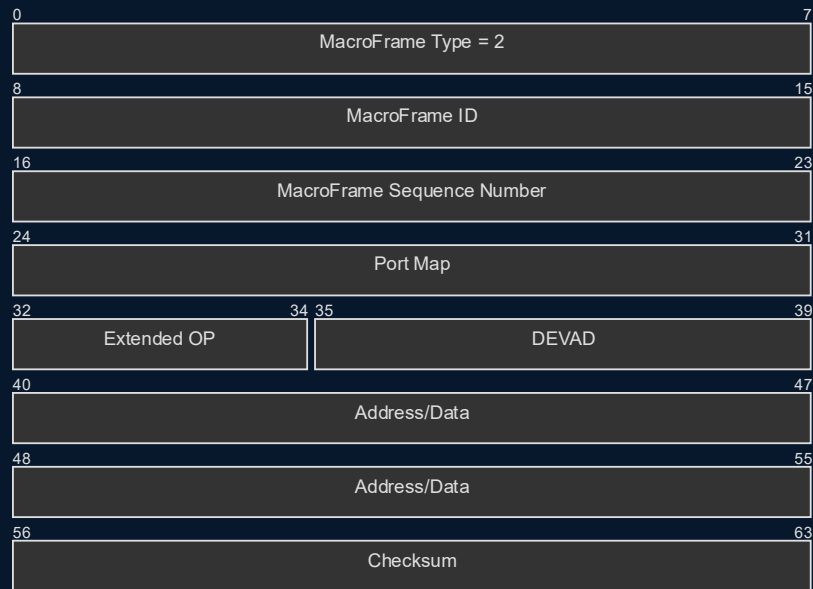
POPI Side Channel MicroFrame Type 1

MacroFrame Type 2 – Clause 45 MDIO

Offers same enhancements as Type 1

Adds Clause 45 OP codes:

- <000> pattern indicates that the frame payload contains the address of the register to access
- <010> pattern indicates that the frame is a post-read-increment-address operation
- Note:
 - While allowing 16 bit address and data in a single MicroFrame is possible, it would come at the detriment of other key features
 - Macro Frame sequence allows easy correlation of MDIO transactions even if address and data are not contiguously sent
- **Open Question:** Should a read have a byte count mechanism to enable long reads with post-read-increment address?



POPI Side Channel MicroFrame Type 2

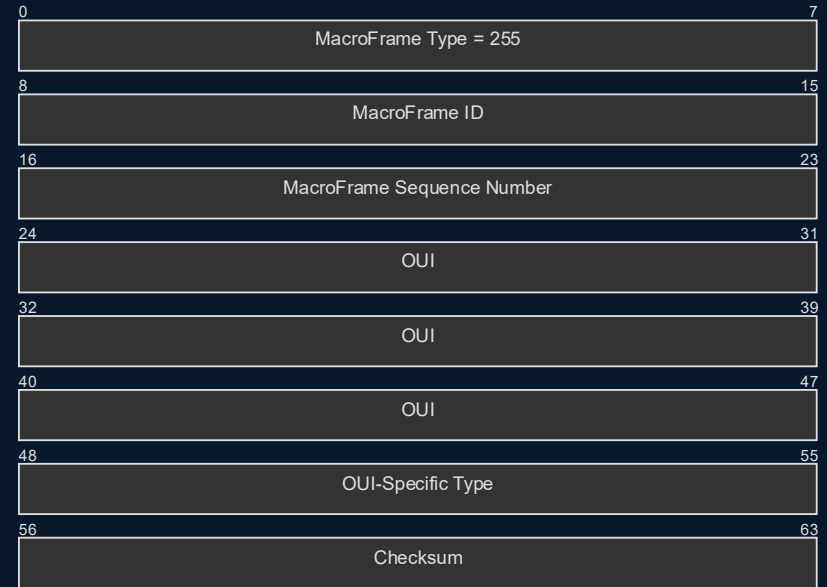
Type Format Examples – OUI-Specific Types

MacroFrame Type 255 – OUI-Specific Types

Allows Expansion of Types without Collisions

Field Descriptions

- **MacroFrame Type** – 255 to indicate OUI-specific
- **MacroFrame ID** – An ID number unique to this MacroFrame type across all outstanding OUI-Specific transactions that permits subsequent MicroFrames to be correlated with this OUI and OUI-Specific Type
- **MacroFrame Sequence Number** – A sequence number, starting at zero, that provides ordering of the MicroFrames associated with this MacroFrame ID
- **OUI** – Organizationally Unique Identifier as issued by the IEEE-SA Registration Authority
- **OUI-Specific Type** – A MacroFrame Type that is defined and unique only in combination with the OUI
- **Notes:**
 - (Almost) All OUI-Specific Type MacroFrames require at least two MicroFrames to be useful
 - LLDP uses a very similar approach, so many stakeholders that would want more types already have an OUI assigned



POPI Side Channel MicroFrame Type 255

Questions and Discussion