PHY Error Allocation for Linear and Partially Retimed Implementations

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Supporters

Background

IEEE 802.3 provides retimed chip-to-module (AUI-C2M) electrical interface specifications. This bring many advantage one of which is the guarantee of interoperability which is important for an IEEE specified link.

At 400 Gb/s/lane, power, latency and implementation complexity motivate architectures with fewer retiming functions. Implementation like CPO, NPO, which traditionally use unretimed (Linear) or partially retimed (Transmitter side retimed only) will be pervasive because density and power are the defining attributes.

A PHY may therefore contain fewer independently specified AUIs than a conventional retimed reference path.

The PHY-level error objective should remain fixed even when the internal implementation topology changes.

This contribution provides a path forward for a clear recognition of non-fully retimed interfaces while maintaining the expectation of performance in 802.3 links.

LPO and OIF RTLR as explicit use cases.

LPO MSA 200G DR specification

The LPO module is linear on transmit and receive paths; the host carries retiming and signal processing. The MSA adds coupled host/module electrical and optical tests and procedures.

OIF RTLR (Retimed Transmitter, Linear Receiver)

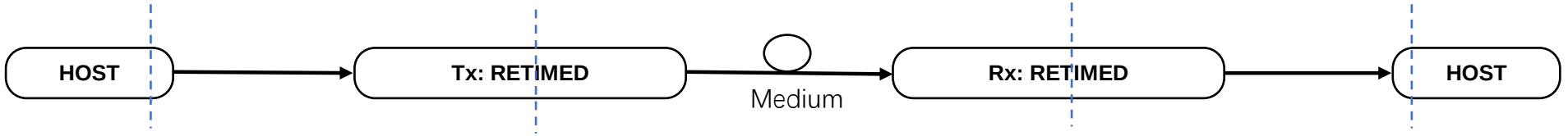
RTLR keeps module-side retiming in the optical transmit path but removes receiver-side retiming. OIF treats the linear receive channel as relying on host SerDes capability.

NPO/CPO and other ASIC package adjacent implementations

Current industry discussions are currently looking at implementing 400Gbps/Lane devices as NPO (Near Package Optics). This allows the implementations to use shorter and better channels. Many of the NPO devices would be using LPO and RTLR.

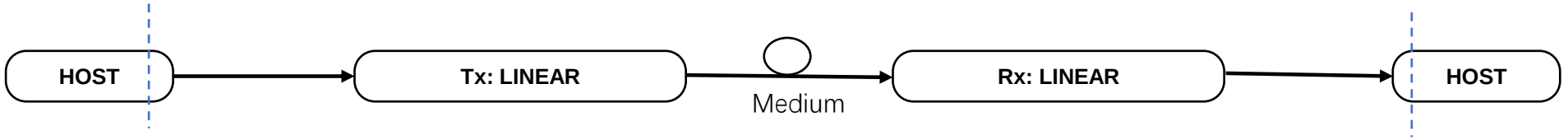
Three module architectures; different retiming boundaries

Fully retimed



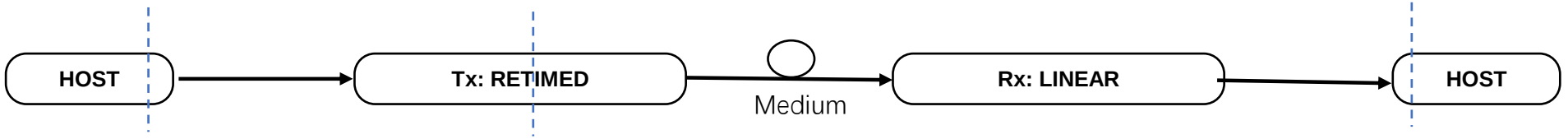
Independent electrical boundary in both directions

LPO



Host DSP/equalization participates in both signal paths

RTLR



Retimed optical transmitter; linear optical receiver,

Retiming Boundary

Impact on Error Allocation

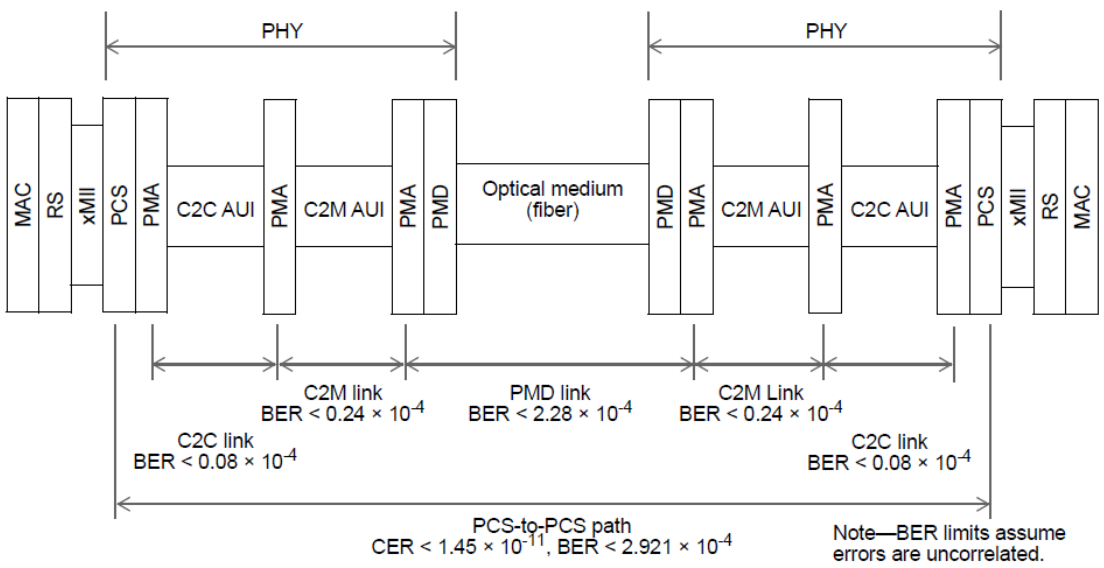


Figure 174A–9—Error allocations for optical PHY types with no FEC sublayer

Fully retimed

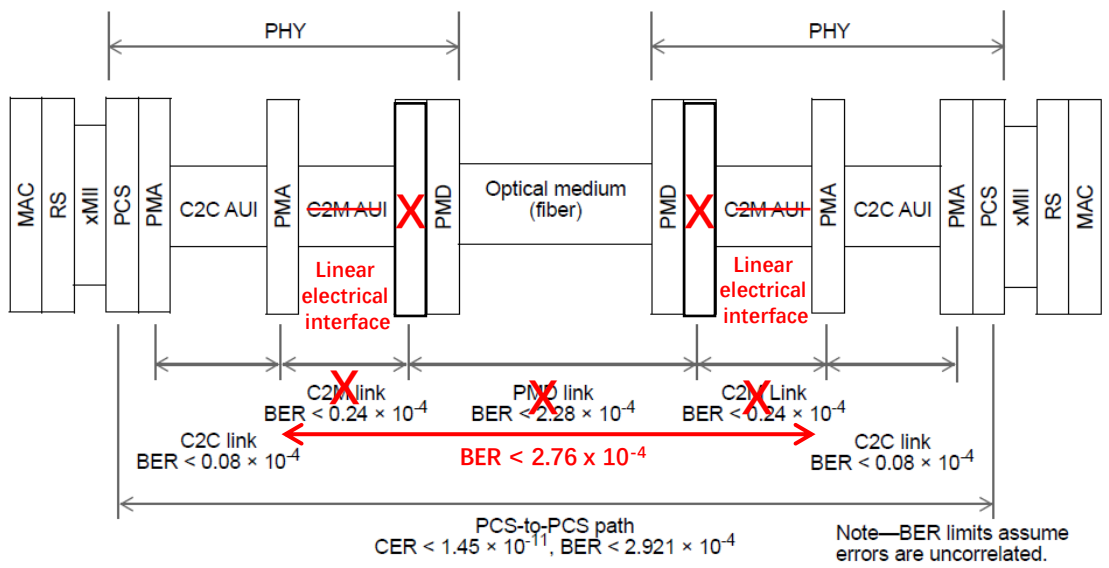


Figure 174A–9—Error allocations for optical PHY types with no FEC sublayer

LPO

In the LPO implementation, the two independently retimed C2M interfaces are replaced by linear electrical interfaces. Consequently, the individual BER allocations for the two C2M links and the PMD link are combined into a single error budget of 2.76×10^{-4} for the complete electrical and optical signal path. This allows implementation flexibility in distributing errors across the three segments while preserving the overall PCS-to-PCS error performance requirement.

Note: the formally added BER of the 3 segments is precisely 2.75947×10^{-4}

IEEE precedent: P802.3ds Clause 193.2/194.2

In the 802.3DS draft the following text was added to address the different error allocations:

> *"The BERadded may differ based on allocations as specified in Table 174A-1 when there are fewer AUI interfaces in a specific implementation."*

What the precedent establishes:

1. The complete PHY error objective remains applicable.
2. The receiver error allowance may vary with the number of AUIs in the implementation.
3. Clause 193.2 does not specify LPO or RTLR interoperability; it recognizes topology-dependent allocations.

Proposed P802.3dv text approach

Illustrative insertion into the applicable PMD error ratio allocation subclause

A complete PHY is expected to meet the frame loss ratio specifications in 174A.6.

“The BERadded allocation may differ, based on the allocations specified in Table 174A-1, when the number of independently specified AUI interfaces differs from the reference PHY architecture in a specific implementation.”

NOTE—Implementations may include linear pluggable optics (LPO) or retimed transmitter, linear receiver (RTLR) architectures, for which one or more otherwise assumed retimed AUI functions are absent.
PHY frame loss objective and applicable PMD compliance requirements remain unchanged.

Proposed Task Force direction and next steps

Proposed direction for discussion

> Adopt architecture-neutral error allocation language for P802.3dv, explicitly identifying LPO and OIF RTLR as examples of implementations in which the retiming topology differs from the reference PHY architecture.

Follow-on work:

1. Identify the P802.3dv reference PHY path and assumed AUIs.
2. Prepare an implementation/topology table and derived BERadded allocations.
3. Validate PMD-adjacent and PCS-level error measurements for LPO and RTLR examples.