Package Channel Study for 400G per Lane

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Introduction

- IEEE P802.3dj defined two classes of packages
  - Class A is loss-optimized, designed for standard lower-radix or loss-sensitive implementations.
    - Shorter trace (~33mm) and lower impedance (87.5 ohms)
  - Class B is high-radix optimized for switch ASIC
    - Longer trace (~45mm) and higher impedance (92.5 ohms)

- We shared simulated and measured package data in Sep. interim (he_x_400GPL_01_2609.pdf)
  - Both low-loss and high-loss packages were provided.
  - Questions were received on via architectures, impedance, etc.

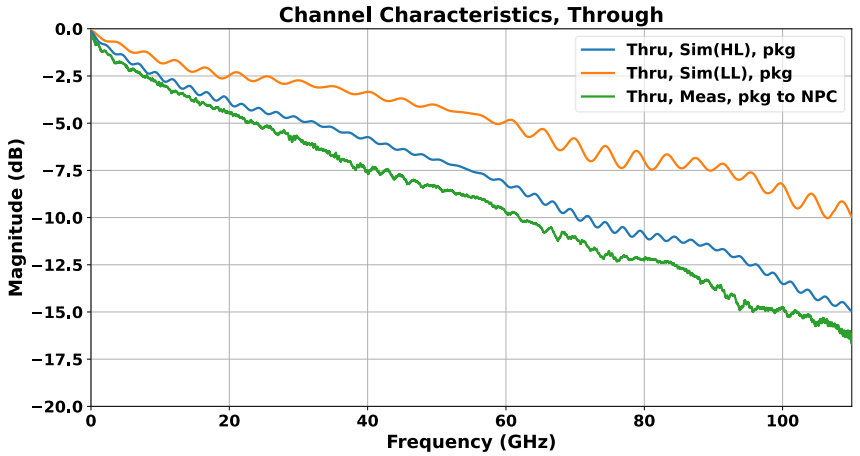
- In this contribution, we will share more details on our 400G per lane packages, aiming to build consensus on package model baselines.

Recap on the package data in last presentation

- **Mock-up PKG thru simulation (preliminary)**

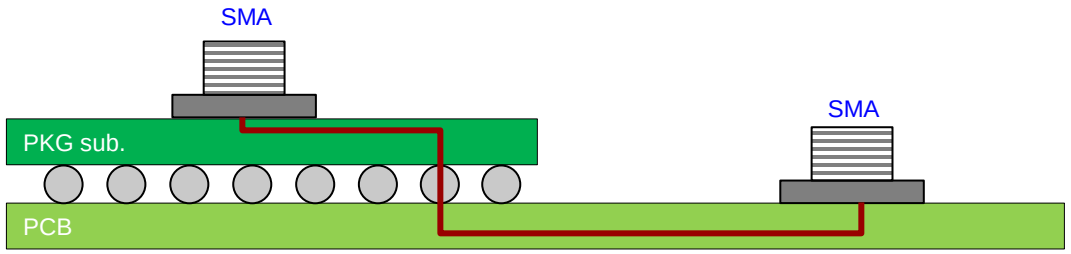
PKG Core layer	~1200 μm MLC
PKG build-up	9 BU layers for HL 7 BU layers for LL
PKG TL impedance	85 Ohm
Device type	Switch chip for HL AI chip for LL
BGA size	350μm (typical)
BGA pitch	0.65mm
PCB type	HDI

PKG data will be updated in following contents

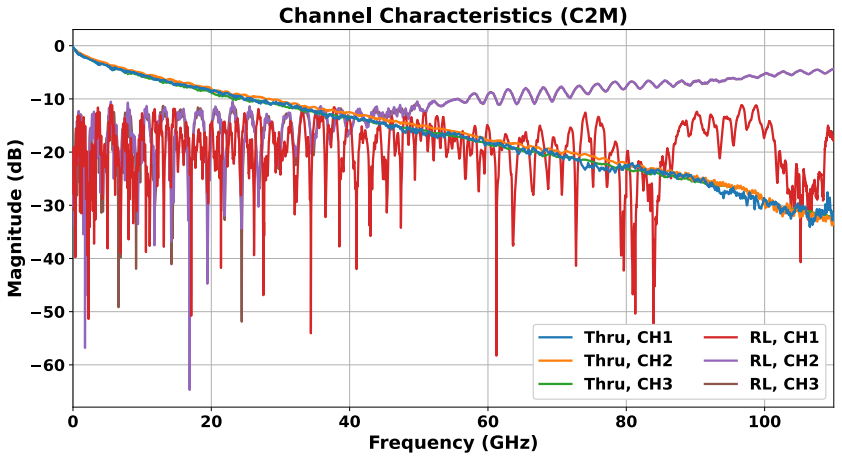


- **PKG-2-NPC measurement**

  - Measurement results **are NOT fully corresponding to the sim. data** above
  - Measurement setup is demonstrated as below



PKG (0.65 ball pitch, 1200μm single layer core) + HDI PCB



Case study of different package types

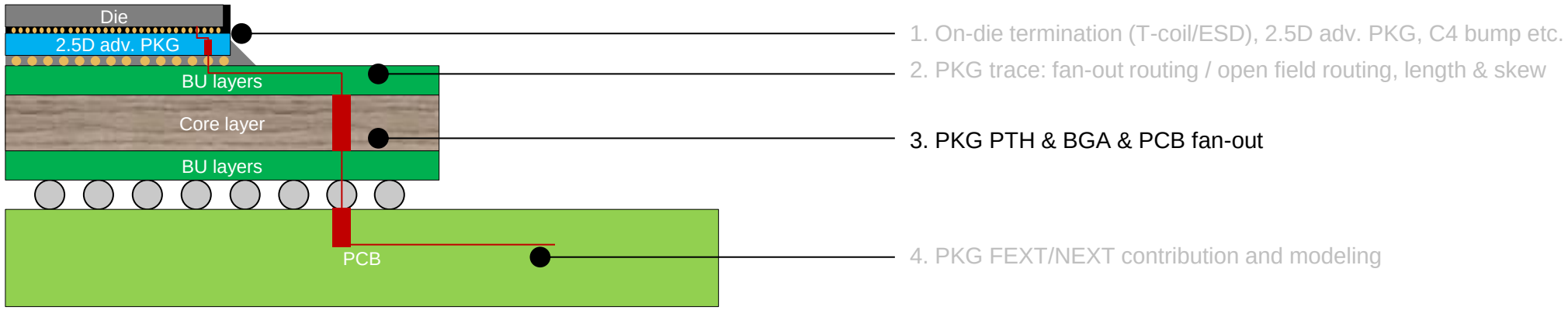
- **Mock-up PKG type I**

	Mock-up PKG Type I
Die size / 2.5D unit size	3x~7x reticle
Package type	FCBGA + 2.5D advanced PKG
Build-up layer count	7 ~ 11
Core layer thickness	1200~1600 μm
PKG sub. size	~ 110x110 mm²
BGA pitch	0.9~1.0 mm

- **Mock-up PKG type II:**

	Mock-up PKG Type II
Die size / 2.5D unit size	1~3x reticle
Package type	FCBGA + Monolithic / 2.5D
Build-up layer count	5 ~ 9
Core layer thickness	400~1200 μm
PKG sub. size	< 70x70 mm²
BGA pitch	≤ 0.65 mm

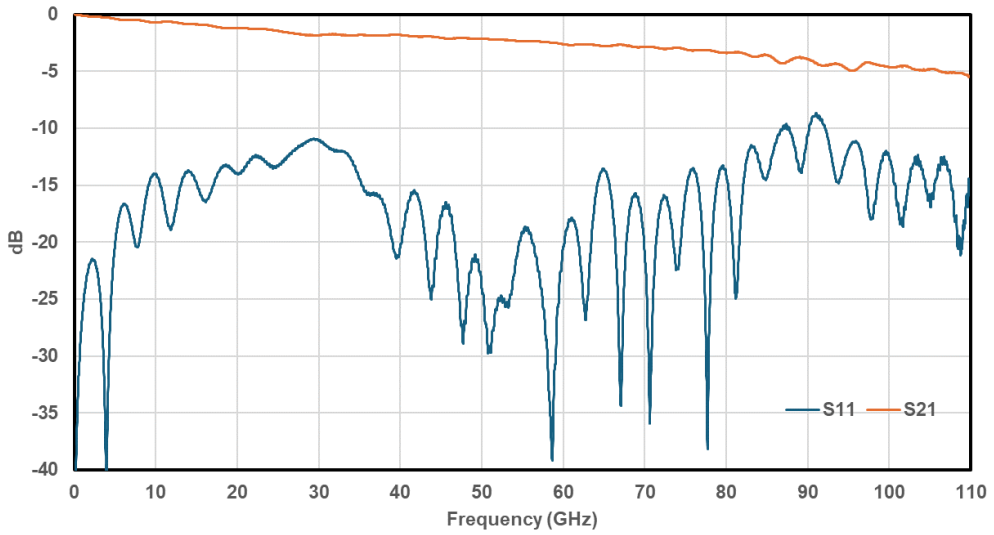
- **Key parts in typical PKG modeling**



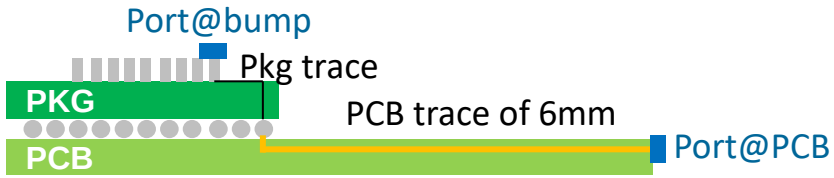
Measurement results of typical package I

- **Measurement results: BW > 110GHz**

	Mock-up PKG Type I
Stack-up	9-4-9
PKG Core layer	~1200μm, multi-layer core
PKG build-up	Normal ABF & laser drill
PKG TL impedance	85 Ohm
BGA size	600μm (typical)
BGA pitch	1.0mm
PCB type	HDI



- **Peer data:**
  - Marvell achieved >100GHz roll-off frequency based on the simulation results in DesignCon 2026.
    [Ref: 448G Package Interconnects Design, Xiangrui Su, et al., Marvell, DesignCon 2026]
  - The paper states that the **BGA diameter is between 500 and 600 μm**.
  - It can be inferred that the **BGA pitch is approximately 0.9~1.0 mm, witch is a normal choice for giant switch/AI chips.**

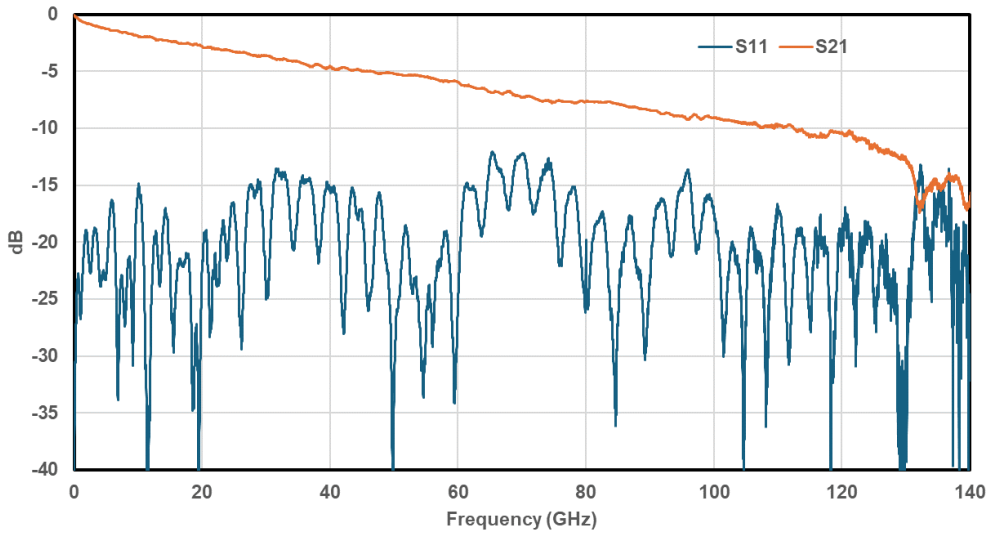


Simulation model diagram

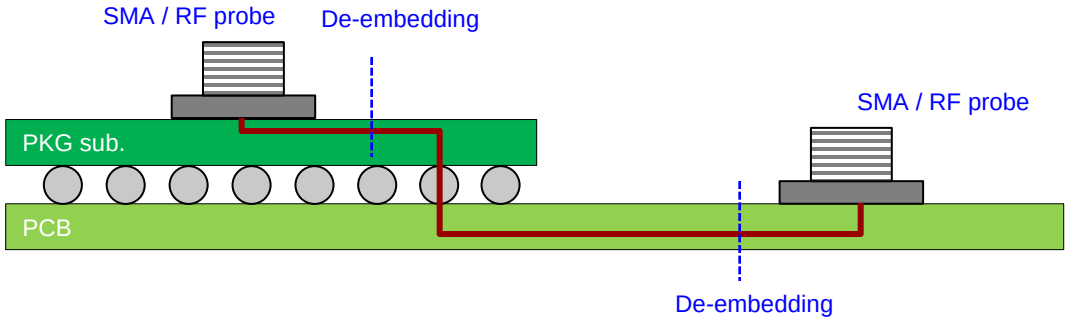
Measurement results of typical package II

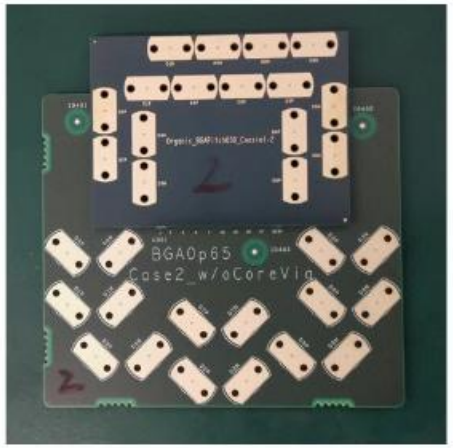
- **Measurement results: BW > 125GHz**

	Mock-up PKG Type II
Stack-up	8-2-8
PKG Core layer	~1200μm, single layer core
PKG build-up	Normal ABF & laser drill
PKG TL impedance	85 Ohm
BGA size	350μm (typical)
BGA pitch	0.65 mm
PCB type	HDI



- **Measurement setup**





Summary and outlook

- **This material primarily discussed the transition between PKG and PCB**
  - PKG core PTH and laser drills, BGA and PCB fan-out
  - Physical size of different components varies according to the package types
- **Two mock-up PKG measurement results shows:**
  - PKG bandwidth >110GHz for 1.0mm ball pitch
  - PKG bandwidth >125GHz for 0.65mm ball pitch
- **Outlooks**
  - PKG trace length could be further estimated, Class A ~33mm and Class B ~45mm may NOT match the actual situation
  - Characteristic impedance of PKG trace could be further discussed
  - A mathematical accurate definition for link bandwidth (e.g. frequency of ILD > x dB or RL > xx dB)
  - The equivalent model for the bump area (on-die termination, 2.5D structures and C4 bump) need to be updated
  - Other potential package types also need to be discussed (e.g. CPC, CPC-like ICA/CPX etc.)

Thank you!