Impact of Low-Loss Build-Up Materials on Future 400G/lane Package Channels

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Socionext

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Acknowledgement: The authors would like to acknowledge several engineers from AGC Inc., Dexerials Corporation, and Thintronics Inc. for technical discussions and for sharing publicly disclosable material-property information.

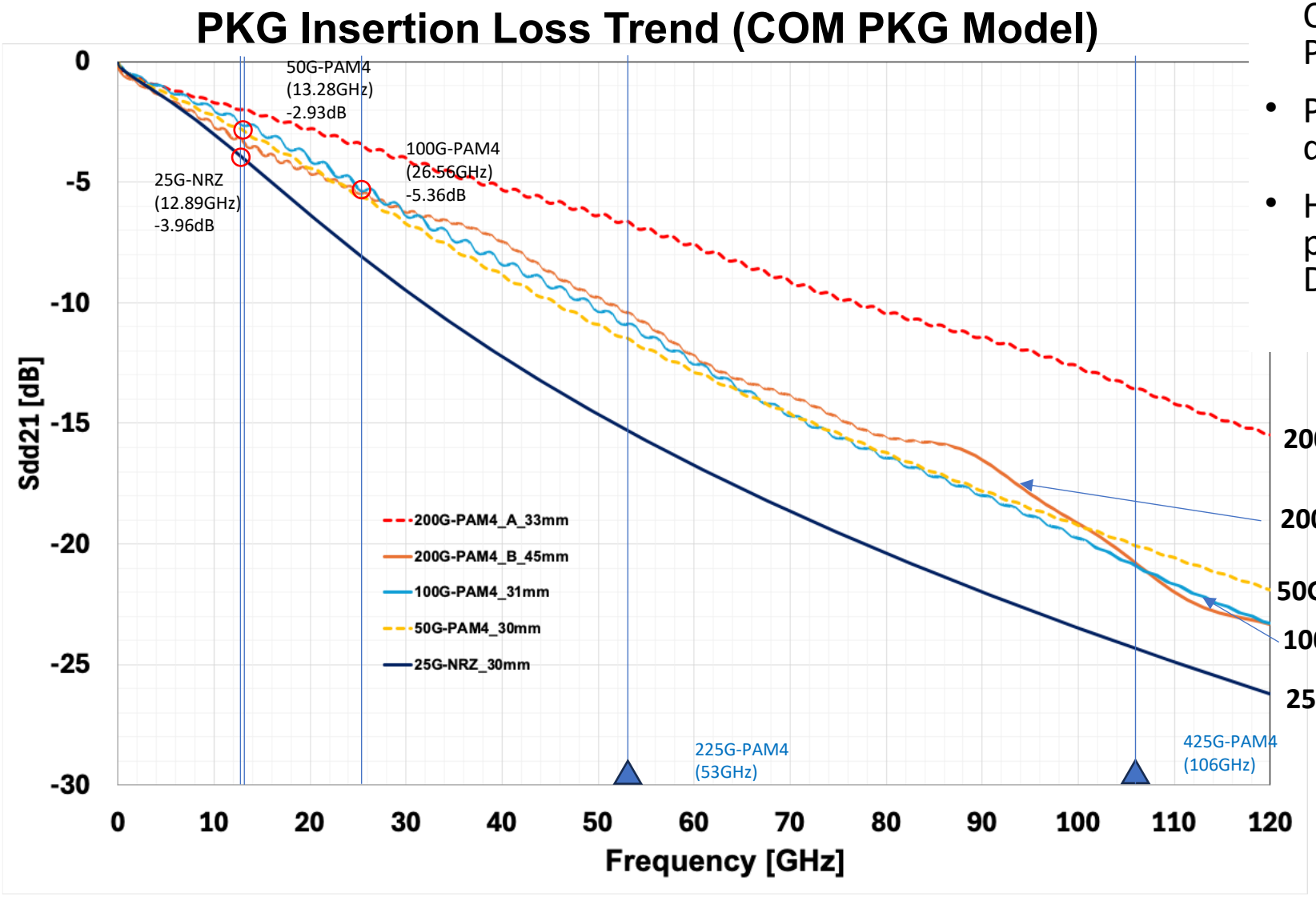
1. Objective

- Previous studies investigated package-channel feasibility for future 400G/lane signaling and evaluated dielectric-loss sensitivity using a measurement-correlated package model.
- This contribution extends the study by investigating how advanced build-up materials may reduce package insertion loss.
- The study focuses on:
  - Dielectric loss reduction (Df)
  - Dielectric constant reduction (Dk)
  - Geometry optimization enabled by lower Dk
  - Potential impact of conductor roughness reduction
- The objective is to identify practical opportunities for package-loss reduction beyond simple Df scaling.

This contribution is an update to sakai_400GPL_01a_2605.
(Relating to build-up material characteristics.)

2. Background

Package Loss is Becoming a Critical Challenge



- Future 400G/lane signaling is expected to require channel operation beyond 100 GHz.
- As signaling speed increases:
  Dielectric loss increases
  Conductor loss increases
  Package-channel margin becomes limited
- Previous studies mainly focused on dielectric-loss sensitivity.
- However, advanced substrate materials may provide additional benefits beyond simple Df reduction alone.

3. Previous Study Summary

Previous Contribution (sakai_400GPL_01a_2605 date May 05 2026)

A measurement-correlated package model was established using package test structures.

The previous study evaluated:

- Channel loss decomposition
- Df sensitivity
- Potential package-loss reduction achieved by lowering dielectric loss

The study assumed:

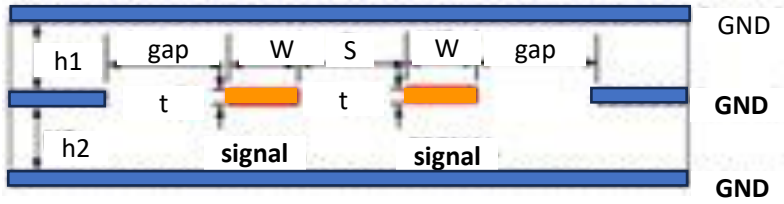
- Constant package geometry
- Constant conductor characteristics
- Constant impedance target

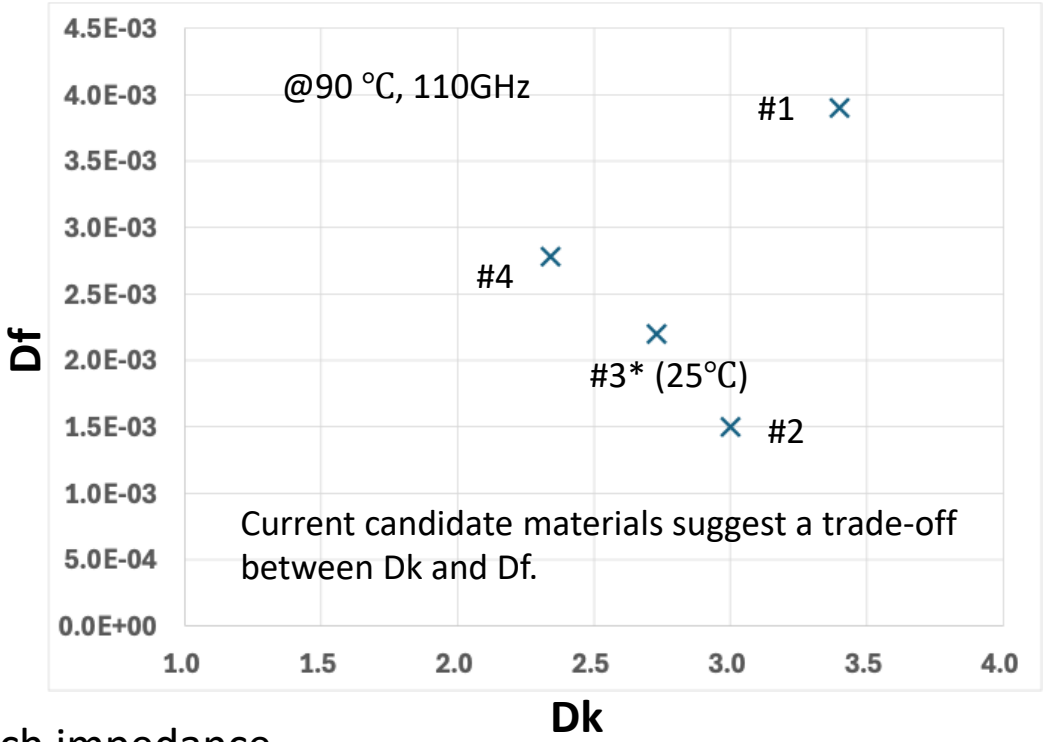
As a result, only dielectric-loss effects were captured.

4. Potential Low Dk/Df materials

	material	Dk	Df	Ra	temp	freq	W	S	gap	note
				nm	℃	GHz	um	um	um	
	GL-107 Equivalent	3.40	3.0.E-03	100	25	60	23	63	55	
	GL-107 Equivalent	3.40	3.0.E-03	100	25	110	23	63	55	extrapolated (freq)
#1	GL-107 Equivalent	3.40	3.9.E-03	100	90	110	23	63	55	extrapolated (freq)
	Material-A	3.00	1.0.E-03	100	25	110	23	63	55	
#2	Material-A	3.00	1.5.E-03	100	90	110	23	63	55	extrapolated (temp)
	Material-B	2.70	1.6.E-03	100	25	60	28	50	55	
#3*	Material-B	2.73	2.2.E-03	100	25	110	28	50	55	
	Material-C	2.34	1.8.E-03	100	20	65	32	42	55	
	Material-C	2.34	2.2.E-03	100	25	110	32	42	55	extrapolated (freq)
#4	Material-C	2.34	2.8.E-03	100	90	110	32	42	55	extrapolated (freq/temp)

*: 25 ℃ value (90 ℃ data not available)

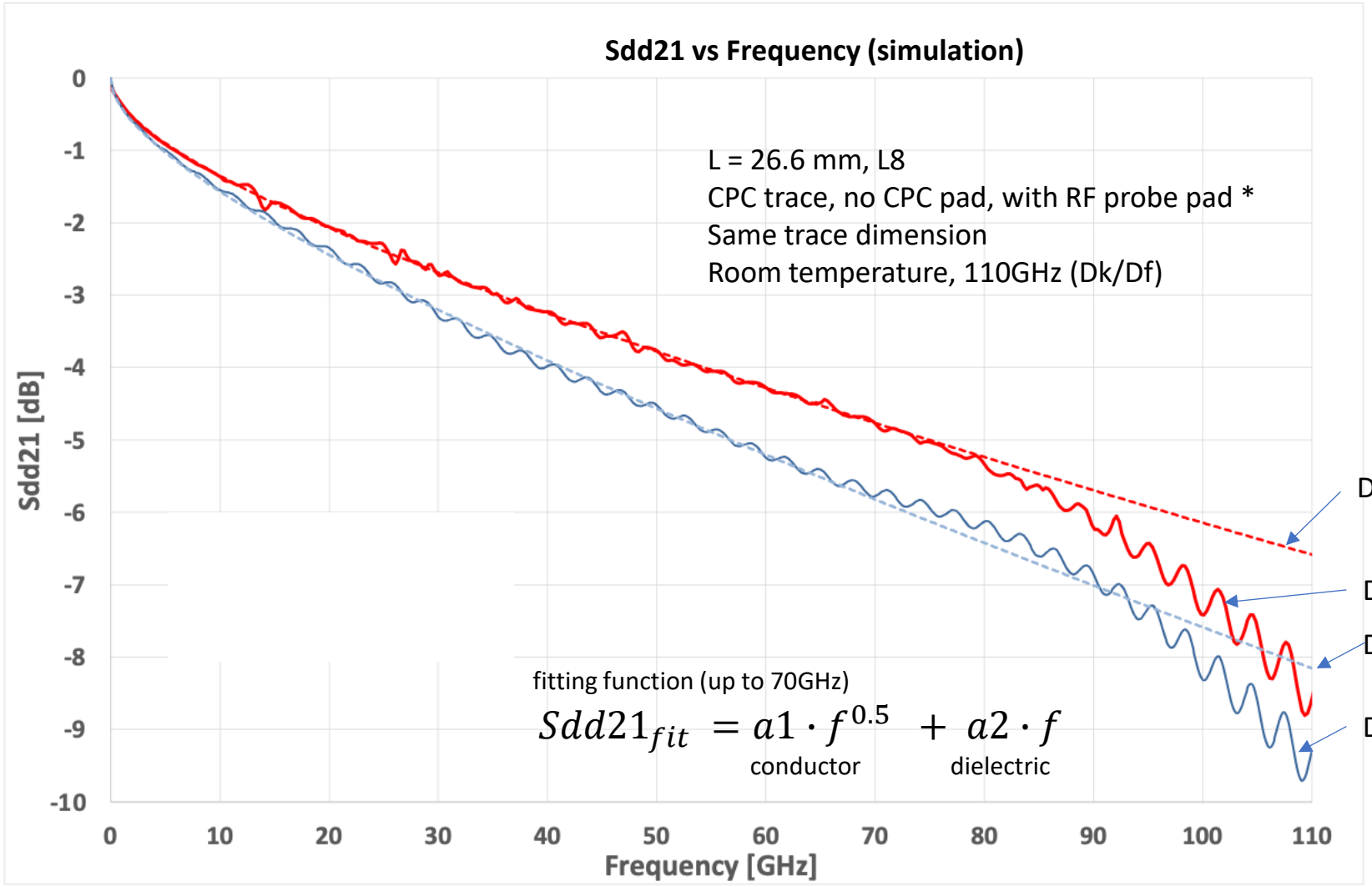




- Frequency dependency of Dk is relatively small.
- Frequency dependency of Df depends on the material.
- Temperature dependency of Df depends on the material.
- For the lower Dk materials further geometry tuning is required to match impedance.
- In this study, 92.5 ohm is used as the target impedance. Lower impedance target (e.g. 85 ohm) is future work.
- Analysis of Material-C is future work.

5. Results: Material-A (1/2)

- Lower Dk/Df material shows insertion loss reduction.



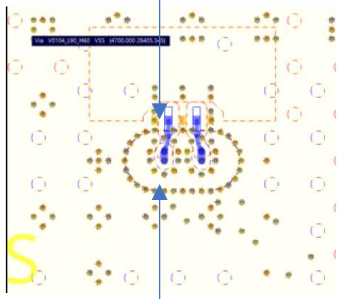
Dk = 3.0, Df = 1.0 e-3 (fitted)

Dk = 3.0, Df = 1.0 e-3

Dk = 3.4, Df = 3.0 e-3 (fitted)

Dk = 3.4, Df = 3.0 e-3

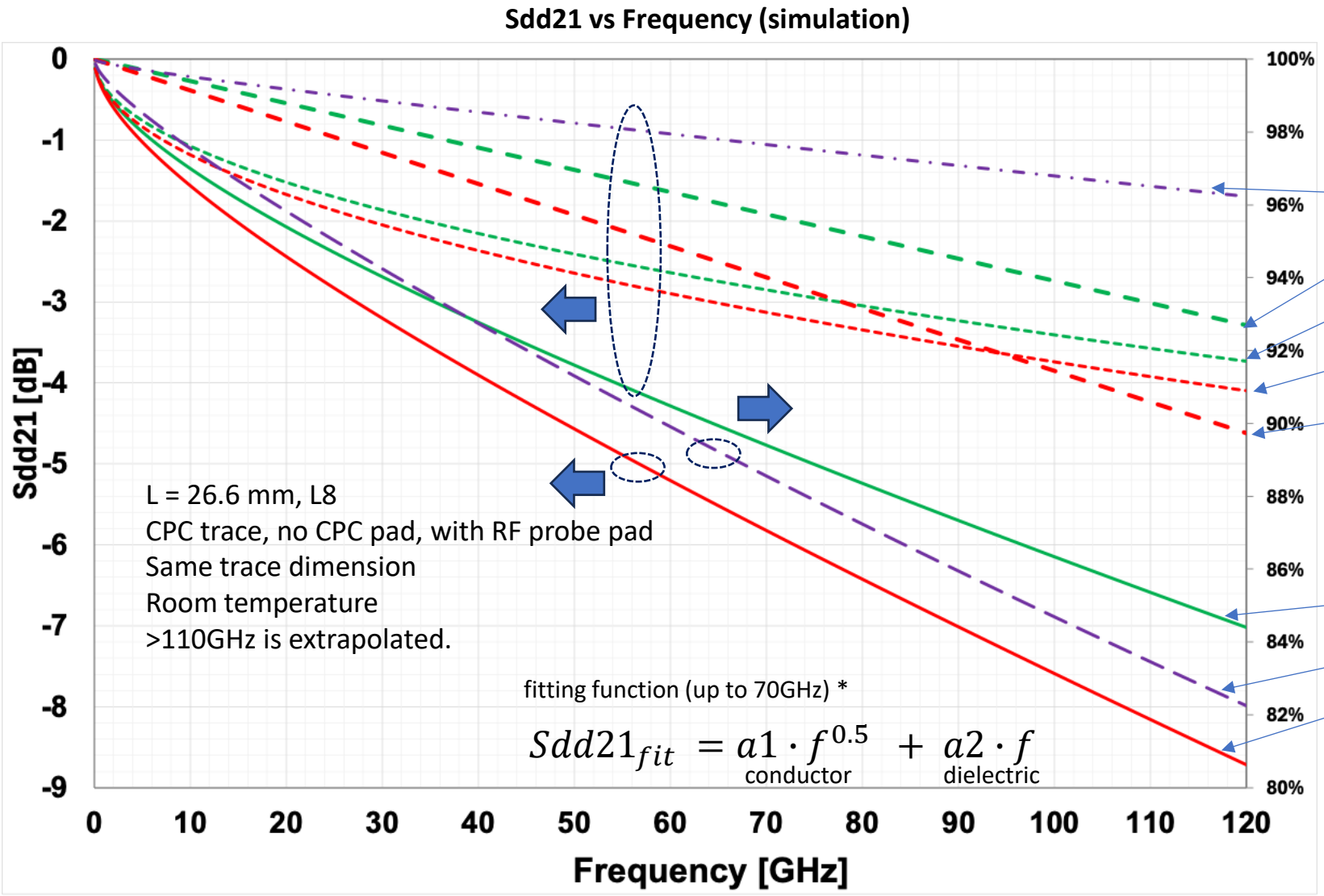
RF probe pad



- CPC pad removed to exclude the pad-induced roll-off (see Appendix D)
- GND via modified to reduce impedance mismatch.

*: Keeping RF probe pads is for the future measurement and model correlation, though some degradation above 70GHz is observed.

5. Results: Material-A (2/2)



- Though the Df value reduced to 1/3, the insertion loss improvement is limited as conductor loss associated with Dk and Ra becomes dominant.

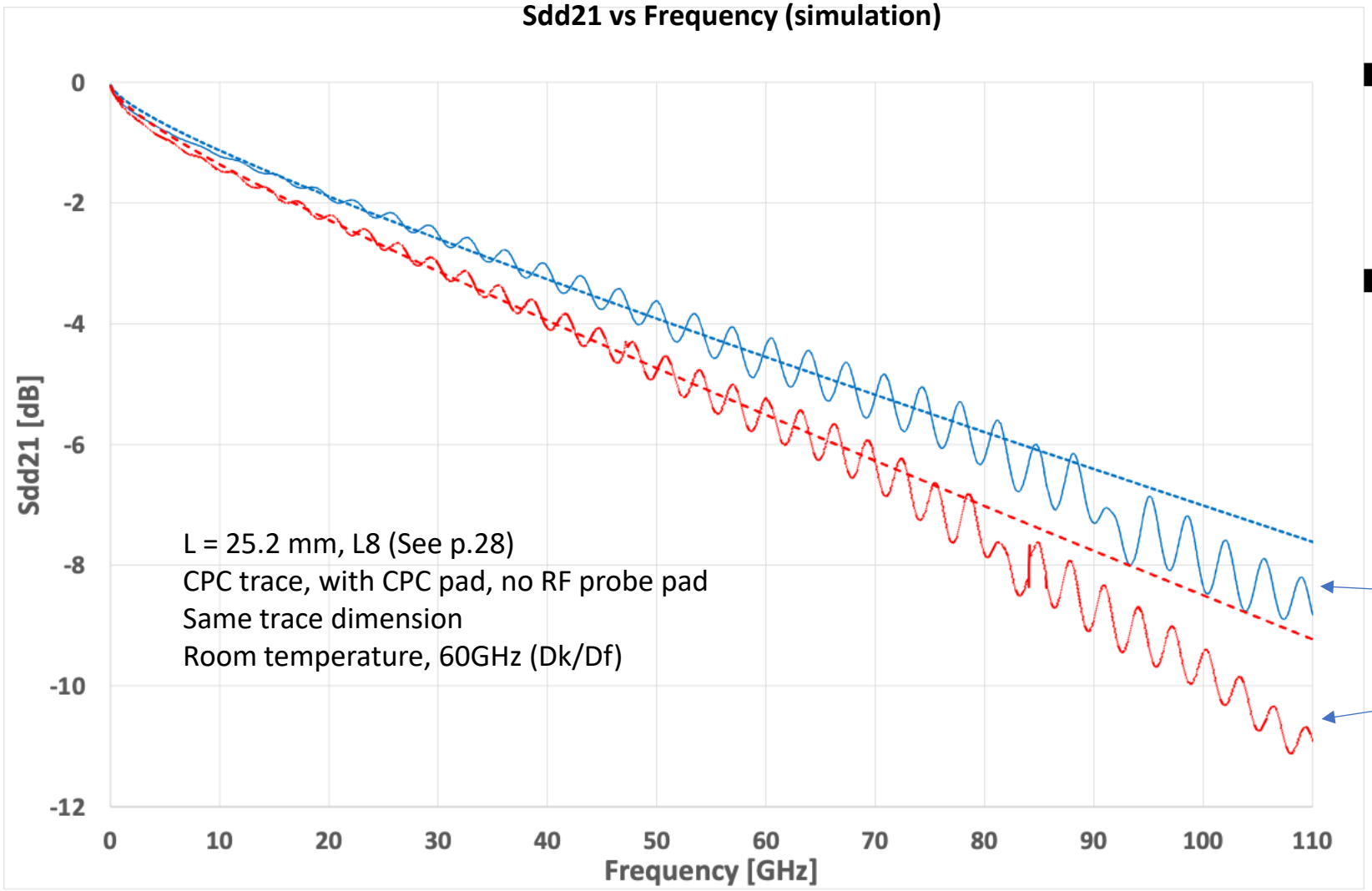
-ΔIL = IL(new material) – IL(GL107 eq.) [dB]
smaller (more negative) value is better

Dielectric: Dk = 3.0, Df = 1.0 e-3
Conductor: Dk = 3.0, Df = 1.0 e-3
Conductor: Dk = 3.4, Df = 3.0 e-3
Dielectric: Dk = 3.4, Df = 3.0 e-3

Total Dk = 3.0, Df = 1.0 e-3
IL Ratio (Material-A / GL-107 Equivalent) [%]
Total: Dk = 3.4, Df = 3.0 e-3 (fitted)

*: With this fitting function, part of the conductor loss caused by surface roughness is included into a2. So, this decomposition is a coarse estimation.

5. Results: Material-B (1/2)



- Both lower Df and lower Dk are expected to contribute to the insertion-loss reduction.
- In this case, only the Dk and Df values were changed, while the geometry remained unchanged. Further tuning is required to optimize the performance.
- Ripple in IL is caused by the CPC pad and the impedance mismatch (105 Ω vs. 92.5 Ω); it is expected to be reduced with proper termination by the connector (future work).

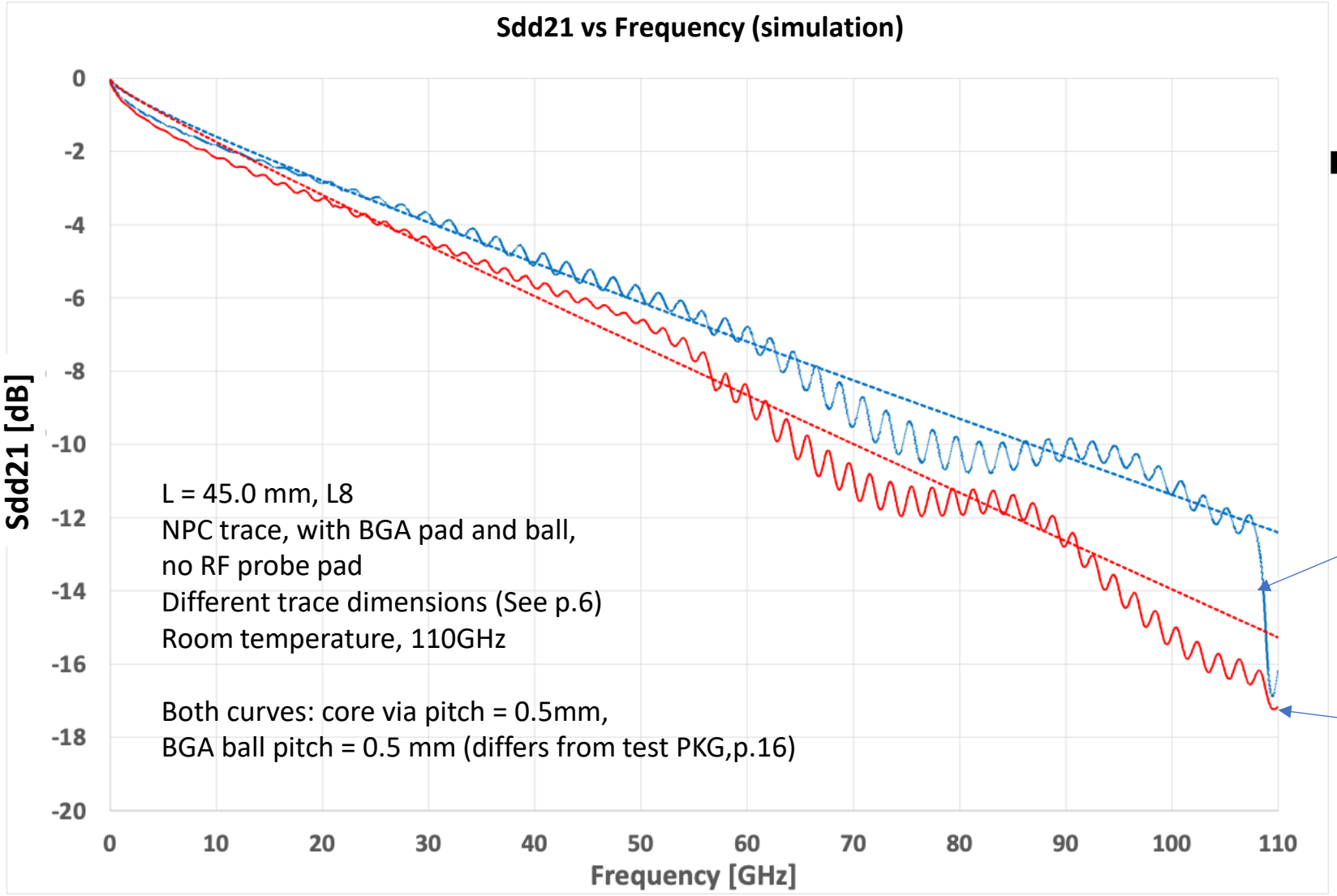
Total Dk = 2.70, Df = 1.6 e-3
Material-B (Zdiff 105 ohm)

Total: Dk = 3.4, Df = 3.0 e-3
GL-107 equivalent (Zdiff 93 ohm)

fitting function (up to 70GHz)

$$Sdd21_{fit} = \underset{\text{conductor}}{a1 \cdot f^{0.5}} + \underset{\text{dielectric}}{a2 \cdot f}$$

5. Results: Material-B (2/2)



- With lower Dk, it is necessary to modify the trace dimension to adjust impedance to the target value.
- Lower Dk allows a wider trace for the same target impedance. The resulting conductor-loss benefit could not yet be isolated in this study. (see p.12).

Total Dk = 2.73, Df = 2.2 e-3
- Observed sharp dip near 110GHz may come from resonance of BGA pad and/or ball , further study is ongoing.

Total: Dk = 3.4, Df = 3.0 e-3

fitting function (up to 70GHz)

$$Sdd21_{fit} = \underset{\text{conductor}}{a1 \cdot f^{0.5}} + \underset{\text{dielectric}}{a2 \cdot f}$$

5. Results: Insertion-Loss Improvement Summary

ΔIL = IL(GL107 eq., Dk 3.4 / Df 3.0e-3) − IL(new material) [dB] (dB/mm in parentheses)

Case	Material (Dk / Df)	Temp/Freq	Pad	Channel	Trace W/S	53GHz 212G PAM4	85 GHz 425G PAM6	106GHz 425G PAM4
1 (p.7-8)	Mat-A 3.0 / 1.0e-3	RT/110GHz	RF probe no CPC	CPC 26.6 mm	Same 23/63 µm	0.9 (0.032)	1.3 (0.049)	1.6 (0.060)
2 (p.9)	Mat-B 2.70 / 1.6e-3	RT/60GHz	No RF probe CPC	CPC 25.2 mm	Same 23/63 µm	0.9 (0.036)	1.4 (0.054)	1.6 (0.065)
3 (p.10)	Mat-B 2.73 / 2.2e-3	RT/110GHz	No RF probe NPC (BGA ball)	NPC 45.0 mm	Tuned 28/50 µm	1.4 (0.030)	2.3 (0.051)	2.9 (0.065)

- At 106 GHz, ΔIL ≈ 1.6 dB for 26.6 mm / 25.2 mm CPC and ≈ 2.9 dB for 45 mm NPC, i.e. ≈ 0.060-0.065 dB/mm in all cases.
- With the same trace geometry, Material-A (low Df) and Material-B (low Dk) give similar per-mm improvement (pad conditions differ; see table).
- Trace-width tuning (Case 3) shows no significant additional per-mm benefit within reading accuracy. **A dedicated same-channel study will be required to quantify the conductor-loss benefit enabled by wider traces.**
- The conductor/dielectric split of the two-term fit is indicative only: roughness-related loss can be absorbed into the f-linear term.
- Material-B additionally enables wider traces, although the corresponding conductor-loss benefit has not yet been isolated.

Values read from the fitted curves (Sdd21_fit = a1·f^0.5 + a2·f) on pp.8–11; reading accuracy ≈ ±0.1 dB.

6. Future Works

- ✓ Lower impedance channel evaluation (e.g. ~ 85 ohm)
- ✓ Roughness optimization (Ra reduction)
- ✓ Combined Dk/Df/Ra scaling
- ✓ 400G/lane COM assessment

7. Summary

- Advanced build-up materials provide an insertion-loss improvement of approximately 0.06 dB/mm at 106 GHz.
- Material-A and Material-B provide similar per-mm improvement.
- Lower Dk potentially enables wider traces for the same impedance, but the resulting conductor-loss benefit is still to be quantified through a dedicated same-channel comparison.
- Additional improvement may be possible through conductor surface optimization (roughness reduction).

7. Summary (cont.)

- Implications for IEEE 802.3dv
  - Package loss should not be modeled only by Df scaling.
  - Advanced build-up materials provide approximately 0.06 dB/mm insertion-loss improvement in the evaluated channels.
  - Lower Dk enables wider traces, but the resulting conductor-loss benefit still requires further study.
  - Realistic future material roadmaps should be considered when establishing package assumptions for 400G/lane studies.

Thank you!

Questions?

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This document represents preliminary results for discussion within IEEE and does not imply consensus or endorsement by any members. The data and analysis are provided for reference and further technical discussion.

Appendix

A. Test PKG Overview
B. Model correlation with measured data
C. How We Isolate Intrinsic Package Behavior
D. Observation: The >70 GHz Roll-Off Originates from Interface Effects
E. References

A. Test PKG Overview

	spec/target
PKG Size	65.0 mm x 65.0 mm
Trace Length: Bump Pad ~ BGA Ball	33.0 mm/45.0 mm
Trace Length: Bump Pad ~ CPC Pad	18.0 mm/26.6 mm
BGA Ball Pitch / Size	0.8 mm (hexagonal) / 0.50mm (dia)
CPC Pad Pitch / Size	PN pair: 0.6 mm Tx-Tx/Rx-Rx: 1.2 mm (vert) Tx-Tx/Rx-Rx: 1.8 mm (horz) Tx-Rx: 1.8 mm (vert) / 0.43mm (dia)
Differential Impedance	92.5 ohm

	spec/target
Layer Stackup	9-2-9 (20Layers)
Total Thickness	2176 um
Core Thickness (*2)	1280 um
Cu thickness	15 um
Dielectric Thickness	30 um
Trace Line/Space (designed)	15 um /15 um (min) 23 um/63 um (BGA/NPC) 20 um/49 um (CPC)
BU Material(*1)	GL107 equivalent, Dk 3.40/Df 0.0030
Core Material(*1)	E795G(LH) equivalent, Dk 3.96/Df 0.008
Surface Treatment(*4)	CZ8401 equivalent, Ra = 100 nm

- Assuming “class B(*3)” equivalent usage.
  - high radix/lane count
  - high density
  - no skip layers

(*1): at Room Temp. @60 GHz
- material vendor’s “table value”

(*2): Assuming large PKG size ~120 mm-sq,
- Also to mitigate PKG warpage.

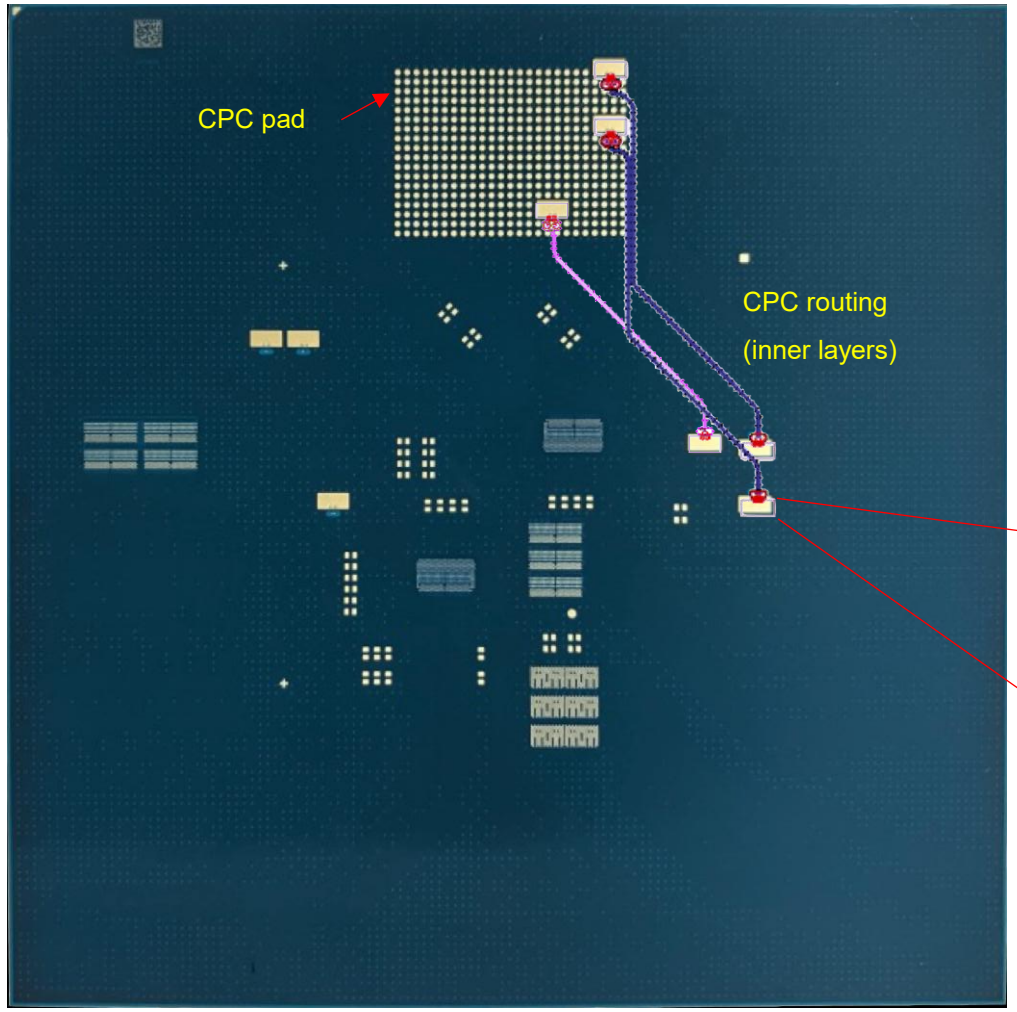
(*3): Please refer to IEEE P802.3dj draft.

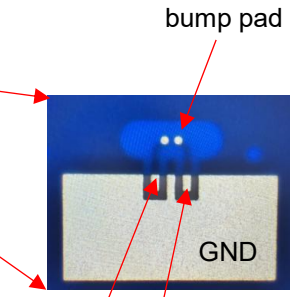
(*4): Vendor’s “catalog value”

CPC: Co-Packaged Copper
NPC: Near Package Copper (Using BGA ball and PCB connection)
BU: Build Up

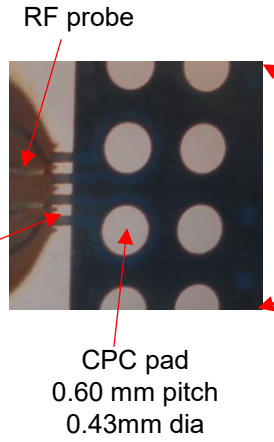
A.1 PKG Substrate (CPC)

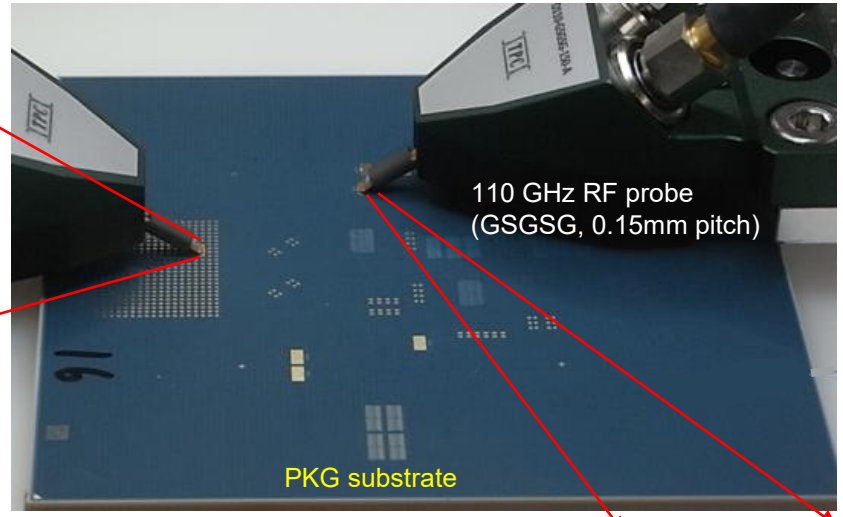
top view (bump/CPC side)

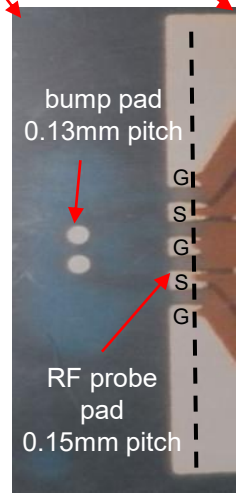




Both bump pads and CPC pads are with RF probe pads for measurement.





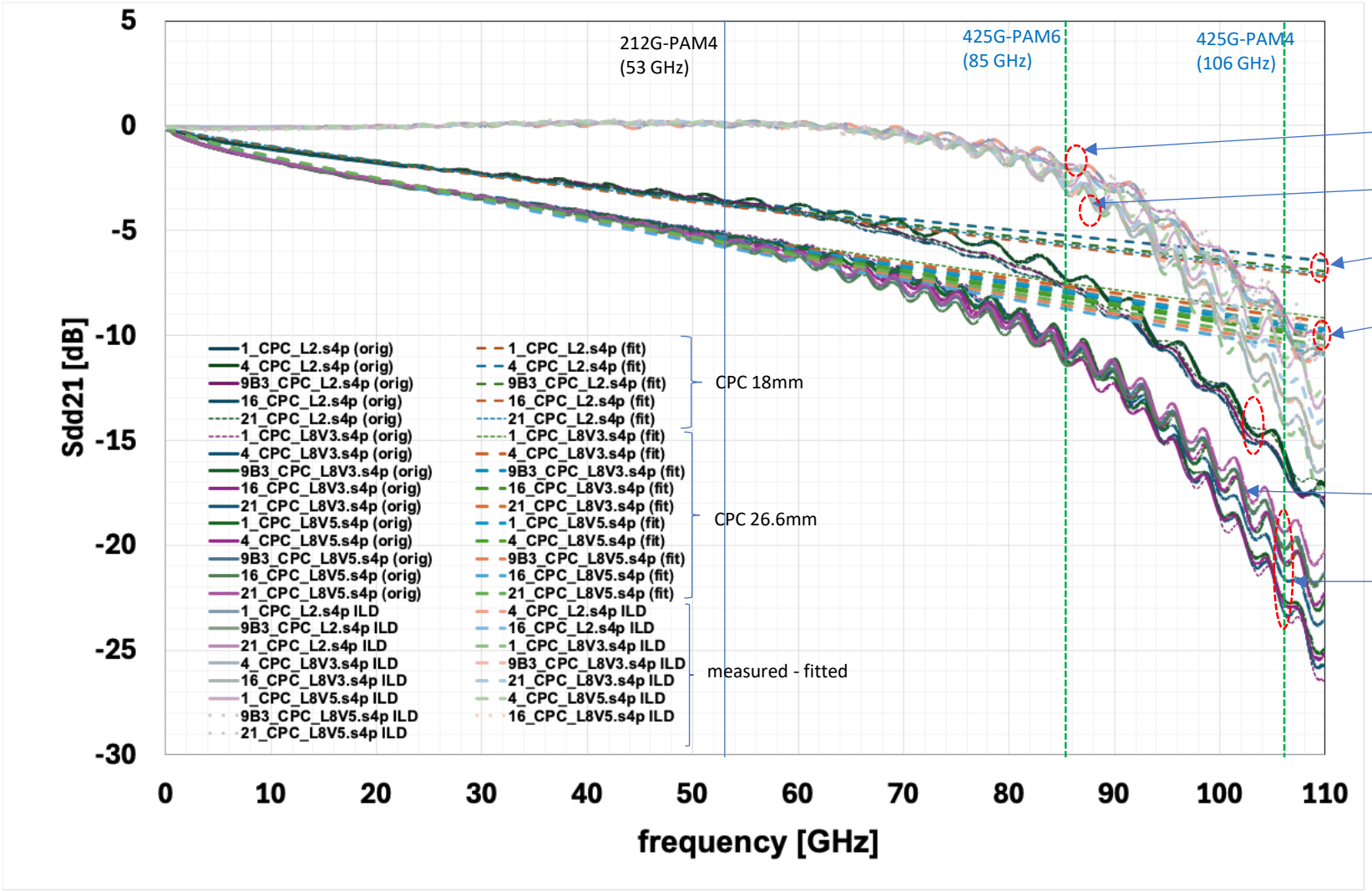


reference plane
at RF probe tip
(calibration is done here)

- To measure up to 110 GHz, 0.15mm pitch GSGSG RF probe was used.
- To absorb the different pitch (CPC pad, bump pad), additional PKG routing was required to the RF probe pads.

- We understand this may introduce artificial effects in measurement. By taking correlation and measurement, we can build the correlated model and eliminate these effect in simulation.

A.1.1 measured Sdd21 (CPC)



fitting function

$$Sdd21_{fit} = \underbrace{a1 \cdot f^{0.5}}_{\text{conductor}} + \underbrace{a2 \cdot f}_{\text{dielectric}}$$

measured - fitted_18mm

measured - fitted_26.6mm

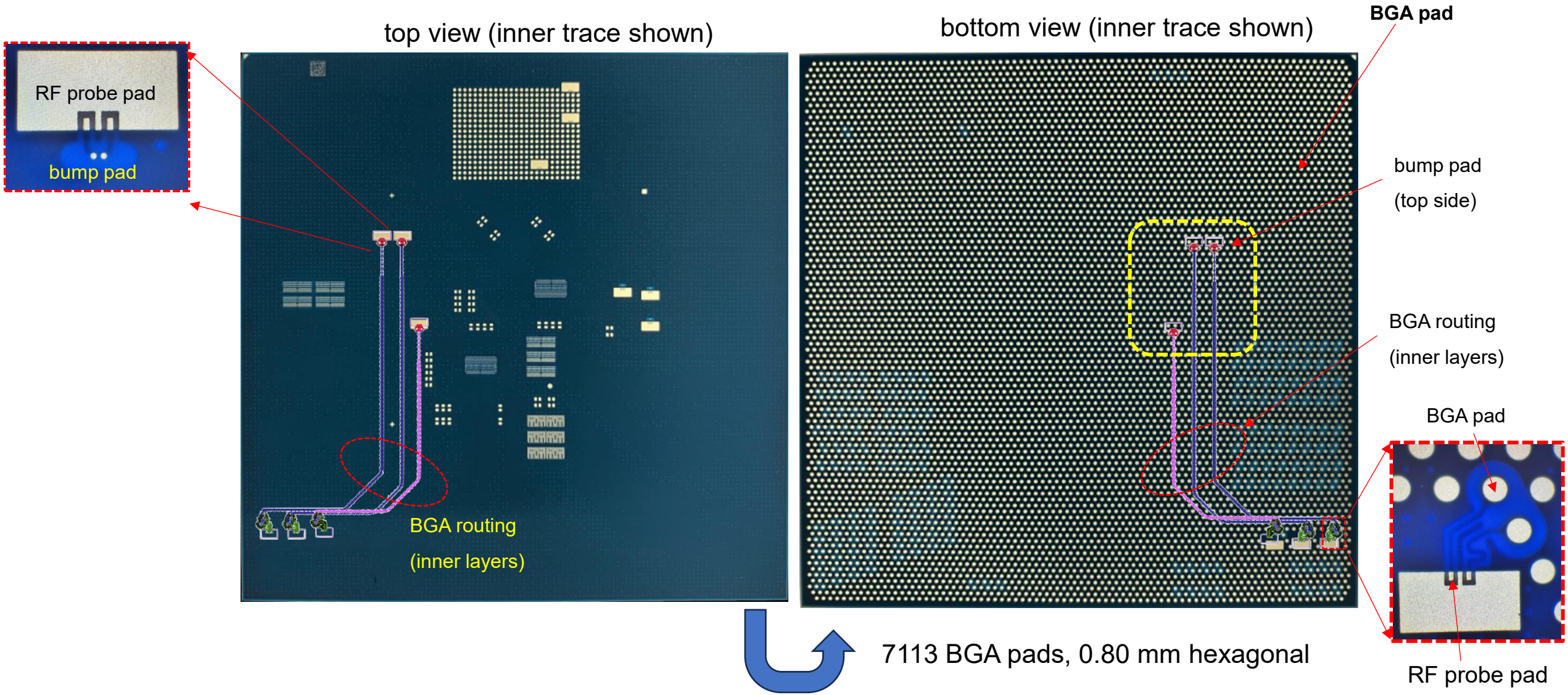
fitted_18mm(up to 70 GHz)

fitted_26.6mm(up to 70 GHz)

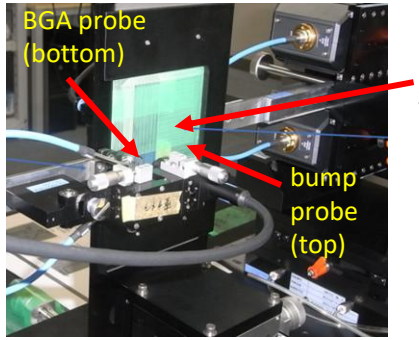
measured_18mm (5-samples)

measured_26.6mm (2-type x 5-samples)

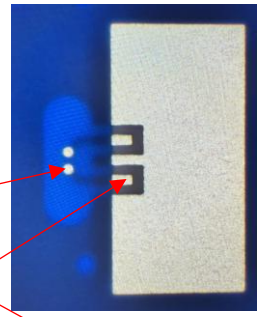
A.2 Test Package Substrate (NPC/BGA)



A.2.1 PKG Substrate (NPC/BGA) Measurement



PKG
Substrate
(vertical)



bump pad

RF probe pad

to VNA port

1.00 mm conn

RF probe

bump side (top)

PKG substrate

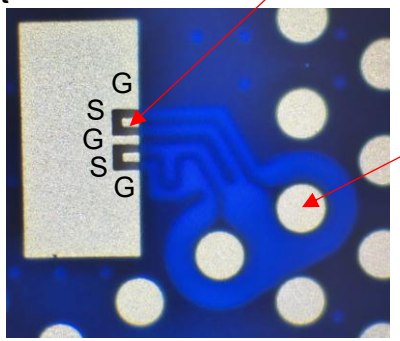
BGA side (bottom)

RF probe

RF probe pad

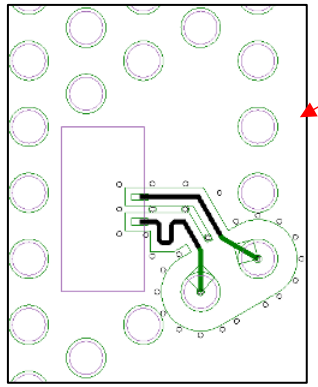
1.00 mm conn

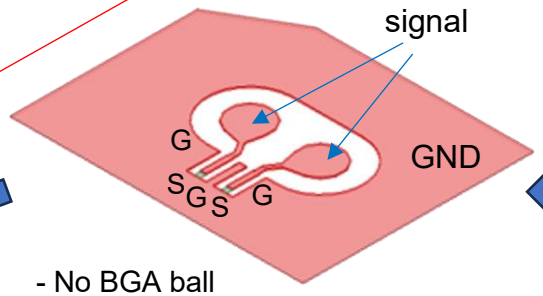
to VNA port



BGA pad

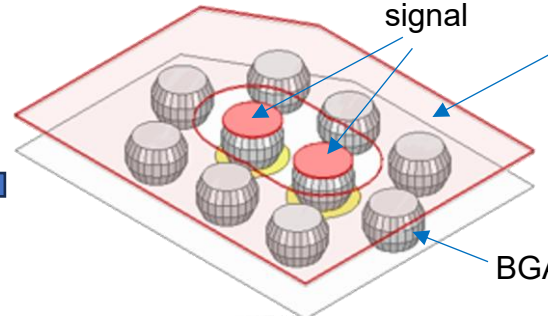
BGA measured structure





- No BGA ball
- 150um RF probe pitch
- GSGSG

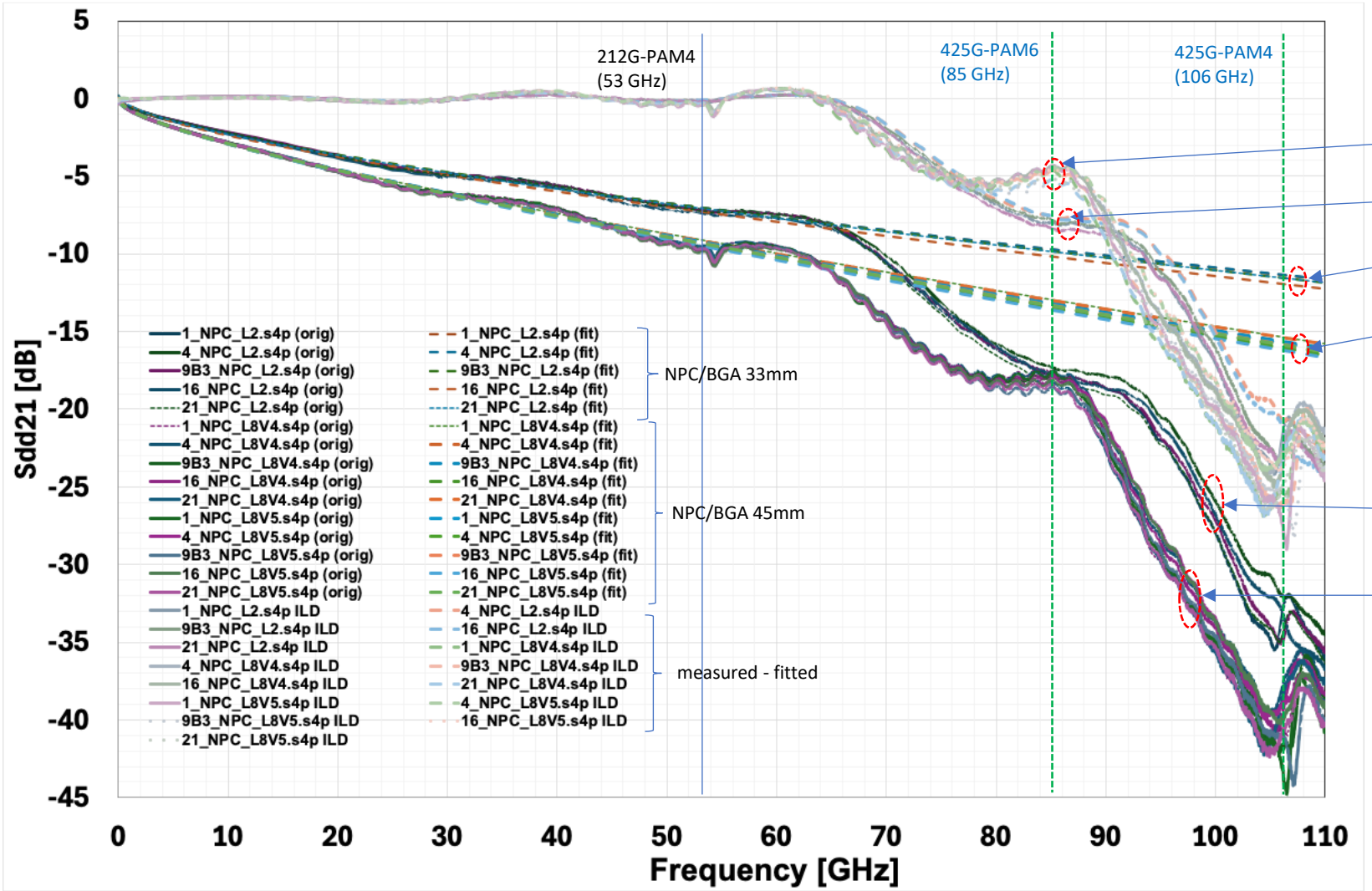
BGA actual structure



- RF probe cannot probe directly, due to pad pitch (0.8mm).
- Need “GSGSG” structure for 110 GHz measurement.

- Measurement of the NPC/BGA substrate required simultaneous probing from both top and bottom sides to capture through-path characteristics.
- This caused “fixed” RF probe direction for stable measurement.
- As the BGA balls are hexagonally placed, it is necessary to route from BGA ball pad to RF probe pad with “non-straight” routing lines.

A.2.2 measured Sdd21 (NPC/BGA)



fitting function

$$Sdd21_{fit} = a1 \cdot f^{0.5} + a2 \cdot f$$

conductor dielectric

measured - fitted_45mm

measured - fitted_33mm

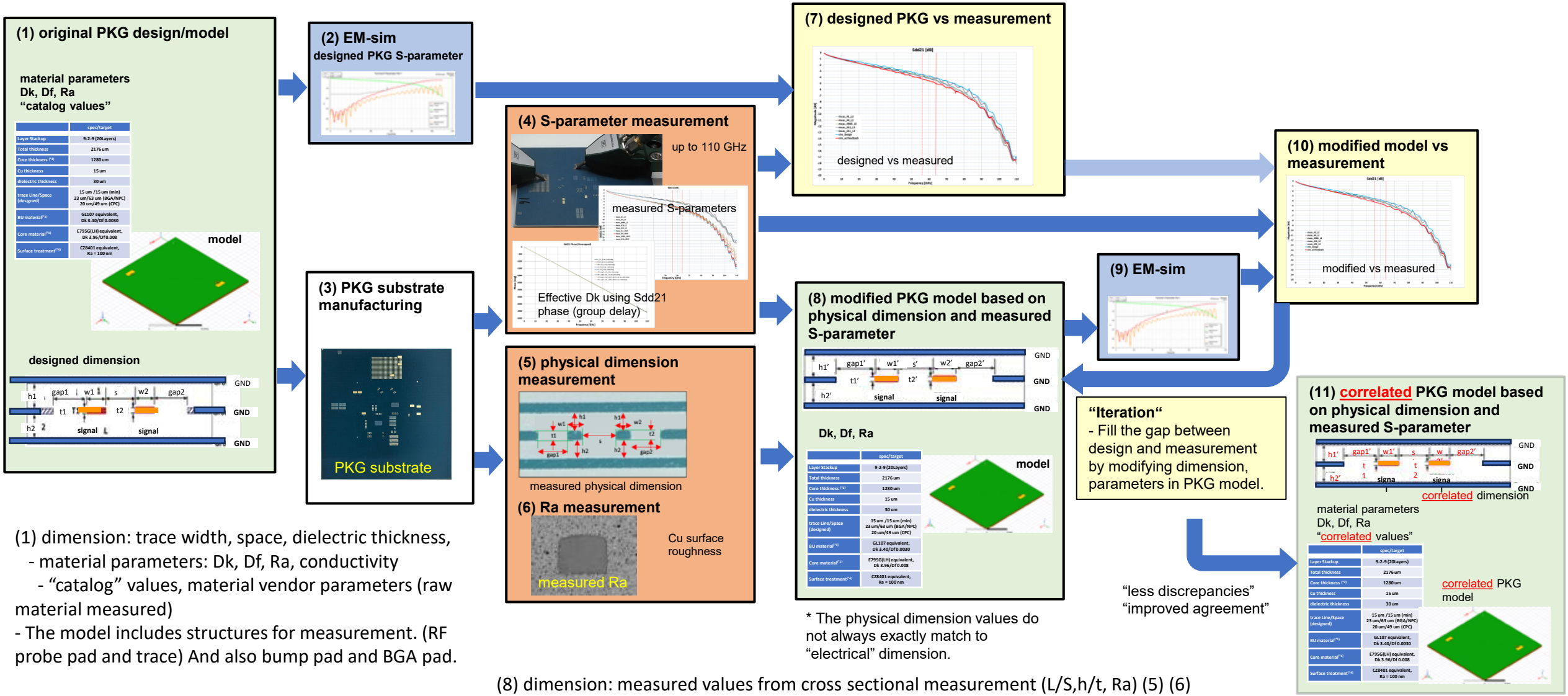
fitted_33mm(up to 70 GHz)

fitted_45mm(up to 70 GHz)

measured_33mm (5-samples)

measured_45mm (2-types x 5-samples)

B. Model correlation with measured data



(1) dimension: trace width, space, dielectric thickness,
- material parameters: Dk, Df, Ra, conductivity
- "catalog" values, material vendor parameters (raw material measured)
- The model includes structures for measurement. (RF probe pad and trace) And also bump pad and BGA pad.

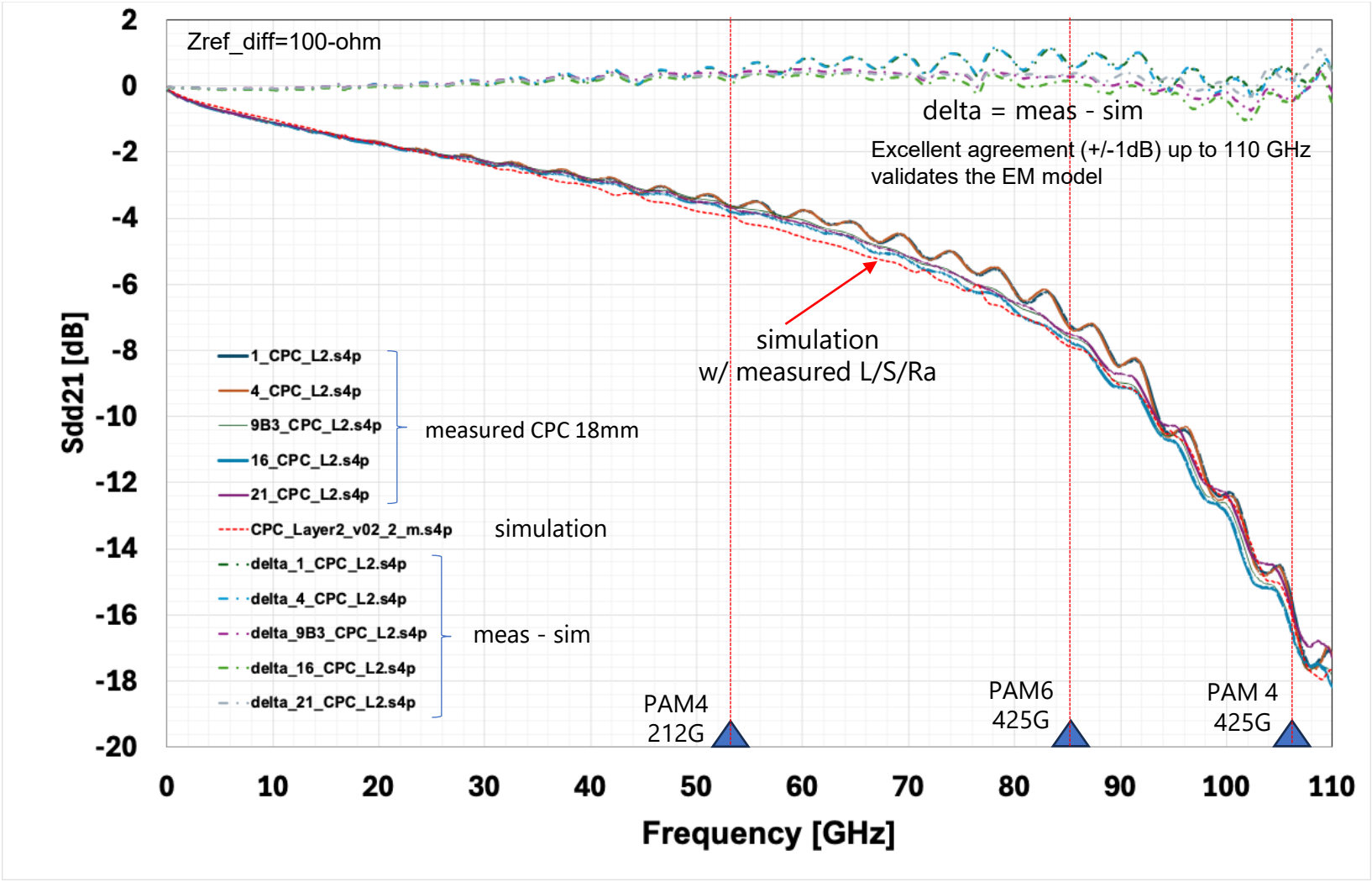
* The physical dimension values do not always exactly match to "electrical" dimension.

(8) dimension: measured values from cross sectional measurement (L/S,h/t, Ra) (5) (6)
(4) Dk_eff: fitting to measured Sdd21 phase (group delay)

B.1 Simulation

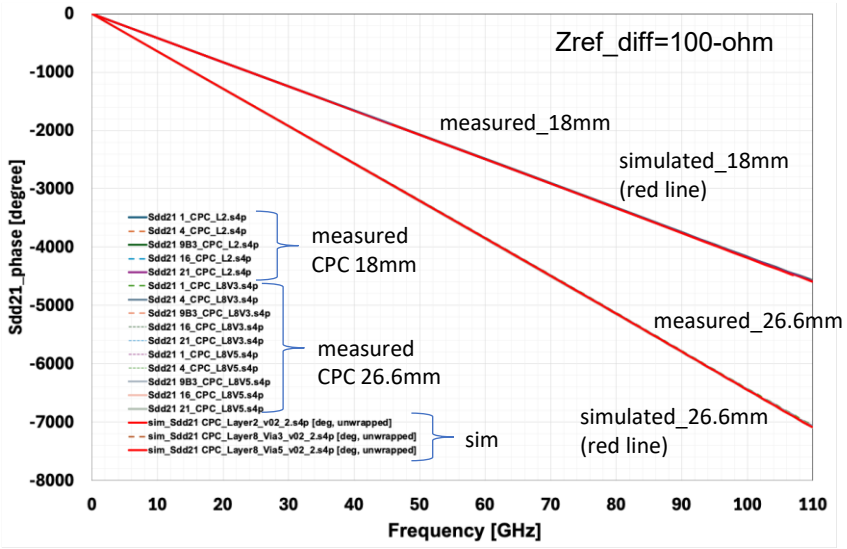
- 1st step:
  - dimension: trace width, space, dielectric thickness,
  - material parameters: Dk, Df, Ra, conductivity
    - “catalog” values, material vendor parameters (raw material measured)
- 2nd step:
  - dimension: measured values from in-line measurement (L/S, Ra)
  - material parameters: fitting to measured S-parameter values
  - Exclude CPC pad and RF probe pad effects by simulation model modification.
  - Update COM PKG model using updated CPC PKG trace model (tentative TP0p/TP5p)
- 3rd step (This contribution): Modify dimension, structure and material parameters will be available for production in 2~3 years.

B.2 Correlated PKG Model: Agreement with Measurement



The measured results correlate well with the simulated results of the PKG trace with the RF probe pad.

- Both bump pads and CPC pads are with RF probe pads for measurement.



- Also, simulated Sdd21 phase correlates well with measured results. (Dk_eff was derived from group delay fitting to ensure phase accuracy.)

C. How We Isolate Intrinsic Package Behavior

Step A: De-embedding RF Probe Interfaces:

- Remove the artifacts of the 0.15mm-pitch GSGSG probe pads and the associated escape routing.
- This shifts the reference plane from the probe tip to the TP0d/TP5d (die-side bump pad).

Step B: Extraction of Intrinsic Channel (TP0p to TP5p):

- Remove the CPC pad and the breakout region (defined as the pad plus approximately 1mm of routing).
- This isolates the intrinsic trace, leaving only the through-via and the horizontal routing.

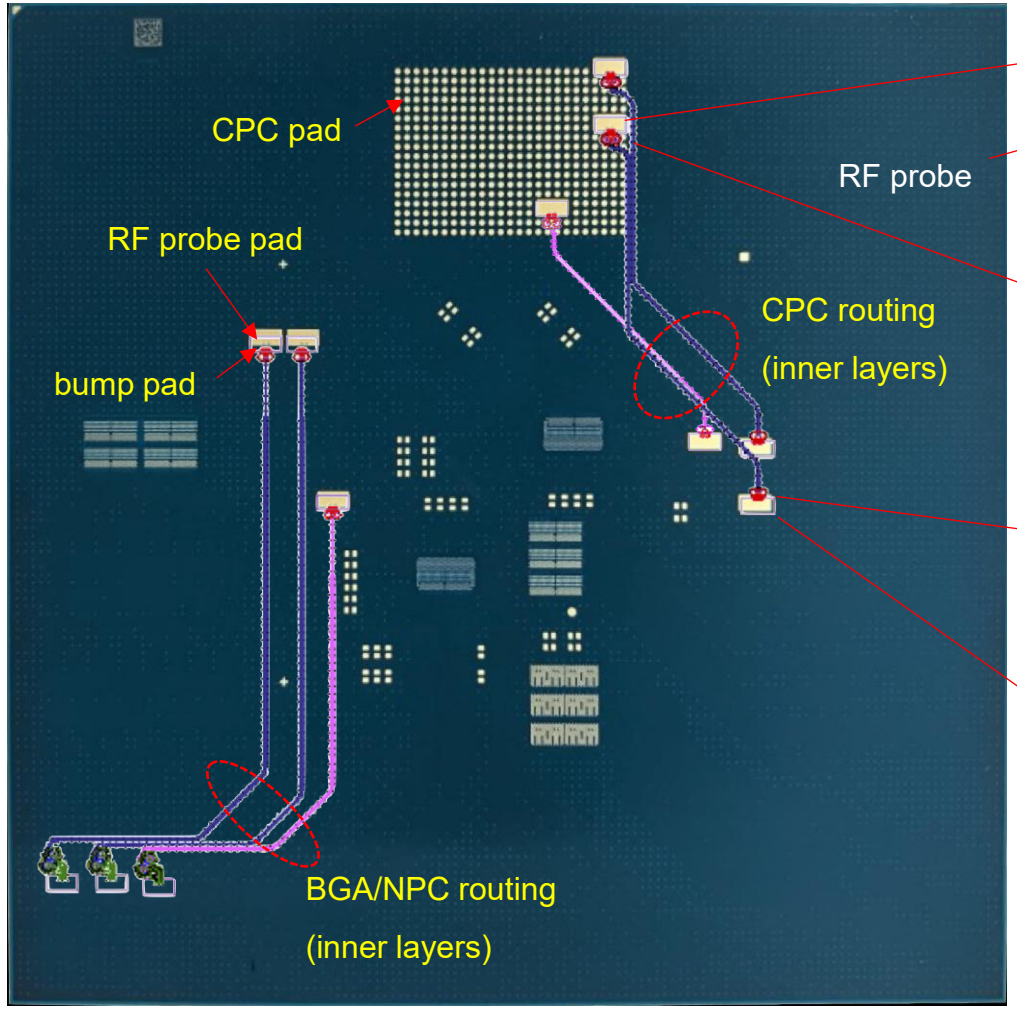
Step C: Comparative Roll-off Analysis:

- Compare the S-parameters of the "Full Interface Model" vs. the "Intrinsic Model" to quantify the exact contribution of the CPC pad to the insertion loss roll-off.

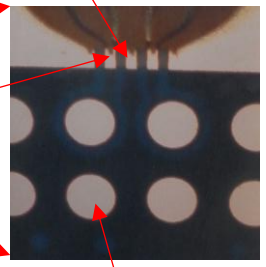
Conclusion: CPC pad appears to dominate the observed > 70 GHz roll-off in this measurement configuration.

C.1 Isolate Intrinsic Package Behavior

PKG Substrate Top View



RF probe pad (A)

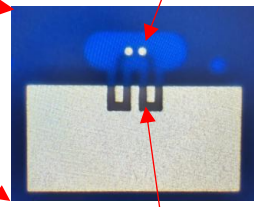


CPC pad (B)

430um diameter

bump pad *

80um diameter



RF probe pad (A)

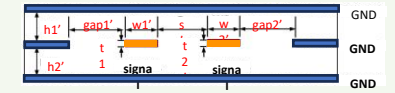
80um width

Step 0: Measured (Full structure)
Step A: Remove Probe Pads (Artifact of measurement setup)
Step B: Remove CPC Pads (Artifact of strictly defining "PKG trace")

(1) Run the EM simulation using correlated dimension and material parameters.

(2) See the effect of RF probe pad and CPC pad/breakout.

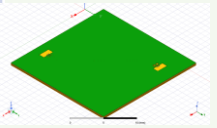
(11) correlated PKG design based on physical dimension and measured S-parameter



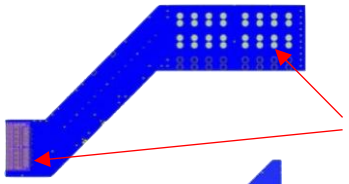
material parameters Dk, Df, Ra "correlated values"

	spec/target
Layer Stackup	9-2-9 (20Layers)
Total thickness	2176 um
Core thickness [*2]	1280 um
Cu thickness	15 um
dielectric thickness	30 um
trace Line/Space (designed)	15 um /15 um (min) 23 um/63 um (BGA/NPC) 20 um/49 um (CPC)
BU material[*3]	GL107 equivalent, Dk 3.40/Df 0.0030
Core material[*4]	E795G(LH) equivalent, Dk 3.96/Df 0.008
Surface treatment[*5]	CZ8401 equivalent, Ra = 100 nm

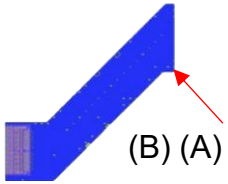
correlated PKG model



	RF probe pad	CPC pad/ breakout	bump pad	PKG channel
(A)	no	yes	yes	TP0d/TP5d ~ TP0/TP5
(B)	no	no	yes	TP0d/TP5d ~ TP0p/TP5p



(A) Exclude RF probe pad
- Both CPC side and bump side



(B) (A) + Exclude CPC pad/breakout

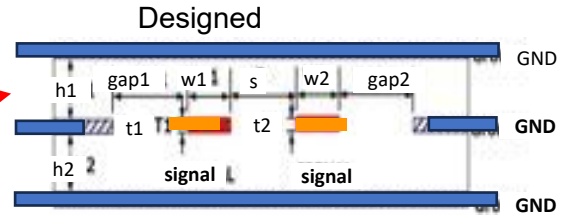
* As the bump pad pitch is far small (~130um), it still exists.

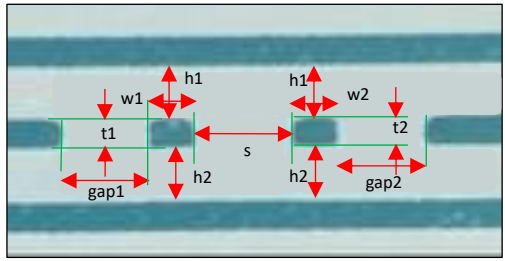
C.2 Isolate Intrinsic Package Behavior

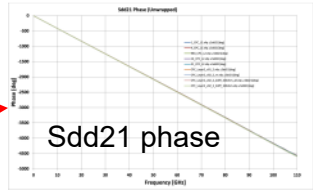
- 1st step : (1), (2)
  - dimension: trace width, space, Cu/dielectric thickness,
  - material parameters: Dk, Df, Ra, conductivity
    - “catalog” values, material vendor parameters (raw material)

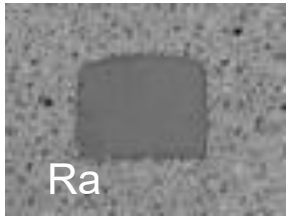
- 2nd step: (5),(6),(8),(9)
  - dimension: measured values from cross sectional measurement (L/S,h/t, Ra)
  - Dk_eff: fitting to measured Sdd21 phase/ group delay

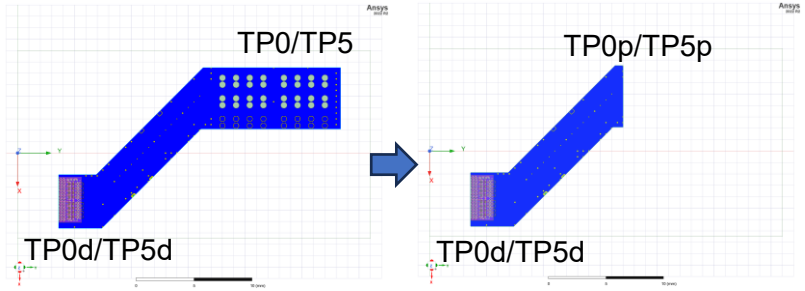
  - Exclude CPC pad and RF probe pad effects by simulation model modification.
  - Update COM PKG model using updated CPC PKG trace model (tentative TP0p/TP5p)





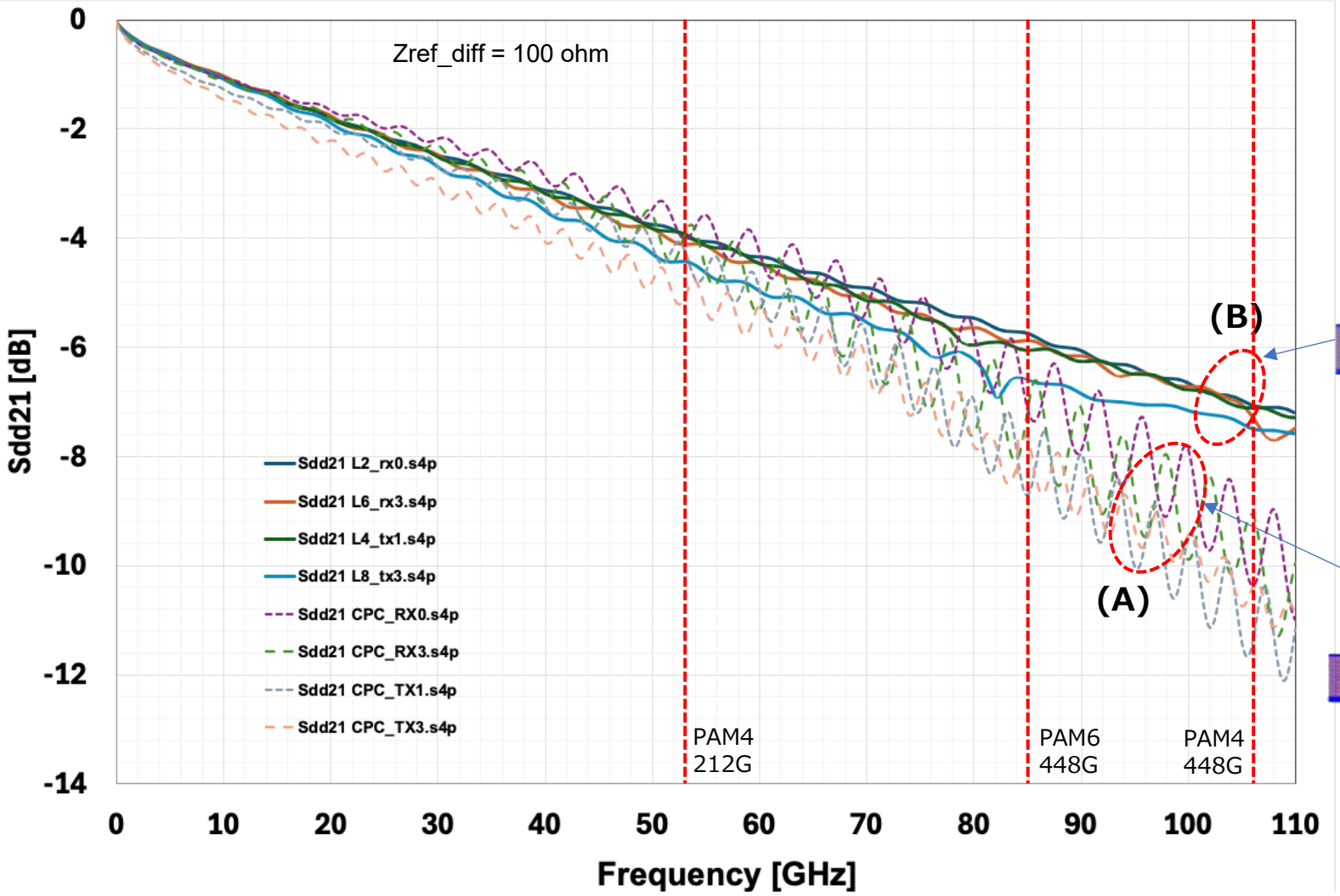






- 3rd step (This contribution): Modify dimension, structure and material parameters will be available for production in 2~3 years.

D. Observation: The >70 GHz Roll-Off Originates from Interface Effects

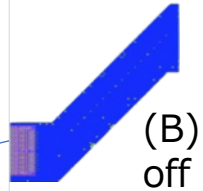


CPC pad & breakout dominate the observed roll-off in this configuration.

trace length [mm]

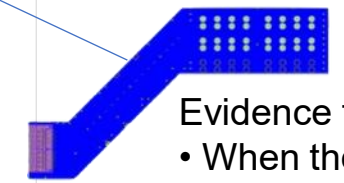
trace	(A)	(B)
L2_rx0	19.6	16.9
L6_rx3	19.5	15.8
L4_tx1	23.3	16.5
L8_tx3	25.2	16.0

	RF probe pad	CPC pad/ breakout	bump pad	PKG channel
(A)	no	yes	yes	TP0d/TP5d ~ TP0/TP5
(B)	no	no	yes	TP0d/TP5d ~ TP0p/TP5p



(B) Without CPC pad, no significant roll off is observed even with bump pad.

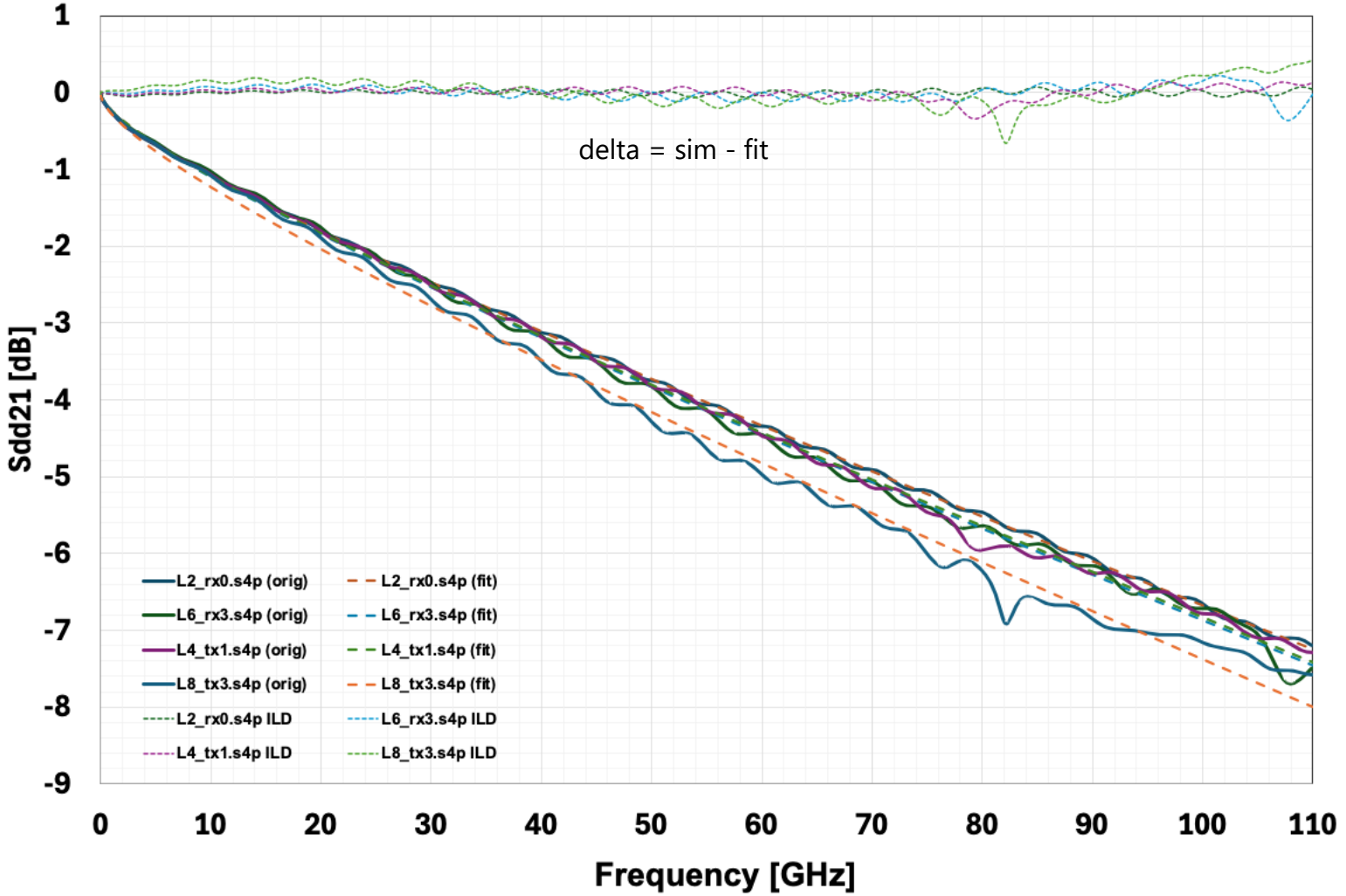
(A) Without RF probe pad and with CPC pad, significant roll off is still observed.



Evidence from Model (B):

- When the CPC pad is removed (Model B), the insertion loss follows a standard linear-root frequency roll-off:
- Agreement is maintained up to 110 GHz, proving that dispersion and dielectric loss are the only significant factors for the trace itself.

D.1 Intrinsic PKG Traces Without Interface Effects



(B) Without CPC pad, fitting to simple equation
$Sdd21_{fit} = a1 \cdot f^{0.5} + a2 \cdot f$
(intrinsic PKG trace only) correlates well with the model. (~+/-0.5dB up to 110 GHz)

- No fundamental roll-off is observed up to ~110 GHz under the evaluated boundary conditions.

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- The following are previous contributions related to this study:

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Thank you!

Questions?

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