IEEE P802.3dv · NOVEMBER 2026 PLENARY

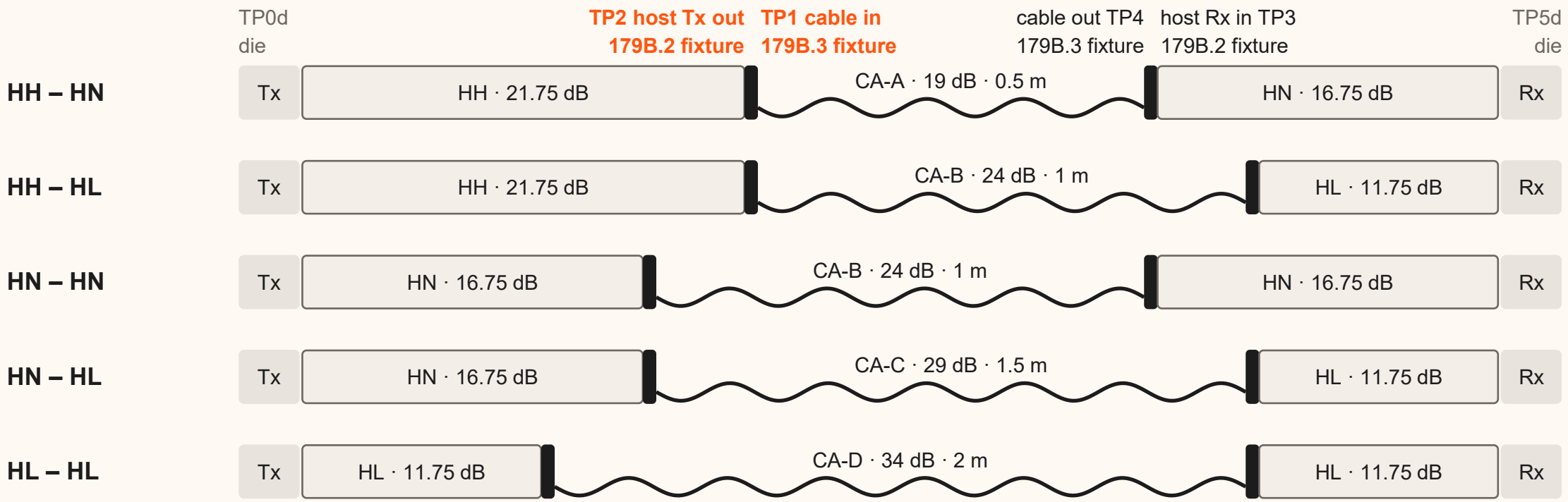
Captive Retimed Cables for 400GPL

Proposal

C2M electrical interfaces with explicit Captive Retimed Cable assembly requirements for error performance, delay, skew, startup and recovery.

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802.3dj CR: cable reach is traded against host loss

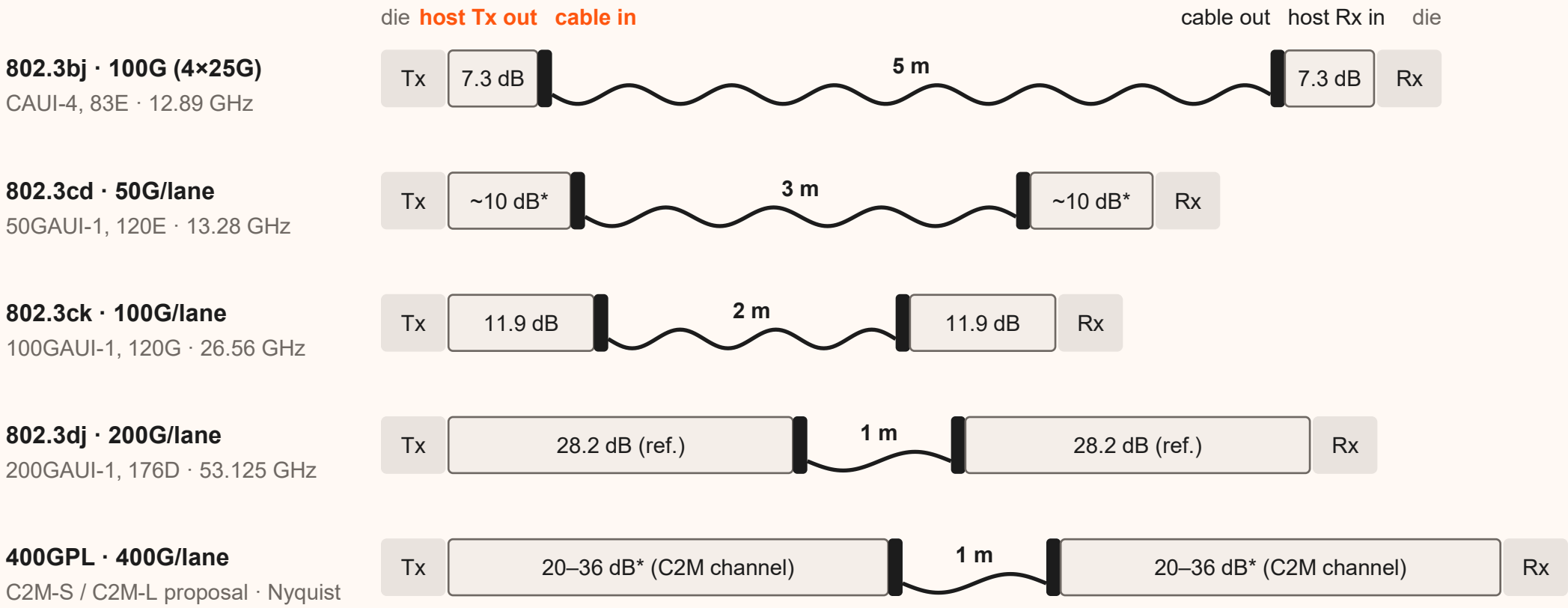


Each dB of cable comes out of the host

Reference loss allocations at 53.125 GHz
Reference arithmetic: TP0d–TP5d = TP0d–TP2 + TP1–TP4 + TP3–TP5d − 2 × 8.75 dB = 40 dB.
Lengths are the expected reach of each cable class

Copper reach objectives and AUI host loss

Host segments: AUI-C2M reference host loss at Nyquist
cable: CR reach objective

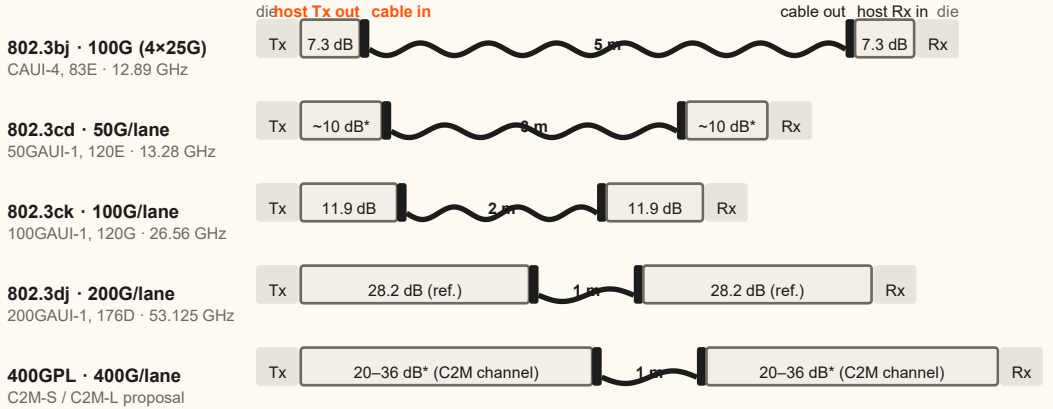


Target CR Reach shrinks faster than the AUI host budget grows

Only a module or Fully Retimed port can use the C2M budget

Fully retimed solutions resolve the trade-off

- **Only a module or Fully Retimed port can use the C2M budget**
- Various **captive** retimed cable solutions are gaining ground in the industry. **none can claim 802.3 compliance as an assembly**
  - **Electrical (AEC)**
  - **AOC**
  - **RF Waveguide**
  - **Optical slow and wide (uLED/uVCSEL)**



- **<u>What they share</u> :**
  - The host sees a retimed AUI-C2M port and never pays for cable length. The medium and its electronics are captive: a closed system that, today, has no full official verification definition.

- **<u>What they lack :</u>**
  - No 802.3 requirement on the assembly as a whole: no error allocation for the internal path, no delay or skew limit through the assembly. Captive optics can borrow Clause 180 PMDs; nothing requires it.

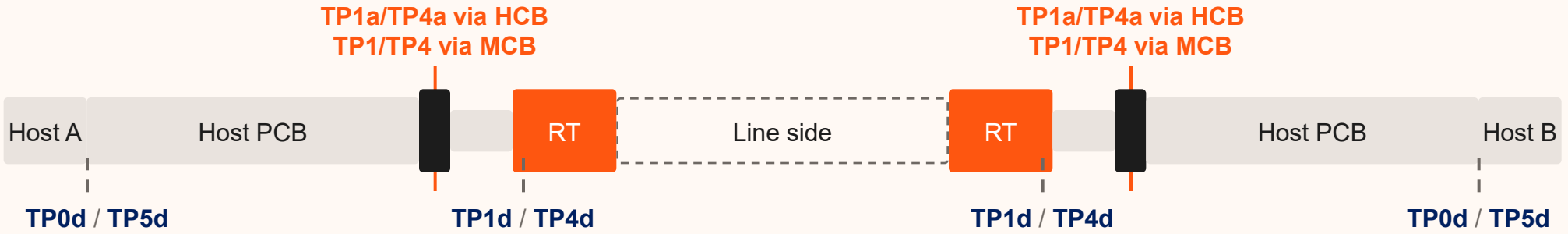
Active cable nomenclature

Name	Cable	Host port sees
DAC Direct attach copper, passive		CR PMD (Clause 179)
ACC Active copper cable, linear		CR-like port; no IEEE cable spec
Half AEC Retimer on Rx-to-host path only		Rx: AUI-like · Tx: CR-like
AEC Active electrical cable, retimed		AUI-C2M (Annex 176D)
AOC Active optical cable		AUI-C2M (Annex 176D)

Scope of this presentation : Captive active cable assemblies with C2M electrical interfaces at both ends, retiming in both transmission directions, and transparency to the host PCS/FEC stream. The internal medium may be electrical, optical or RF.

Terminology: lusted_3df_02a_2207

Captive Retimed Cable architecture and compliance boundaries



Orange: compliance points accessed through HCB/MCB fixtures
blue: die-level reference points

Specified today (176D)

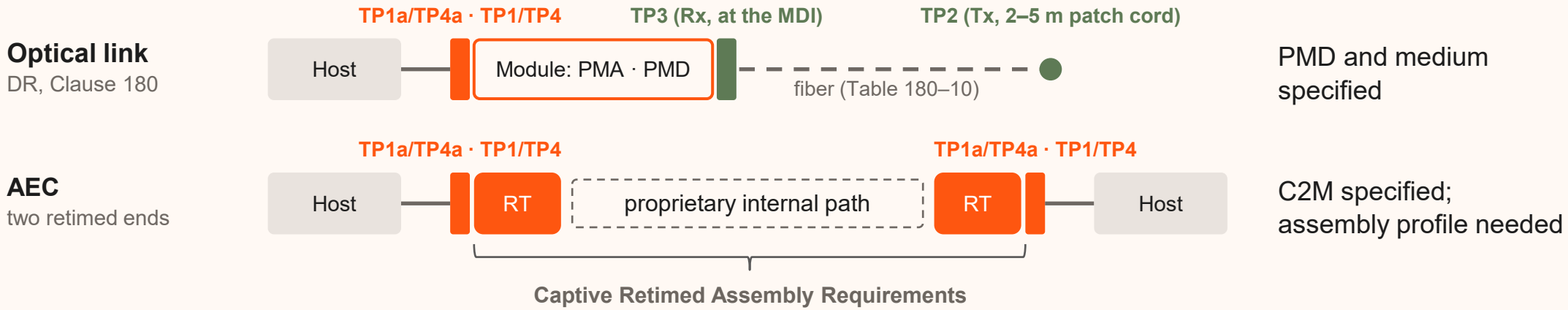
- Module input TP1 / output TP4 (176D–5 / –3)
- Host output TP1a / input TP4a (176D–2 / –4)
- ILT (E1), RTS and adjacent-interface signaling
- 46.08 ns: component Tx+Rx including channel*

Specific definition needed

- Assembly error allocation and stressed test
- Assembly delay, lane skew and variation
- Internal readiness/fault mapping to C2M

*176D.5: Tx+Rx sum includes the AUI channel in one direction; this is not a one-way retimer limit.

What 802.3dj D3.2 already covers: DR optical link vs Captive Retimed

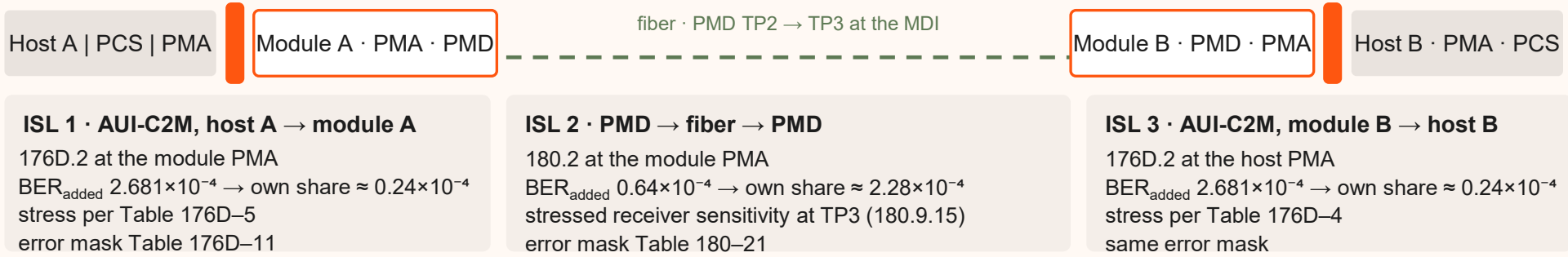


	DR optical link	Captive Retimed Cable
C2M host/module electrical compliance (176D.6)	●	●
C2M receiver error test at adjacent PMA (176D.2)	●	●
C2M component Tx+Rx delay budget (176D.5)	●	●
PCS-to-PCS error expectation (174A.6)	●	●
ILT/RTS and adjacent-interface signaling (178B)	●	●
Error allocation beyond the host C2M interfaces	● 180.2	○
Stressed-test conditions and methods beyond the host C2M interfaces	● 180.9	○
Delay, skew and skew variation beyond C2M	● 180.4	○

DR path tests every link; an while captive cable leaves one untested

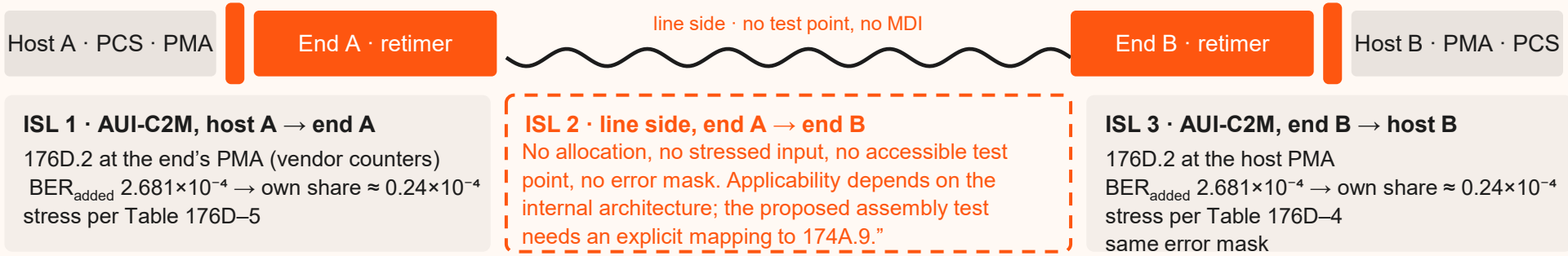
174A.9 tests one inter-sublayer (ISL) link and books the rest at BER_{added}
Component qualification relies on the remaining path meeting the allocation represented by BER_{added}

DR optical link



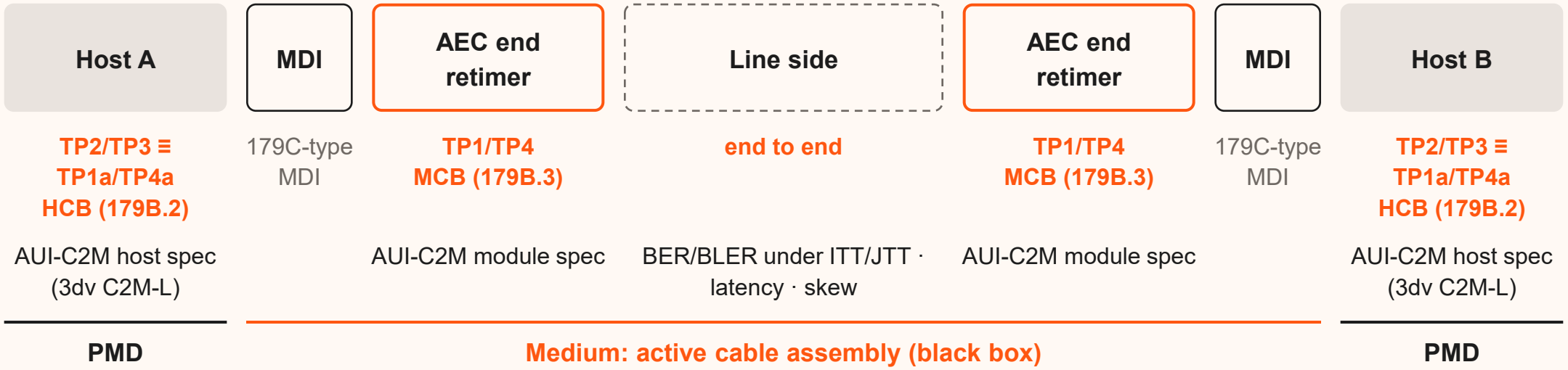
Own shares 0.24 + 2.28 + 0.24 = 2.761×10⁻⁴ ≤ BERtotal 2.921×10⁻⁴ (174A.6): consistent, and every term in the sum is measured by its own test.

Captive Retimed Cable



0.24 + ? + 0.24: the two C2M tests book 2.441×10⁻⁴ for the line side, and nothing verifies it.

Proposal: Captive Retimed Cables as a Specified Building Block



- **Hosts: nothing new**
- **Cable ends: an existing module specification-** Each end meets the AUI-C2M module specification at TP1/TP4 through the MCB
- **Assembly: the new part -** The cable is the medium, a black box held to end-to-end requirements: error ratio under stress, latency and lane skew from end-A TP1 to end-B TP4

Proposed end-to-end test

New item	Proposed test	Reuses
Error ratio through the cable	Stress at end-A TP1 (176D–5); measure at end-B TP4 with a defined measurement receiver; all-lanes histogram method (174A.9.7)	174A.9; BERadded = links outside the boundary, set with the allocation
Latency	One-way delay, end-A TP1 → end-B TP4; limit to be set	176D.5 is a Tx + Rx component budget, not reusable as is
Lane-to-lane skew	Skew and variation added between MDIs	Reference from the CR budgets (179.7): 80 ns / 2.8 ns, not yet applicable
Start-up and recovery	Mapping of line-side readiness and faults into SIGNAL_OK, RTS and the 178B states; start-up and recovery pass criteria	Annex 178B
Both directions, all lanes	A→B and B→A, all lanes active; operating corners, lengths, supported modes	Same setup, mirrored