Frame FEC in EPON Technical Proposal

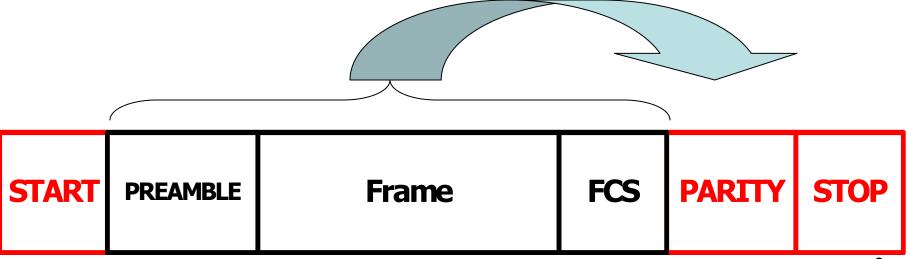
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- Frame based FEC proposal for enhanced performance
- Location of FEC in Ethernet stack
- Clarification of receive, transmit, and synchronization algorithm
- Proposal elaborates on khermosh_1_0102.pdf

Encoding

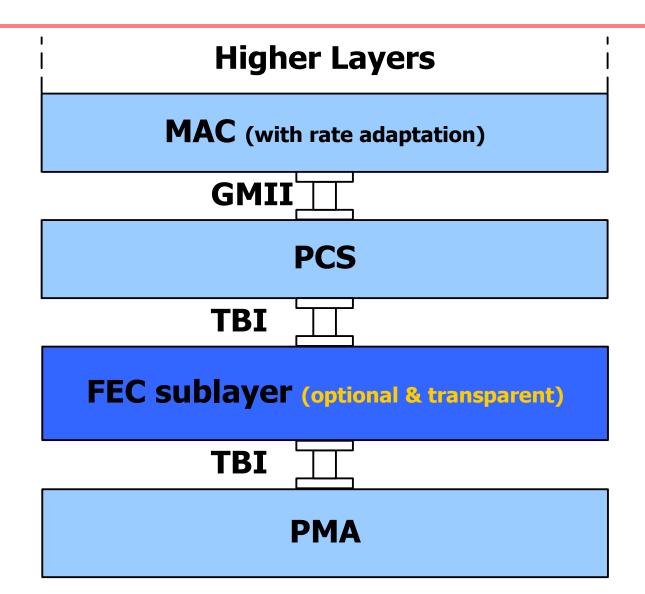
- Parity check bytes added at the end of the frame
- All of the frame is encoded including the preamble, Ethernet header and FCS
- Shortened last frame using virtual zero padding
- Idles are not protected



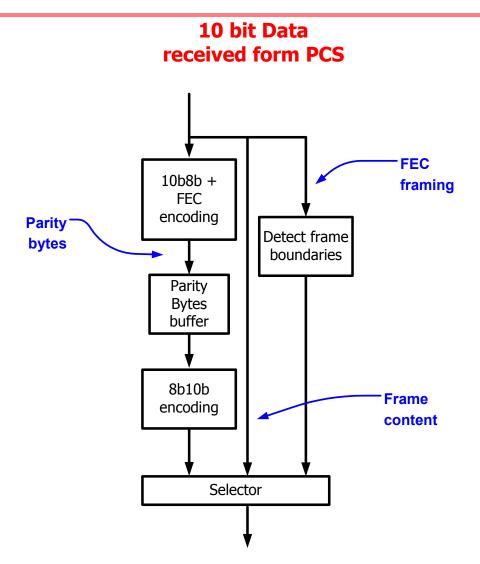
FEC Rate Adaptation

- Receiver (FEC to MAC): Replaces FEC coding with idles
- Transmitter (MAC to FEC): Idles inserted between frames adapting MAC rate.
 - IPG stretching similar to 802.3ae
 - Well known ratio between the frame size to size of additional parity

FEC Layering in Ethernet

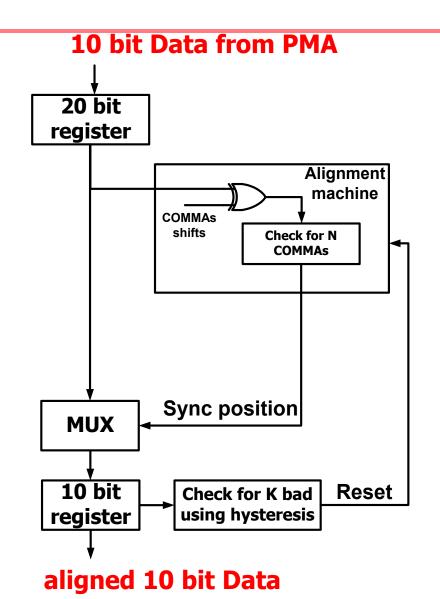


FEC Sub-layer - Tx



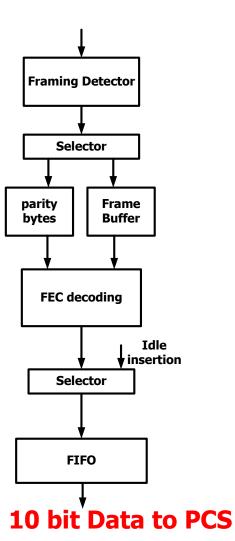
10 bit data to PMA

FEC Sub-layer – Rx Byte Alignment



FEC Sub-layer - Rx

aligned 10 bit Data



Byte alignment in F-FEC

- Byte alignment performed outside PMA
 - Comma detect is disabled in PMA for FEC
- FEC sublayer syncs on Idle phase
 - A few Idles maintain very low false lock probability $P_{false_lock} = P_e^n$
 - Idles are guaranteed at start of burst and during regular transmission
 - Byte alignment is fast
- Use of long hysteresis for sync loss

Probability for Lock Errors

- Probability for a Single error in Comma is 1e-3
- Acquisition is performed following detection of 7 commas
 - The probability for false acquisition is (1e-3)^7
- Probability for acquisition loss
 - Following 7 sequential bad words (with hysteresis) the probability is in the order of (1e-3)^7 – one in every 250,000 years



- FEC framing compatible with legacy Ethernet introduced in khermosh_1_0102.pdf
- Layering proposed below PCS maintaining <u>same</u> <u>1000Base-X PCS and PMA reusing TBI</u>
- PMA to operate with byte alignment disabled
- FEC layer performs byte alignment
- Framing makes use of idle period between frames to hold parity
- MAC stretches the IPG as in 802.3ae