Suggested text for section 45.4.1.XX

START OF TEXT

45.4.1.XX Line Attenuation register

The bit definitions for the line attenuation register are found in table 45-XX

Table 45-20 – Line attenuation register bit definition

Bit(s)	Name	Description	R/W
1.x.15:9	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x.8:0	DS carrier 1 line attenuation	A:=value of bits Attenuation : A/4 (in dB)	LT:RO NT: RO
1.x+1.15:9	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x+1.8:0	DS carrier 2 line attenuation	A:=value of bits Attenuation : A/4 (in dB)	LT:RO NT: RO
1.x+2.15:9	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x+2.8:0	US carrier 1 line attenuation	A:=value of bits Attenuation : A/4 (in dB)	LT:RO NT: RO
1.x+3.15:9	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x+3.8:0	US carrier 2 line attenuation	A:=value of bits Attenuation : A/4 (in dB)	LT:RO NT: RO

45.4.1.XX.1 DS carrier 1 line attenuation (1.x.8:0)
TBD
45.4.1.XX.2 DS carrier line attenuation (1.x+1.8:0)
TBD
45.4.1.XX.3 US carrier 1 line attenuation (1.x+2.8:0)
TBD
45.4.1.XX.4 US carrier 2 line attenuation (1.x+3.8:0)
TBD

END OF TEXT

Suggested text for section 45.4.1.11

START OF TEXT

45.4.1.11 TX PSD Level register

The bit definitions for the TX PSD Level register are found in table 45-34

Table 45-34 – TX PSD Level register bit definition

Bit(s)	Name	Description	R/W
1.x+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: RO
1.x+4k.8:0	DS carrier 1 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: RO
1.x+1+4k.15:9 1.x+1+4k.8:0	Reserved DS carrier 2 TX PSD level	Value always 0, writes ignored P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: RO LT:R/W NT: RO
1.x+2+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: RO
1.x+2+4k.8:0	US carrier 1 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: RO
1.x+3+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: RO
1.x+3+4k.8:0	US carrier 2 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: RO

45.4.1.11.1 DS carrier 1 line attenuation (1.x+4k.8:0)
TBD
45.4.1.11.2 DS carrier line attenuation (1.x+1+4k.8:0)
TBD
45.4.1.11.3 US carrier 1 line attenuation (1.x+2+4k.8:0)
TBD
45.4.1.11.4 US carrier 2 line attenuation (1.x+3+4k.8:0)
TBD

END OF TEXT

Suggested text for section 45.4.1.12

START OF TEXT

45.4.1.12 NT TX PSD Level register

The bit definitions for the NT TX PSD Level register are found in table 45-35. The register is defined only for LT port types

Table 45-35 – TX PSD Level register bit definition

Bit(s)	Name	Description	R/W
1.x+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+4k.8:0	NT DS carrier 1 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: undefined
1.x+1+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+1+4k.8:0	NT DS carrier 2 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: undefined
1.x+2+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+2+4k.8:0	NT US carrier 1 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: undefined
1.x+3+4k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+3+4k.8:0	NT US carrier 2 TX PSD level	P:=value of bits in two's complement (i.e. bit 8 is sign bit) PSD level=P/4-100 dbm/Hz	LT:R/W NT: undefined

45.4.1.12.1 NT DS carrier 1 line attenuation (1.x+4k.8:0)
TBD
45.4.1.12.2 NT DS carrier line attenuation (1.x+1+4k.8:0)
TBD
45.4.1.12.3 NT US carrier 1 line attenuation (1.x+2+4k.8:0)
TBD
45.4.1.12.4 NT US carrier 2 line attenuation (1.x+3+4k.8:0)
TBD

END OF TEXT

Suggested text for section 45.4.1.XX

START OF TEXT

45.4.1.XX Interleaver setting register

The bit definitions for the Interleaver setting register are found in table 45-XX.

Table 45-XX – Interleaver setting register bit definition

Bit(s)	Name	Description	R/W
1.x+2k.15:12	Reserved	Value always 0, writes ignored	LT:R/W NT: RO
1.x+2k.11:10	DS Interleaver block size	00 – DS Interleaver turned off 01 – DS Interleaver block size = 100 10 – DS Interleaver block size = 50 11 – DS Interleaver block size = 25	LT:R/W NT: RO
1.x+2k.15:9 1.x+2k.7:0	Reserved DS Interleaver depth	Value always 0, writes ignored M:=Value of bits M=0 – DS Interleaver turned off M>0 - DS Interleaver depth is M	LT:R/W NT: RO LT:R/W NT: RO
1.x+1+2k.15:12	Reserved	Value always 0, writes ignored	LT:R/W NT: RO
1.x+1+2k.11:10	US Interleaver block size	00 – DS Interleaver turned off 01 – DS Interleaver block size = 100 10 – DS Interleaver block size = 50 11 – DS Interleaver block size = 25	LT:R/W NT: RO
1.x+1+2k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: RO
1.x+1+2k.7:0	US Interleaver depth	M:=Value of bits M=0 – DS Interleaver turned off M>0 - DS Interleaver depth is M	LT:R/W NT: RO

45.4.1.XX.1 DS Interleaver block size (1.x+2k.11:10)
TBD
45.4.1.XX.2 DS Interleaver depth (1.x+2k.7:0)
TBD
45.4.1.XX.3 US Interleaver block size (1.x+1+2k.11:10)
TBD
45.4.1.XX.4 US Interleaver block size (1.x+1+2k.7:0)

TBD

END OF TEXT

Suggested text for section 45.4.1.XX

START OF TEXT

45.4.1.XX NT Interleaver setting register

The bit definitions for the NT Interleaver setting register are found in table 45-XX. The register is defined for LT port types only

Table 45-XX – NT Interleaver setting register bit definition

Bit(s)	Name	Description	R/W
1.x+2k.15:12	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+2k.11:10	NT DS Interleaver block size	00 – DS Interleaver turned off 01 – DS Interleaver block size = 100 10 – DS Interleaver block size = 50 11 – DS Interleaver block size = 25	LT:R/W NT: undefined
1.x+2k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+2k.7:0	NT DS Interleaver depth	M:=Value of bits M=0 – DS Interleaver turned off M>0 - DS Interleaver depth is M	LT:R/W NT: undefined
1.x+1+2k.15:12	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+1+2k.11:10	NT US Interleaver block size	00 – DS Interleaver turned off 01 – DS Interleaver block size = 100 10 – DS Interleaver block size = 50 11 – DS Interleaver block size = 25	LT:R/W NT: undefined
1.x+1+2k.15:9	Reserved	Value always 0, writes ignored	LT:R/W NT: undefined
1.x+1+2k.7:0	NT US Interleaver depth	M:=Value of bits M=0 – DS Interleaver turned off M>0 - DS Interleaver depth is M	LT:R/W NT: undefined

45.4.1.XX.1 NT DS Interleaver block size (1.x+2k.11:10)
TBD
45.4.1.XX.2 NT DS Interleaver depth (1.x+2k.7:0)
TBD
45.4.1.XX.3 NT US Interleaver block size (1.x+1+2k.11:10)
TBD
45.4.1.XX.4 NT US Interleaver block size (1.x+1+2k.7:0)

TBD

END OF TEXT

Suggested text for section 45.4.1.XX

START OF TEXT

45.4.1.XX IB register

The bit definitions for IB register are found in table 45-XX.

Table 45-XX – IB register bit definition

Bit(s)	Name	Description	R/W
1.x.15:15	*trig*	*r_trig* in LT port *o_trig* in NT port "0" – normal state "1" – active state	LT:RO NT: RO
1.x.14:14	*flag*	*r_flag* in LT port *o_flag* in NT port "0" – normal state "1" – active state	LT:RO NT: RO
1.x.13:13	IB-1(*fp_1*)	Far-end TPS_TC #1 defect/failure "0" – Normal state "1" – failure condition	LT:RO NT: RO
1.x.12:12	IB-2(*fp_2*)	Far-end TPS_TC #2 defect/failure "0" – Normal state "1" – failure condition	LT:RO NT: RO
1.x.11:11	IB-3(*fp_3*)	Far-end TPS_TC #3 defect/failure "0" – Normal state "1" – failure condition	LT:RO NT: RO
1.x.10:10	IB-4(*fp_4*)	Far-end TPS_TC #4 defect/failure "0" – Normal state "1" – failure condition	LT:RO NT: RO
1.x.9:9	IB-5(*Reserved*)	Reserved for future use "0" – Normal state "1" – TBD condition	LT:RO NT: RO
1.x.8:8	NTR	NTR marker "0" – NTR marker not transmitted "1" – NTR marker transmitted	LT:RO NT: RO
1.x.7:7	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x.6:6	IB-6(*Reserved*)	Reserved for future use "0" – Normal state "1" – TBD condition	LT:RO NT: RO
1.x.5:5	IB-7(*flos_cr1*)	Far-end Loss of carrier 1 "0" – Normal state "1" – loss state	LT:RO NT: RO
1.x.5:5	IB-8(*flos_cr2*)	Far-end Loss of carrier 2 "0" – Normal state "1" – loss state	LT:RO NT: RO

1.x.4:4	IB-9(*rdi*)	Far-end Severely errored frame detected "0" – Normal state "1" – Failure state	LT:RO NT: RO
1.x.3:3	IB-10(*Reserved*)	Reserved for future use "0" – Normal state "1" – TBD condition	LT:RO NT: RO
1.x.2:2	IB-11(*Reserved*)	Reserved for future use "0" – Normal state "1" – TBD condition	LT:RO NT: RO
1.x.1:1	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x+1.15:15	Reserved	Value always 0, writes ignored	LT:RO NT: RO
1.x+1.14:14	IB-12(*FPO*)	Far End power-off failure "0" – Normal state "1" – power failure condition	LT:RO NT: RO
1.x+1.13:13	IB-12(*flpr*)	Far End Loss-Of-Power defect "0" – Normal state "1" – power failure condition	LT:RO NT: RO
1.x+1.12:9	Proprietary	For Proprietry application "0" – Normal state "1" – TBD condition	LT:RO NT: RO
1.x+1.8:0	Reserved	Value always 0, writes ignored	LT:RO NT: RO

END OF TEXT

Suggested text for section 45.4.1.XX

START OF TEXT

45.4.1.XX Electrical length register

The bit definitions for the Electrical length register are found in table 45-XX.

Table 45-XX – Electrical length register bit definition

Bit(s)	Name	Description	R/W
1.x.15:0	Electrical length	Electrical length (in feet)	LT:RO NT: RO

45.4.1.XX.1 Electrical length (1.x.15:0)
TBD

45.4.1.XX NT Electrical length register

The bit definitions for the NT Electrical length register are found in table 45-XX. The register is defined only for LT port types

Table 45-XX – NT Electrical Length bit definition

Bit(s)	Name	Description	R/W
1.x.15:0	Electrical length	Electrical length (in feet)	LT:RO NT: undefined

45.4.1.XX.1 NT Electrical length (1.x.15:0)
TBD

END OF TEXT