61.0.0.0.1 Scrambler

The scrambler used is identical to the definition in Clause 49. The payload of the block is scrambled with a self-synchronizing scrambler. The scrambler shall produce the same result as the implementation shown in Figure 61–1

serial data input

scrambled data output

Figure 61–1—Scrambler

. This implements the scrambler polynomial[1]:

$$G(x) = 1 + x^{39} + x^{58} \tag{1}$$

There is no requirement on the initial value for the scrambler. The scrambler is run continuously on all payload bits. The sync header bits bypass the scrambler.

61.0.0.0.2 Descrambler

The descrambler processes the payload to reverse the effect of the scrambler using the same polynomial. It

shall produce the same result as the implementation shown in Figure 61–2

scrambled data input

serial data output

Figure 61–2—Descrambler

---

[1]The convention here, which considers the most recent bit into the scrambler to be the lowest order term, is consistent with most references and with other scramblers shown in this standard. Some references consider the most recent bit into the scrambler to be the highest order term and would therefore identify this as the inverse of the polynomial in equation (1). In case of doubt, note that the conformance requirement is based on the representation of the scrambler in the figure rather than the polynomial equation.