MDIO for IEEE 802.3ah

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What is MDIO for ?

‘.. A simple, two wire, serial interface to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY.’

(Clause 22.2.4)

MDIO signals

- MDC – Management Data Clock
  - Sourced from the STA (Station Management Entity)
- MDIO – Management Data Input / Output
  - Bi-directional multi-drop bus

Clause 22 MDIO

- Used for control and status of 10 Mbps, 100 Mbps, and 1000 Mbps PHYs
- Up to 32 PHYs per MDIO
- Up to 32 registers per PHY (16 bits each)
- Two types of MDIO frame (read and write)
- 2.5MHz MDC clock speed
- Electrical interface specifies 5V tolerant I/O

Issues with Clause 22 MDIO

- Only two 16-bit registers left unused
  - 802.3af acquired two registers
- 5V tolerant I/O requirement
- Does not cater for PHYs made up of multiple devices

Clause 45 MDIO

- Defined by 802.3ae
- Used by 10 Gbps PHYs
- New indirect addressing scheme
- New low voltage electrical interface

Clause 45 – Indirect Addressing

- Four new MDIO frame types defined
  - Address, read, write, post read increment address
- Two frames required to access a register
  - ‘Address’ frame followed by an ‘operation’ frame
- 32 PHYs per MDIO
- 32 MMDs (MDIO Manageable Devices) per PHY
  - 5 reserved by 802.3ae
- 65 536 registers per MMD (16 bits each)

Clause 45 – Electrical Interface

- 1.2V electrical interface
- Possible to use the new electrical interface with the Clause 22 frame format

Clause 45 MDIO further info

Previous EFM presentation :

http://www.ieee802.org/3/efm/public/sep01/turner_1_0901.pdf

802.3ae presentation :

http://www.ieee802.org/3/ae/public/jul00/law_1_0700.pdf

Summary

- Clause 22 used for control and status of 10 / 100 / 1000 Mbps PHYs
  - Only two registers spare
- Clause 45 used for 10 Gbps PHYs
  - Many registers spare for future speeds and features