101.3.2.2 64B/66B Encode

The 64B/66B encoder shall perform the functions specified in {Figure 49–16}. The 64B/66B encoding process is as described in {49.2.4}, with the following exceptions:

a) the 64B/66B encode process in EPoC PCS operates on 72-bit vectors obtained from the output of the Idle control character deletion process (see 101.3.2.1), rather than directly from the XGMII; and

b) the 64B/66B encode process in EPoC PCS operates on bursty data stream produced by the Idle control character deletion process, unlike in 10GBASE-R PCS, where data stream to the input of the 64B/66B encoder is taken directly from the XGMII and hence continuous.

101.3.3.6 64B/66B Decode

The 64B/66B decoder shall perform the functions specified in {Figure 49–17}. The 64B/66B decoding process is as described in {49.2.11}, with the following exceptions:

a) the 64B/66B decode process in EPoC PCS produces 72-bit vectors fed into the Idle control character insertion process (see 101.3.3.7), rather than directly into the XGMII; and

b) the 64B/66B decode process in EPoC PCS operates on bursty data stream produced by the FEC decoder, unlike in 10GBASE-R PCS, where data stream to the input of the 64B/66B decoder is taken directly from the descrambler and hence continuous.