Delay Characterization

Response to "TDD and FDD A Path Forward" and more…

July 19, 2012

QUALCOMM®

Qualcomm
ATHEROS

Abstract

- This presentation gives a detailed analysis of the latency/jitter and capacity for FDD and TDD access schemes

- In particular, the scenario illustrated in "TDD Path Forward" IEEE contribution is considered for the FDD vs. TDD comparison

QUALCOMM®

qualcomm
ATHEROS

Background

Scenario (from TDD path forward slides – Ed Mallette)

- 40 CNUs in the network connected to a CLT operating at the data rate of up 1 to Gb/s symmetric - no ONU, no OCU, no OLT

- Each CNU runs a CBR 25 Mbps service and queues on each CNU are always loaded at the rate 25 Mbps

- 300 MHz of contiguous spectrum available for EPoC at 1 - 1.3 GHz

- Passive plant (N+0), 1000 feet maximum reach (max distance to CNU)

QUALCOMM®

Qualcomm ATHEROS

Assumptions

- 10% duplex separation in FDD, leading to ~ 100 MHz of guard band

- 15 us switching time for TDD, leading to ~ 33 us guard time for TDD (max cable length of 1000 feet corresponds to max RTT of ~2.5 us)

  - Assumes that possible reflections of significant amplitude will be fully received within the switching time - corresponds to 6 times the max RTT

- 120 MHz spectrum for 1Gb/s (spectral efficiency of 8.33 bit/s/Hz)

- Equal capacity in DS and US (from traffic model input)

- OFDM transmission with 7.5 KHz carrier spacing and 1.5 us CP, leading to a total duration of ~ 135 us per each OFDM symbol

- Processing time at RX = 1.5 times the symbol duration

- FDD mode or TDD mode are fully embedded in the PHY and upper layers are not aware of the mode used for transmission

- Round robin scheduling and DBA (all CNUs treated the same)

  - Each CNU is given equal resources in DS/US at each polling cycle

QUALCOMM®

qualcomm
ATHEROS

Delay and jitter components

- The delay and jitter are determined by the processing at the PHY and by the resource allocation done by scheduler/DBA (MPCP/MAC delay)

    - min(delay) = min(PHY_delay) + min(MAC_delay)

    - max(delay) = max(PHY_delay) + max(MAC_delay)

    - Jitter = max(delay) – min(delay)

- The PHY components consider the delay due to processing at the transmitter and receiver side, as well as the propagation delay

- The MPCP/MAC components considers instead the additional delay due to the resource allocation and depends primarily on the polling cycle

    - In **DS**, each CNU is served in round robin fashion at each polling cycle and as packets arrive at application randomly, a variable delay from 0 to ~1 polling cycle duration needs to be considered at MPCP/MAC level

    - In **US**, each CNU is allowed to transmit (in a round robin fashion) at each polling cycle after having reported the queue status back to the CLT, so one additional polling cycle needs to be accounted for reporting

    - The MPCP/MAC component is the same for FDD and TDD – the MPCP/MAC is actually not aware of the underlying FDD or TDD PHY operations

QUALCOMM

Qualcomm
ATHEROS

FDD vs. TDD - delay and jitter characterization
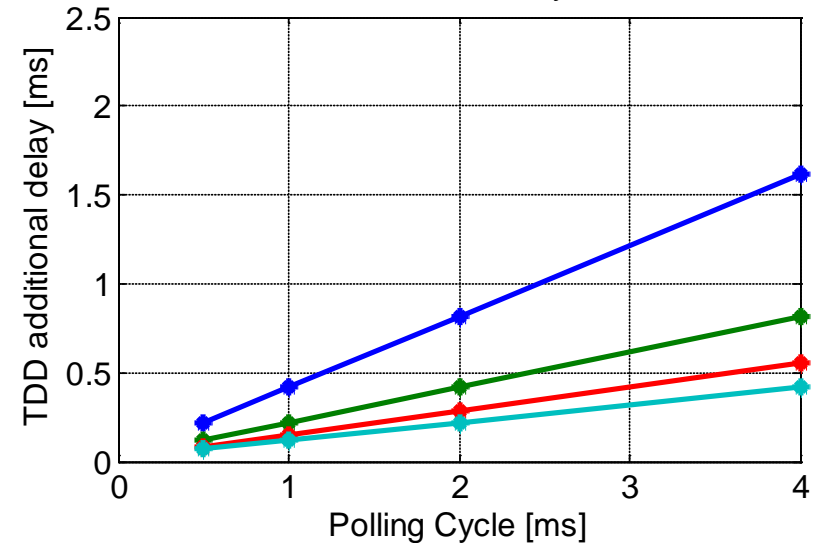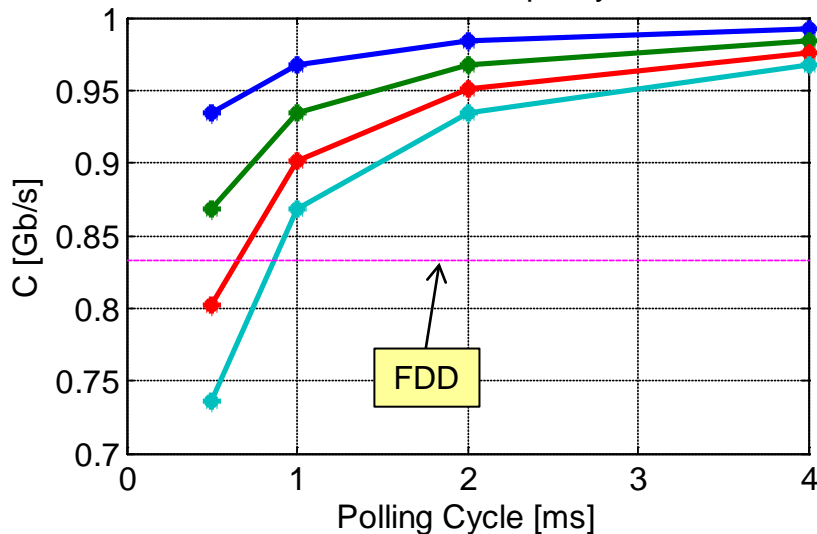
QUALCOMM

Qualcomm ATHEROS
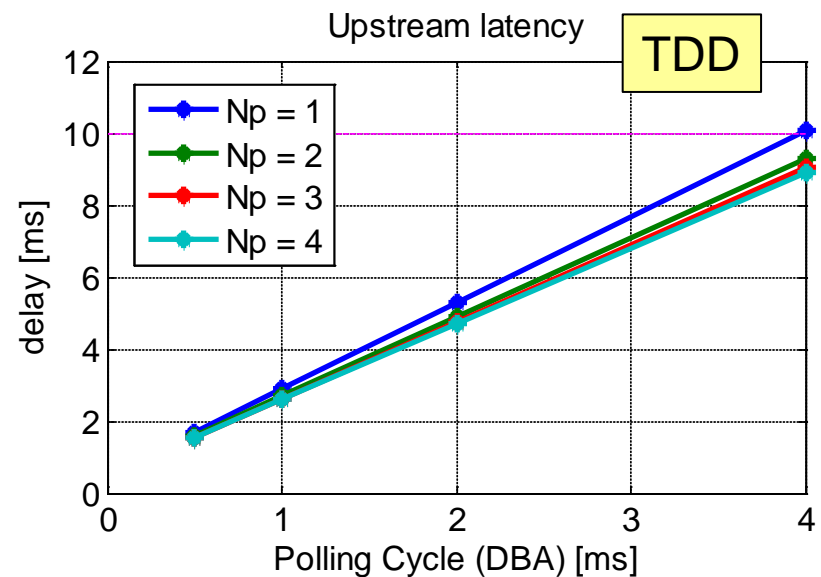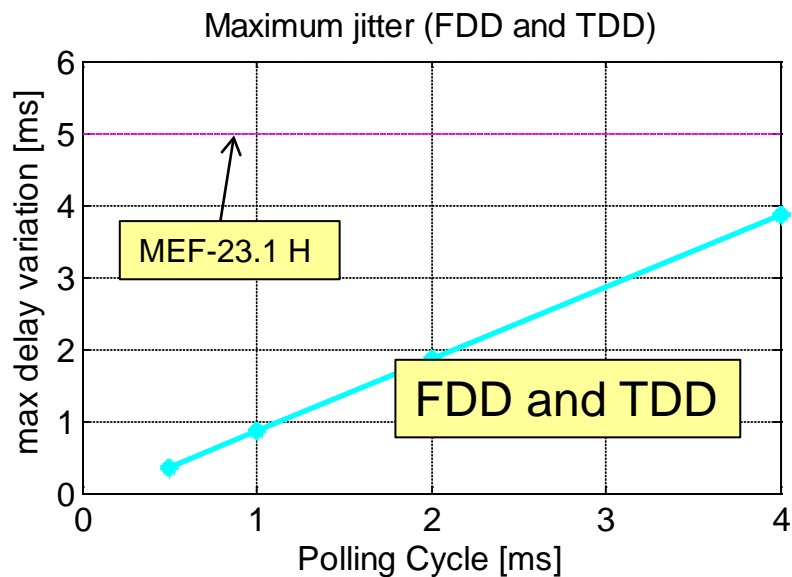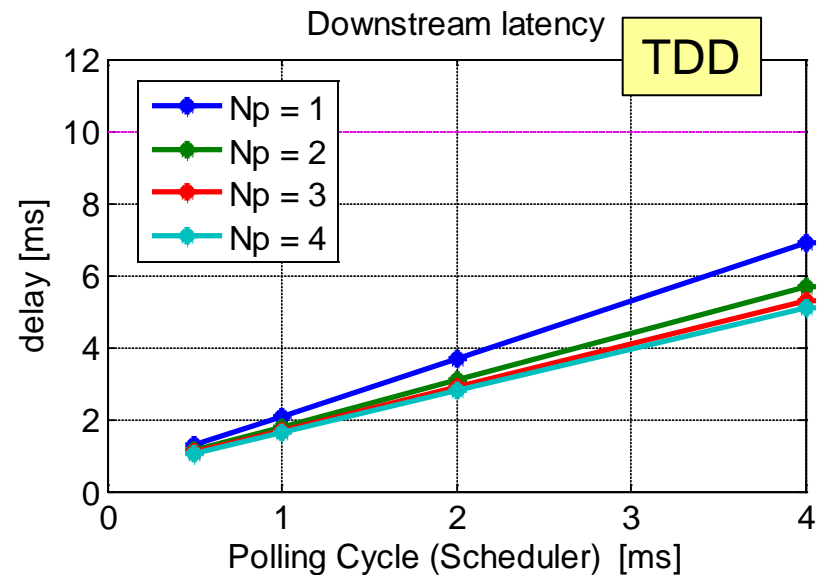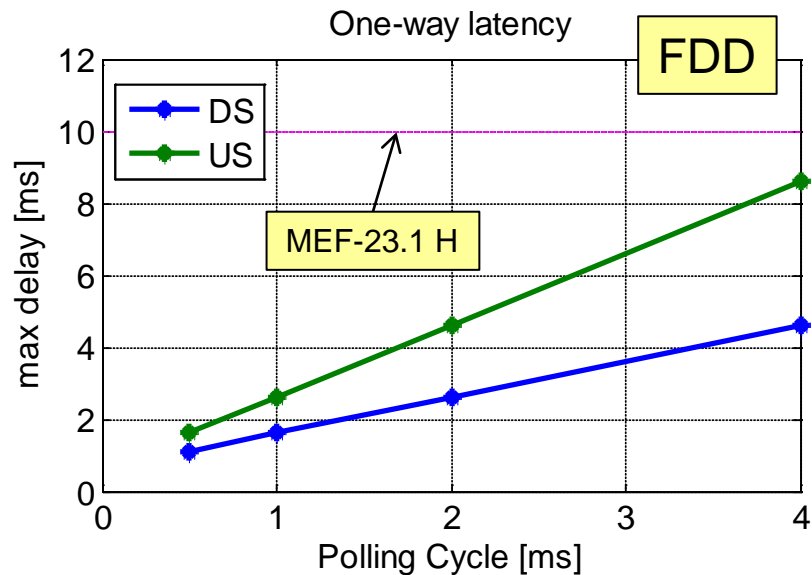
TDD vs. FDD – Differences and Commonalities

DS incremental latency in TDD
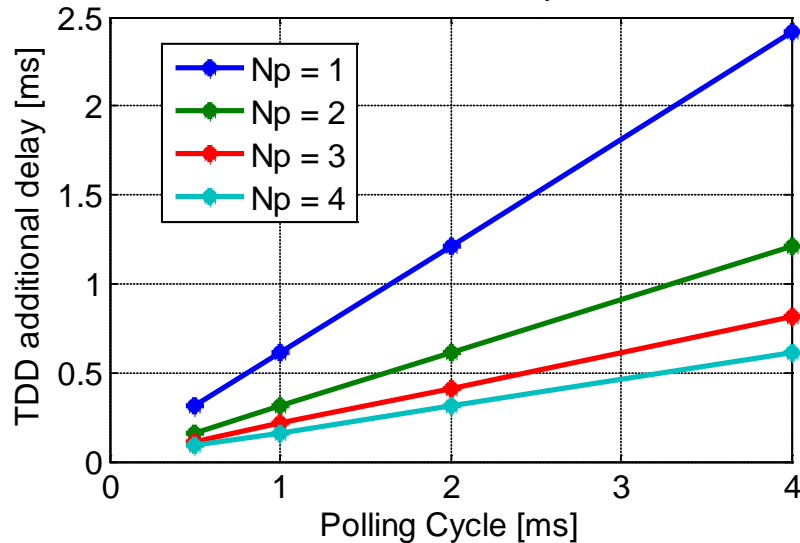
US incremental latency in TDD

DS and US capacity

Maximum Jitter (same for FDD and TDD)

QUALCOMM

qualcomm
ATHEROS
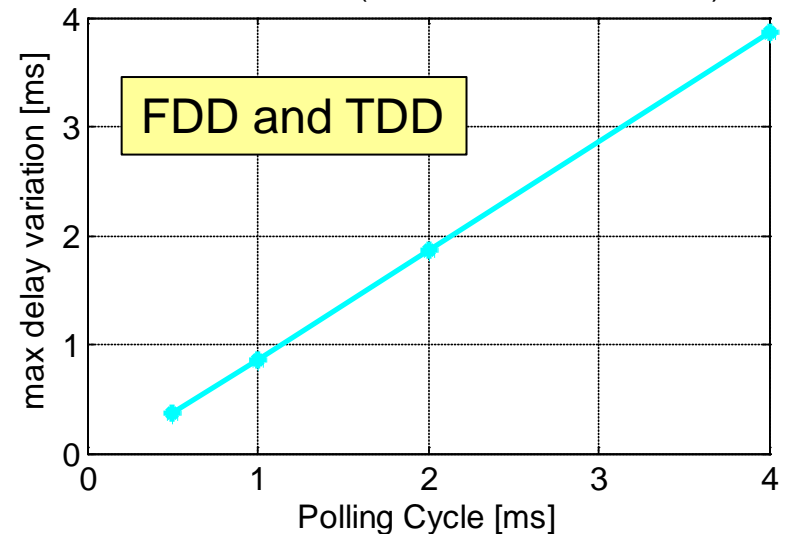
Summary and Conclusions

- For the scenario under consideration: TDD solution outperforms FDD in terms of capacity due to a higher efficiency ratio:
  - ~ 23.5 Mb/s for each CNU in TDD (for a total of 940 Mb/s in each direction)
  - ~ 20.8 Mb/s for each CNU in FDD (for a total of ~ 833 Mb/s)

- Compared to FDD, there is an increment in latency with TDD mode
  - The increment is limited and can be controlled via configuration
    - It depends on the TDD cycle duration and selected guard time
  - For example, selecting a polling cycle of 1 ms and having two TDD partitions per cycle (i.e. a TDD cycle of 0.5 ms), the incremental absolute latency in DS or US is contained within 0.3 ms

- The same jitter could be observed for TDD and FDD
  - No PHY contribution to the jitter, only MAC/MPCP contributes
  - The jitter is determined by the scheduler and polling cycle

QUALCOMM®

qualcomm
ATHEROS

Delay Model improvements - spreadsheet

- Focus on delay but also consider efficiency

  - For both delay and efficiency, two components: PHY and MAC

  - Look at worst and typical cases in rational scenarios

  - Efficiency: need to know how much efficiency is consumed by overhead due e.g. guard interval, guard bands, etc. – focus on relative figures and efficiency on the coax side – how the trade-off affects delay vs. efficiency

- Improve the model with further details

  - Consider symbol duration

  - Consider preamble presence/duration

  - Split propagation time (cable length) from switching time

    - Transmit/receive sharing PHY and influence on the switching time

  - Number of simultaneous transmitters

- Important question is: does the absolute numbers meet the delay/jitter requirements?

Scenario: one single user (single LLID) in the system, running at full speed
→ evaluate the maximal speed that can be sustained for the user

*Data rate (in bps) = Gate Rate (in #gates/sec) * Gate Size (in bits/gate)*   *where*

*Gate Size (in bits/gate) = Gate Quanta (in TQ/gate) * tqSize (in bits/TQ)*   →

*Data Rate (bps) = Gate Rate (#gate/s) * Gate Quanta (TQ/gate) * tqSize (bits/TQ)*

→   *max(DataRate) = max(GateRate) * max(GataQuanta) * tqSize*

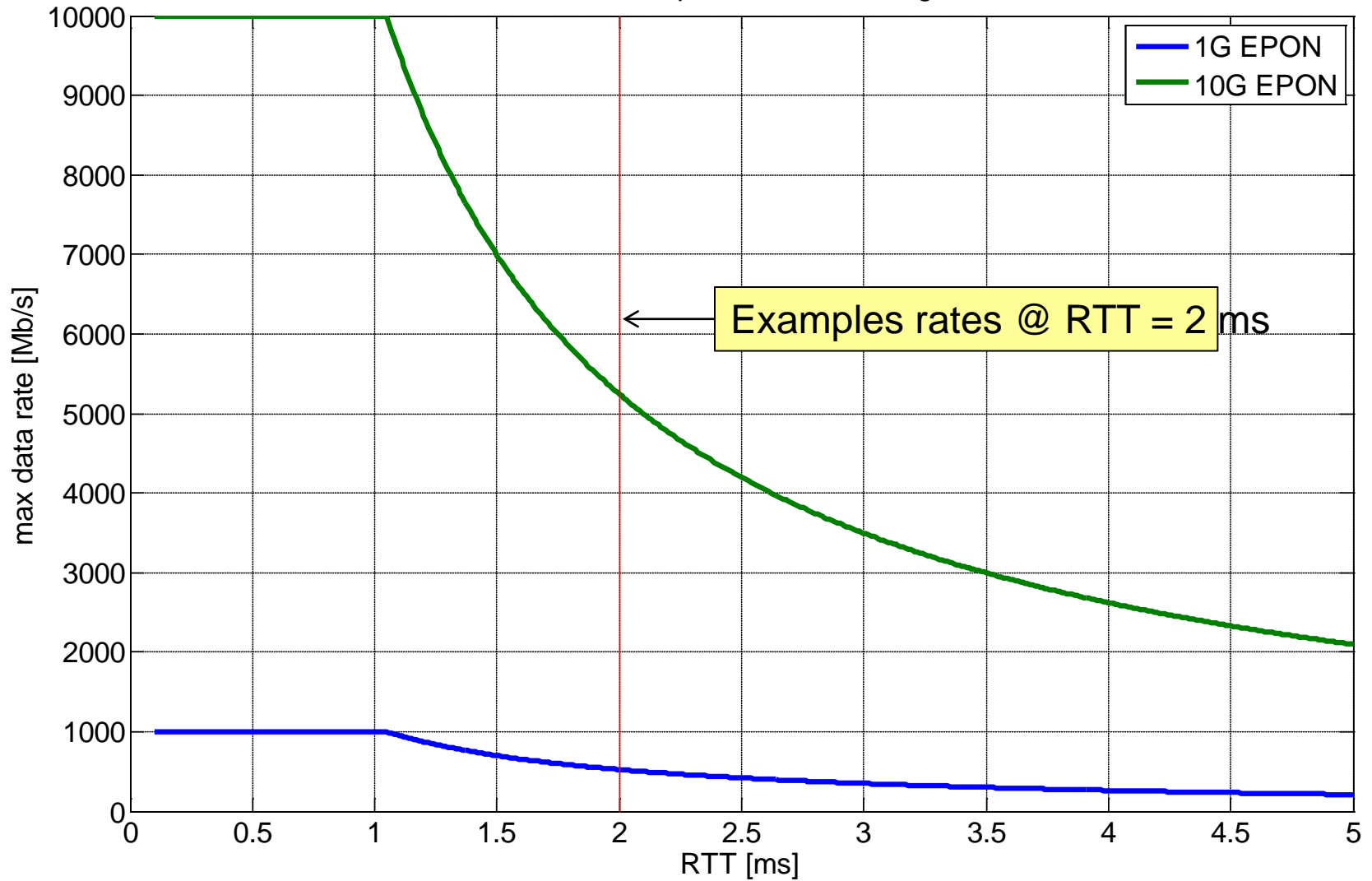$$1/min(RTT)$$ $$max(ReportQuanta) = 2^{16}$$

*e.g.   if the RTT = 2 ms -> max(DataRate) = 500 * 65536 * tqSize*

Clause 64/77 (2 or 20 bytes)

for 1G EPON, this leads to   **max(DataRate)$_{1G}$ = 524.3 Mb/s**

for 10G EPON, this leads to   **max(DataRate)$_{10G}$ = 5.24 Gb/s**

QUALCOMM   qualcomm ATHEROS

Max sustainable peak data rate - single user

Examples rates @ RTT = 2 ms

Backup: Details on Delay Computations

Confidential and Proprietary

FDD Analysis – PHY contribution

- Considering the FDD guard band of 100 MHz, only 200 MHz are used
  - Means 833 Mb/s for DS and US links when splitting it for equal capacity
  - Each CNU can TX/RX at ~20.8 Mb/s in each direction

- The overall delay includes for each OFDM symbol the data collection, the encoding/construction of the symbol, the transmission and propagation time, and the time to process it at the receiver side
  - Packets are collected during the duration of one symbol and then processed for transmission – includes ~ 1 Ts for processing and 1 Ts for transmission
  - Packets are received and processed at the receiver side (Trx ~1.5 * Ts) and then delivered to the MAC – this involves parallel-to-serial conversion, which removes the jitter at PHY level:
    - Max PHY delay is max(PHY_delay) = 3*Ts + Trx + Tprop ~ 0.610 ms
    - Min PHY delay is min(PHY_delay) = max(PHY_delay) ~ 0.610 ms
  - The PHY delay contributions are the same for DS and US transmissions

QUALCOMM®

qualcomm ATHEROS

TDD Analysis – PHY Contribution

- Considering the guard band of 100 MHz, only 200 MHz are used in US

  - Means peak data rates of 2.5 Gb/s in DS and of 1.67 Gb/s in US

  - Equal capacity split is realized by assigning 40% of the available transmit time to DS and 60% to US in each resource partitioning cycle ($\alpha = 0.4$)

  - A guard time between US and DS transmission is needed in TDD, at each DS -> US transition, equal to $Tg = 2*Tswitch + max(RTT) \sim 33$ us

- Different configurations are possible, depending on the DBA cycle and on the number of partitions made within one single cycle. Next slides shows analysis and plots for the following cases:

  - Polling cycle duration $Tdba = [0.5, 1, 2, 4]$ ms

  - Number of DS/US partitions in one cycle $Np = [1, 2, 3, 4]$

  - Equal split of resources: 40% DS and 60% US time assignments

  - TDD mode add latency as compared to FDD mode in the amount of $Tg + T/Np$, where T is either Tds (for US) or Tus (for DS), which account for PHY buffering and delivery of data for the complementary period

    - 1 Ts is discounted as already considering in the FDD part (see next slides)

QUALCOMM Qualcomm ATHEROS

TDD Analysis – PHY contribution (cont.)

- Total transmit time in a DBA cycle $Ttx = Tdba - Np*Tguard$
- DS transmit time $Tds = \alpha * Ttx$
- US transmit time $Tus = (1-\alpha) * Ttx$

- DS capacity $Cds = 2.5 * Tds/Tdba$
- US capacity $Cus = 1.67 * Tus/Tdba$

- Maximum DS latency $Dtdd = Dfdd + Tg + Tus/Np$
- Maximum US latency $Dtdd = Dfdd + Tg + Tds/Np$

- As for FDD, there is no jitter added by PHY layer and the delay for transferring the packet is the same for each packet

QUALCOMM

qualcomm
ATHEROS

MPCP/MAC contribution – FDD and TDD

- Different configurations are possible, depending on the polling cycle:
  - Polling cycle duration Tsched= Tdba = [0.5, 1, 2, 4] ms

- For DS, the following contributions are considered:
  - $min(MAC\_delay\_DS) = 0$
  - $max(MAC\_delay\_DS) = Tsched - Ts^{(*)}$
  - $Jitter\_DS = max(MAC\_delay\_DS) - min(MAC\_delay\_DS) = Tsched - Ts$

- For US, the following contributions are considered:
  - $min(MAC\_delay\_US) = Tdba$
  - $max(MAC\_delay\_US) = 2*Tdba - Ts$
  - $Jitter\_US = max(MAC\_delay\_US) - min(MAC\_delay\_US) = Tdba - Ts$

  - In case of persistent scheduling (fixed bandwidth allocation), 1 Tdba needs to be removed from the US delays above making the US and DS delays the same

(*) There is one symbol to discount as packets arriving just after the time queuing is terminated for the current symbol, will be first at the next scheduling cycle and get transmitted immediately at t2 = t1 + Tsched-Ts

QUALCOMM®

Qualcomm
ATHEROS