More on the Feasibility of a100GE MAC

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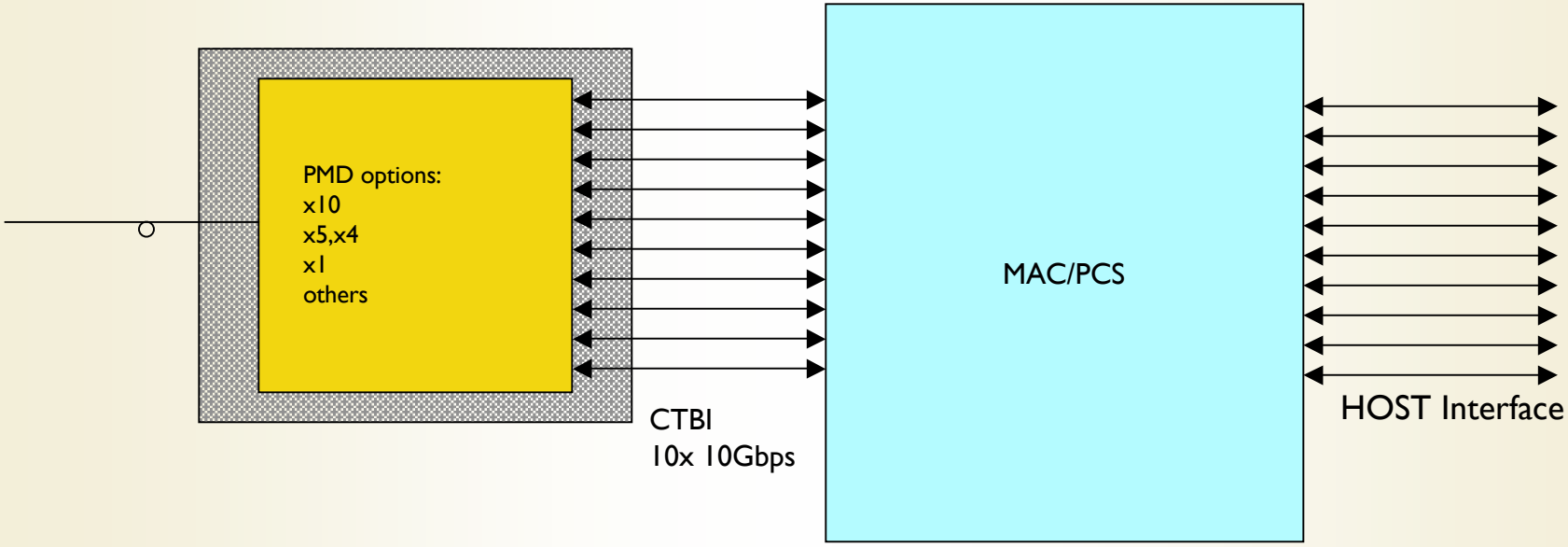
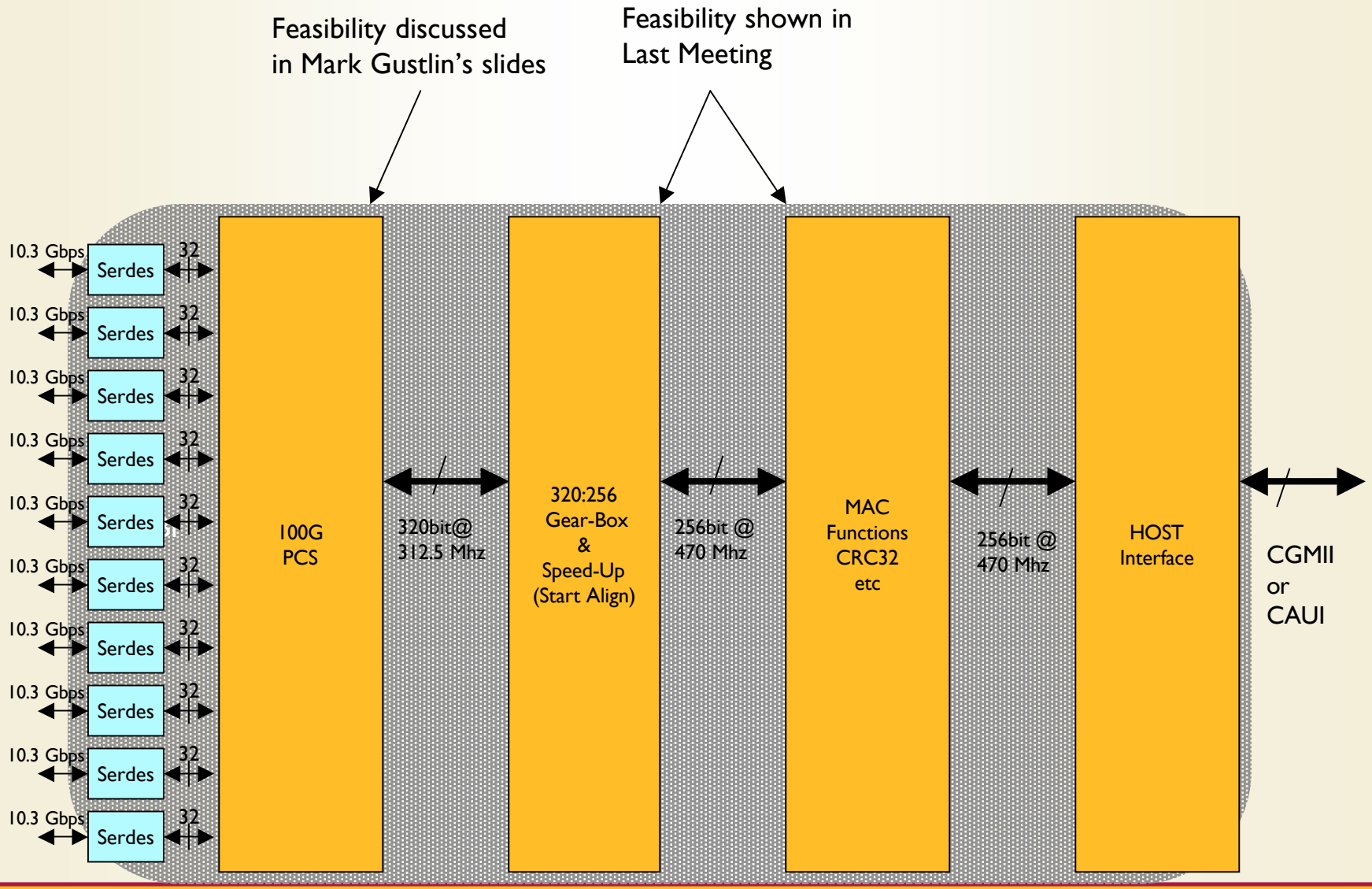
100G MAC


PMD options:
x10
x5,x4
x1
others
CTBI
10x 10Gbps
MAC/PCS
HOST Interface

100G MAC Feasibility

- Deal with Feasibility of:
  - CTBI Interface ?
  - PCS ?
  - Digital Core ✔
    - Gear-box ✔
    - Internal Bus ✔
    - CRC32 ✔
  - Host Interface (CGMII or CAUI) ?
  - The complete solution ?

Example of a PCS & MAC



Recap of Major Digital Blocks (90nm CMOS)

Blocks		Size (in Kgate)	Notes
CRC32 Checker and Generator	320 @ 425 Mhz	400	Post Place & Route result
	256 @ 470 Mhz	400	
Gear-Box	(320:256)@ 390 Mhz	10	Rough estimate using Synthesis only with no optimization (No P&R)
Striping across 10 Lanes	Columns (32 bits)	2	
	Words (64 bits)	10	
De-scrambler (self-sync 10GE)	32 bits x (10 instances)	50	
	320 bits		
Scrambler	32bits x (10 instances)	10	
	320bit @425 Mhz	35	
Full PCS64/66 (10 instances)	32bits @ 321.8 Mhz (10 instances)	440	Post Place & Route result 10GE PCS with 32:33 Gearbox

Sizes are used for reference, actual implementation might vary (based on tools, process, additional features such as diagnostic, etc)

CGMII or CAUI interface options

- To implement 100Gbps interface, the following options can be used:
  - 10x 10 Gbps (as in CTBI)
  - 16x 6.25 Gbps
  - 20x 5.00 Gbps
  - 32x 3.12 Gbps
  - 64x 1.56 Gbps
  - 80x 1.25 Gbps

Data for Comparison

- Using Existing silicon (.13u CMOS):
  - SPI4.2 (LVDS from 600 to 1200 Mbps)
  - XAUI and double XAUI (3.125 to 6.25 Gbps)
  - XFI (10.3 Gbps)
- Different criteria impact power and area:
  - Reach (long or short)
  - Type of channels to be supported
  - Jitter specs to be met
  - Other design and technology considerations

Example of Relative Area & Power

For 100Gbps Interface	LVDS 1.25Gbps	CML 3.125Gbps	CML 5Gbps	CML 6.25Gbps	CML 10Gbps
Power	2x	1.8x	1.25x	1x	2.6x
Traces	5x	2x	1.25x	1x	0.6x
Area (Active + Bumps)	.9x	1.8x	1.25x	1x	2.2x

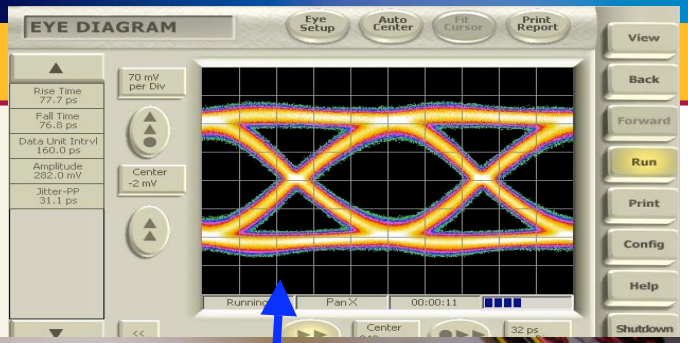
Based on existing silicon (.13u CMOS)

Possible Interfaces

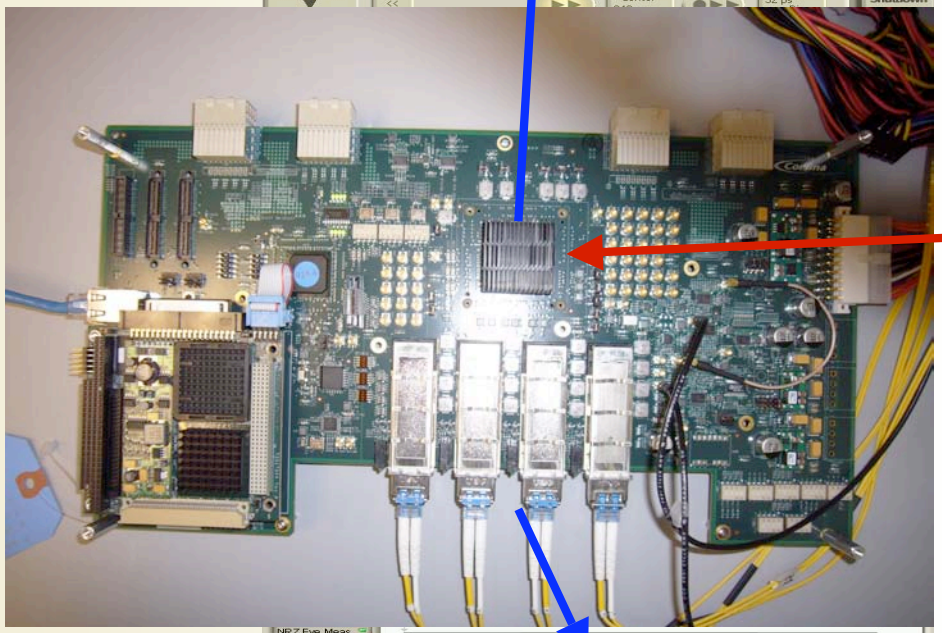
- CAUI using CML
  - 16x 6.25G using 64/66 coding (6.44 Gbps)
  - 20x 5G using 8B10B coding (6.25 Gbps)
- CGMII using LVDS
  - 80x 1.25G + 10 bit control
  - 64 data bit + 1 control @ 1.5625Gbps

Putting It All Together

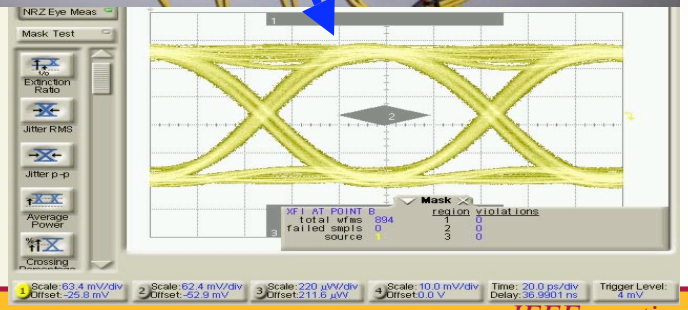
- Are there existing designs with
  - Line interface of 10x 10Gbps or Equiv.
  - Host interface of 16x 6.25Gbps or Equiv.
  - Large Digital core
    ??
- Current Technology (.13 u):
  - 4x 10Gbps
  - 16x 6.25Gbps
  - Large digital core



Interlaken Interface Eye Diagram
6.25Gbps over 12” FR4 and
HMZD connector



MAC ASIC (.13 u CMOS)
Quad XFI (4x 10Gbps) and
Dual Interlaken (16 x 6.25 Gbps)



XFI Interface Eye Diagram
10.3125Gbps measured electrically
with Intel XFP compliance board

Conclusion

- A 100G MAC is feasible and of a reasonable complexity
- Multiple implementation of 100G digital core are feasible in standard CMOS
- A "lower" rate interface CGMII or CAUI is possible
- When considering technical feasibility, an existing implementation in .13u provides the required 100GE host interface, and approximately half the line rate.