Technical Feasibility of SMF & MMF 100GE Transceivers

IEEE 802.3 Higher Speed Study Group

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Chris Cole

chris.cole@finisar.com

Finisar

Outline

- Applicable HSSG Fiber Optic Ad Hoc SMF study alternatives
- 100GE System Architecture
- SMF 100GE Transceiver Architecture
- SMF Transceiver Technical Feasibility Status
- SMF Transceiver Optical Link
- SMF Transceiver Thermal and Mechanical Concept
- SMF 100GE Transceiver Technical Feasibility Discussion
- SMF Transceiver Economic Feasibility (copy from prior presentation)
- MMF 100GE Transceiver Architecture
- MMF Transceiver Mechanical Concepts
- MMF 100GE Transceiver Technical Feasibility Discussion.

Reach (Technical) Feasibility of 100GE Alternatives

SMF	10km 1310nm	40km 1310nm	10km 1550nm	40km 1550nm
10x10G DML	yes (10λ span needs semi-cooling)	yes (need new DML & RX APD/SOA)	yes (need new DML)	maybe (need new DML)
10x10G EML	yes	yes (need RX APD/ SOA)	yes	yes
5x20G / 4x25G DML	yes (need new DML)	maybe (need new DML & RX SOA)	maybe (need new DML)	no
5x20G / 4x25G EML	yes (need new EML)	yes (need new EML & RX SOA)	yes	yes (need RX DC)
2x50G DQPSK DML	no	no	no	no
2x50G DQPSK EML	yes (need I/Q ML)	yes (need I/Q ML, RX DC & SOA)	yes (need I/Q ML & RX DC)	yes (need I/Q ML & RX DC)

Green shading designates alternatives under detailed study by Fiber Optic Ad Hoc contributors.
Red ovals designate alternatives which are subjects of this presentation.

Cost (1/Economic Feasibility) of 100GE Alternatives

SMF	10km 1310nm	40km 1310nm	10km 1550nm	40km 1550nm
10x10G DML	low	mid	low	mid
10x10G EML	mid	mid	mid	mid
5x20G / 4x25G DML	low	mid	low	not feasible
5x20G / 4x25G EML	mid	mid	mid	not economically feasible (RX DC)
2x50G DQPSK DML	not feasible	not feasible	not feasible	not feasible
2x50G DQPSK EML	high	not economically feasible (RX DC)	not economically feasible (RX DC)	not economically feasible (RX DC)

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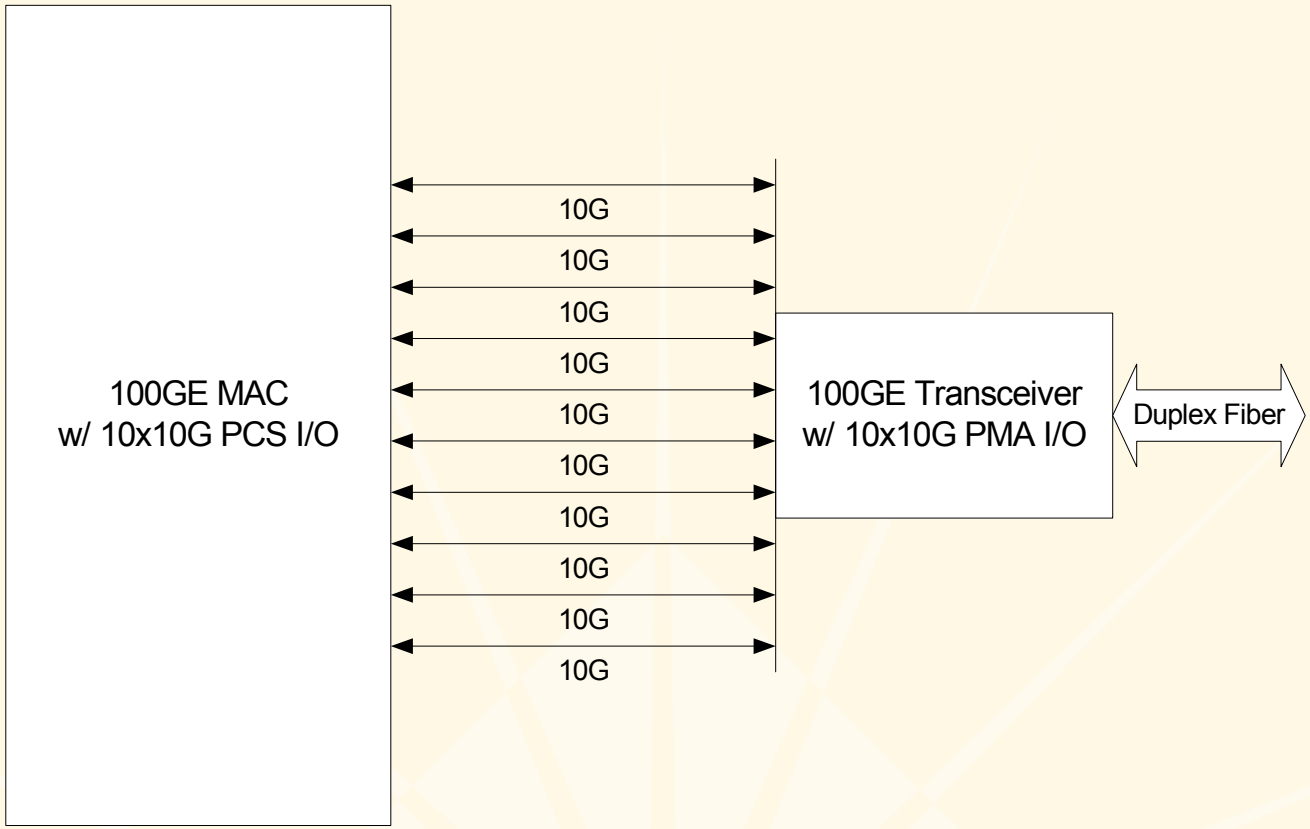
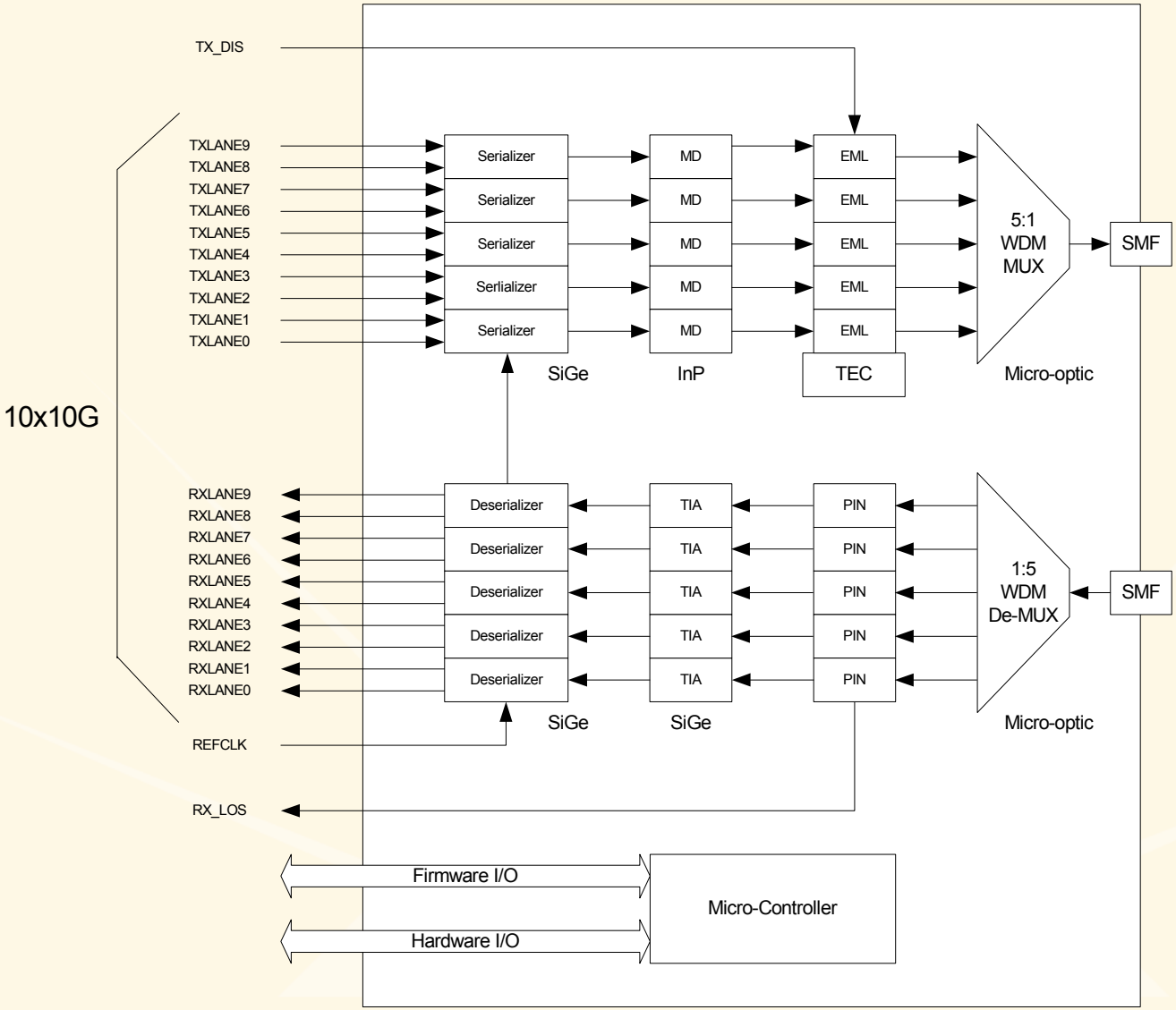
100GE System Architecture



PCS performs skew alignment and lane re-ordering.

10km 5x20G EML Transceiver Architecture



10km 5x20G EML Transceiver Technical Feasibility

Item	Status	Comments
Optical Link Budget	open	Similarity to 10GE-ER 40km link shown. To be completed in this presentation.
Quint SiGe SerDes	√	40G SiGe SerDes commercially available, 20G operation shown.
Quint InP Mod Driver	√	40G InP MDs commercially available, 20G operation shown.
Quint EML TOSA w/ WDM Mux	√	40G 1550nm EMLs commercially available, 20G operation shown. 1310nm also feasible. Mux micro-optics commercially available.
Quint PIN/TIA ROSA w/ WDM DeMux	√	40G 1310nm/1550nm PIN/TIAs commercially available, 20G operation shown. DeMux micro-optics commercially available.
Connector / I/O Signal Integrity	√	Enhanced PT20 SMT Connector available. 10G signal integrity shown.
Mechanical / Thermal	open	To be completed in this presentation.

Laser Eye Safety SMF Maximum per λ Power Limits

- 1550nm
  - AEL Class1 eye safety limit: 10dBm
  - SMF coupling ratio + M.U.: 2dB
  - 1 λ max power limit: 8dBm
  - 4 λ max power limit: 2dBm
  - 5 λ max power limit: 1dBm
  - 10 λ max power limit: -2dBm
- 1310nm
  - AEL Class1 eye safety limit: 12dBm
  - SMF coupling ratio + M.U.: 2dB
  - 1 λ max power limit: 10dBm
  - 4 λ max power limit: 4dBm
  - 5 λ max power limit: 3dBm
  - 10 λ max power limit: 0dBm
- SMF coupling ratio is dependant on the specific TOSA launch design.

10km 5x20G EML Transceiver per λ Optical Link

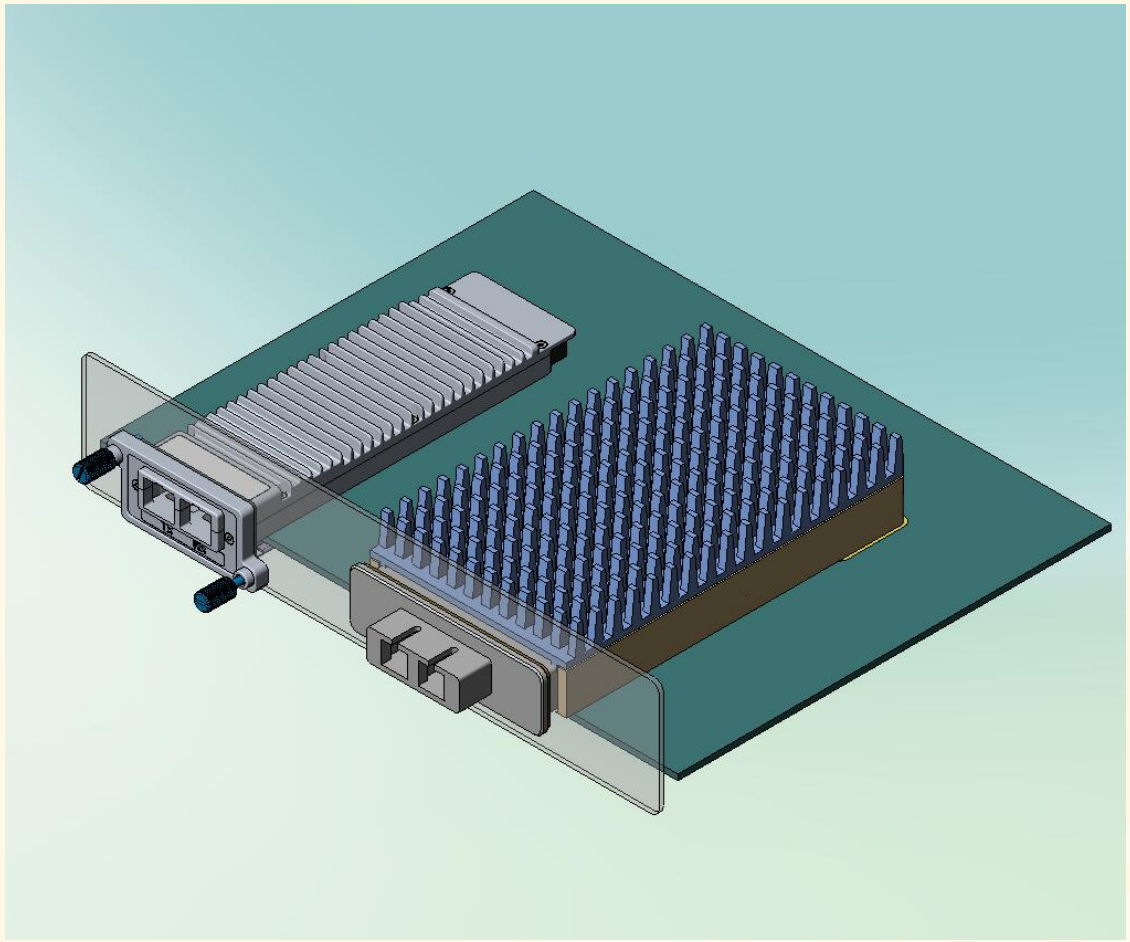
- 1550nm TP2 to TP3 per λ link budget
  - Max output power: 0dBm
  - Min output power: -3dBm
  - Min receiver sensitivity: -10dBm
  - Max path penalty (@200ps/nm CD): 2dB
  - Link budget: 5dB
  - Max loss (2dB fiber + 3dB other loss): 5dB
- 1310nm TP2 to TP3 per λ link budget
  - Max output power: 1dBm
  - Min output power: -2dBm
  - Min receiver sensitivity: -10dBm
  - Max path penalty (@60ps/nm CD): 1dB
  - Link budget: 7dB
  - Max loss (4dB fiber + 3dB other loss): 7dB
- Same per λ optical link budget can be used for the 4x25G EML alternative. If the output power becomes limited by eye safety, 4x25G would have 1dB extra power available versus 5x20G.
- It will be beneficial to extend the 10GE Link Model to higher Baud to have a common framework for evaluating and comparing optical link budgets.

10km 5x20G EML Transceiver Power

10GE-ER XENPAK Component	Power Watts	10km 5x20G Transceiver Component	Power Watts
XAUI (SiGe)	2.2	Quint 2:1 SerDes (SiGe)	6.5
Mod Driver (InP)	0.5	Quint MD (InP)	2.5
EML + TEC TOSA	1.5	Quint EML + TEC TOSA w/ WDM micro-optic Mux	5
PIN/TIA ROSA	0.3	Quint PIN/TIA ROSA w/ WDM micro-optic DeMux	1.5
other ICs	0.3	other ICs	0.5
Maximum operating power	**~5W**	**Maximum operating power**	**~16W**

10km 4x25G Transceiver Power is about 14W, due one less channel.

SMF 100GE Transceiver Mechanical Concept



- Pluggable 100GE Transceiver next to 10GE XENPAK.
- Latching mechanism not shown.
- Separate heat sink integral with line card cage (XFP style.)
- 55mm wide Enhanced PT20 SMT Connector (SFP+ style.)
- SC fiber connectors.
- 60mm x 100mm heat sink surface area.
- 10mm heat sink height with 1” space constraint.
- 16W supported with good airflow design.

100GE Transceiver Technical Feasibility Discussion

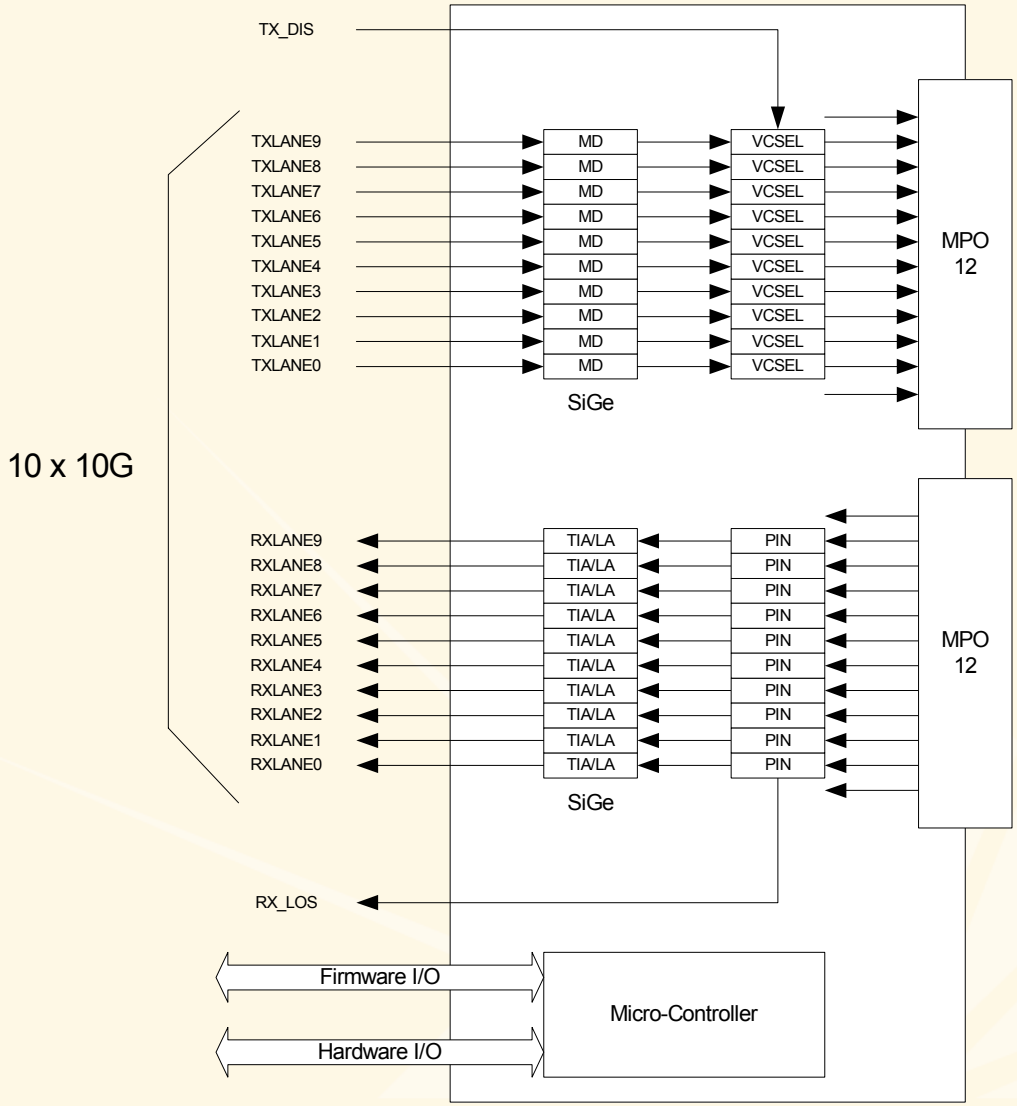
- A 10km SMF Optical Link Budget can be met with cooled 5x20G EML and 5x20G PIN/TIA 100GE alternative at 1550nm or 1310nm. √
- A Mechanical / Thermal design of a cooled 5x20G EML and 5x20G PIN/TIA 100GE Transceiver is technically feasible. √
- A 10km 100GE SMF Transceiver based on cooled 5x20G EMLs is technically feasible. Low risk development can be initiated.
- A 10km 100GE SMF Transceiver based on cooled 4x25G EMLs is also technically feasible. Development risk is similarly low.
- In the long term, 5x20G or 4x25G cooled EML alternatives are not necessarily the basis for the lowest cost or lowest power 100GE Transceivers.
- The challenge for the 100GE 10km SMF standard is to enable first generation Transceivers that use existing technology with low development risk, and also enable follow on Transceivers with significantly reduced cost, power and size as new technologies become available. The choice of wavelength operating point, spacing and count should accommodate existing and future technologies.
- It is desirable for the 100GE 10km SMF standard to be incrementally extendable to 40km.

10km 5x20G Transceiver Economic Feasibility (Cost)

Component	10GE-ER XENPAK	10km 5x20G Transceiver	Comments
SerDes	1x	3x	XAUI (SiGe) vs. Quint 2:1 SerDes (SiGe)
Mod Driver	1x	4x	Single MD (InP) vs. Quint MD (InP)
TOSA	1x	4x	Single EML TOSA vs. Quint EML, DWDM Mux (micro-optic)
ROSA	1x	5x	Single PIN, TIA ROSA vs. DWDM DeMux, Quint PIN, Quint TIA
PCBA & mechanical	1x	2x	FR4 PCBA, XENPAK parts vs. Nelco PCBA, new form factor parts
Test	1x	1x	Single channel testing vs. five channel parallel testing
TOTAL	**1x**	**4x**	**Weighted average of initial products at similar volumes**

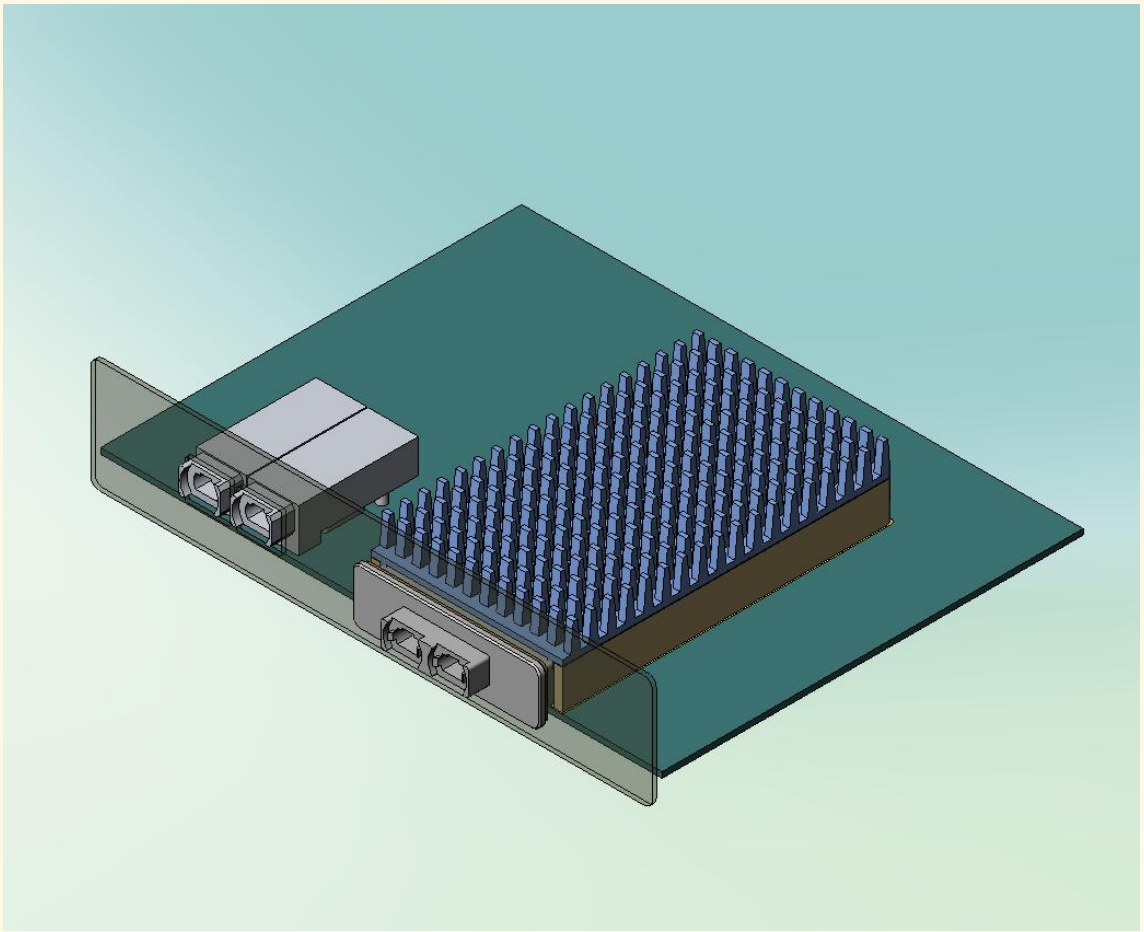
Copy of Relative Cost table from “Technical & Economic Feasibility of 20GBaud 100Gb Transceivers,” C. Cole, IEEE HSSG, 11/15/06, Dallas, TX.

100m 10x10G 850nm OM3 Transceiver Architecture



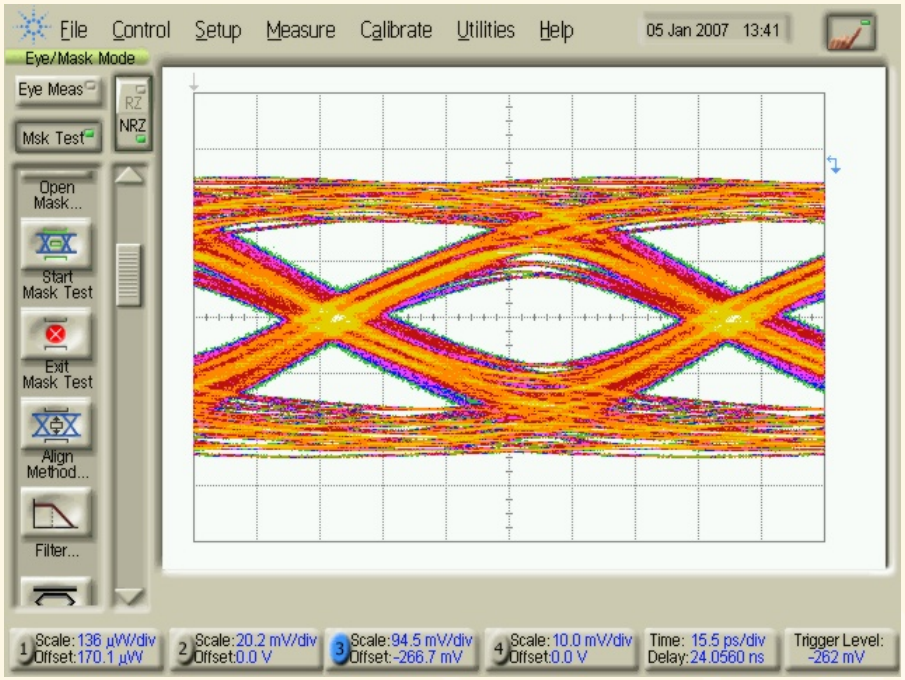
- MMF Transceiver parallel optics architecture as supported in “Parallel Optical ~10x~10G 100-Gigabit Ethernet” J. Jewell, et.al., Picolight, HSSG January 17-19, 2007, Monterey, CA.
- Alternate two Transceiver parallel optics architecture, with separate TX and RX blocks, also proposed in the Jewell Jan 17-19 presentation.
- 10x10G VCSEL array yield is the main economic feasibility (cost) issue.

100m MMF 100GE Transceiver Mechanical Concepts



- Pluggable MMF 100GE Transceiver with dual MPO connector next to two SNAP12s.
- SMF 100GE Transceiver mechanics will meet all requirements of the MMF parallel optics application, however the size is much larger then necessary.
- Technical feasibility of a SNAP12 based 100GE Transceiver is dependant on 10G I/O electrical performance, which is technically challenging as shown in the following signal integrity study.

MegArray BGA Connector 10G Signal Integrity



10G signal path

Anritsu MP1763B PPG (PRBS 2^7-1)→
SMA terminated coax →
coax to PCB transition →
2” FR-4 co-planar 50Ω line →
MegArray-300 BGA pin pair (J29) →
2” Nelco broad-side coupled 50Ω line →
PCB to coax transition →
SMA terminated coax →
Agilent 86100A/86112A (20GHz) DCA.

- The test set-up 10G eye closure is excessive due to impedance mismatch at 300-pin MegArray BGA connector; 35Ω:50Ω, and mismatches at PCB transitions; 65Ω:50Ω, as measured with an Agilent 54754A Differential TDR Module.
- It may be possible to get good MegArray BGA connector 10G performance, through PCB RF tuning techniques on both sides of the interface.
- Alternately, a short version of SMF 100GE Transceiver mechanics (ex. 4cm depth) is technically feasible for MMF 100GE Transceiver.

MegArray BGA Connector 10G Signal Integrity, cont.

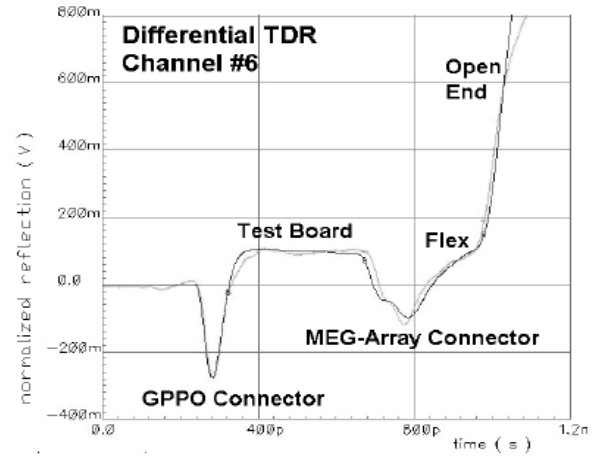


Figure 5: Measured (gray curve) and simulated (black curve)

2003 IBM initial test board TDR measurements identifying MegArray BGA connector capacitive impedance mismatch problem:

Christian Schuster, et al., "Electrical Interconnect Design and Optimization for 120 Gbps Parallel Optical Transmitter Module and Test Station," *Proc. 7th IEEE Workshop Signal Propagation on Interconnects*, 2003, pp. 133–136.

Follow-on work achieves excellent MegArray 10G signal integrity, and demonstrates fully the Technical Feasibility of 12x10G parallel optics SNAP12 Transceivers.

- Daniel Kuchta, et al., "120 Gb/s VCSEL based Parallel Optical Transmitter and Custom 120 Gb/s Testing Station," 2003 IEEE LEOS Annual Meeting Conference Proceedings (IEEE Cat. No.03CH37460) 150-1 vol.1 2003
- Daniel M. Kuchta, et al. "120-Gb/s VCSEL-Based Parallel-Optical Interconnect and Custom 120-Gb/s Testing Station," Journal of Lighwave Technology, Vol. 22, No. 9, Sept. 2004, pp. 2200-2212.
- Daniel M. Kuchta, et al. "120 Gb/s VCSEL-based Parallel Optical Links," CPT 2005 Eighth International Symposium on Contemporary Photonics Technology.