Title:
BER measurements for 100GbE
Subject:
IEEE 802.3 Higher Speed Study Group

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Agenda

- BER (10^{-12}, 10^{-13}, 10^{-15} ?) as the ultimate figure of merit for link performance
- Multiply lanes: sequential or simultaneous measurement
- BER-measurements on link components or modules (TX, (channel,) RX) to verify their performance and to predict final link performance
- TX measurements, eye-opening / phase margin / Total Jitter measurement
- RX measurements, sensitivity / jitter tolerance
- Design for test considerations
- Conclusions

Target BER <10^{-12}?

- heavily influences
  - test time and cost of test
  - when target BER is selected too small measurement is no more practical within given time

line rate	1E+10			
BER	1E-12	1E-13	1E-14	1E-15
# of errors	average time until # of errors occur			
3	5.0	50.0	8.3	3.5
10	16.7	2.8	27.8	11.6
50	83.3	13.9	5.8	57.9
	minutes	hours	days	

Table 1: measurement time vs # of detected errors and BER

BER as the ultimate link performance figure of merit

- BER measurement as final check for system performance is desirable
- final architecture is not yet determined:
  10x 10Gb/lane, 5x 20Gb/lane, 4x 25Gb/lane, ...
- shall tests be done on a single lane or on the whole link?
  - probably on the whole link (test case close to mission mode)
  - simultaneous test on multiple lanes, at least simultaneous stimulation to include crosstalk effects
- is test equipment required for this final test or will it be built-in (BIST)?
  - a BER performance check maybe possible as BIST
- can performance characterization (margin test) be achieved by BIST?
  - a BER margin test may not be feasible w/ built-in measurement engines!

Multiply lanes: sequential or simultaneous measurement

	sequential single lane tests w/ serial BERT	simultaneous multi-lane tests w/ parallel BERT
variety / availability of test equipment	high >5	low (2)
in depth (jitter) characterization / lane	ok	ok / (?), today not as convenient as w/ serial BERTs
test automation	needs RF relays: issues w/ reliability, performance, ...	ok
test time	x number of lanes	x1
cost of test equipment	typically x2 of price/channel of parallel BERT	price / channel typically ½ of serial BERT
system-like test (crosstalk)	no	yes
timing measurements between channels e.g. skew	no	yes

=> Simultaneous multi-lane tests w/ parallel BERT seems advantageous

TX measurements (1)
Total Jitter (TJ) measurement

- TX total jitter important to predict system performance
- several “measurement” methods to determine TJ and its components (real time scope, sampling scope, TIA, BER-scan) have been discussed widely
  - all methods except BER-scan have to rely on extrapolation, partially from very low data depths
  - BER-scan measurement w/ bathtub-curve result display well known
    - can be used as full measurement (very time consuming when measured down to low BERs $<10^{-12}$) or
    - as relatively data-rich basis for extrapolation
  - “fast BER-scan” to determine TJ for target BER available as well

TX measurements (2)
Fast TJ measurement

- Regular BER-scan measures BER point by point (eventually w/ predefined break parameters such as # of errors or # of bits)
- Goal of fast TJ algorithm is to bracket the point in time where BER=BER_{target} w/ sufficiently low resolution (e.g. 10mUI)
- Fast TJ algorithm based on the fact that a BER measurement follows a Poisson distribution (only two possible outcomes, detected bit correct or wrong)
- Search for target BER proceeds according to decision criteria as of table 2 / figure 1: while receiving bits and errors constantly monitoring if accumulated measurement depth already sufficient to decide with given confidence level that actual BER is above or below target BER and so the next point in time can be measured or if more bits need to be accumulated
- http://cp.literature.agilent.com/litweb/pdf/5989-2933EN.pdf or ../5989-3151EN.pdf

95% confidence level lower limits, BER > 10–12		95% confidence level upper limits, BER < 10–12	
Min number of errors	Max number of compared bits (x1e12)	Max number of errors	Min number of compared bits (x1e12)
1	0.05129	0	2.996
2	0.3554	1	4.744
3	0.8117	2	6.296
4	1.366	3	7.754
5	1.970	4	9.154
6	2.613	5	10.51
7	3.285	6	11.84

Table 2: Statistics for lower and upper limits on BER of 10^{-12}, on the 95% confidence level.

To convert to *BER* of 1eN, just replace the exponent "12" with N.

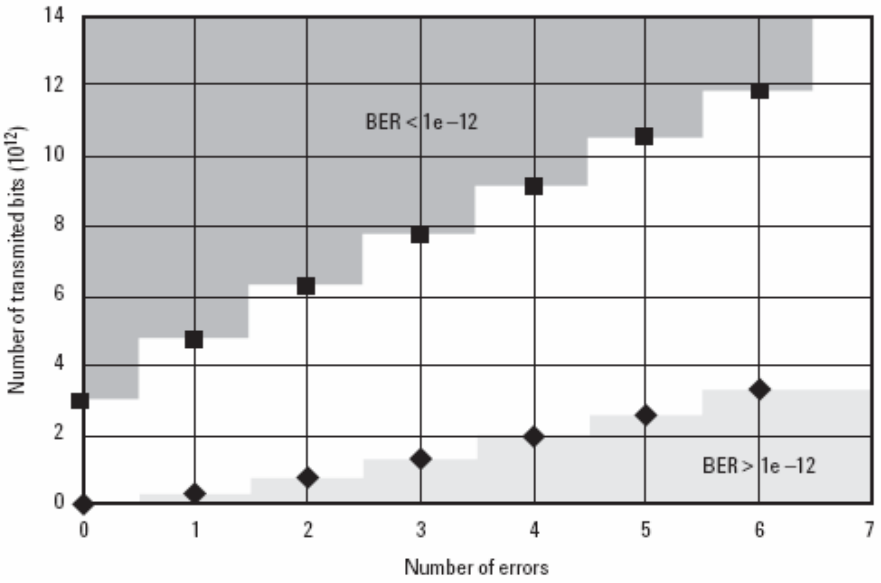


Figure 1: The 95% confidence level boundaries for upper (dark grey) and lower (light grey) limits on a BER of 1e–12

TX measurements (3)
Fast TJ measurement – gain vs full BER-scan

- **Measurement Times vs RJ_{rms} for a 1ps delay resolution and three different DJ_{PkPk} values w/ an optimized BER-scan and a fast TJ measyurement**
- **Time saving depends on jitter amplitude and distribution: typ. 40 (15...150)**

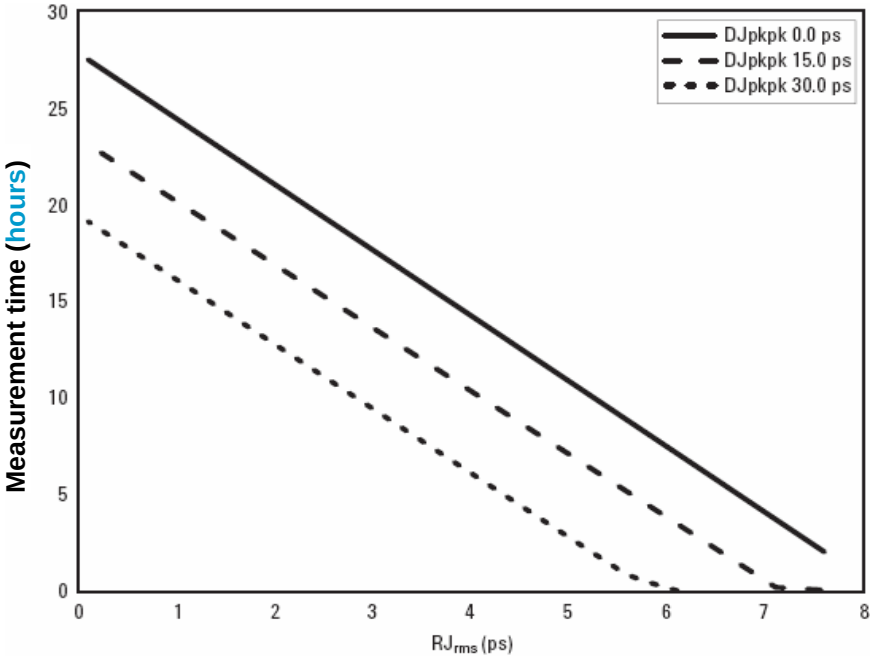


Figure 2: Optimized BER-scan measurement (bathtub curve) - the higher the Total Jitter, the faster the measurement!

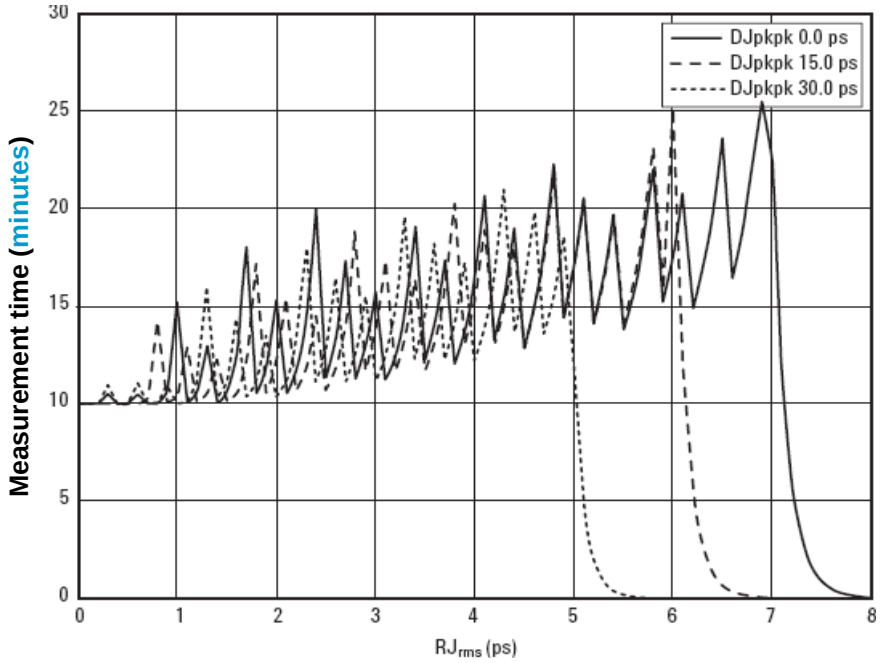
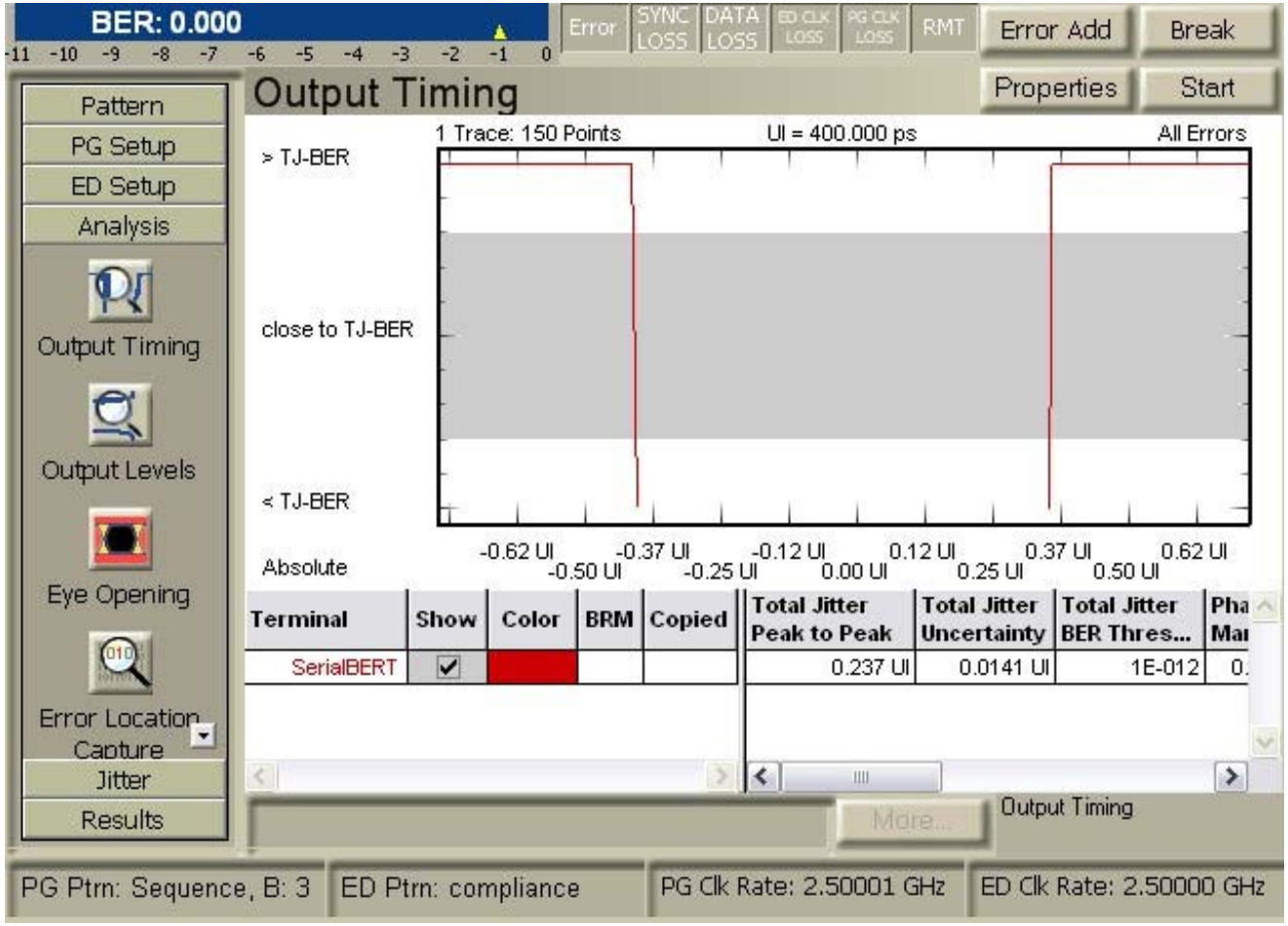


Figure 3: Fast total jitter measurement

TX measurements (4)
Fast TJ measurement implementation example



- fast TJ result display = simplified BER-scan result display
- only three different vertical “levels” according to fig. 1
  - BER > BER_{target} (white)
  - BER ~ BER_{target} (grey)
  - BER < BER_{target} (white)

Figure 4: Fast total jitter measurement implementation example

RX measurements
principle and *test* vs *characterization*

- test principal: stimulate RX under test with deliberately distorted test signal and check RX's "error free" detection
- distinguish between jitter tolerance *test* and *characterization* measurement
- *test:*
  - check, if BER < limit, when stimulated with specified jitter cocktail
  - doable, even for BER $<10^{-12,}$ as it is just one measurement
- *characterization:*
  - find performance limit (BER>spec) depending on different jitter contributors, such as RJ, PJ, ISI, ...
    (stimulate with distorted signal, measure BER; depending on BER in- or de-crease predefined jitter component(s) and repeat)
  - test time very high especially for BER $<10^{-12}$
  - alternative methods need to be investigated;
    possibly w/ extrapolation similar to TJ measurements on TXs

“Design for test” considerations

- TX waveform test:
  - predefined test pattern(s) generated internally (inside the core)?
  - arbitrary test patterns to be generated through external PG-stimulus
    - access through RX
    - direct / near-end loop-back w/o data alteration (no de-/en-coding, ...)!
    - how to set RX into loop-back mode? no complicated (OOB) signaling / sequencing!
- RX sensitivity or jitter tolerance test: how to check error free detection?
  - built-in comparator, error detector and counter?
    - how to read out result?
    - how to do automated characterization?
  - loop-back to TX to check with external (BERT-) ED
    - how to set RX into loop-back mode? no complicated (OOB) signaling / sequencing!
    - direct / near-end loop-back w/o data alteration (no de-/en-coding, ...)!

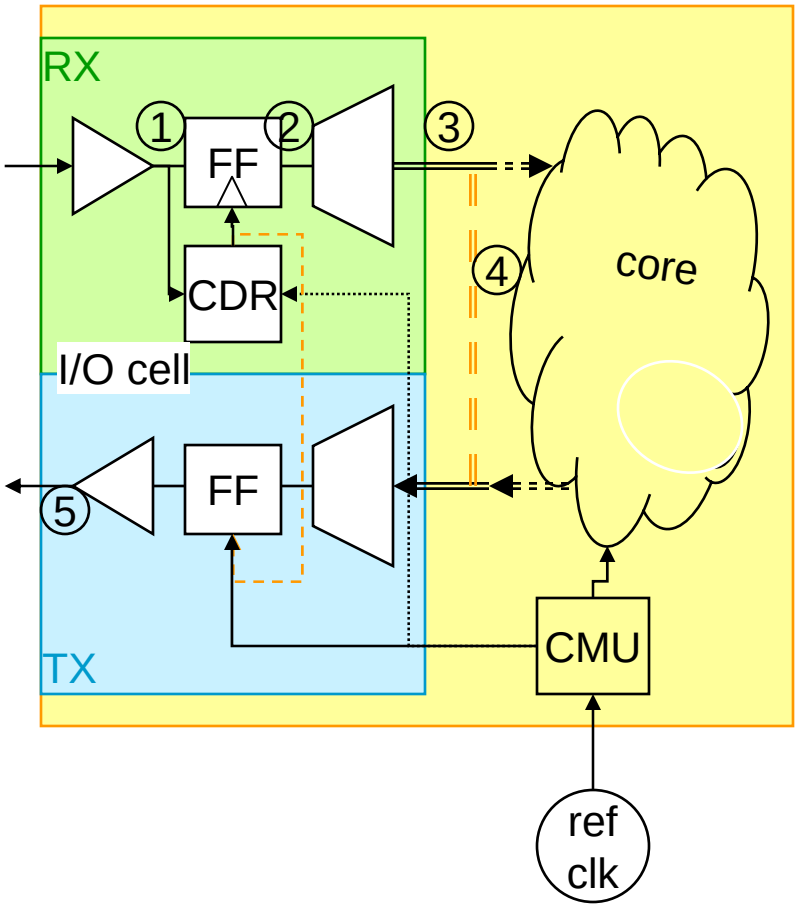


Figure 5: Simplified block diagram of TRX

Conclusions

- specification of target BER< 10^{-12} can be disastrous in terms of test time / testability at all
- simultaneous test with parallel BER seems advantageous vs sequential test of single lane
- BER measurements
  - mandatory as final figure of merit for complete system
  - for TXs: the only real TJ ***measurement*** down to low BERs
  - for RX:
    - an error check of any kind is necessary for sensitivity / jitter tolerance test
    - characterization down to low BERs may require new test methods
- design for testability w/ standard physical layer instruments = near end loop back w/o data alteration!!