

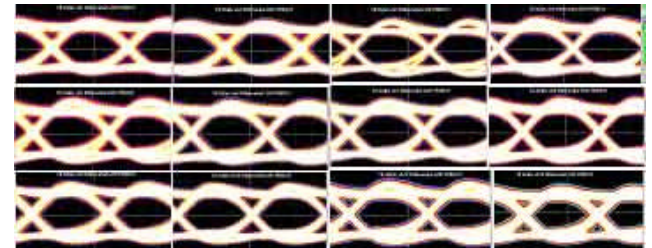
Parallel-Optical ~10x~10G 100-Gigabit Ethernet

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Technical Feasibility

- 10x10G combines 2 technologies, both in product stage with >100,000 parts in the field for each:
 - 1x10G (10GBASE-SR)
 - 12x2.7G parallel optical interconnects
- Combining these into 10x10G:
 - Start with 12x2.7G
 - Replace VCSEL/PIN arrays with 10G versions
 - Replace driver/receiver arrays with 10G versions
 - Refine packaging for 10G integrity
 - Deal with issues of crosstalk, etc

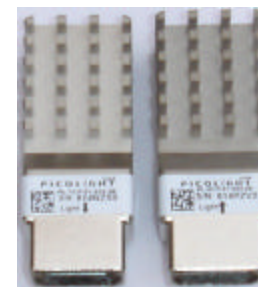
OFC
2003
Demo



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Possible Initial Configurations

(Generally less aggressive than the 12x10.3G demo at OFC 2003)

10x10.3G w/ 66B/64B encoding (as in 10GbE)

- + uses only 10 channels, 10 fibers
- + 10.3Gbaud same as 10GbE
- + possibly compatible with 10km formats
- coupling capacitors larger but not a significant issue
- long run lengths incur slight margin penalty (baseline wander)

10x12.5G w/ 8B/10B encoding

(Why not 8x12.9G w/ 66B/64B?)

- + uses only 10 channels, 10 fibers
- 12.5Gbaud [®] reliability/performance issues to be resolved
- + possibly compatible with 10km formats
- + coupling capacitors straightforward
- + no long run lengths

12x10.4G w/ 8B/10B encoding

- uses 12 channels, 12 fibers
- + 10.4Gbaud ~same as 10GbE
- not likely compatible with 10km formats
- + coupling capacitors straightforward
- + no long run lengths

100m 10x10Gig Transceiver Costs

(Initial 10,000 parts/year volumes)

Component	10GBASE-SR XENPAK	10x10Gig	Comments
SERDES	1x	0x	N/A for 100G
Driver IC + TOSA	1x	8x	Driver integrated w/ TOSA Arrayed 10G chips
ROSA	1x	8x	Arrayed 10G chips
PCBA/Mech	1x	2x	
Test	1x	5x	Increased test efficiency required
TOTAL	1x	4x	Weighted average at initial volumes

100m 10x10Gig Transceiver Costs

(Initial 10,000 parts/year volumes)

Component	12x2.7G Parallel	10x10Gig	Comments
SERDES	0x	0x	N/A for either
Driver IC + TOSA	1x	4x	Driver integrated w/ TOSA Arrayed 10G chips
ROSA	1x	4x	Arrayed 10G chips
PCBA/Mech	1x	3x	
Test	1x	5x	Increased test efficiency required
TOTAL	1x	4x	Weighted average at initial volumes