Technical Feasibility of 4x10G and 10x10G Electrical Interfaces

IEEE 802.3 Higher Speed Study Group

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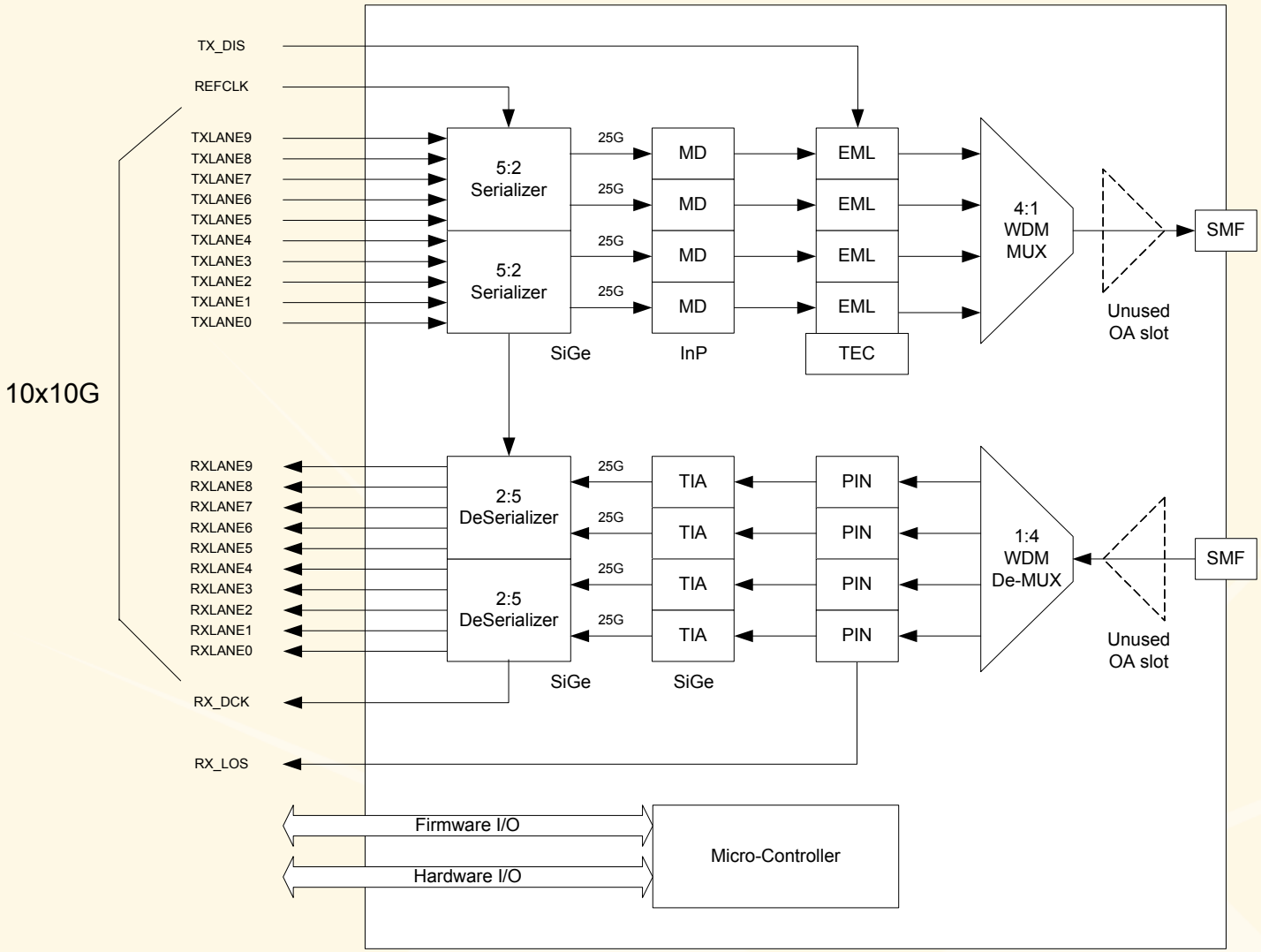
Outline

- SMF Transceiver Architecture
- MMF Transceiver Architectures
- Current 10G I/O Electrical Specifications
- Discussion

SMF 4x25G 1310nm Transceiver Architecture

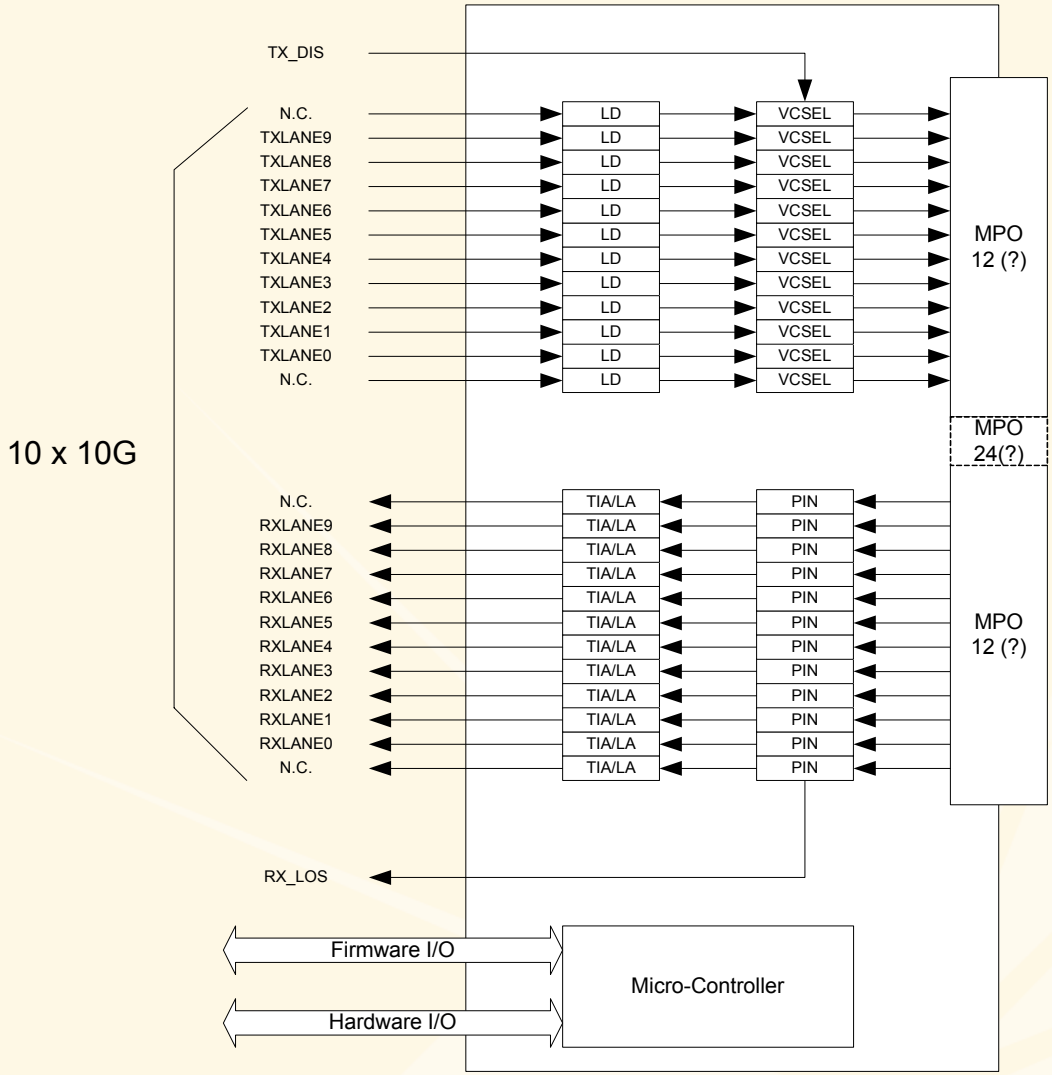


- SMF Transceiver retimes the interface.
- CDRs are part of the SerDes function.

Alternate SMF 4x25G Transceiver Architecture View

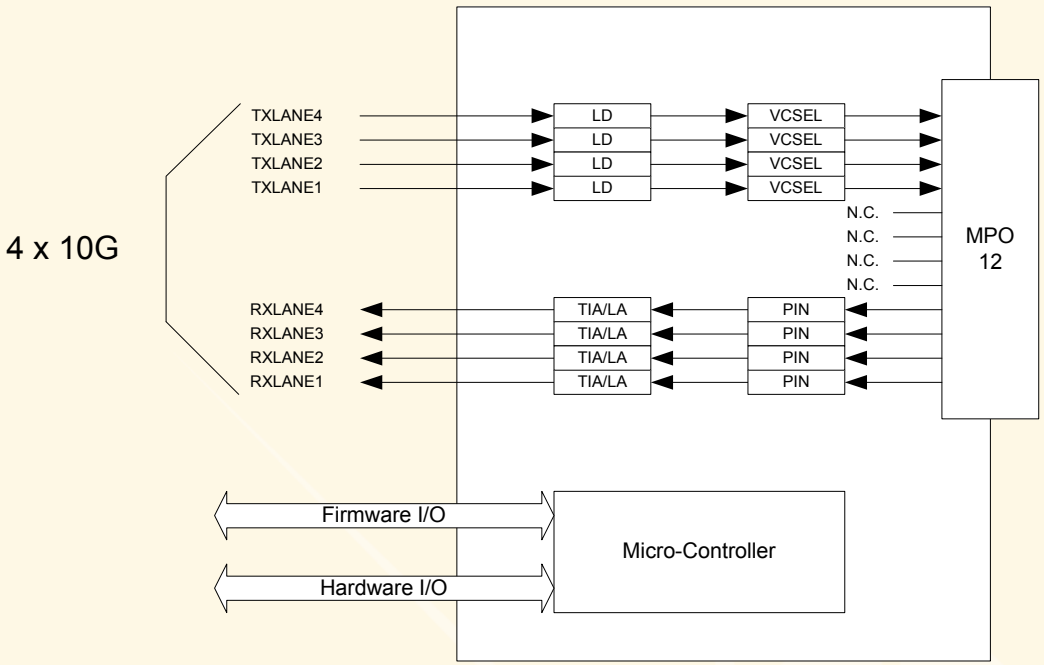
"Multi-headed Frankenstein,"
Piers Dawe, Avago Technologies,
28-31 May 2007

MMF 10x10G 850nm Transceiver Architecture



- Lowest cost, lowest power MMF Transceiver does not retime the interface, (no CDRs.)
- Two 12-fiber MPO cables vs. one 24-fiber MPO cable is an open question.
- Requirement for MMF functionality in the same large form factor as SMF Transceiver is an open question. (A small form factor only for MMF Transceivers is possible.)
- Aligning 100GE MMF parallel PMD solution with 12x10G Infiniband may be beneficial.

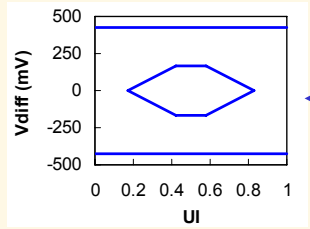
MMF 4x10G 850nm Transceiver Architecture



- Lowest cost, lowest power MMF Transceiver does not retime the interface, (no CDRs.)
- QSFP is a candidate 4x10G MMF form factor
- A common 10G electrical I/O and optical specification between 40GE and 100GE is an open question. (Full set of 10x10G interface requirements may differ from full set of 4x10G interface requirements.)
- Aligning 40GE MMF parallel PMD solution with 4x10G Infiniband may be beneficial.

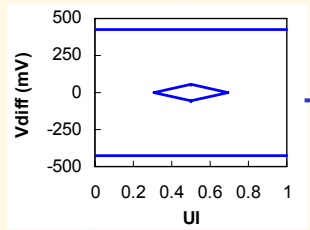
Current 10G I/O Electrical Specification Observations

- **XFI (XFP I/O)**
  - Designed for retimed PMDs (w/ CDR)
  - 30cm Host trace targets (no equalization)
  - 3 dB margin for crosstalk and reflection
  - Easy Host design.
  - Straightforward Module design
- **SFI (SFP+ I/O)**
  - Designed for existing non-retimed PMDs (w/o CDR)
    - 10GBASE-SR (300m OM3)
    - 10GBASE-LRM (220m OM1, OM2)
    - 10GBASE-LR
  - 30cm Host trace targets (w/ equalization)
  - Equalizer must also support the entire 10GBASE-LRM fiber link
  - Difficult Host and Module design
    - Jitter budget tight with open issues
    - Measurements challenging with open issues.



C C'

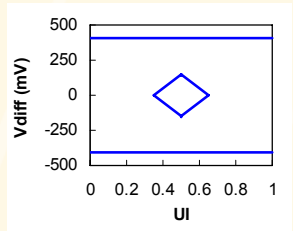
TJ ≤ 0.34 UI
DJ ≤ 0.18 UI



B B'

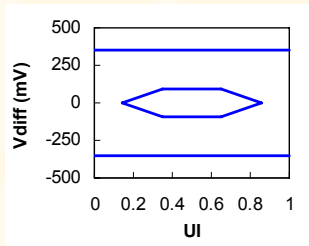
TJ ≤ 0.61 UI
NonEQJ ≤ 0.41 UI

HOST PMD



C C'

TJ ≤ 0.70 UI
DJ ≤ 0.42 UI



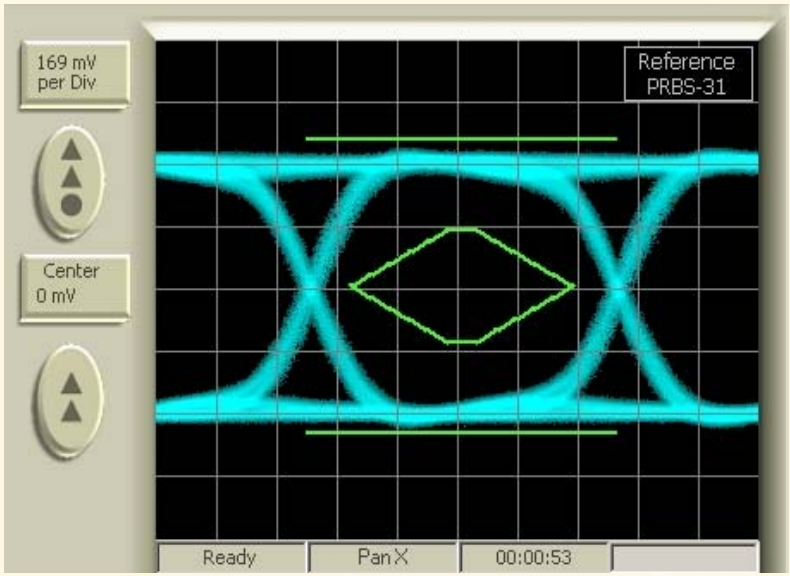
B B'

TJ ≤ 0.28 UI
DDJ ≤ 0.1UI
PWS ≤ tbd
UJ ≤ 0.023 UIrms

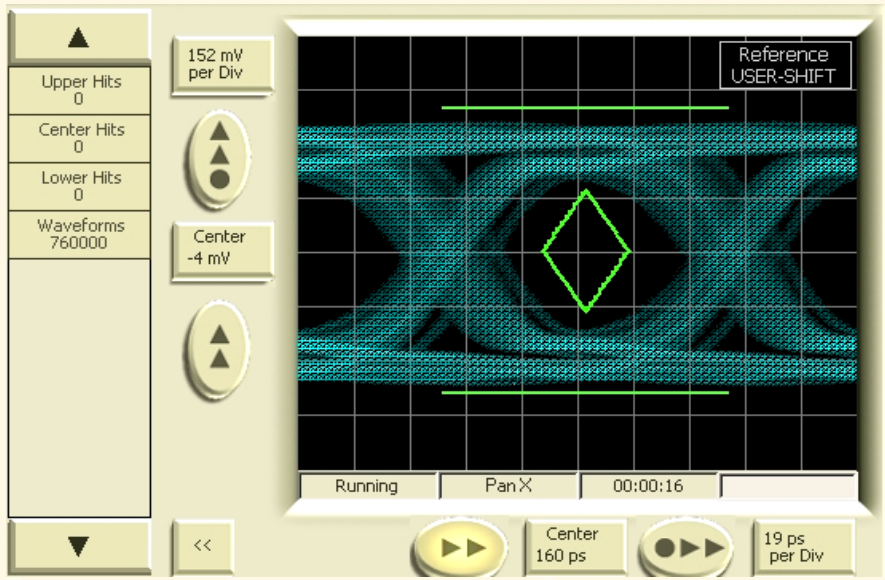
Current 10G I/O Electrical Specification Considerations

- **XFI for N x 10G**
  - Requires CDRs in all PMDs
  - Adds ~ 5W with current technology
  - More then doubles power dissipation of 100m MMF
  - Adds significant cost to 100m MMF PMD
  - Dominates cost of <10m Cu PMD.
- **SFI for N x 10G**
  - Over-specifies the Electrical Interface
  - Adds cost and complexity for 100m MMF
    - Requires more Host equalization than needed
    - Requires more expensive testing than needed
  - Provides no margin for additional crosstalk due to 4 or 10 parallel lanes
  - Has open specification issues driven by –SR and –LRM that need to be resolved.

Single Channel Un-retimed 10G 100m OM3 Link



TX: Synthesis Research BertscopeS



RX: Synthesis Research BertscopeS

- **TX** + 0.04 B.U.J. → 5" FR-4 → Eval Card → SFP+ 10GE-SR Transmit path
- → 100m OM3 → SFP+ 10GE-SR Receive path → Eval Card → Cables → **RX**
- Significantly better RX eye is obtained if TX pre-emphasis and proper Host Card are used.
- 100m OM3 link has Technically Feasible margin to deal with multi-lane crosstalk levels previously presented at the HSSG, for example the analysis and measurements in cole_01_1106.

Discussion

- **Current 10G I/O Electrical Specifications for N x 10G applications**
  - XFI would increase power and cost of N x 10G MMF (and Cu) PMDs
  - SFI would increase power and cost of N x 10G Host
  - XFI and SFI do not take advantage of 100m reduced MMF reach
  - Neither XFI nor SFI lead to the lowest overall system cost
- **New N x 10G I/O Electrical Specification**
  - Optimizes power and cost of 40GE and 100GE MMF systems
- **Recommendations for new N x 10G I/O Electrical Specifications**
  - Define a non-retimed PMD interface derived from SFI specifications
  - Retain return loss specs of SFI
  - Take advantage of extra jitter budget of 100m (vs. 300m) MMF PMD
    - Allocate budget to retain high yield, low cost of 100m MMF PMD
    - Allocate remaining budget to electrical link at B and C points
  - Use the MMF jitter budget to define <10m Cu PMD
  - Use extra electrical link budget to simplify Host design:
    - Minimize Equalizer requirements for Host TX and RX
    - Increase design and test margin
  - Specify limiting interface (unless new problems require a linear interface)
- **Obtain measurement data to quantify crosstalk penalties**