100 GbE, 10X10 Alternative

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Economic & Technical Feasibility

Reach (Technical) Feasibility of 100GE alternatives

SMF	10km 1310nm	40km 1310nm	10km 1550nm	40km 1550nm
10x10G DML	yes (10λ span needs semi-cooling)	yes (need new DML & RX APD/SOA)	yes (need new DML)	maybe (need new DML)
10x10G ML	yes	yes (need RX APD/ SOA)	yes	yes
5x20G / 4x25G DML	yes (need new DML)	maybe (need new DML & RX SOA)	maybe (need new DML)	no
5x20G / 4x25G ML	yes (need new EML)	yes (need new EML & RX SOA)	yes	yes (need RX DC)
2x50G DQPSK ML	yes (need I/Q ML)	yes (need I/Q ML & RX DC & SOA)	yes (need I/Q ML & RX DC)	yes (need I/Q ML & RX DC)
1x100G TDM ML	yes (need new ML & maybe RX DC)	yes (need new ML & RX DC & SOA)	yes (need new ML & RX DC & SOA?)	yes (need I/Q ML & RX DC & SOA?)

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Economic factors for 10 x 10 option

- **Commercially available components**
  - 10 GE already in volumes of 300-500k/year
- **Mature technologies**
- **Known yield and cost factors**
- **Multiple vendors**
- **Leverages 10GE volume manufacturing**
  - 10 G Lasers, Laser Arrays
  - 10 G PIN Photodiodes
  - 10 G Laser drivers
  - 10 G TIAs
- **10G Test equipment & manufacturing infrastructure already in place throughout the entire supply chain.**

Economic factors >> Early deployment

- Addresses immediate needs of some end users
- Addresses all reaches (30m to 40km)
- No need to wait for new chips (i.e. gear box, 20 and 25 GHz lasers, detectors)
- 10 Gbs electrical interfaces are all well defined
- 10 Gbs optics also well understood (link budgets, BER, performance specs)
- Can identify implementation issues early on
- Interfaces directly with 10 Gbs board design technology

Economic factors>> Path to future cost reduction

- Integration of discrete components
  - Laser arrays
  - Pin arrays
  - TIA arrays
  - Driver arrays
  - Integrated MUX / DEMUX
- Uncooled architectures can be designed
- Continue to leverage 10 Gbs cost curves

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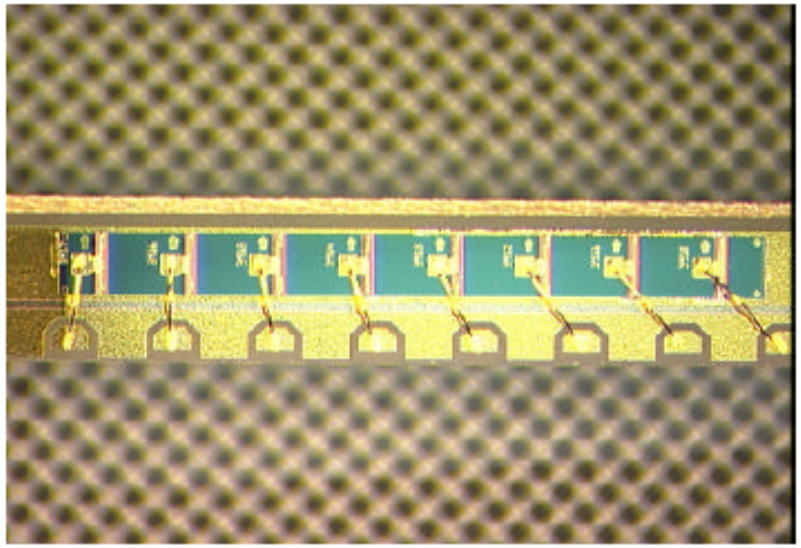
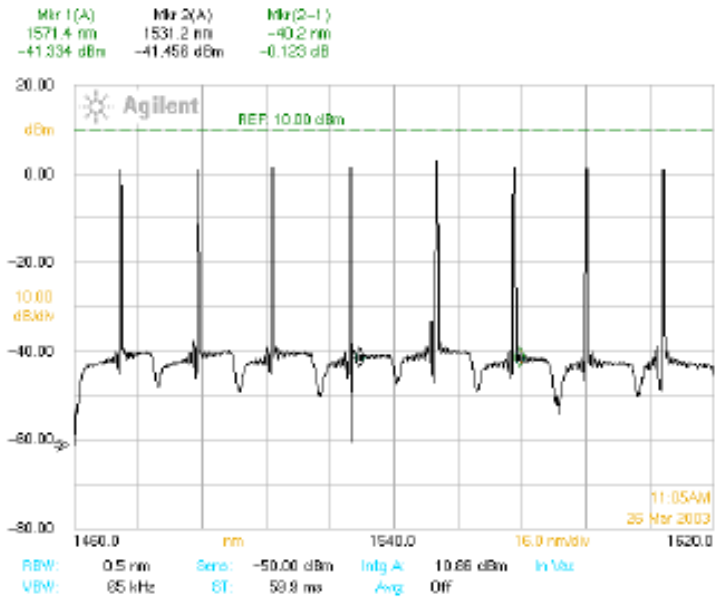
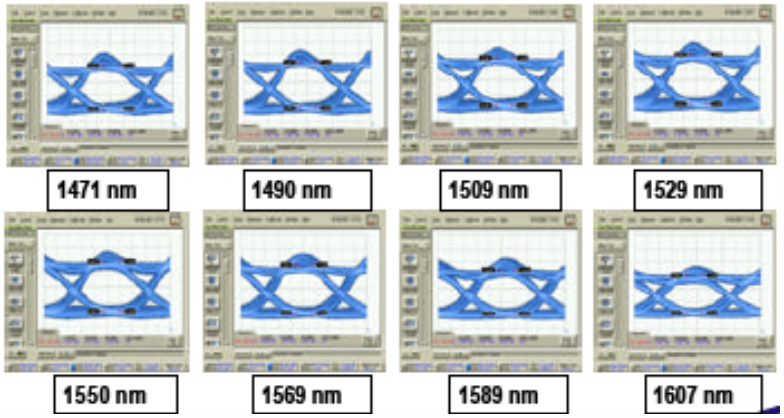
Technical feasibility of laser arrays





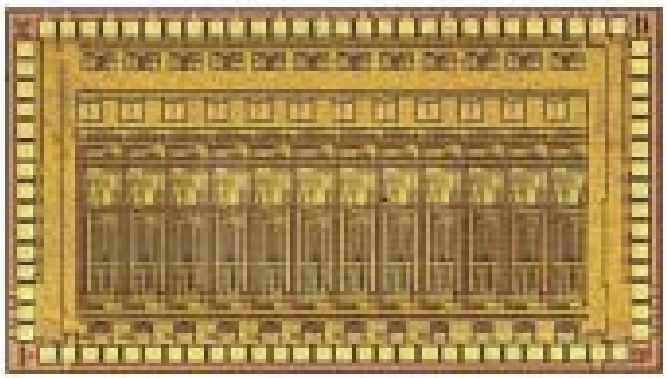
- *8 x 10Gb/s CWDM DFB array*
- *1470 – 1610nm, 20nm spacing*
- *Open, clean 10G back-to-back eyes*



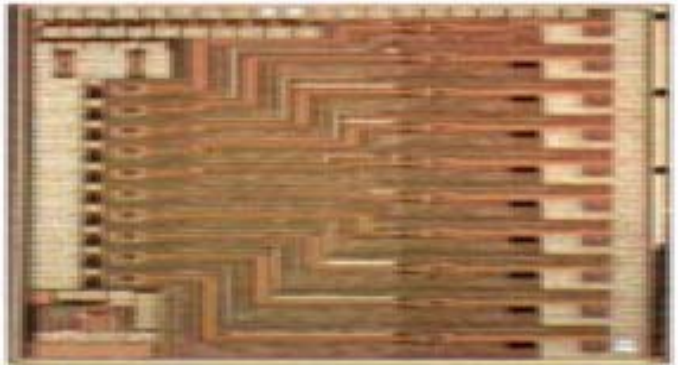
Technical feasibility of chipset arrays

- Quad 3.125G laser drivers, TIAs and Serdes arrays are shipping in volume today
- 20G (4x 5G) QSFP products have started to ramp
- Quad XAUI Serdes available from multi-vendors for 10GbE, backplane and Infiniband
- Some 10 x 10 G arrays already exist (pictures below)
- Std CMOS and SiGe BiCMOS processes for single chip solutions can be reused for arrays

Examples of 10G TIA Arrays



ZARLINK SEMICONDUCTOR



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