Market, Technical, Cost and Solution Considerations for HSSG

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Outline

- Key Messages
- HSSG Market Requirements
- HSSG Technical Feasibility
- HSSG Cost Considerations
- HSSG Solution Considerations
- Summary

Key Messages

- HSSG should target 100GbE as the next speed bump for Ethernet
  - Needed to get ahead of next generation platform requirements
  - Lower speeds (e.g. 40 GbE) will not be enough
  - HSSG should also address blade backplanes along with data centers, metro and long haul networks
- 100Gb/s Technology is feasible today
  - 40G (OC768) shipping today in volume
  - Optical technology exist today
- Datacom apps likely to drive next generation Ethernet speeds
  - Cost effectiveness of the solution is key for deployment
  - Shorter reach optics for data centers ➜ lowered optics costs

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I/O scales with Moore's Law

1. Future I/O BW requirements will drive revolutionary changes!

2. Chip-to-Chip interconnect rates scale with Moore's Law

3. Out of the box or blade rates, follow the chip-to-chip rates

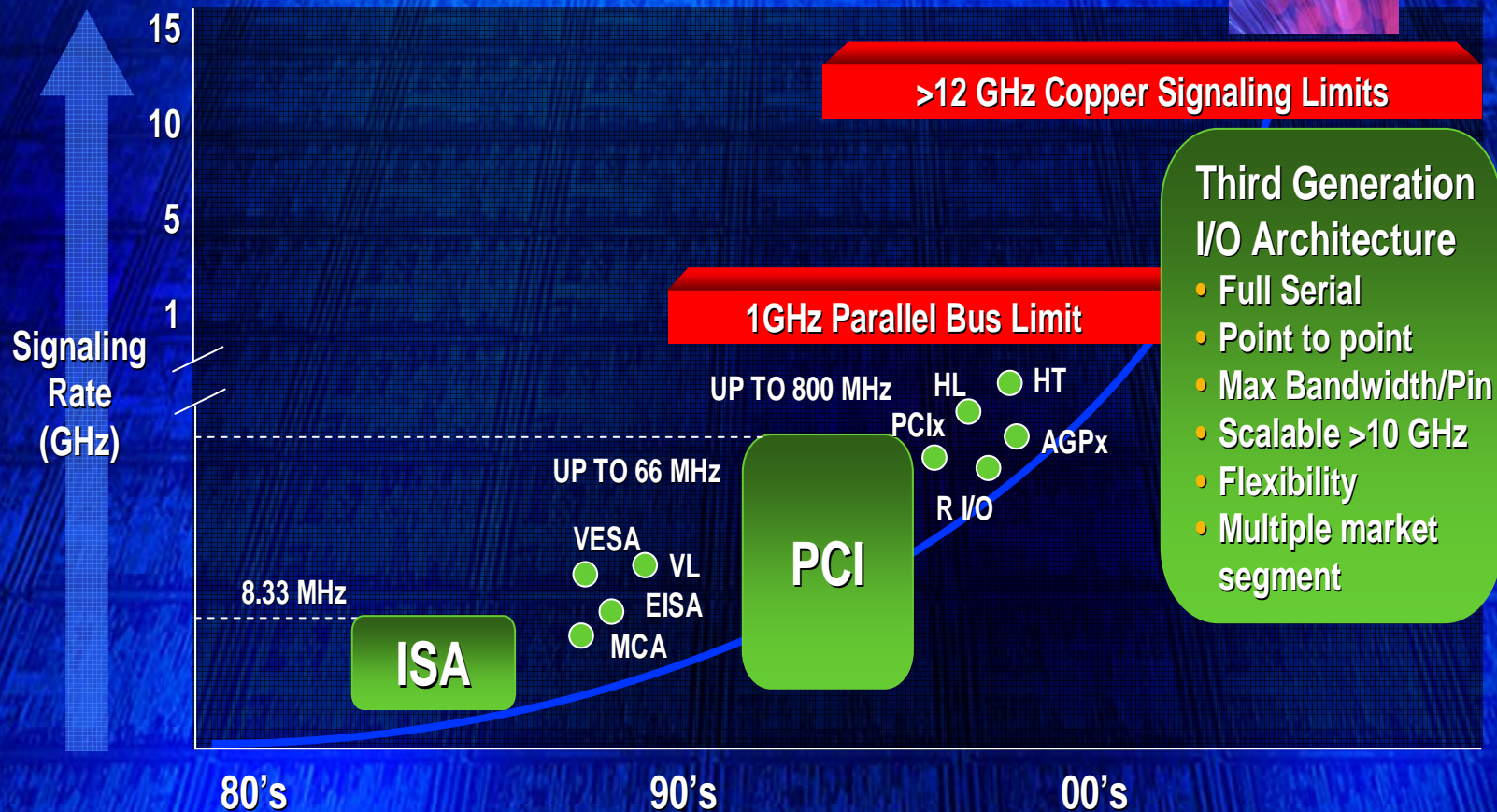4. By ~2010, we will see 100G backplane data rate reqmts
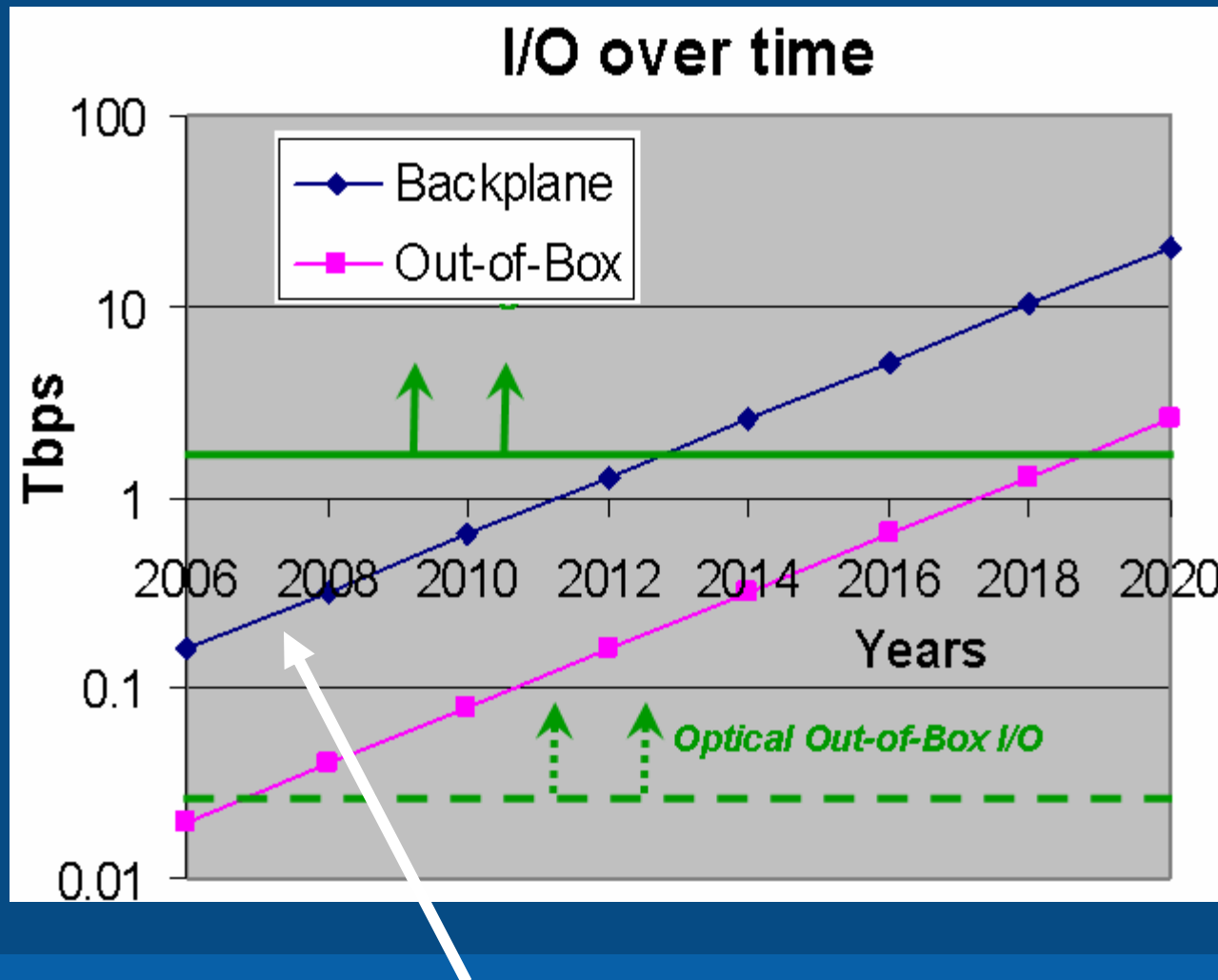
Moore's Law exponential increase in transistor densities will drive equal growth in backplane data rates.
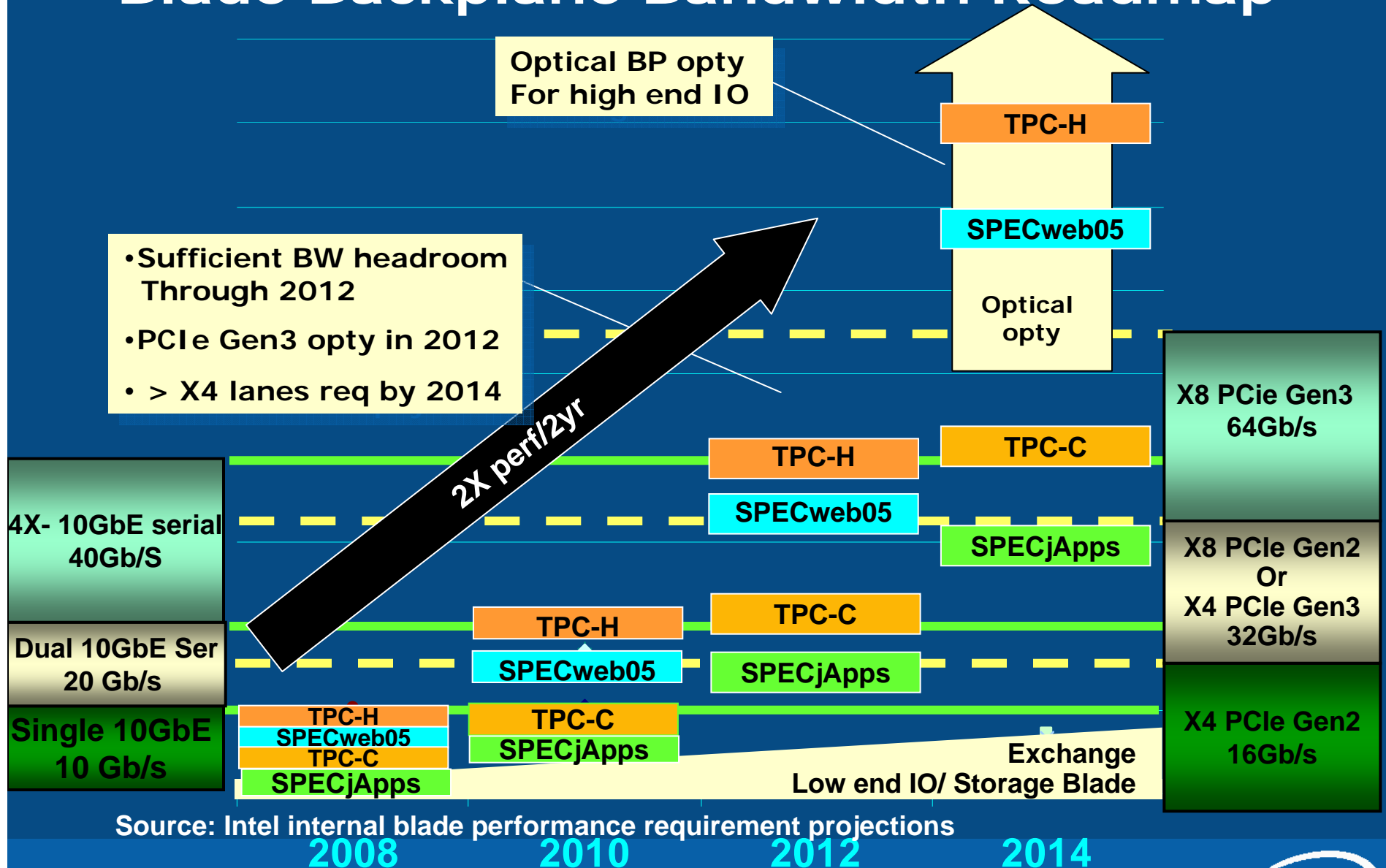
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I/O Architecture Evolution

Optical Interconnects

Signaling Rate (GHz)

15
10
5
1

>12 GHz Copper Signaling Limits

Third Generation I/O Architecture
- **Full Serial**
- **Point to point**
- **Max Bandwidth/Pin**
- **Scalable >10 GHz**
- **Flexibility**
- **Multiple market segment**

1GHz Parallel Bus Limit

UP TO 800 MHz   HL   HT
PCIx
AGPx
UP TO 66 MHz
R I/O

PCI

VESA   VL
EISA
MCA

8.33 MHz

ISA

80's   90's   00's

*Intel Fall IDF 2006 Presentation

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Intel **Developer** Forum Spring 2001

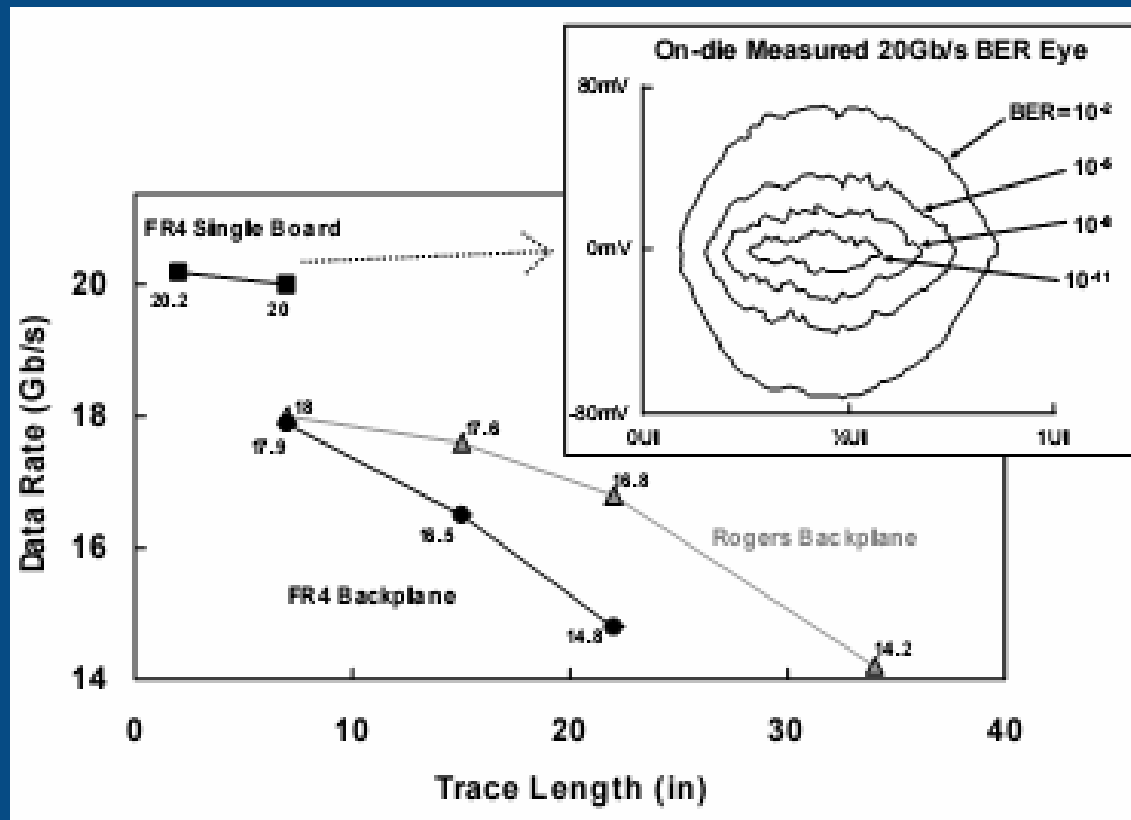**Platform I/O Bandwidth capabilities increasing**

Technical Feasibility of 100GbE

- Solutions available today
  - 40G Shipping
  - Low cost DWDM (LX4) shipping
    - Future - LX5 (4x25G?)
  - VCSEL arrays (snap 12 connectors) shipping
- Integrated Silicon Photonics
  - High Data Rate - High integration a reality today.
  - 10Gb/s CMOS modulators have been shown 2005 (Intel)
  - Higher rate modulators currently being developed
- HSSG for Backplanes
  - Optical backplane on the horizon
  - 4x25 and 5x20 seem equally doable, 4x20 may be easier because of VCSEL and CMOS limitations

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20Gb Electrical transmission

- 20 Gb transmission over FR4 using 90nm CMOS demonstrated.

- 7" FR4 with 2 sockets and packages, using Tx and Rx equalization

- Power consumption of 11.8 mW/Gb/s

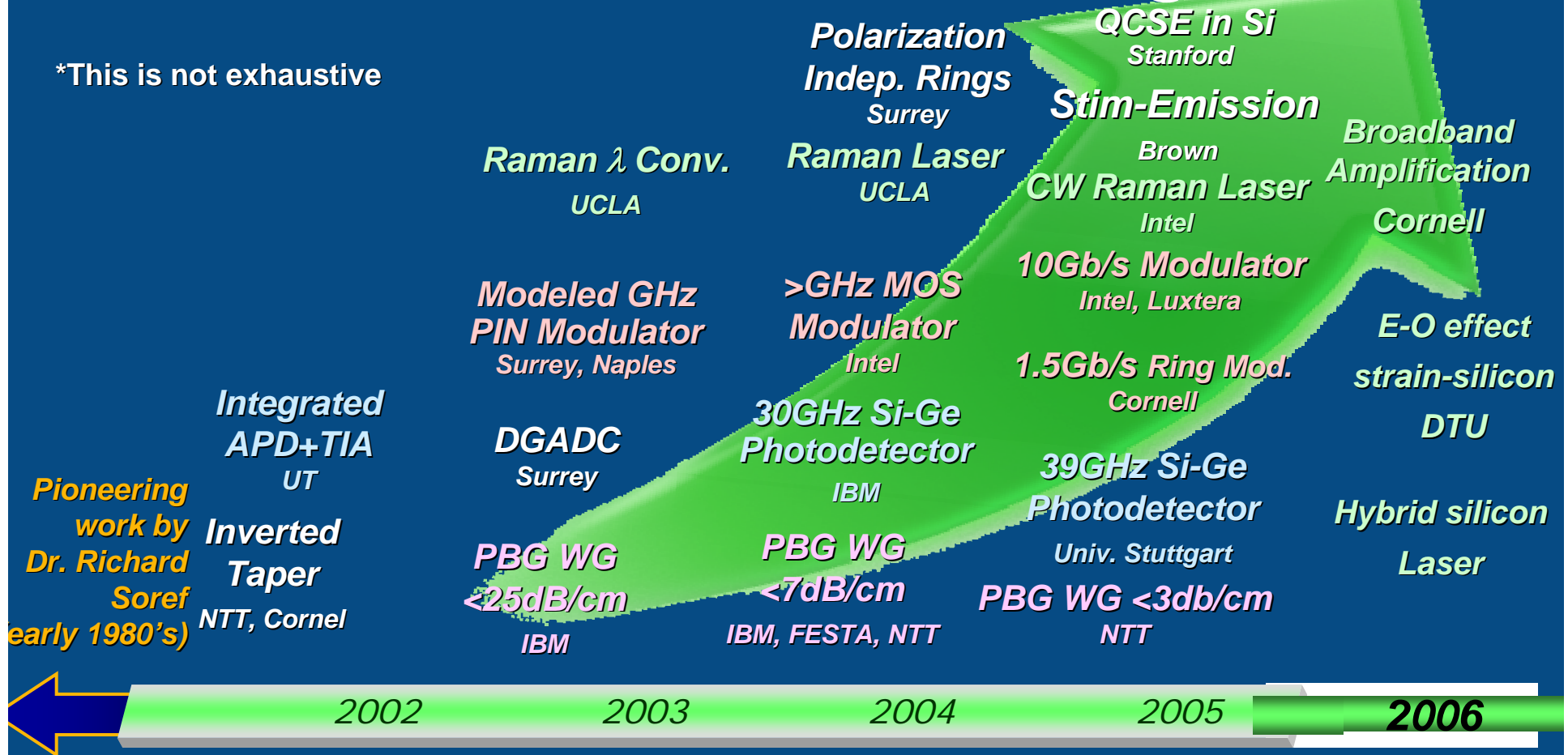- As CMOS moves to 65nm and 45nm feasible electrical rates will increase.

Technology exists today!

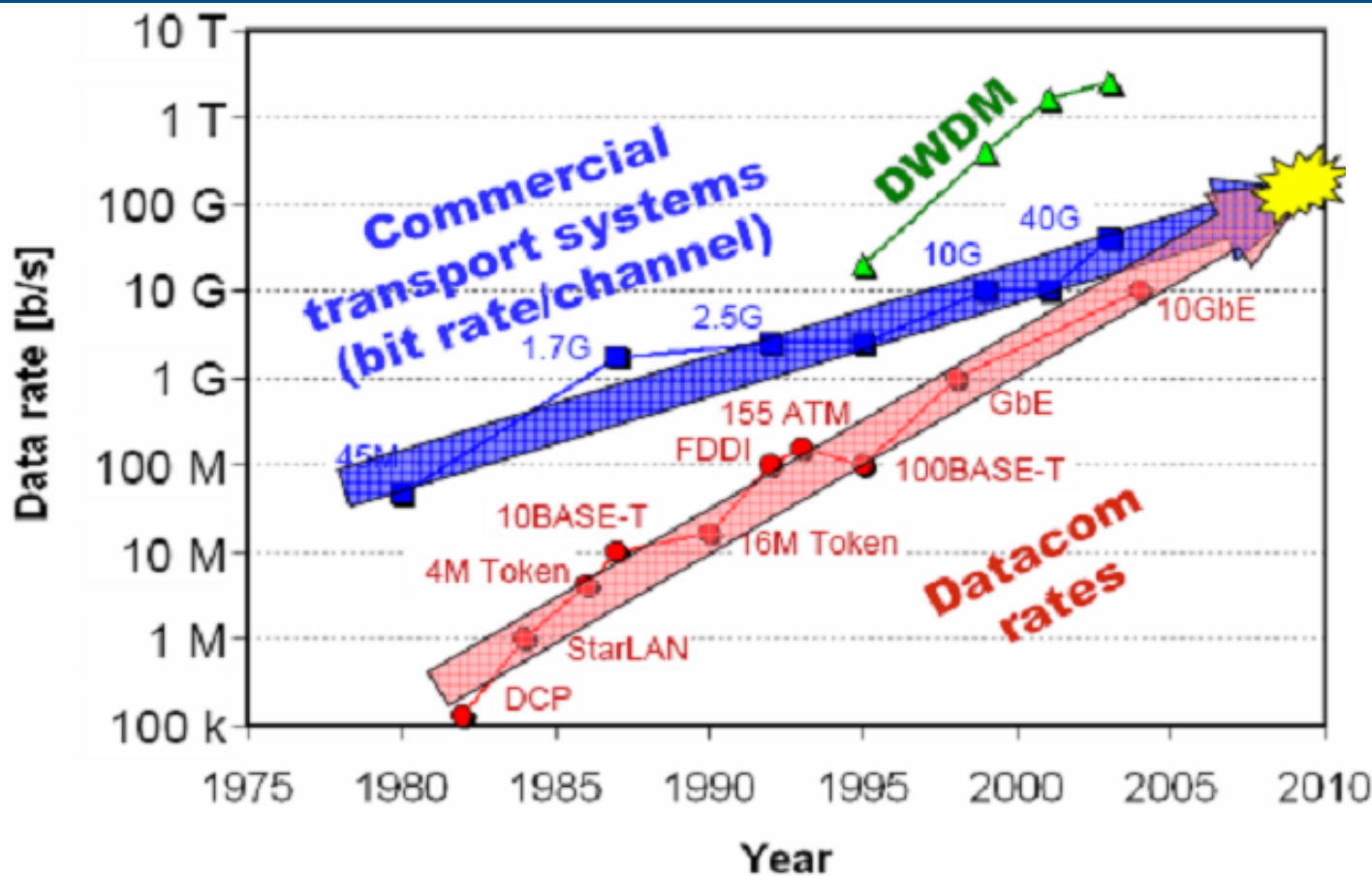(intel)

Technical Feasibility:
Si Photonics Recent Progress

*This is not exhaustive

Pioneering work by Dr. Richard Soref (early 1980's)

Integrated APD+TIA
UT

Inverted Taper
NTT, Cornel

Raman λ Conv.
UCLA

Modeled GHz PIN Modulator
Surrey, Naples

DGADC
Surrey

PBG WG <25dB/cm
IBM

Polarization Indep. Rings
Surrey

Raman Laser
UCLA

>GHz MOS Modulator
Intel

30GHz Si-Ge Photodetector
IBM

PBG WG <7dB/cm
IBM, FESTA, NTT

QCSE in Si
Stanford

Stim-Emission
Brown

CW Raman Laser
Intel

10Gb/s Modulator
Intel, Luxtera

1.5Gb/s Ring Mod.
Cornell

39GHz Si-Ge Photodetector
Univ. Stuttgart

PBG WG <3db/cm
NTT

Broadband Amplification
Cornell

E-O effect strain-silicon
DTU

Hybrid silicon Laser

2002   *2003*   *2004*   *2005*   **2006**

Device performance making significant advances

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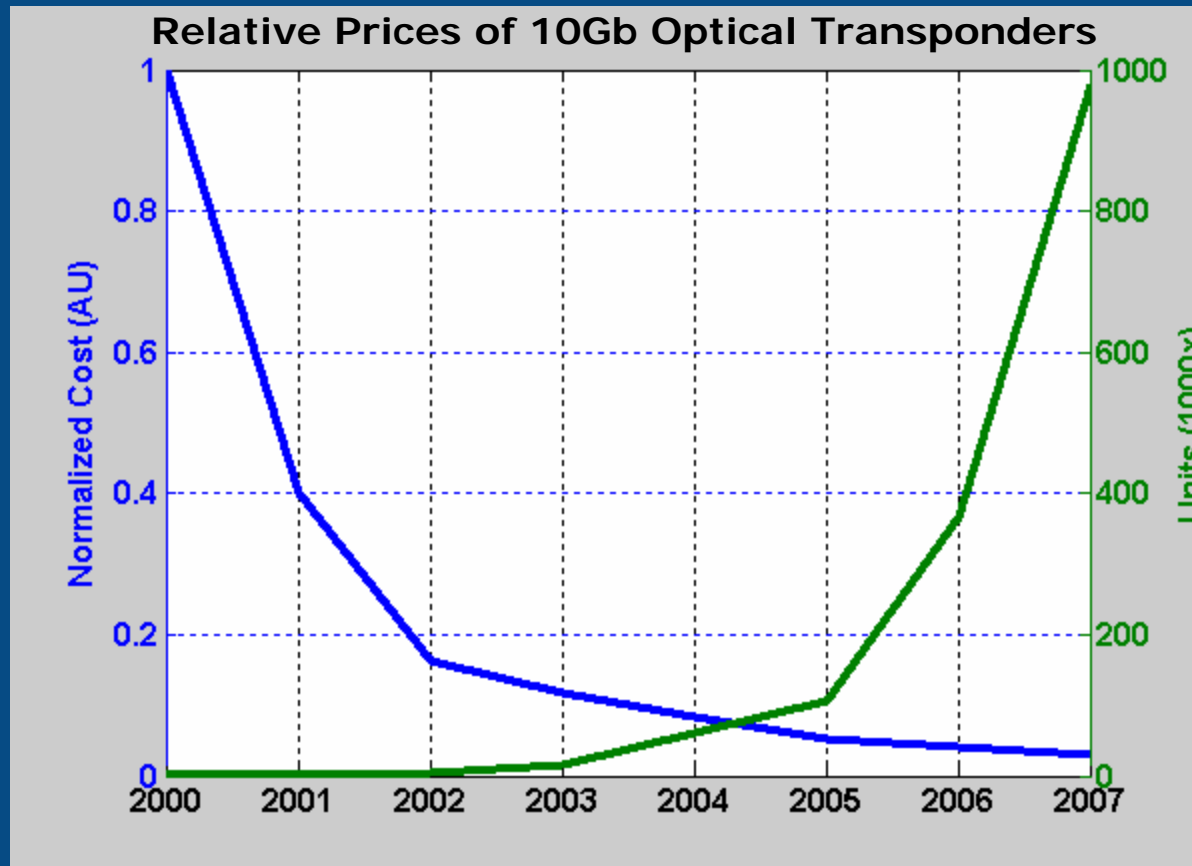# Datacom will drive next generation technologies

- Traditionally Datacom has trailed Telecom

- 100GE will be a disruptive technology.

- 100GE will be an inflection point, Datacom becomes the driver of technology.

Cost Effectiveness of the solution is key for deployment

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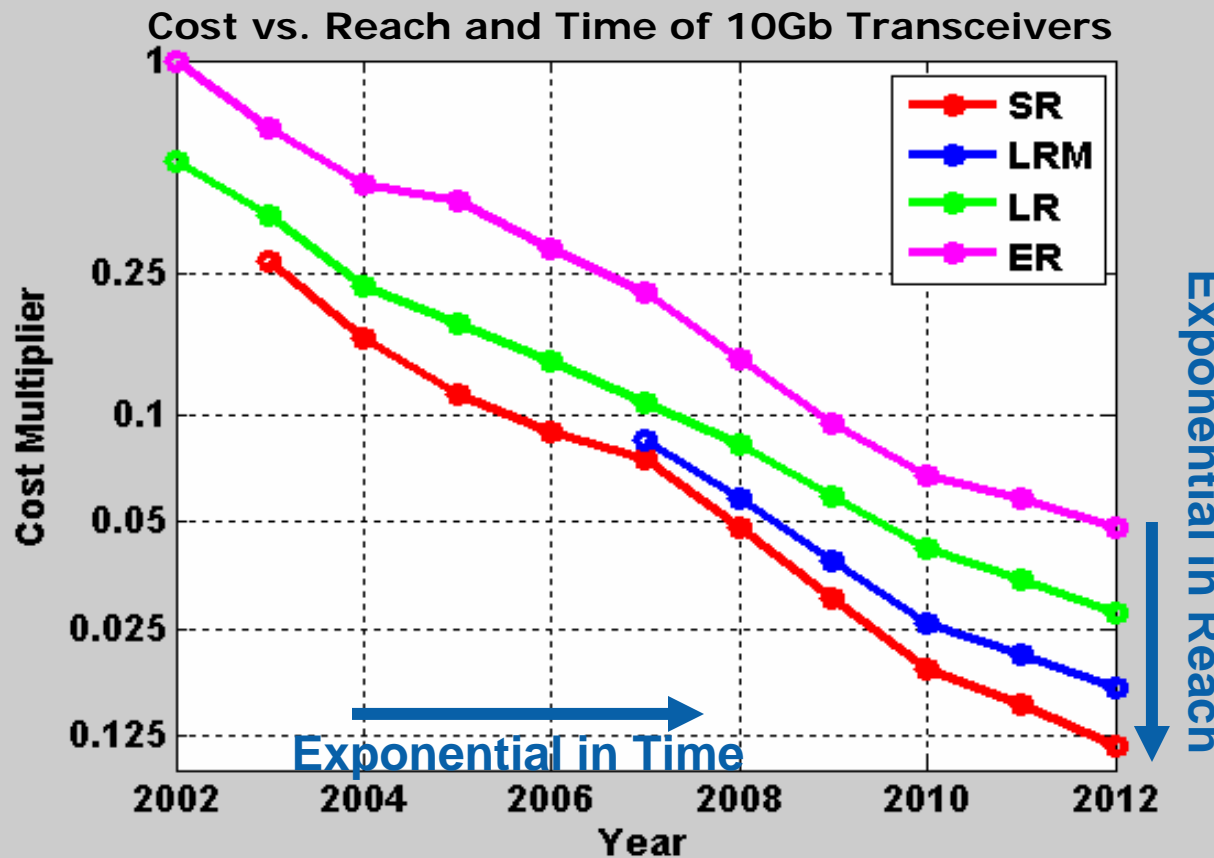
Cost vs. Units 10GE

Relative Prices of 10Gb Optical Transponders

- Volume has increased exponentially
- Cost has dropped exponentially

Increased unit volume results in lower costs

Cost vs. Reach

Cost vs. Reach and Time of 10Gb Transceivers

Legend:
- SR (red)
- LRM (blue)
- LR (green)
- ER (magenta)

Y-axis: Cost Multiplier (1, 0.25, 0.1, 0.05, 0.025, 0.125)

X-axis: Year (2002, 2004, 2006, 2008, 2010, 2012)

Exponential in Time

Exponential in Reach

- Short links are cheaper.
- Cost Multiplier between long and short links has remained 'constant'
- Shorter links will drive volume and cost

Shorter reach optics (datacom) = Lower cost

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100G Ethernet Considerations

- Lower Speed solutions are less interesting
  - 40GbE for backplanes is available today
    - 4 Lanes 10G-KR
  - Won't meet platform requirements by time standards are released (4+ years)
- 100GbE Solution Possibilities
  - 10 lanes of 10G BASE-KR
    - Routing problem would be quite severe
  - 4x25Gb 'KR' like link
    - CMOS implementations will be a challenge
    - Trace routing problem reasonable
  - 5x20Gb 'KR' like link
    - CMOS implementations still a challenge
    - Trace routing problem reasonable

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100GE Optical Considerations

- Optical backplane on the horizon
  - time until roll out still unclear?
- Both a 4x25 and 5x20 seem equally doable.
- 5x20 may be easier because of VCSEL and CMOS limitations
  - A 5x lane split seems un-natural.
- Low number of links (4-5) links
  - high data rate CMOS and Lasers
  - large amount of equalization required for backplane
  - Relaxed routing requirements.
- High (8-10) links
  - Can leverage current KR specs.
  - Routing and connectors become an issue.
  - Number of Lasers becomes costly.

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Tradeoffs for # of lanes Proposal

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Summary

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Backup

Drive optics to high volume & low cost

Optical : Copper

Metro & Long Haul
0.1 – 80 km

Rack to Rack
1 to 100 m

Chip to Chip
1 – 50 cm

Board to Board
50 – 100 cm

Billions

Millions

Thousands

Volumes

Decreasing Distances→

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