PENNSTATE CICTR Center for Information and Communications Technology Research

IEEE 802.3 Higher Speed Study Group

Nexans

Towards 100G over Copper

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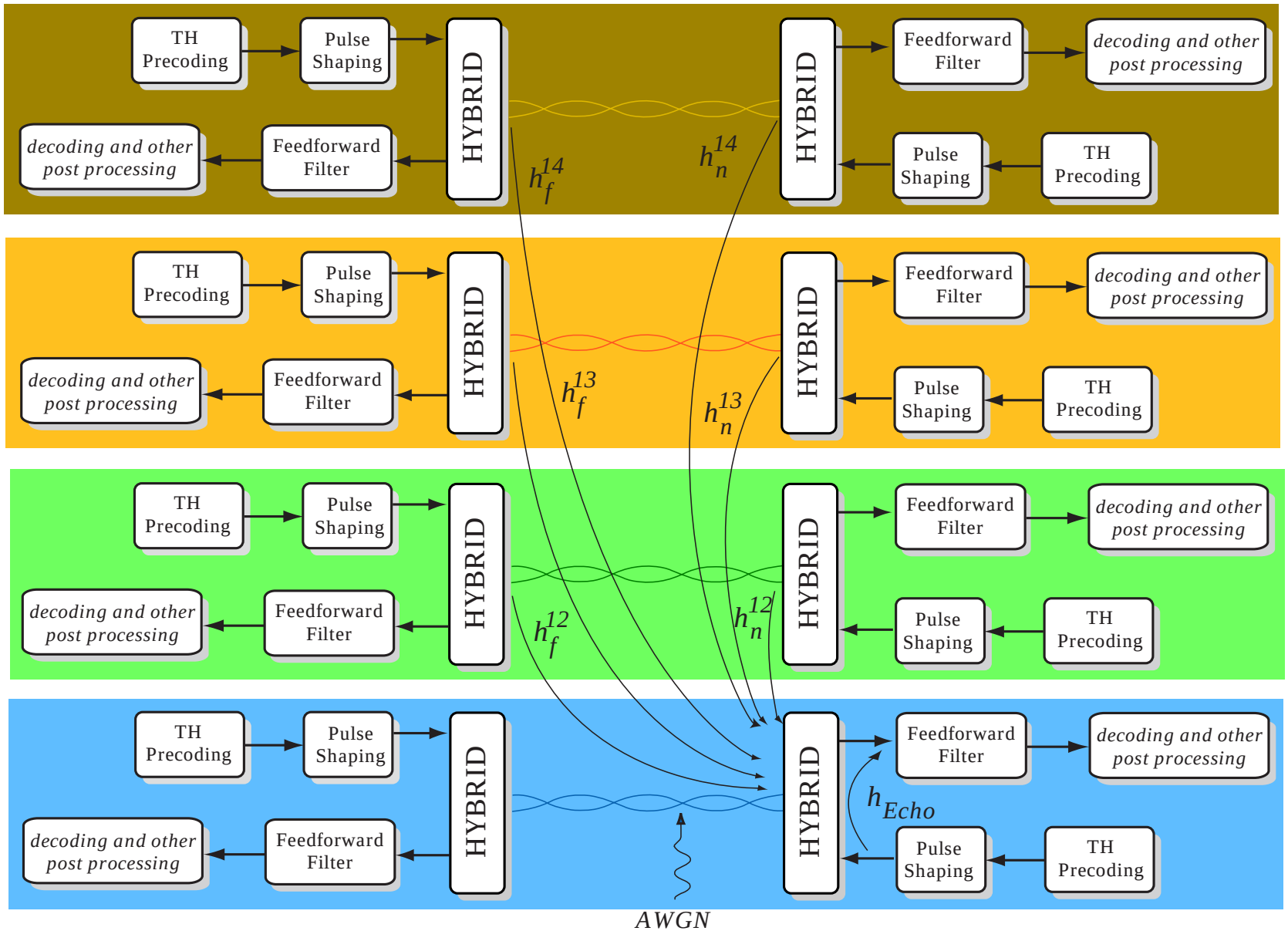
Outline

- Capacity calculation
  - →CAT-7A 50m and 100m
- Pre-coding
  - →Tomlinson-Harashima pre-coding (THP)
- Trellis coded modulation (TCM)
- Low-density parity check codes (LDPC)
- Interference cancellation
  - →Echo cancellation
  - →X-Talk cancellation
- Conclusions


TH Precoding
Pulse Shaping
HYBRID
Feedforward Filter
decoding and other post processing
h_f^{14}
h_n^{14}
h_f^{13}
h_n^{13}
h_f^{12}
h_n^{12}
h_{Echo}
AWGN

Shannon Capacity Calculations

- Using measured data on CAT-7A, channel capacity is presented in
  - → Theoretical AWGN Channel: $C = W \log_2\left(1+\frac{S}{N}\right)$
  - → Single-carrier capacity assuming coding gain $g_c \sim 5$ dB and SER=10^{-12}.
  - → Water-filling capacity assuming a coding gain of approximately 5dB and SER=10^{-12}:

$$b_m = \max_{g_n} \sum_{n=1}^{N} \frac{1}{2} \log_2\left(1+\frac{\mathrm{SNR}_n}{\Gamma}\right)$$

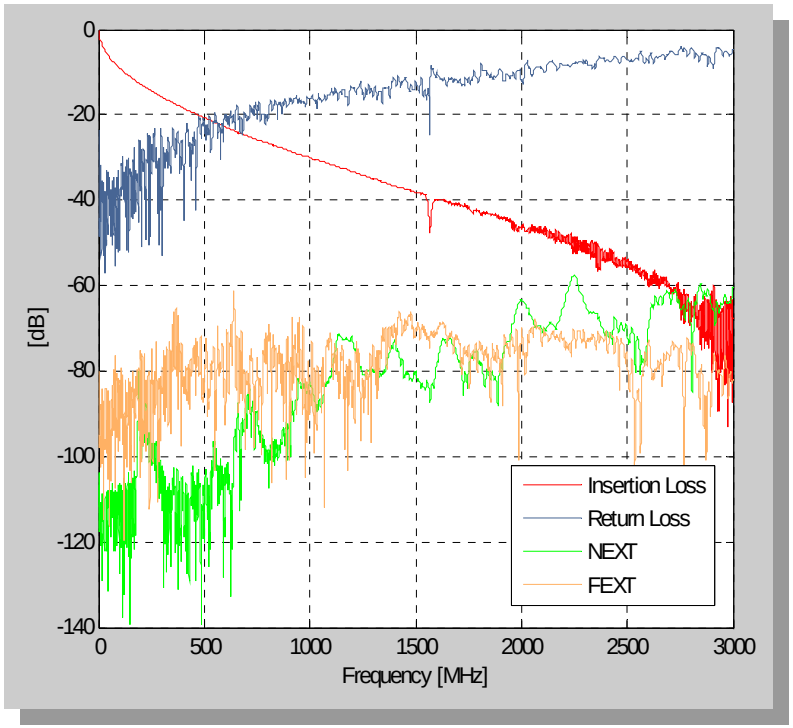
$$s.t \quad \sum_{n=1}^{N} \varepsilon_n = N\bar{\varepsilon}_x$$

Capacity Calculations

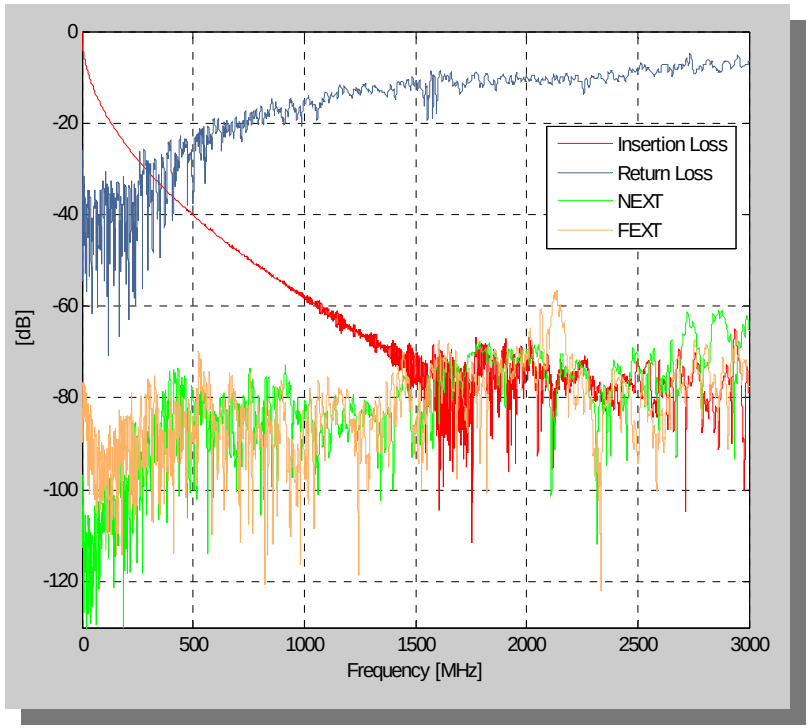
Modulation	M-PAM
Pulse Shaping	Raised Cosine
Interference Canceller	N.L.M.S
Launch Power	10 dBm
Mean Background Noise Level	-165 and -150 dBm/Hz
Load Resistance	100 Ω

Characteristics of CAT-7A

CAT-7A: 50m



CAT-7A: 100m

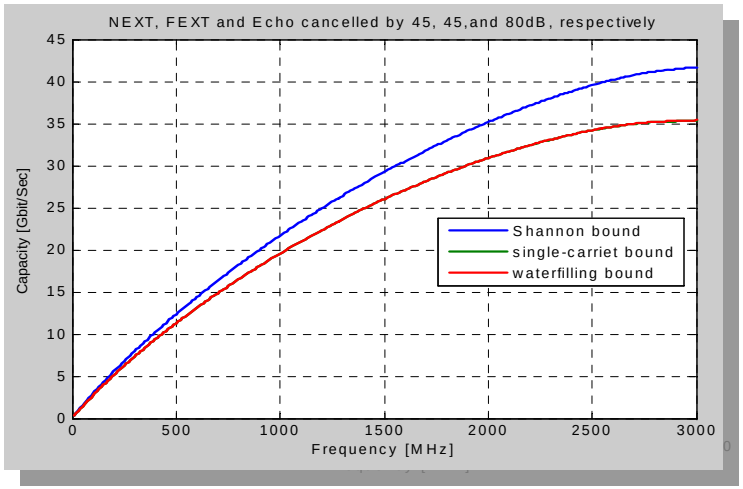


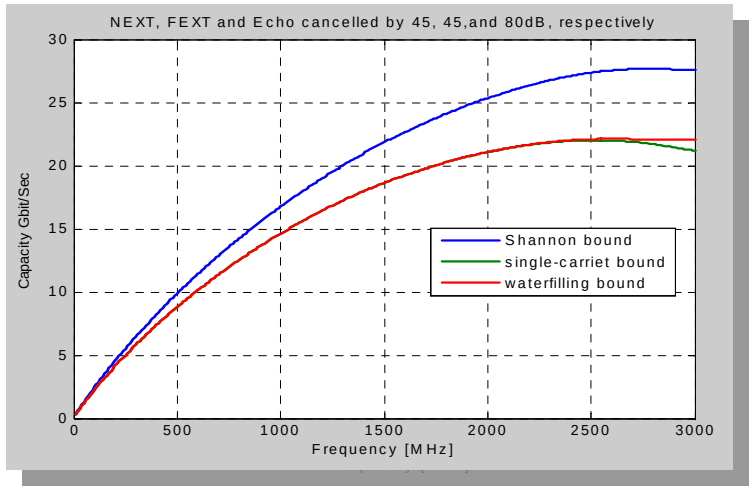
Shannon Capacity per Pair on CAT-7A

$N_0 = -165\ dBm/Hz$

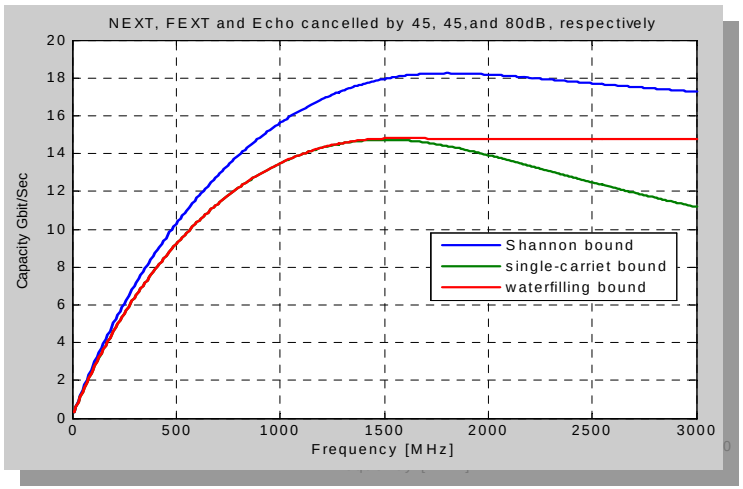
$N_0 = -150\ dBm/Hz$

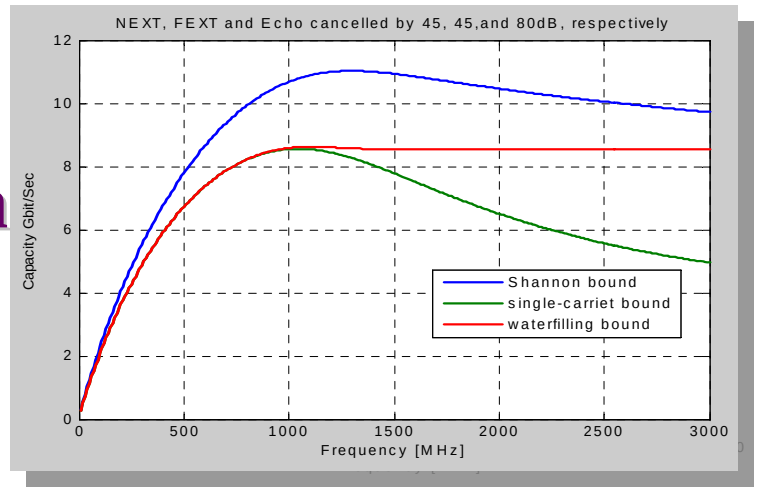
50 m





100 m





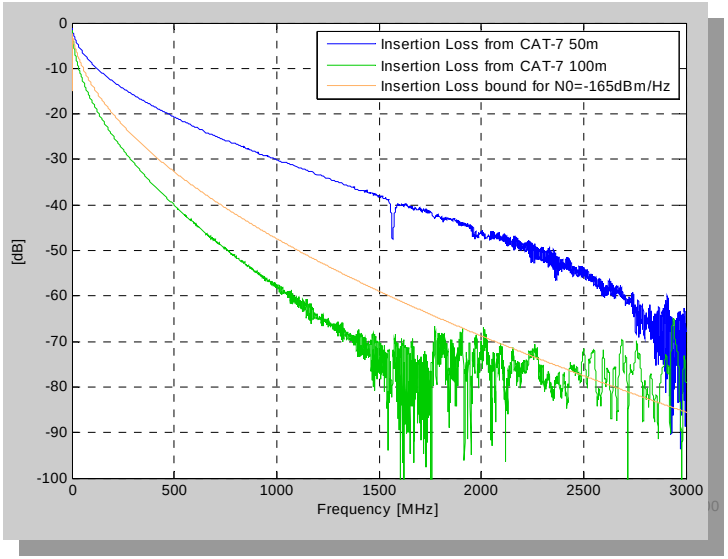
Towards 100G/100m

- There is a gap between current spectrum of 100m cable and the estimated lower bound.
- Assuming optimum bandwidth of about 2.5GHz, symbol rates up to 5 GSym/Sec are possible for 25Gbps on each pair; a total of 100 Gbps bit rate.
- To achieve 25Gbps, each symbol should carry at least 5 bits; 32-PAM. This complicates A/D and D/A conversions; thus for now; more than a few level PAM is not practical [1].

> "*The implementation of a 10GBASE-T PHY chip in a commercially available CMOS process requires significant innovation in communication theory, analog mixed-signal design, and DSP design*"

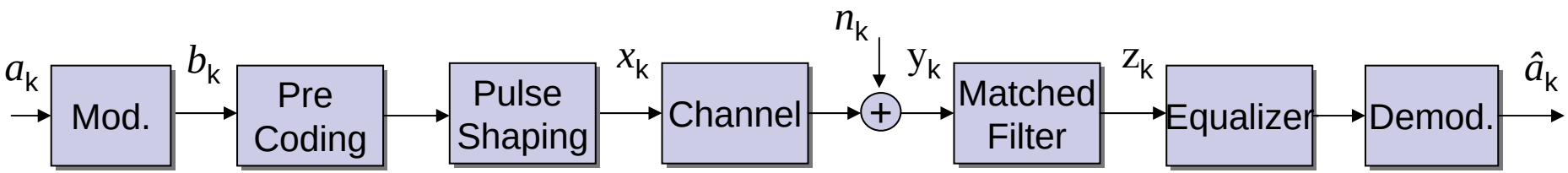
- Work is underway on VLSI implementation of high-speed data converters:

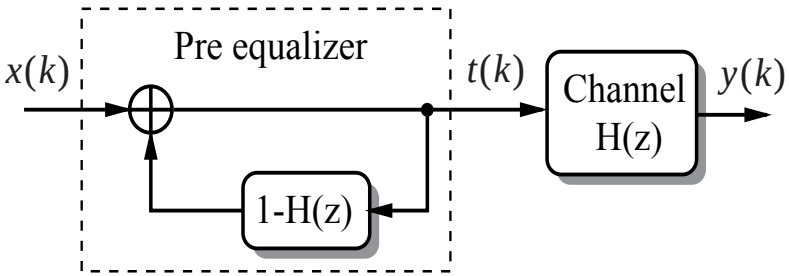
  "20 GS/s 8 b ADC with a 1 MB memory in 0.18 µm CMOS", Poulton et. al., Agilent, IS SCC'03.

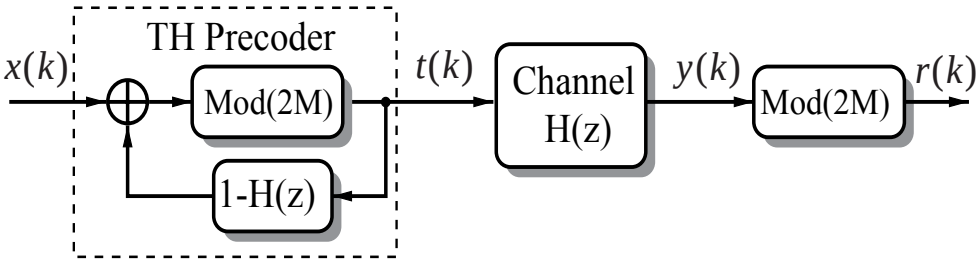


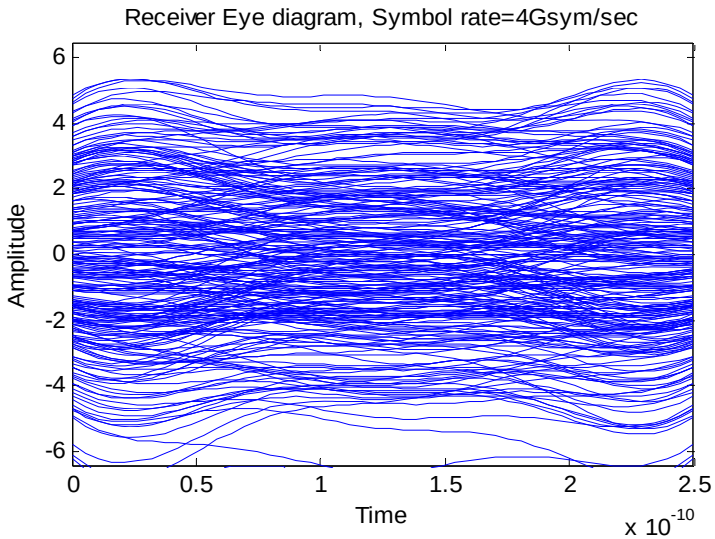
[1] Dr. Joseph N. Babanezhad, "10GBASE-T PHYs Pose Challenges to Designers", Comms Design, Feb 25, 2004.

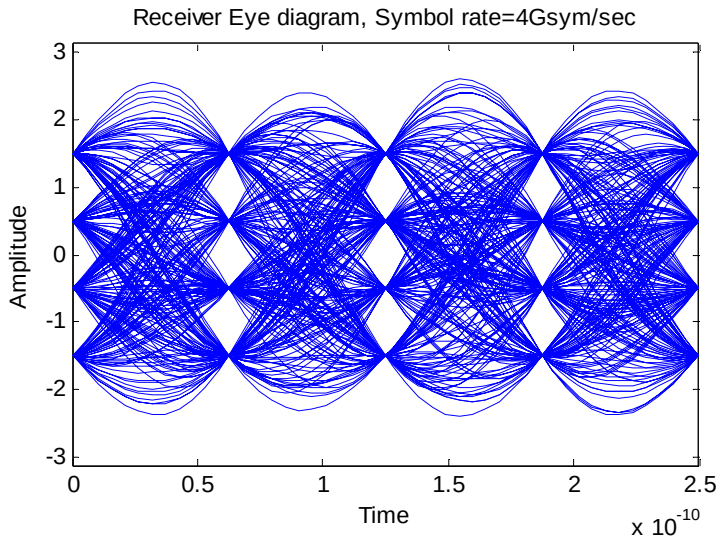
Pre-coding: TX Equalization











Pre-coding: TX Equalization

- With this method the received signal is ISI-free, so ideal-channel decoding can be performed at the channel output. The performance achieved is equivalent to the performance that would be obtained, provided ISI could be perfectly equalized at the receiver with decision feedback equalization.

- It can reduce error propagation and allows us to use current capacity-achieving channel codes, like LDPC in a natural setting.

Note:

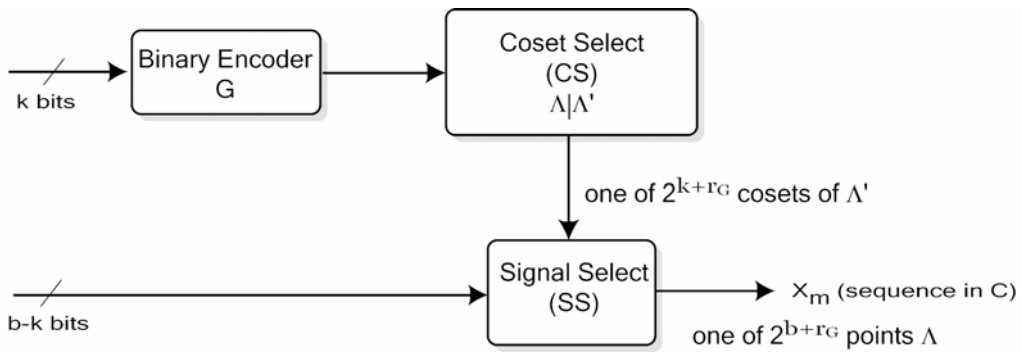
- TH pre-coding, requires storing a number of non-integer valued (analog) past transmitted samples.

Trellis Coded Modulation

- The redundant coded information selects signals from expanded constellation.
- Preserves bandwidth efficiency.
- Combines coding and modulation.
- Protects the most significant bits (MSB's) by set partitioning and the least significant bits (LSB's) by increasing Euclidean distance.

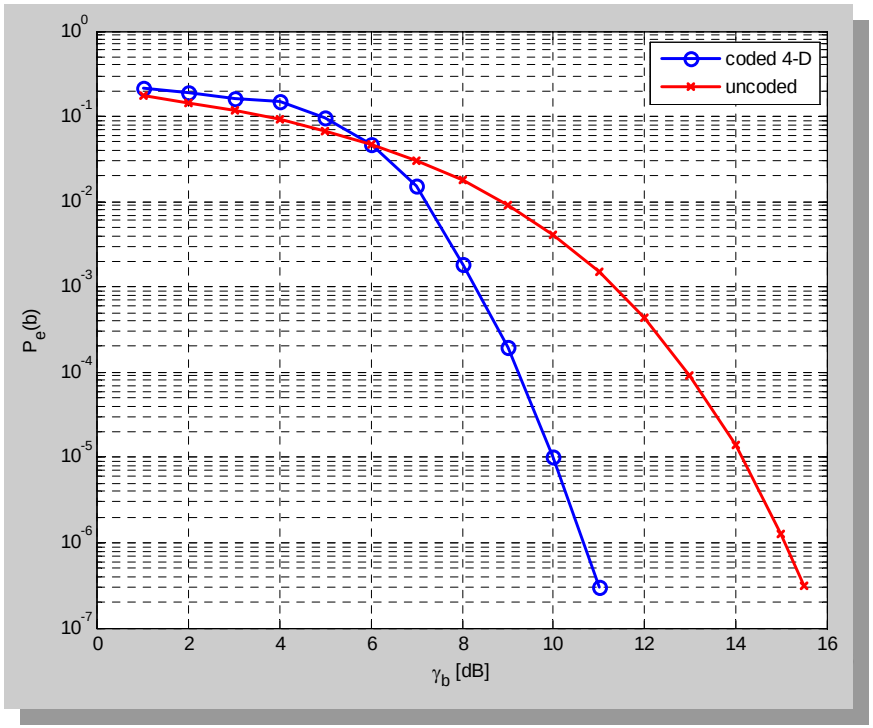
- 4-D TCM

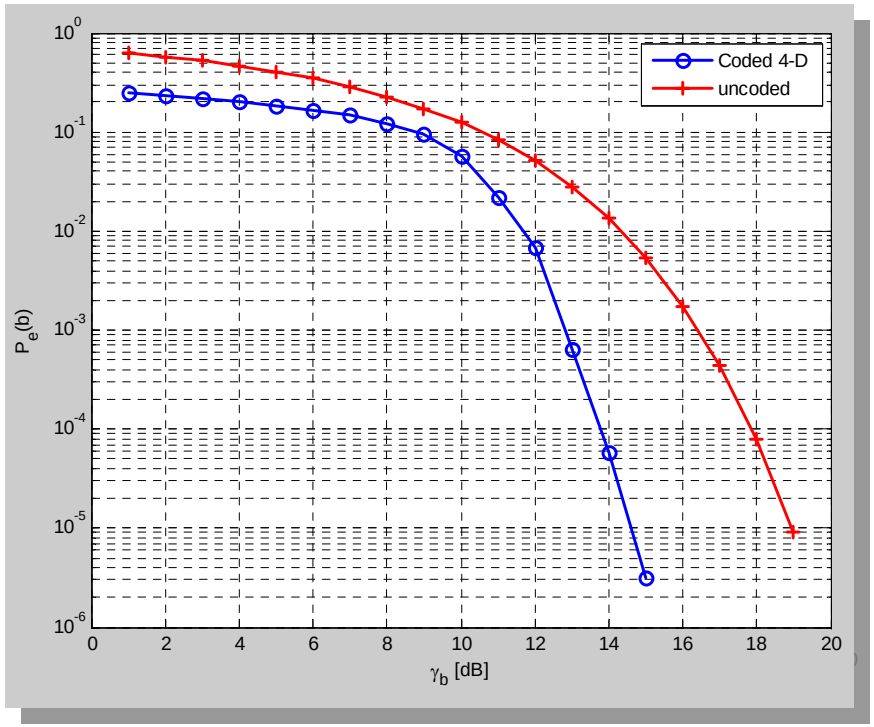
  $\rightarrow \mathbb{Z}^4/\mathbb{D}_4/\mathbb{RZ}^4/\mathbb{RD}_4/\ldots$



Trellis Coded Modulation, Results

- 4-D Trellis (Z^4 or 2×QAM)
- Two 4-D TCM have been evaluated for 50m CAT-7A
  - →35Gbps, 7 bits per symbol
  - →55 Gbps, 11 bits per symbol



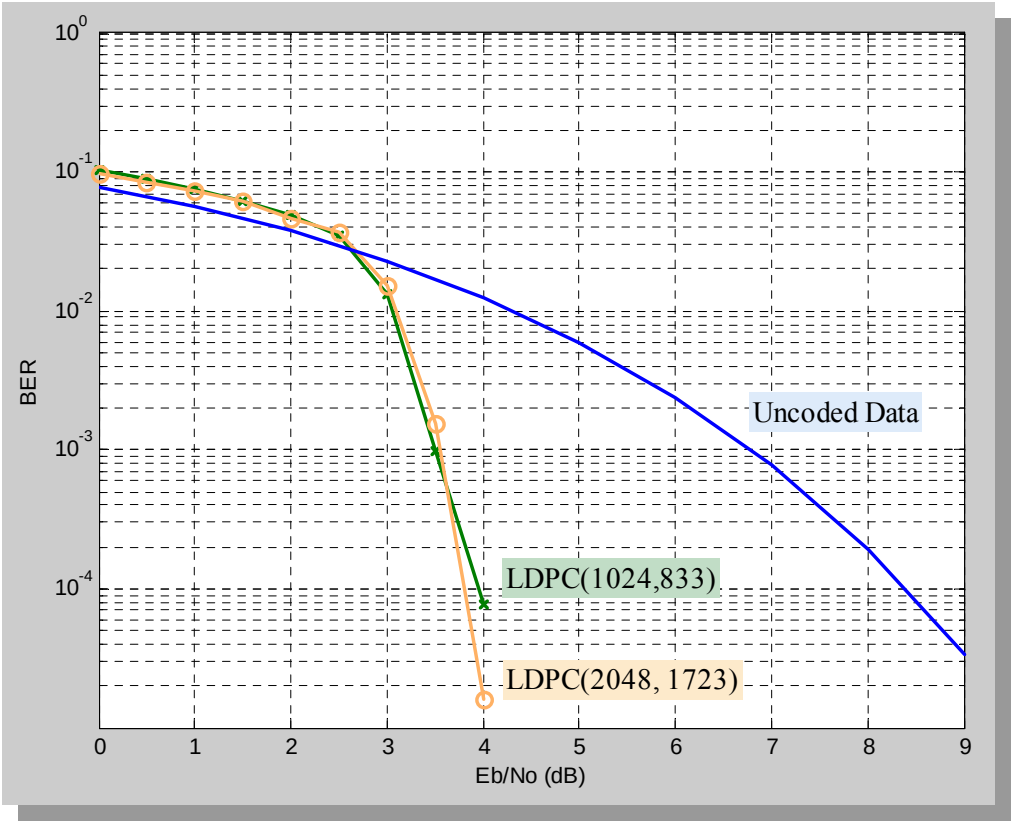


Low-Density Parity Check Code

- Linear error-correcting code that has a parity check matrix H with a small number of nonzero elements in each row and column.
- Approaching Shannon capacity
  - → Irregular LDPC code with a code length 1 million. (Richardson:1999)
  - → Another design by (Chung:2001), 0.0045 dB away from capacity
- Suitable for parallel implementation
- With LDPC codes, error detection comes for free.
  - → This can be used to dynamically halt the iterations.
  - → No outer error detecting code is needed.

LDPC Results

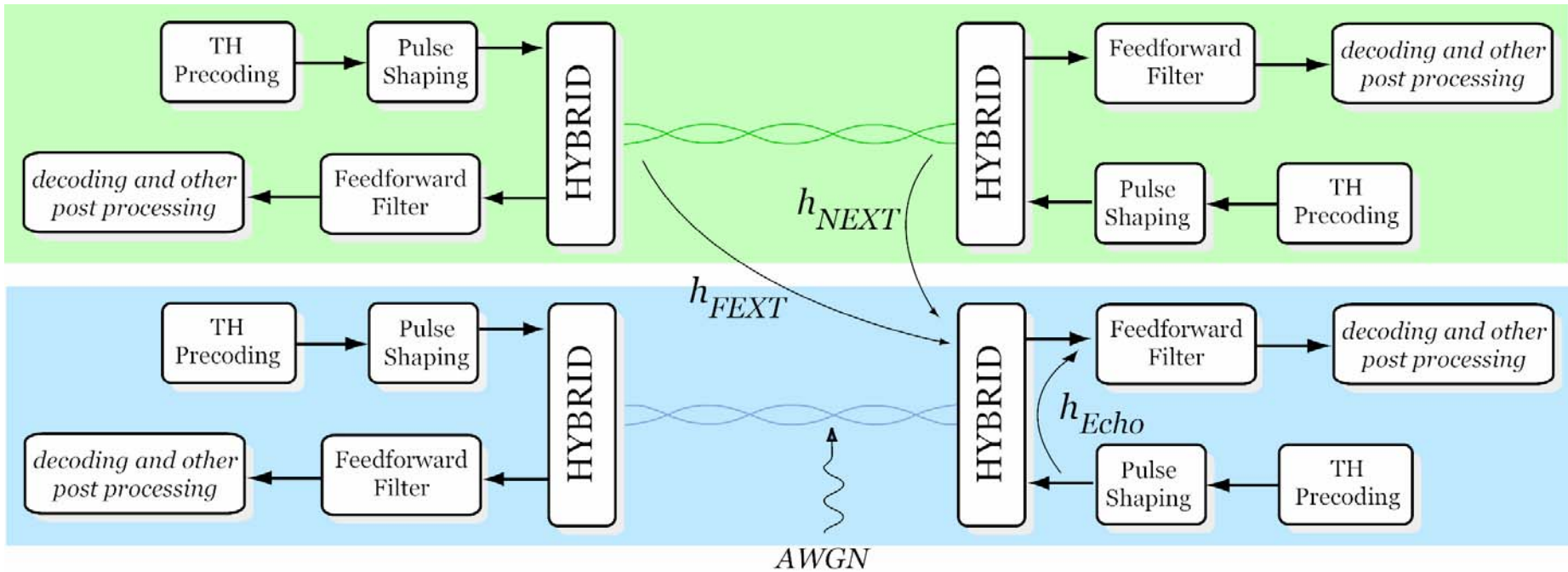
- LDPC (1024, 833) and LDPC (2048, 1723)



- Increasing the block size improves performance, substantially.
- However, long data frames introduce latency that may not be acceptable.

Interference

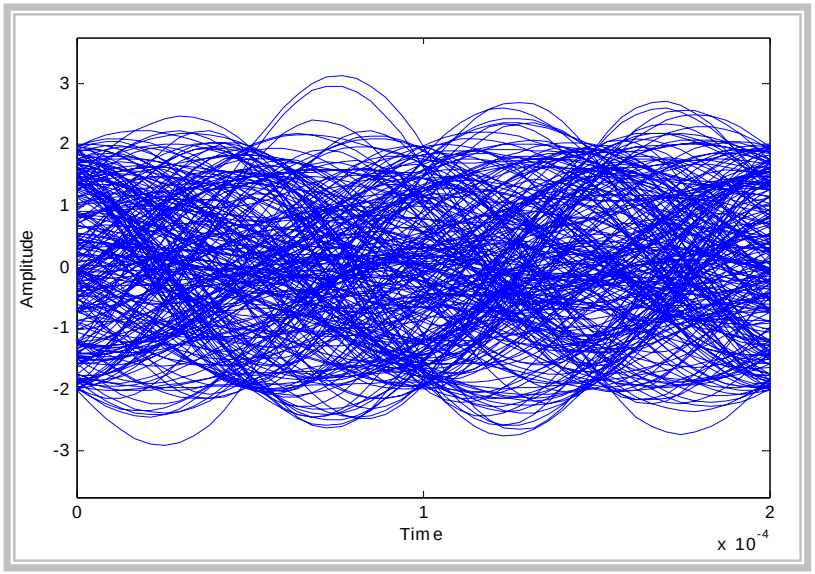
- Interference sources
  - → Echo
  - → FEXT
  - → NEXT
  - → Due to the great shielding, Alien X-talk is negligible for CAT-7A cables.

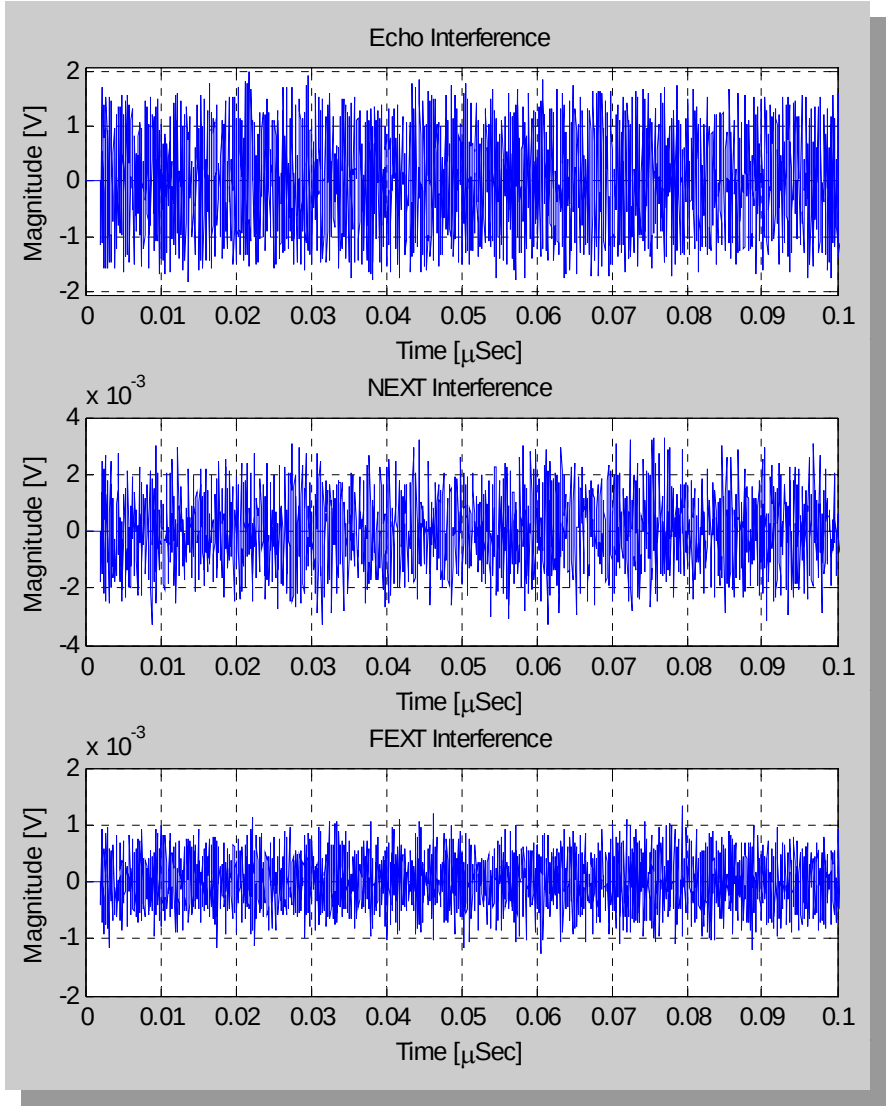


Interference

- Major source of interference is Echo.
- The interferences caused by FEXT and NEXT are well below the signal levels.

→ $E_x/E_{NEXT} = 66.1$ dB
→ $E_x/E_{FEXT} = 74.9$ dB
→ But $E_x/E_{Echo} = 9$ dB

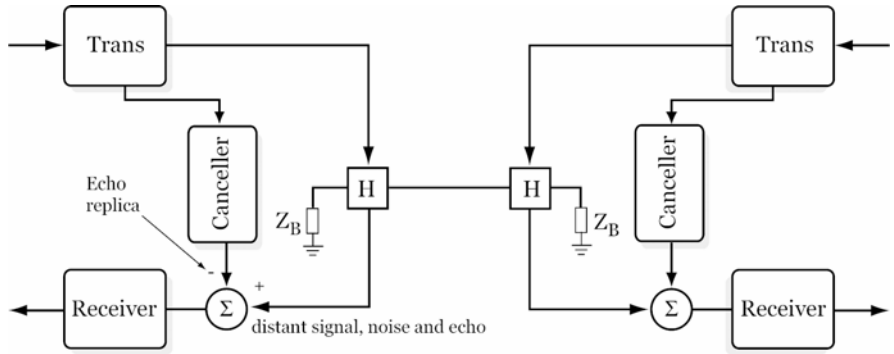




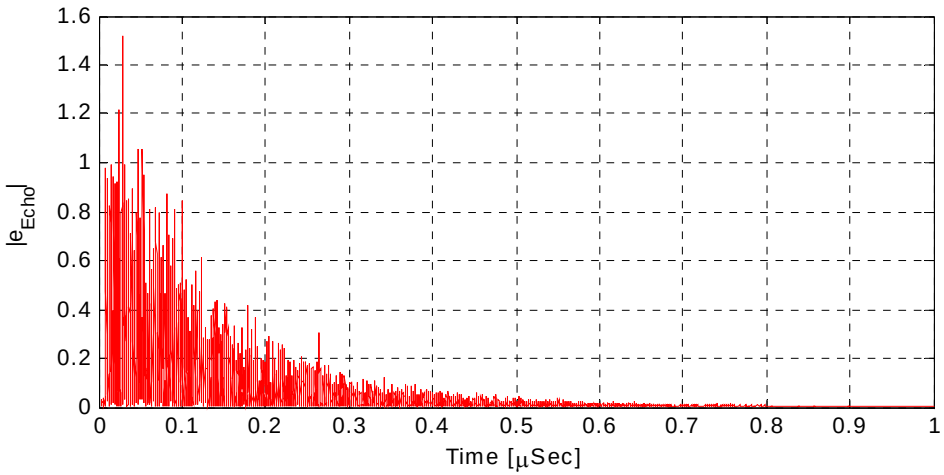
V_{pp}=3 volts, Symbol Rate = 5 Gsps on CAT-7A 50m.

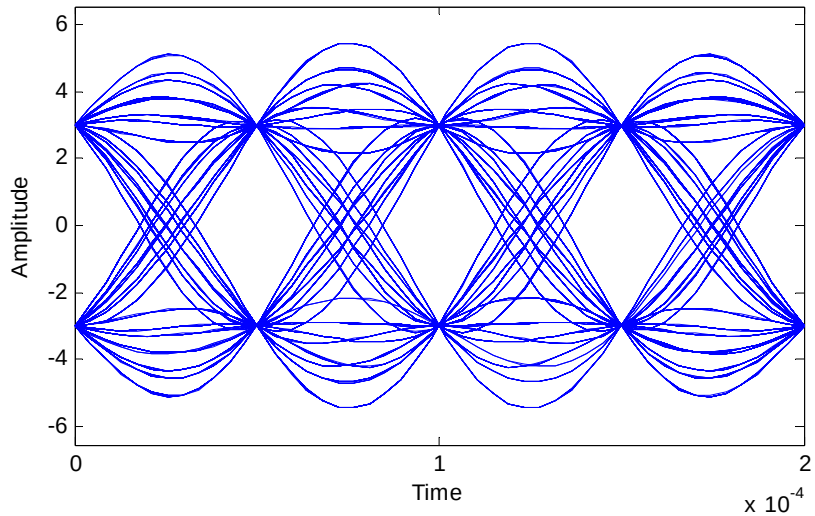
Echo Canceller

- Data-driven echo canceller is used, where the driving signal is the data stream at the input to the local transmitter rather than the line signal at its input (training).



- The well known *normalized least mean square* (NLMS) is used.

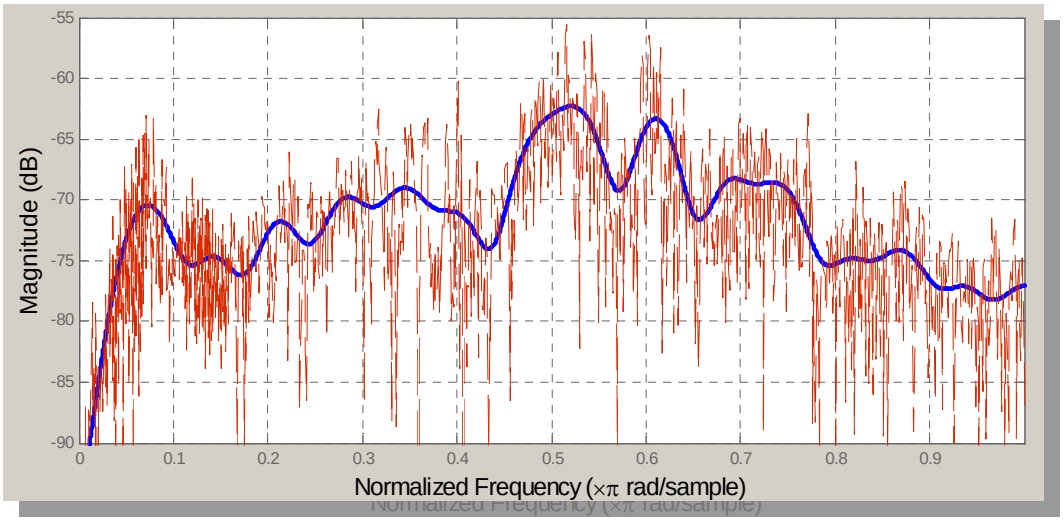




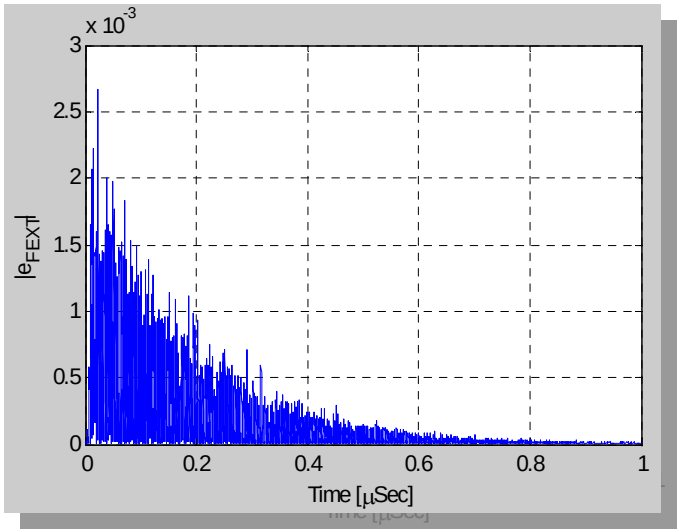
256 taps, E_x/E_{Echo}= 67.9 dB

FEXT & NEXT Canceller

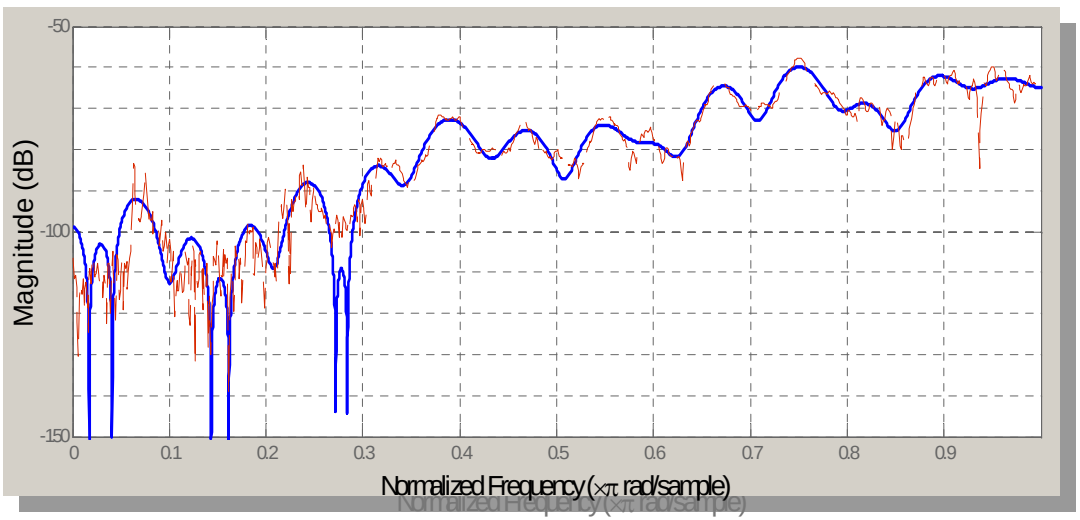
Fitted FIR model



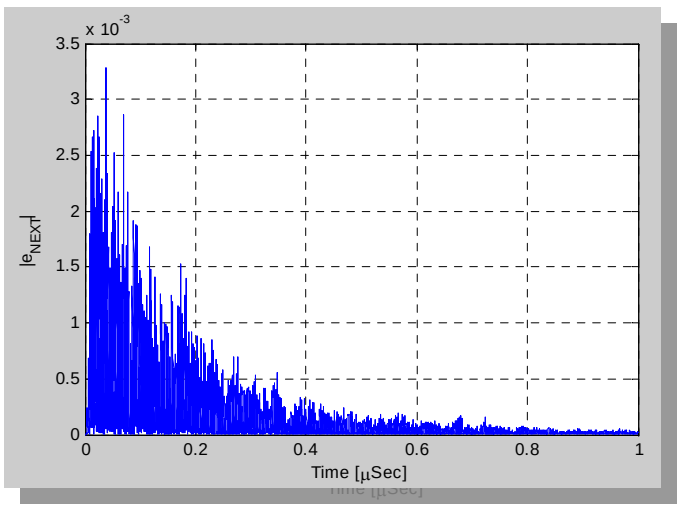
Adaptive filter's error (256 taps NLMS)



Fitted FIR model



Adaptive filter's error (256 taps NLMS)



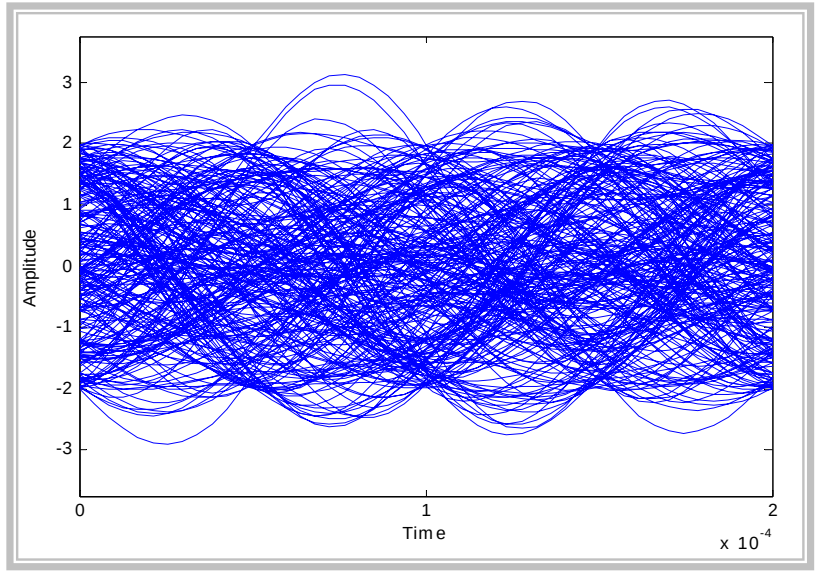
Interference Cancellation, Results

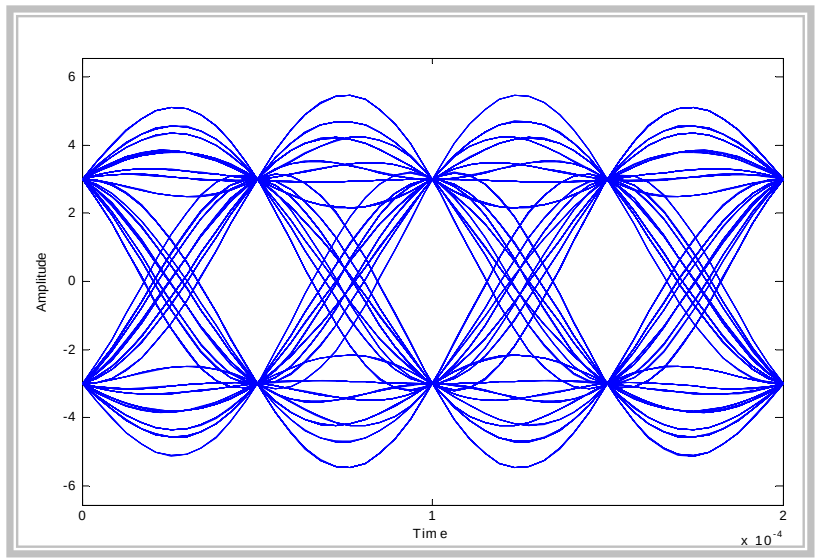
- All filters are adaptive normalized LMS.

- Echo Canceller
  - → 256 taps
  - → E_x/E_{Echo}=9.1dB before and 107 dB after cancellation
  - → Total attenuation>90dB

- NEXT Canceller
  - → 256 taps
  - → E_x/E_{NEXT}=66.2dB before and 107.9dB after cancellation
  - → Total attenuation>41dB

- FEXT Canceller
  - → 256 taps
  - → E_x/E_{FEXT}=75.0dB before and 108dB after cancellation
  - → Total attenuation>33dB





Conclusions

→ Capacity calculations done for different lengths CAT-7A cable show maximum cable length to deliver 100 G is less than 100 meters.

With our assumptions, the capacity of 100 m cable is about 70 Gbps and the capacity of 50 meters cable is > 100 Gbps. We expect that the maximum length to deliver 100 G is somewhere between 70 to 80 meters.

→ Pre-coding schemes prove useful for > 10G high-rate data transmissions, as well.

→ Designed multidimensional trellis-coded modulation and its performance evaluated in different scenarios.

→ Designed LDPC and assessed performance in some cases.

→ Echo, FEXT & NEXT were included in the model and proper cancellation applied. Our simulations verified that Echo is the major source of interference in these applications.

Future Plans

- As for 40G over 100m, this appears quite feasible.
- We intend to keep on working toward reaching 100 Gbps on 100m, to identify potential, practical improvements needed beyond CAT-7A.