

A blurred photograph of several people in business attire walking in a hallway. In the upper right corner, there is a sign with the numbers '2' and '3' in white on red circular backgrounds. The overall scene is out of focus, suggesting movement.

# 100GbE Components for SMF Reaches IEEE 802.3 Higher Speed Study Group

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# Outline

- **System Vendor View**
- **Transmitter Side Technology**
- **Receiver Side Technology**
- **Electrical Interface**
- **CTBI vs. APL**
- **Conclusion**

# System Vendor View

- **As a system vendor developing 100GbE optical transport systems. We are following with great interest the evolution of the 100G client side interface through the IEEE HSSG, and other industry meetings targeting this area of development.**
- **The timely development of a standard for client side interface is needed to validate our long haul segment design which has crossed the threshold from the Research phase to the product development phase, and the need to interoperate with external 100GbE interfaces and network elements.**
- **Efforts to establish a MSA among component vendors to create 100GbE client side module should be accelerated to iron out remaining issues while finalizing the physical form factor.**

# Transmitter Side Technology (1)

## Initial Implementation

- We are pleased to see the progress achieved so far by component vendor on key issues, such as a movement toward a consensus that the transmitter is a 4x25G WDM architecture which in our view is a solution that is least susceptible to component reliability issues compared with other solutions like 10x10G or 5x20G proposed early on.
- 1312nm center wavelength is also something that we support to reduce dispersion effect compared to 1550nm wavelength.
- Today's technology in our view support such architecture by approaching this design problem from two ends, chip and package, combining them to achieve modulation capability at 25G
  1. Using EML chip technology available for 40G rate today.
  2. Integrating laser driver into TOSA to reduce the Rise Time to improve link margin for 10km links.
  3. Using XMD TOSA and ROSA packaging technology available for 10G rate today.

# Transmitter Side Technology (2)

## The Path to Next Gen Design

- Cost reduction and design flexibility are two items the component vendors rank high on their list.
- 1312nm center wavelength provides flexibility for laser technology development at 25G rate and a path to next generation module design.
  1. VCSEL device
  2. Uncooled Quantum Dot DFB
  3. EML arrays with micro TECs

# Receiver Side Technology

- For 10km reach, PIN based receiver with similar approach to the transmitter of using 40G chip design and combine it with 10G package (XMD) design.
- For 40km reach, PIN receiver with SOA is a feasible solution to start and for future design the use of 25G APD will achieve the performance needed and eliminate the use of SOA.
- 400GHz spacing will provide the flexibility to reduce the design requirements of the SOA, as opposed to wider channel spacing.

# Electrical Interface

- **Pluggable module is a must.**
- **Electrical connector technology today can deliver such solution.**
- **The module should be a simple E/O, O/E converter with PMA/PMD interface, with coding and decoding shifted to the board.**
- **Heat sink integrated with the module case (X2, Xenpack like design).**
- **40GbE can be covered with the same module with Rate-Select option for multiple Receiver Bandwidth settings.**

# CTBI vs. APL

→ Both CTBI and APL offer good solutions with attractive features, although we see some road blocks for the APL option that can impact the length of its development cycle such as:

1. APL control protocol needs to be specified
2. APL needs a new-generation Silicon technology that usually comes with increased power dissipation which can be a challenge for board density
3. We're not sure of the impact of APL on 100GbE over OTN and Backplane interface
4. APL has a high level of complexity.

→ We can support CTBI for the following reasons:

1. This implementation can be supported with today's chip technology (faster development cycle).
2. More flexible with Virtual Lanes architecture which enable de-skewing of parallel bus, has very low overhead and it's independent of frame size
3. Single PCS can work with different PMDs
4. Can be used to interconnect backplane
5. Potential for lane error detection scheme
6. Works well with the optical interface we're recommending.



# Conclusion

- An overview has been provided on how a system house sees the potential client side interface for 100GbE can be implemented in the short term, and how future component development can fit well with the architecture being decided today.
- Although the IEEE will not develop an MSA, we believe the industry should initiate an effort in an appropriate venue, we are willing to participate in such MSA effort to provide a system vendor feedback to the other MSA participants as we did in the past by being one of the founding members of both the XFP and XFP-E MSAs.
- We have also stated our initial support for the CTBI solution proposed at previous HSSG meetings.
- Finally, our position stated in this presentation can change to support new initiatives if new data or new architecture can demonstrate that they can meet our objectives.



Thank You