

10GBASE-KR for 40G Backplane

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Outline

This contribution discusses,

- Performance based on 10GBASE-KR Std**
- Theoretical Limit (Saltz SNR) and Time Domain Simulation**
- Performance Improvement**
- Summary**



40G Backplane

A Single Lane, 10GBASE-KR 802.3ap, Clause 72

Main Requirements

Signaling: 10.3125Gbaud(+/-100ppm), 2PAM

Transmitter: 1200mVpp Max, 3-tap Pre-Equalization, Total Jitter < 28%UIpp

Return Loss: 9dB 50M ~ 2.5GHz, 12dB/dec. from 2.5 ~ 7.5GHz

Insertion Loss: < ILmax(f), 24.5dB at 5GHz, Informative

Cross-talk: Defined as ICR, Ratio of IL to Power sum crosstalk, PSXT

$ICR \geq ICR_{min} = 23.3 - 18.7 \log(f/5G)$, Informative

BER: Better than $10^{**(-12)}$

Receiver Interference Tolerance

Broadband noise: 5.2mVrms(5GHzband)

Jitter UI p-p: 13% (random), 3.5%(DCD), 11.5%(sinusoidal)

Total 17 channels are uploaded to verify the system performance.



Channel discussed by 10GBASE-KR

TYCO, 7 Channels

Description		Channel Name	Line Card	No. Connectors	Backplane	Total Length	Loss @ 5GHz
TYCO 7 cases [1]	Signal path One FEXT Two NEXT	Case1	10" Nelco4000 13SI	2	20" Nelco4000 13SI	40"	22.9dB
		Case2	10" Nelco4000 13	2	20" Nelco4000 13SI	40"	24.1
		Case3	10" Nelco4000 6	2	20" Nelco4000 13SI	40"	26.6
		Case4	6" Nelco4000 13	2	20" Nelco4000 13SI	32"	19.0
		Case5	6" Nelco4000 13	2	10" Nelco4000 13	22"	14.2
		Case6	6" Nelco4000 13SI	2	10" Nelco4000 13	22"	16.4
		Case7	6" Nelco4000 13SI	2	1" Nelco4000 13SI	13"	12.9

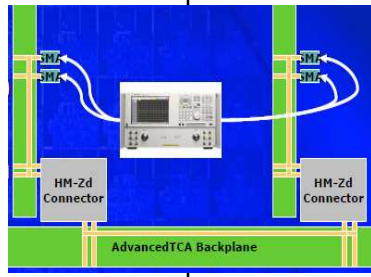


[1] http://www.ieee802.org/3/ap/public/sep04/dambrosia_01_0904.pdf

Channel discussed by 10GBASE-KR

Molex, 2 channels and Intel, 8 channels

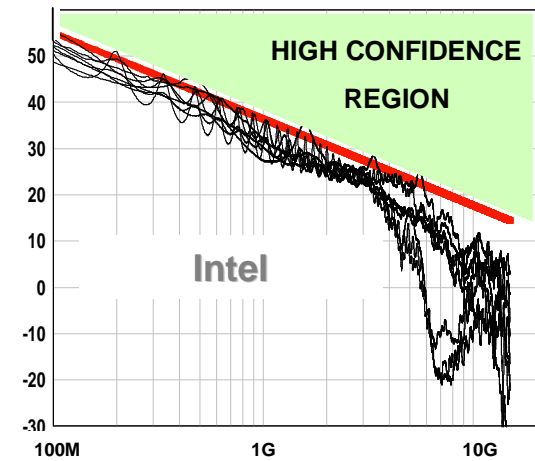
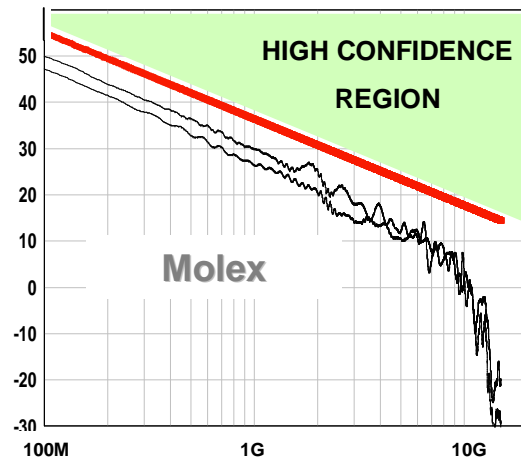
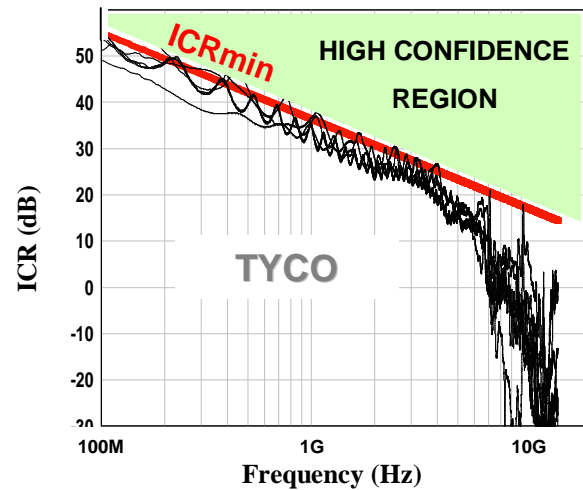
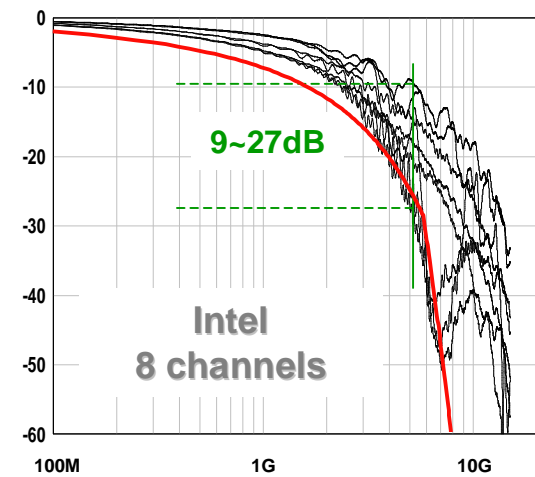
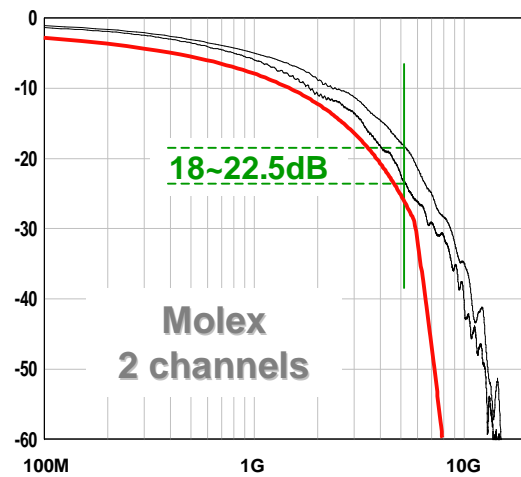
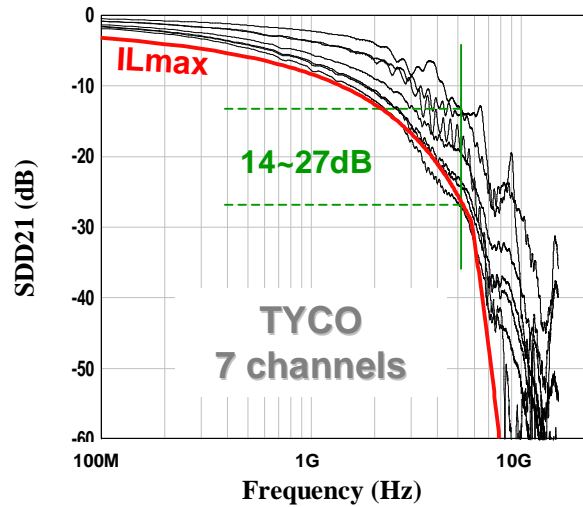
Description		Channel Name	Line Card	No. Connectors	Backplane	Total Length	Loss @ 5GHz
Molex 2 cases [2]	Signal path 3 FEXT 4 NEXT	1m_Improved _1	2.5" + 2.5" Nelco4000 13SI	2	35" Nelco4000 13SI	40"	22.6
		1m_Improved _2	2.5" + 10.5" (?)	2	25" Nelco4000 13SI	38"	17.8
Intel 8 cases [3]	Signal path 2 FEXT 6NEXT	T1	5" + 5" Nelco4000-6	2	---	---	16.8
		T12	5" + 5" Nelco4000-6	2	---	---	24.4
		T20	5" + 5" Nelco4000-6	2	---	---	27.4
		B1	5" + 5" Nelco4000-6	2	---	---	8.9
		B12	5" + 5" Nelco4000-6	2	---	---	14.1
		B20	5" + 5" Nelco4000-6	2	---	---	17.4
		M1	5" + 5" Nelco4000-6	2	---	---	12.3
		M20	5" + 5" Nelco4000-6	2	---	---	19.8



[2] http://www.ieee802.org/3/ap/public/mar06/oganessyan_01_0306.pdf

[3] http://www.ieee802.org/3/ap/public/jun05/peters_01_0605.pdf

IL and ICR



No cases are in "HIGH CONFIDENCE"

Performance Study

The purpose is to confirm **10GBASE-KR** applicability for 40G.

1st Step: Calculate theoretical SNR (Saltz) against broadband noise, measured crosstalk, and IC electronic noise.

2nd Step: Check Jitter and other IC implementation loss by the time domain simulator

3rd Step: Performance Improvement by Crosstalk Canceller

“Noise Margin” is used throughout the discussion.

Noise Margin = [Achievable SNR] – SNR_{required}

SNR_{required} is 17dB for 2PAM, BER = 10⁻¹²

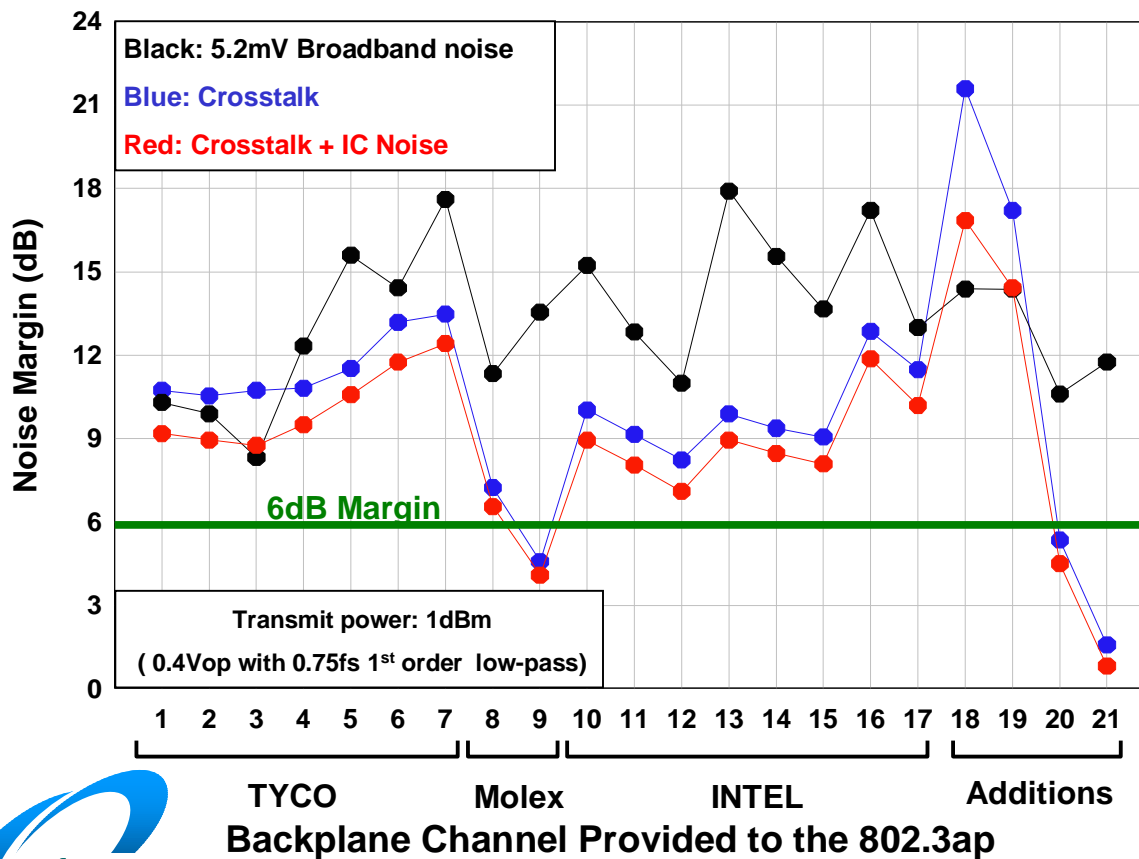
It is preferred to be greater than on the order of 6dB for a robust operation.



Noise Margin by Saltz

Three scenarios :

1. 5.2mV-rms broadband noise defined by 10GBase-KR Receiver Interference Tolerance
2. Measured crosstalk from S-parameter
3. Crosstalk + -140dBm/Hz (IC electronic noise 32nV/sqrt(Hz) into 100ohm)



All except few cases met 6dB margin.

Feasible subject to IC noise floor.

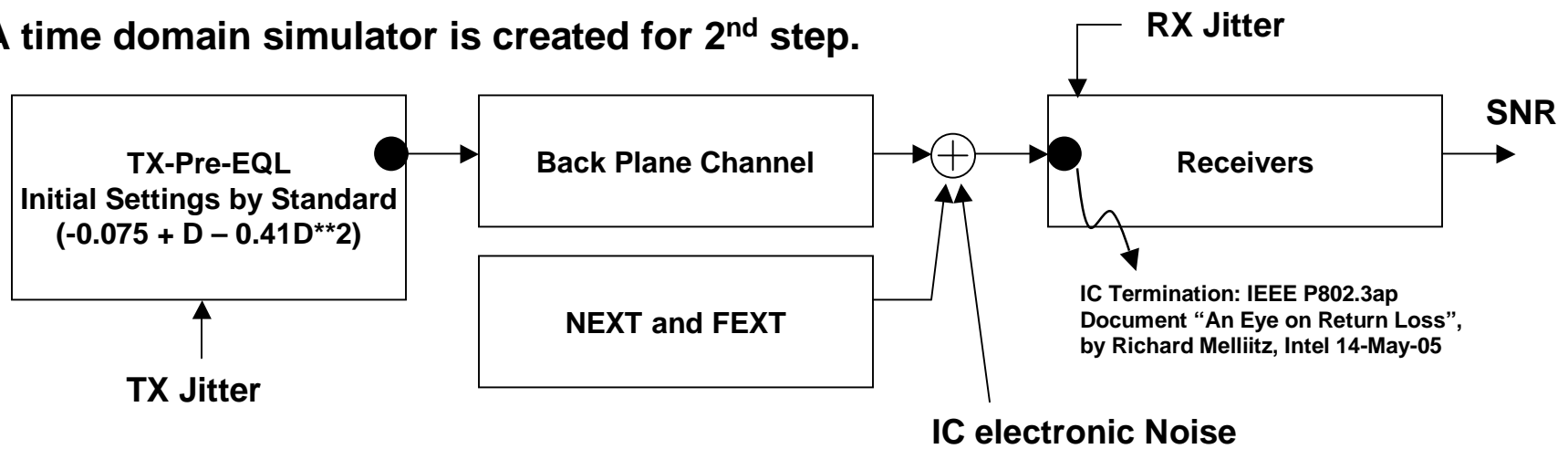
The result does not include

- Jitter
- Implementation loss



Jitter and Implementation Loss

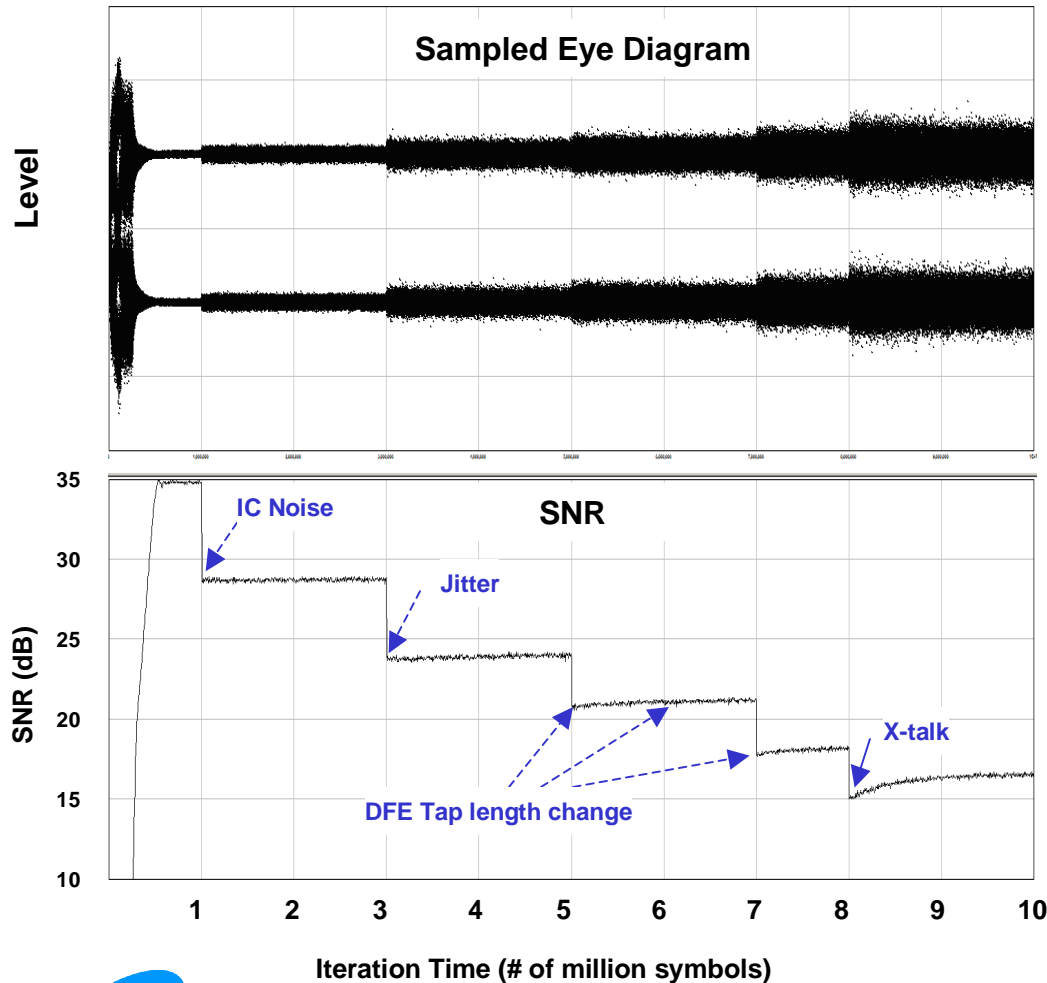
A time domain simulator is created for 2nd step.



- TX Jitter** **0.28UIpp (5 sigma) jitter**
- RX Jitter** **0.21 UIrms random jitter (VCO) + systematic timing recovery jitter**
(bigger than receiver interference tolerance)
- IC Electronic Noise** **-140dBm/Hz**
- FFE** **8tap**
- DFE** **16, 32, 64, and 128tap**
- Crosstalk Canceller added later as an option**



Jitter and Implementation Loss



Following impairments are added one by one after the receiver is fully activated after 1 million-symbol iterations.

- IC noise, -140dBm/Hz
- TX and RX Jitter
- DFE tap length reduction, 128, 64, 32, 16
- FEXT + NEXT

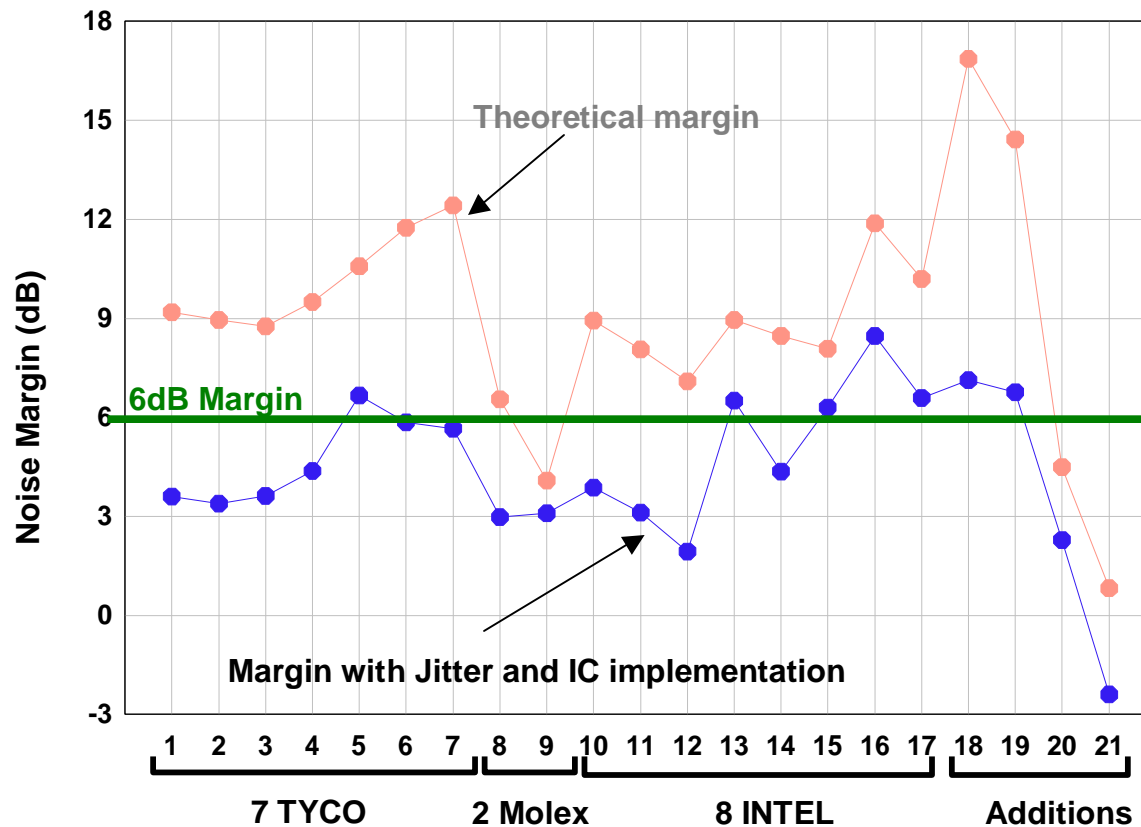
CH12(Intel T20) is shown as an example. All channels were simulated to verify the degradation.



Margin with Jitter and IC

Jitter and IC implementation loss + Crosstalk + -140dBm/Hz IC noise

Receiver Resource: 8 tap FFE + 128 tap DFE



Result represents high performance design and could degrade more.

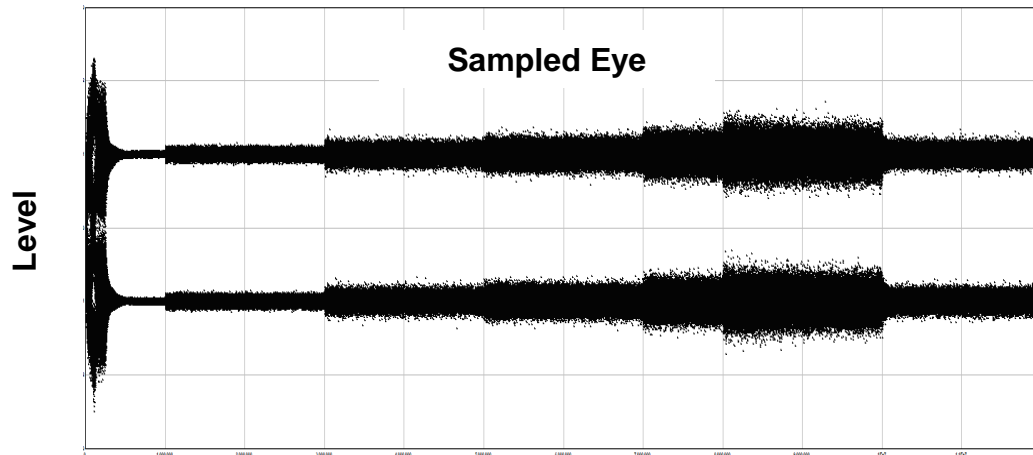
Marginal for many cases.

Industrial systems need to be robust against alien noise, impulsive noise, etc.

How can they be improved?



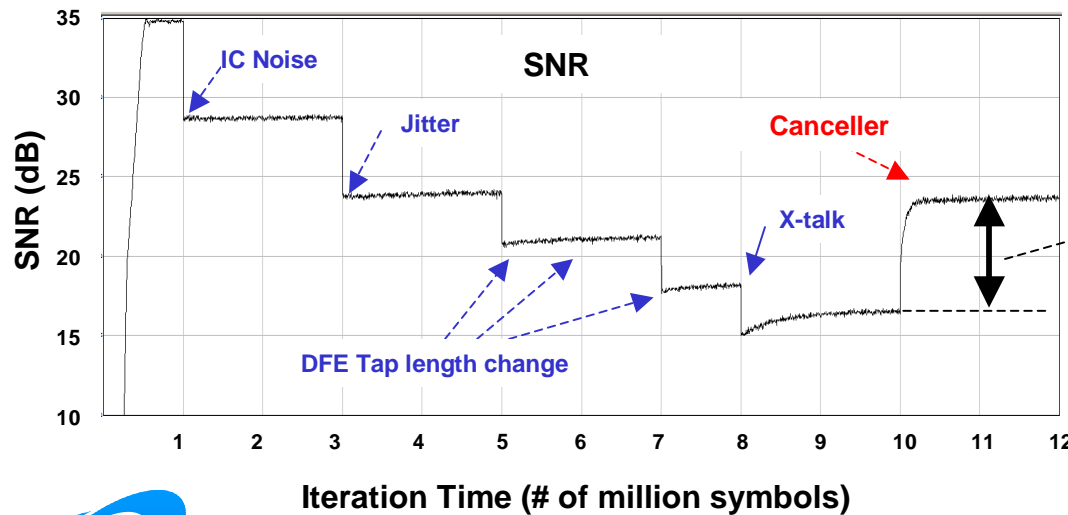
Crosstalk Canceller



Crosstalk cancellation mode (2 million iterations) is added at the end of the behavioral simulation.

Margin was improved by 7dB in this example (CH12, Intel case-3).

Similar improvements shown in the previous chart were confirmed for all cases.

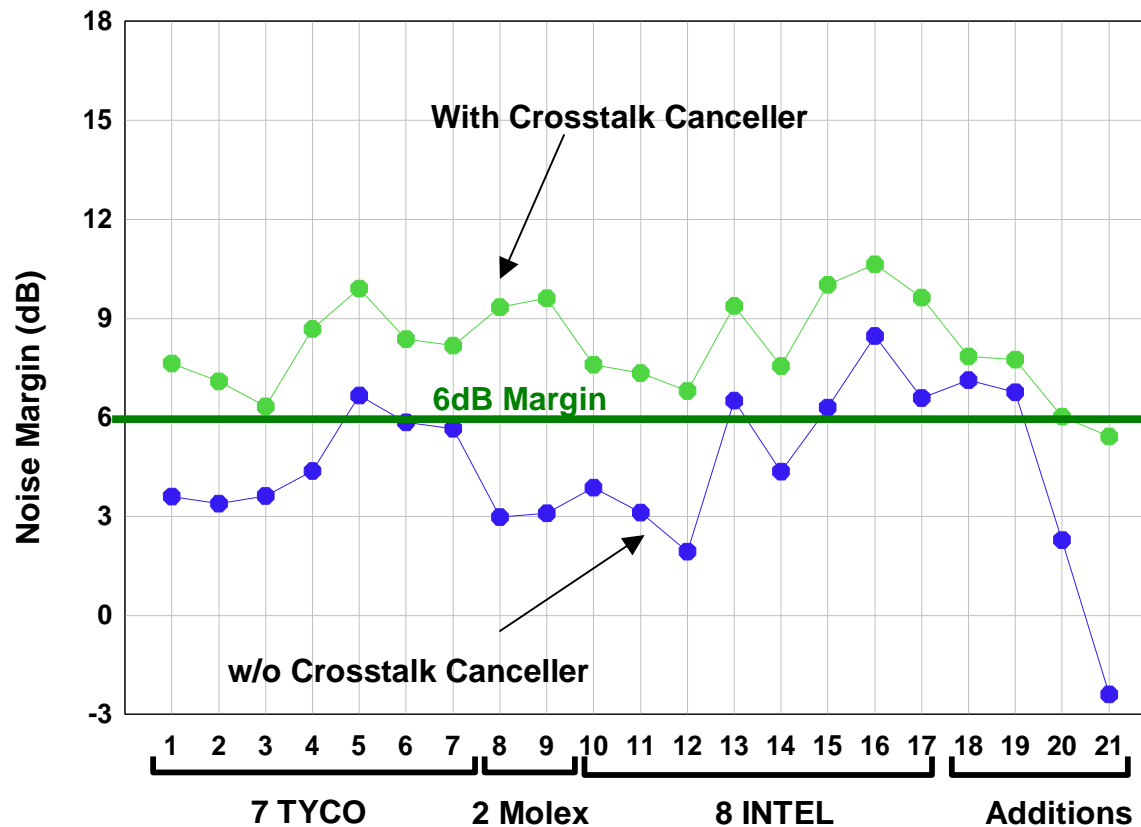


7dB improvement



Crosstalk Canceller

Crosstalk cancellation is possible with 4-lane structure of 40G backplane.



More than 6dB improvement can be made with crosstalk canceller.

Another ~2dB improvement can be with optional FEC.

6dB margin is feasible.



Summary

Performance of 10GBASE-KR is estimated with key IC implementation impairments.

- Performance is marginal with the industrial grade backplane channels.**
- Solution as crosstalk canceller.**
- Even better margin can be obtained by with optional FEC.**
- Recommend HSSG to define additional channel bundling parameters to address crosstalk.**

Therefore, 10GBASE-KR is a good fit as a baseline for 40G system.

