FEC applicability to 40 GbE and 100 GbE

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Outline

- Existing applications of Forward Error Correction in 802.3
  - VDSL (clause 62)
  - 1G EPON (clause 65)
  - 10G Backplane (clause 74)
  - 10G EPON (under development, clause 92)
- Possible needs for Forward Error Correction in 40GbE and 100 GbE
  - 40G Backplane
  - 40km SMF interface for 100 GbE

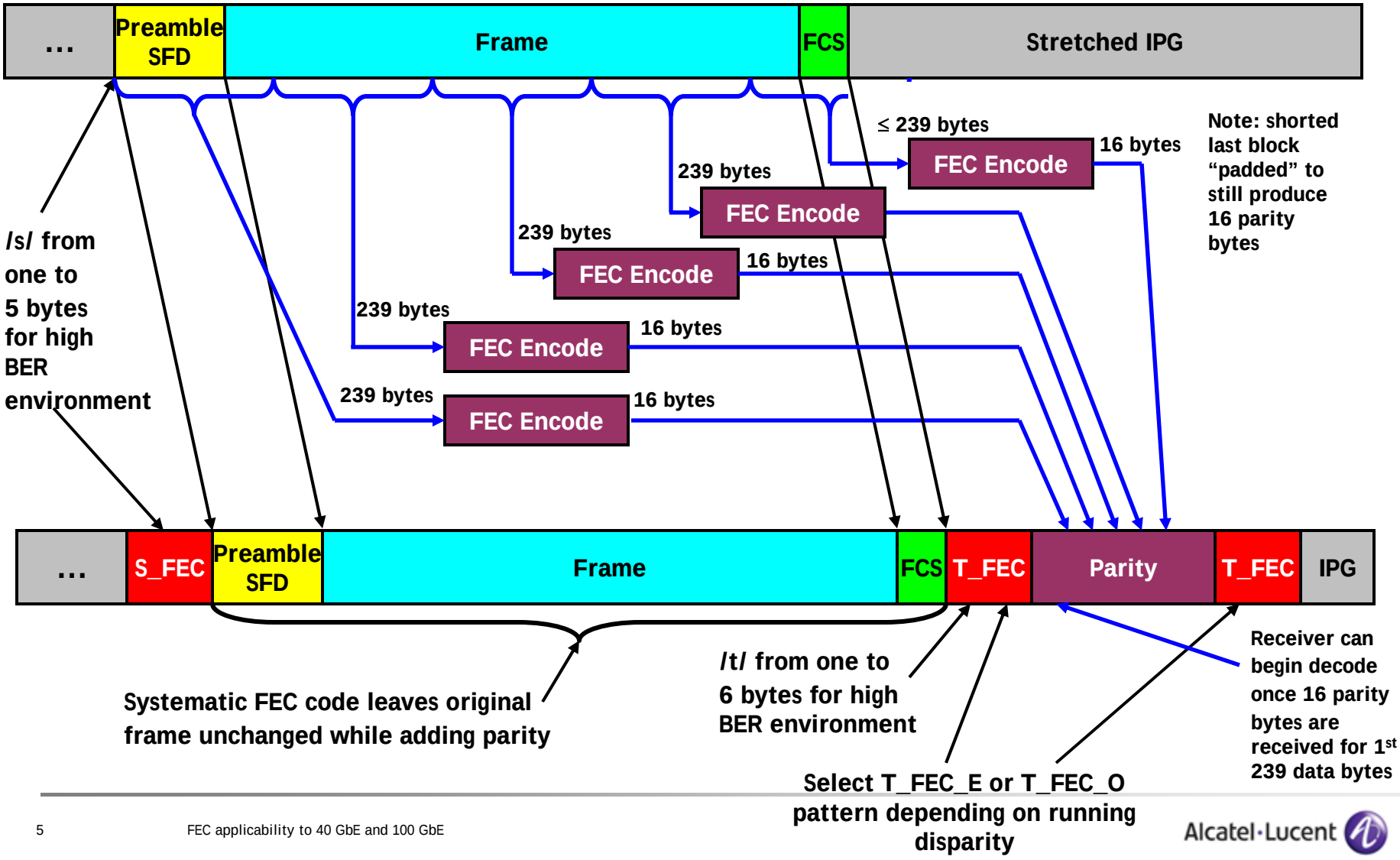
VDSL FEC – Clause 62

- FEC not specified directly in 802.3, but incorporated by reference to ANSI T1.424 VDSL standard
- Supports RS(144,128) and RS(240,224) coding
- Specific to voice-grade twisted pair environment – no apparent applicability to 40 GbE or 100 GbE

Clause 65 – 1G EPON FEC

- FEC is transmitted inband in a stretched IPG, reducing the total throughput of the interface
- Suitable for an environment with multiple subscribers, high split ratios, and where the number of subscribers can be reduced to allow optional FEC to be used without individual subscribers necessarily seeing a decrease in overall throughput
- RS(255,239) FEC per ITU-T G.975

Clause 65 – 1G EPON FEC



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Clause 74 - Backplane FEC

- Uses shortened cyclic code (2112, 2080) by shortening cyclic code (42987, 42955)
- Can correct error bursts up to 11 bits
- Well suited to error bursts in typical backplane channel resulting from error propagation in the receive equalizer
- Framing algorithm
  - Test candidate block start position
  - Descramble block and check for good FEC
  - No match, shift candidate block start by one bit position and try again
  - 4 consecutive blocks good FEC establishes framing; 8 consecutive blocks without good FEC loses framing and start over; from in-frame
  - While this is “brute force”, framing takes <5 Mbit on a 10 Gbit/s stream, <0.5ms

Clause 74 – Backplane FEC

Steal redundant SYNC bits from 32 66-bit blocks to create space for parity bits

Table 74-1 FEC Block Format

T_0	64-bit payload Word 0	T_1	64-bit payload Word 1	T_2	64-bit payload Word 2	T_3	64-bit payload Word 3
T_4	64-bit payload Word 4	T_5	64-bit payload Word 5	T_6	64-bit payload Word 6	T_7	64-bit payload Word 7
T_8	64-bit payload Word 8	T_9	64-bit payload Word 9	T_{10}	64-bit payload Word 10	T_{11}	64-bit payload Word 11
T_{12}	64-bit payload Word 12	T_{13}	64-bit payload Word 13	T_{14}	64-bit payload Word 14	T_{15}	64-bit payload Word 15
T_{16}	64-bit payload Word 16	T_{17}	64-bit payload Word 17	T_{18}	64-bit payload Word 18	T_{19}	64-bit payload Word 19
T_{20}	64-bit payload Word 20	T_{21}	64-bit payload Word 21	T_{22}	64-bit payload Word 22	T_{23}	64-bit payload Word 23
T_{24}	64-bit payload Word 24	T_{25}	64-bit payload Word 25	T_{26}	64-bit payload Word 26	T_{27}	64-bit payload Word 27
T_{28}	64-bit payload Word 28	T_{29}	64-bit payload Word 29	T_{30}	64-bit payload Word 30	T_{31}	64-bit payload Word 31
32 parity bits							

$T_i=0 \leftrightarrow$ Sync=10 $T_i=1 \leftrightarrow$ Sync=01

Additional scrambler to restore DC balance after removing one of the SYNC bits from each 66B block

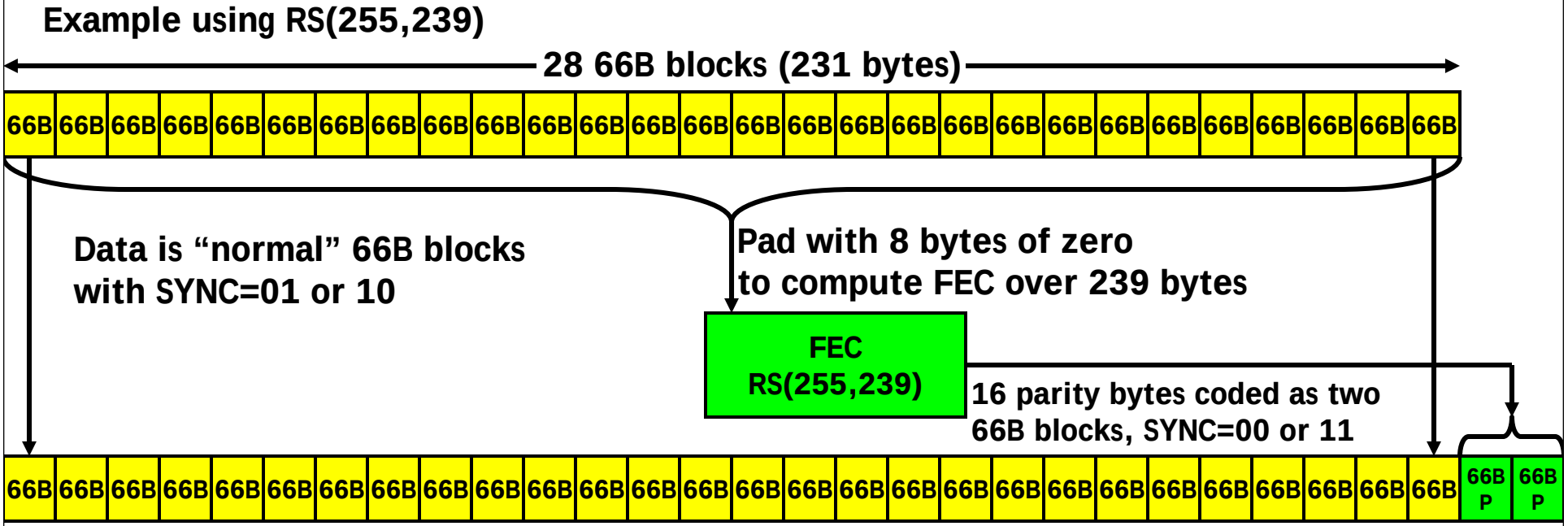
Clause 92 – 10G EPON FEC – under development

Key attributes of solution chosen, but not specific solution

Motion	Text
Orlando 3	10G EPON shall accommodate FEC's parity bandwidth by **reducing** the MAC's effective data rate (**sub-rating**).
Orlando 4	To accept the scheme outlined in slides 3-7 in 3av_0703_mandin_2.pdf as the baseline scheme for upstream FEC framing and synchronization.
Orlando 5	To accept as a baseline scheme the FEC codeword structure depicted in the illustration on slide 5 in 3av_0703_mandin_2.pdf for the downstream (so that the FEC codeword structures on the upstream and downstream are identical).
Geneva 6	The FEC algorithm shall be accept as its input Nx65bit payloads (the second bit of the sync header plus 64 bits of data) pre-pended with padding consisting of zeros to bring the input codeword to the required size; notwithstanding, both bits of the sync header shall be transmitted, while the padding shall not be transmitted, as illustrated in 3av_0705_effenberger_4.pdf.
Geneva 7	To accept as a baseline for FEC framing the presentations 0701_effenberger_1.pdf, 0703_kramer_1.pdf and 0705_lynskey_1.pdf.

Clause 92 – 10G EPON FEC – Possible Example

- **FEC is computed on a 66B codeword basis**
- **M blocks of parity are added per N blocks of data**
- **FEC will add 7-15% depending on the code chosen**



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40 GbE and 100 GbE – Where might we need FEC?

- 40 GbE backplane
  - Since 10G Base-KR needed FEC, 40 GbE backplane will likely require it
  - If 40 GbE backplane ends up looking like 4 lanes of 10G Base-KR at the PCS/physical layer, clause 74 FEC can likely be applied on a per-lane basis with little or no change
- 40 GbE or 100 GbE over metro or long-haul DWDM systems
  - OTN Wrapper provides FEC – no need for it in Ethernet
  - RS(255,239) for cross-vendor interoperability
  - Vendor specific "Super-FEC" (many described in ITU-T G.975.1) for long-haul DWDM systems
- 100 GbE native 40km interface
  - Not known if required

Possible FEC for 100 GbE native 40km interface, if needed

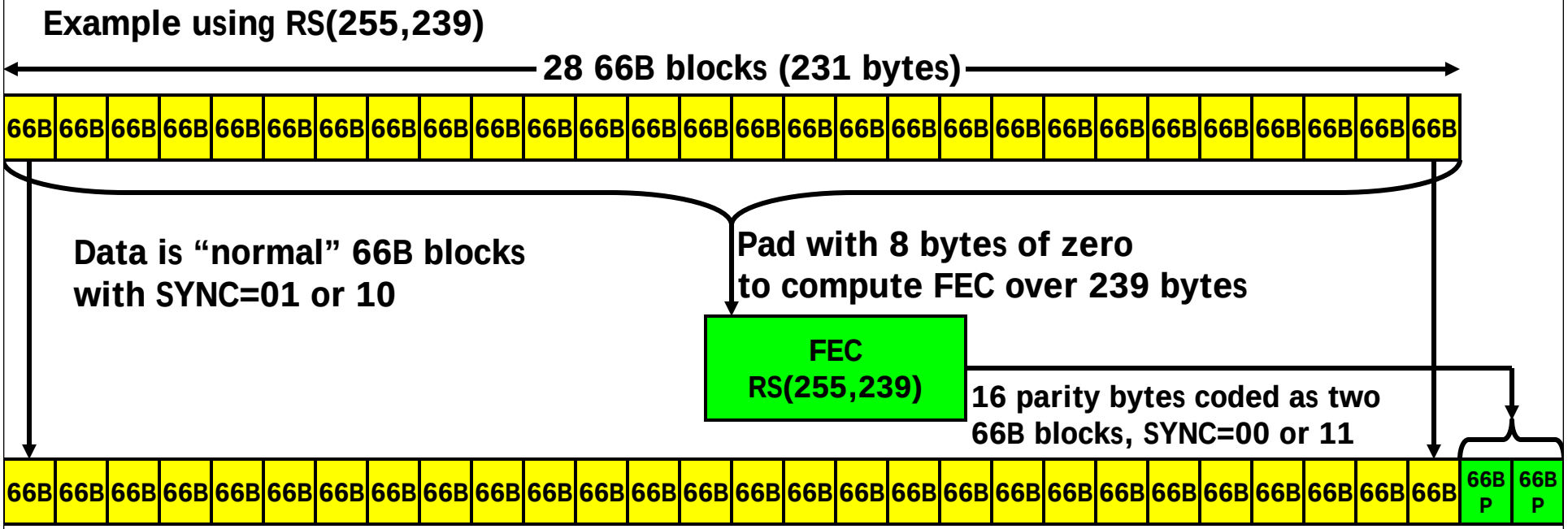
- Would EPON sub-rate FEC be acceptable? Probably not:
  - EPON is inherently used in a multi-subscriber environment where no individual subscriber gets the full bandwidth capability of the interface
  - End users who are dissatisfied with LAG because of bandwidth inefficiency with small numbers of large flows will likely not accept bandwidth reduction based on reach.
  - IF FEC is required for 100 GbE 40km, it would most likely need to be super-rate (increase the lane rate to accommodate the parity) rather than sub-rate

Example: 40km 4x25G DWDM interface using CTBI/virtual lane approach and RS(255,239)

Nominal lane rate without FEC, lane markers inband	25.78125 Gbit/s
Nominal lane rate without FEC, lane markers out of band	25.78282366 Gbit/s
Nominal lane rate with RS(255,239) FEC, add 2 blocks to each 28, lane markers inband	27.62276786 Gbit/s
Nominal lane rate with RS(255,239) FEC, add 2 blocks to each 28, lane markers out of band	27.62445392 Gbit/s

Possible format for 100 GbE 40km FEC format, if needed

- **FEC is computed per physical lane on a 66B codeword basis**
- **M blocks of parity are added per N blocks of data, increasing the lane rate**
- **FEC will add 7-15% depending on the code chosen**



Note: If this technique were to be applied to 40 GbE, the format of the parity blocks is not transcodable to 512B/513B. However, the LAN FEC would be decoded before the adaptation into OTN (the LAN signal WITH added FEC wouldn't fit standard ODU3 anyway)

Conclusions

- Assuming that 40 GbE backplane looks like four lanes of 10G Base-KR, clause 74 FEC can likely be reused
- Ethernet FEC is not needed for metro and long-haul DWDM applications, as OTN takes care of these cases
- IF FEC is required the 40km 100GbE interface, it likely needs to be a super-rate solution (increasing the lane bit-rate to add parity). The technique of adding M parity blocks to N 66B data blocks under consideration in 802.3av could likely be applied