Proposal of PMD architectures for HSSG

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Outline

- Proposal of Parallel PMDs
  - Transmission Rate
  - Transmission Reach
- Future Challenges
  - Skew compensation
  - Electrical interface
  - Error correction
  - EDC

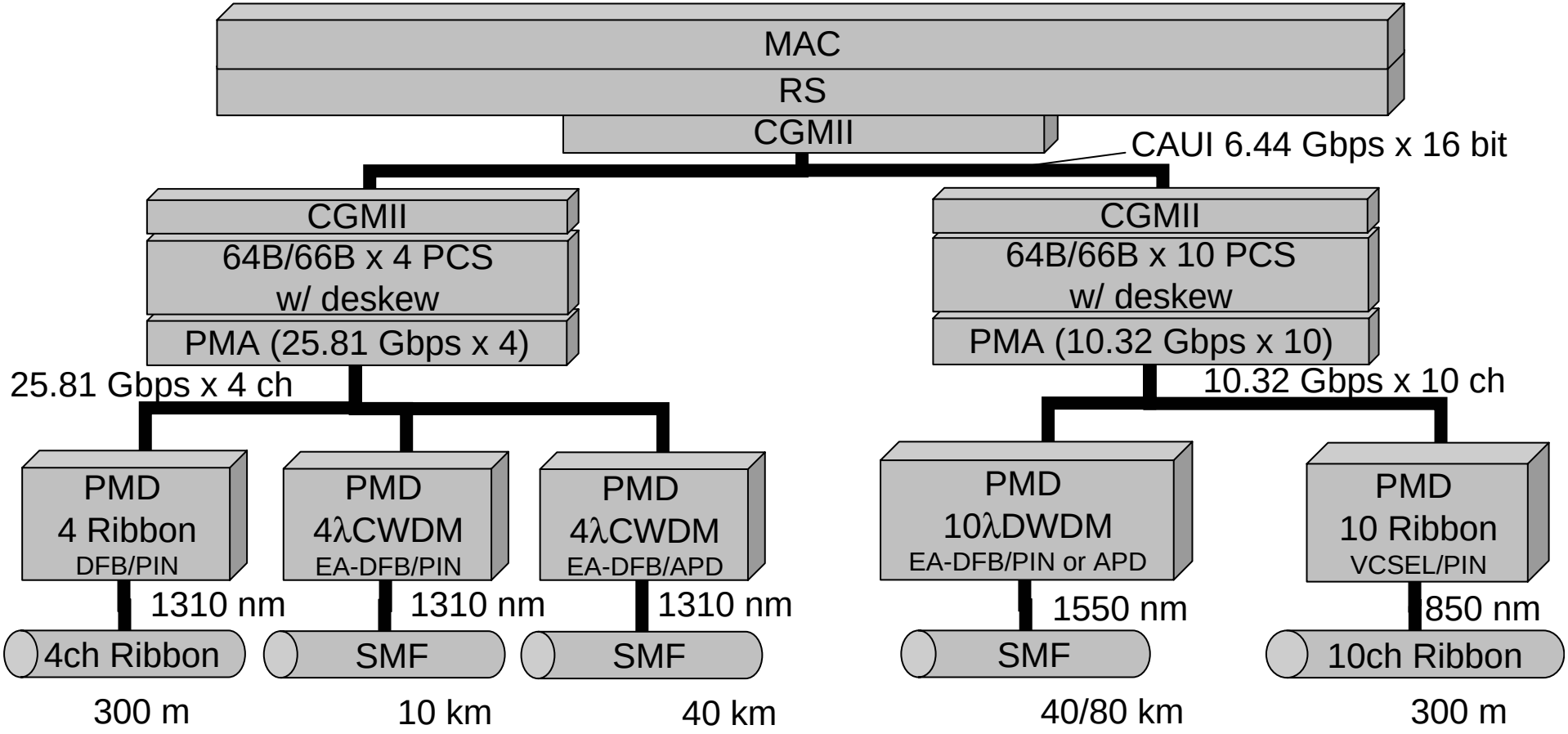
Market

- Improvements
  1. FTTH upgrade
     - Increasing bandwidth
  2. Content
     - Increasing bandwidth requirements
       - HDTV
  3. Backbone Network
     - Metro area: Internet Service Providers
       - Today 10 – 40 Gbps, Next 100 Gbps
     - Data Center

Requirements

- Wider Bandwidth: ~ 100 Gbps
- Longer Reach: 100 m ~ 80 km
  - APL will be feasible for long-haul transmission
- Low Cost:
  - Small number of optical components
  - Compact CMOS-ICs
- Low Power Consumption
- Low Latency

Brainstorming possible PMD architectures



EA-DFB: DFB integrated with Electro-absorption modulator

- 10 ch architectures (technically easy)
  -> 4ch architectures (cost effective)

Possible PMD architectures (25 Gbps x 4 ch)

#	Name	Method (pitch)	LD	PD	Wave -length	Fiber	Reach
1-1	LC4	CWDM (24.5 nm)	Un-cooled EA-DFB	PIN	13xx	SMF	10 km
1-2		DWDM (8 nm)	Cooled DFB				
2	EC4	CWDM 24.5 nm	Un-cooled EA-DFB	APD	13xx	SMF	40 km
3	SC4	Ribbon	DFB	PIN	1310	SMF Ribbon	300 m

- CWDM pitch (24 nm): equal to LX4
- DFB-LD (low-cost) requires 8-nm DWDM pitch for 10-km transmission

Estimation: 25 Gbps x 4 ch

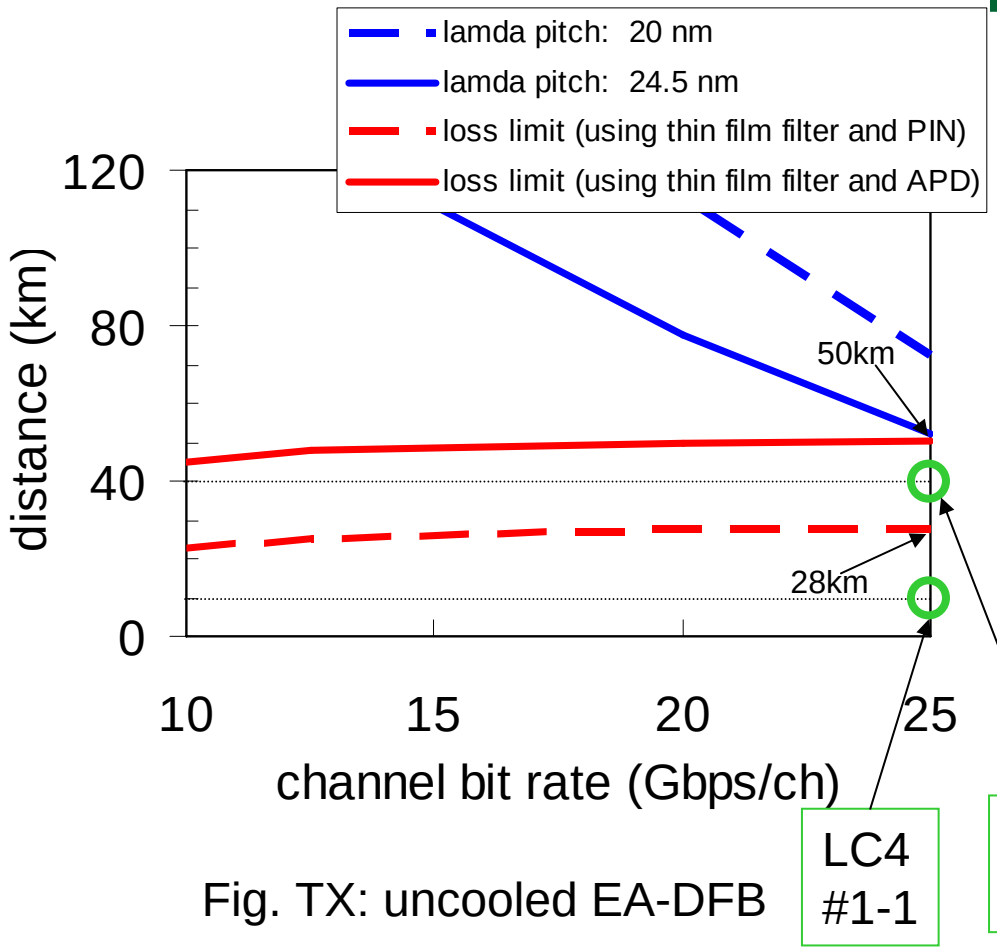


Fig. TX: uncooled EA-DFB

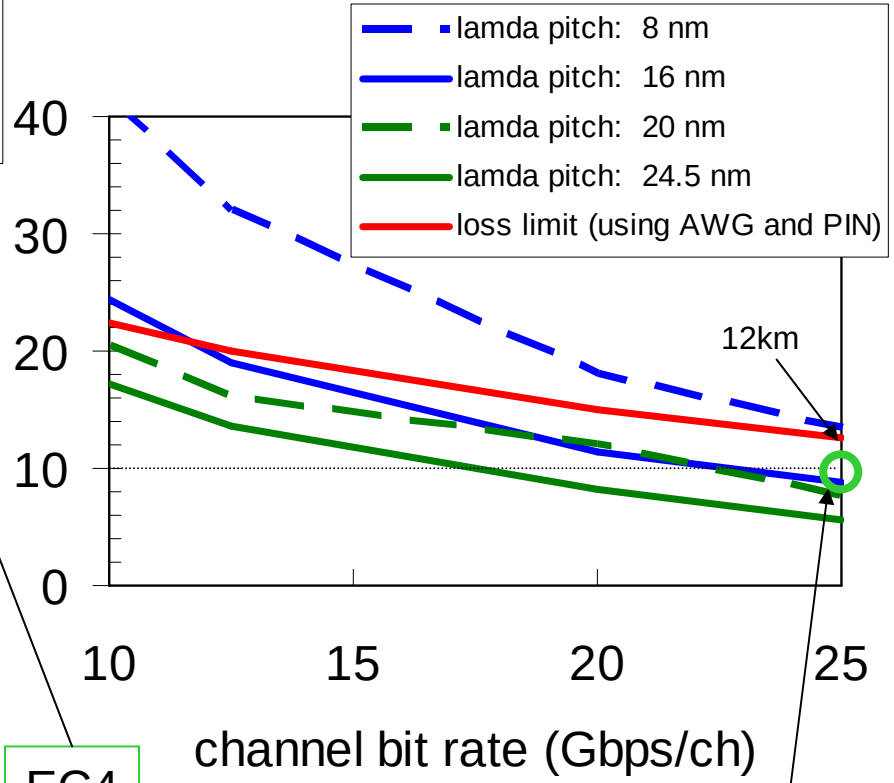


Fig. TX: cooled DFB

LC4 #1-1

EC4 #2

LC4 #1-2

EA-DFB Dispersion Tolerance: 1600 nm/ps, DFB: 170 nm/ps

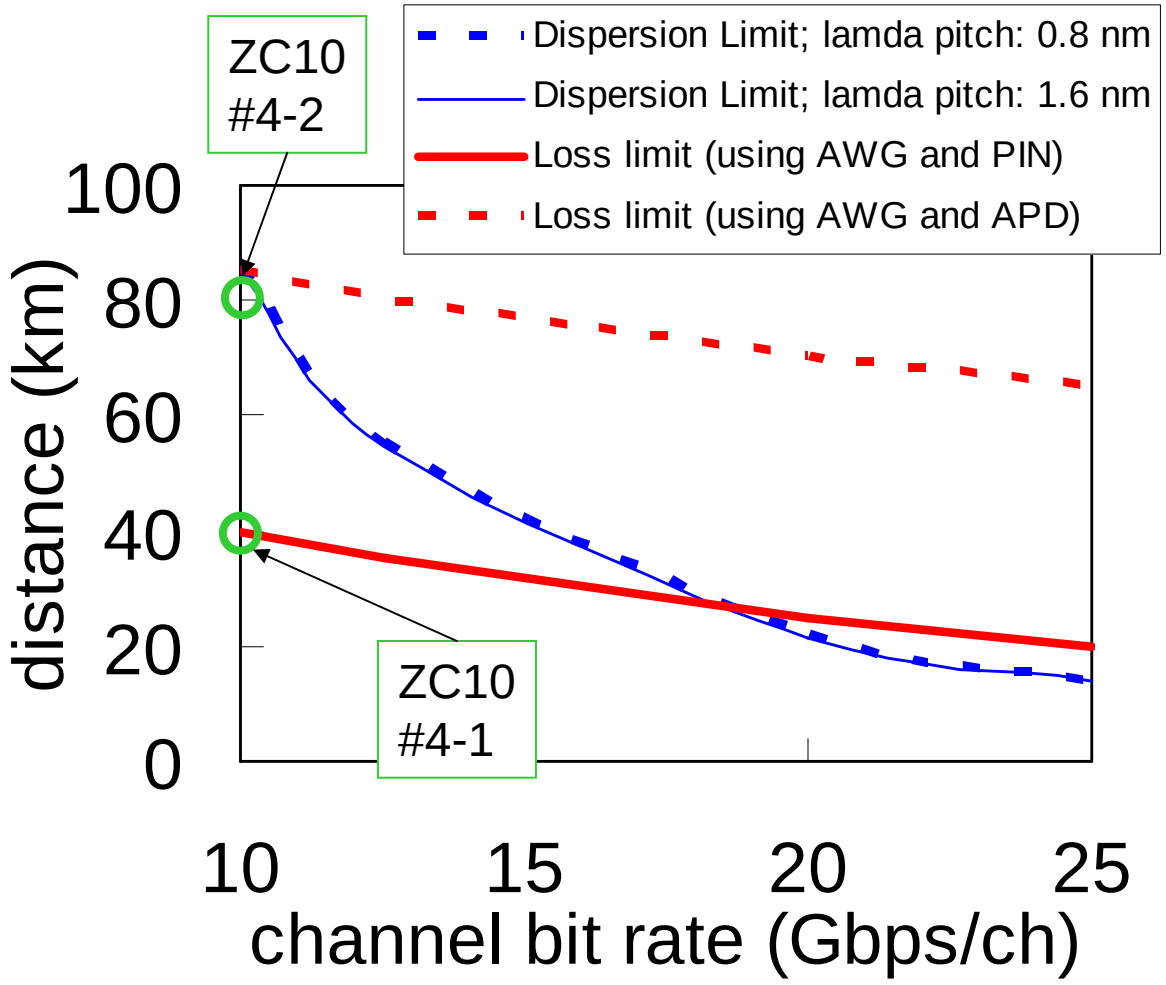
Minimum Optical Receiver Power @ 25 Gbps; PIN: -14 dBm, APD: -23 dBm

Possible PMD architectures (10 Gbps x 10 ch)

#	Name	Method (pitch)	LD	PD	CH	Wave -length	Fiber	Reach
4-1	ZC10	DWDM (0.8 nm or 1.6 nm)	Cool EA-DFB	PIN	10	15xx	SMF	40 km
4-2				APD	10	15xx	SMF	80 km
5	SC10	Ribbon	VCSEL	PIN	10	850 (13xx)	MMF Ribbon	300 m

■DWDM pitch (0.8 nm/1.6 nm): equal to ITU-grid
- •Wide pitch: prefer to monolithic integrated LD array

Estimation: DWDM 10 Gbps x 10 ch

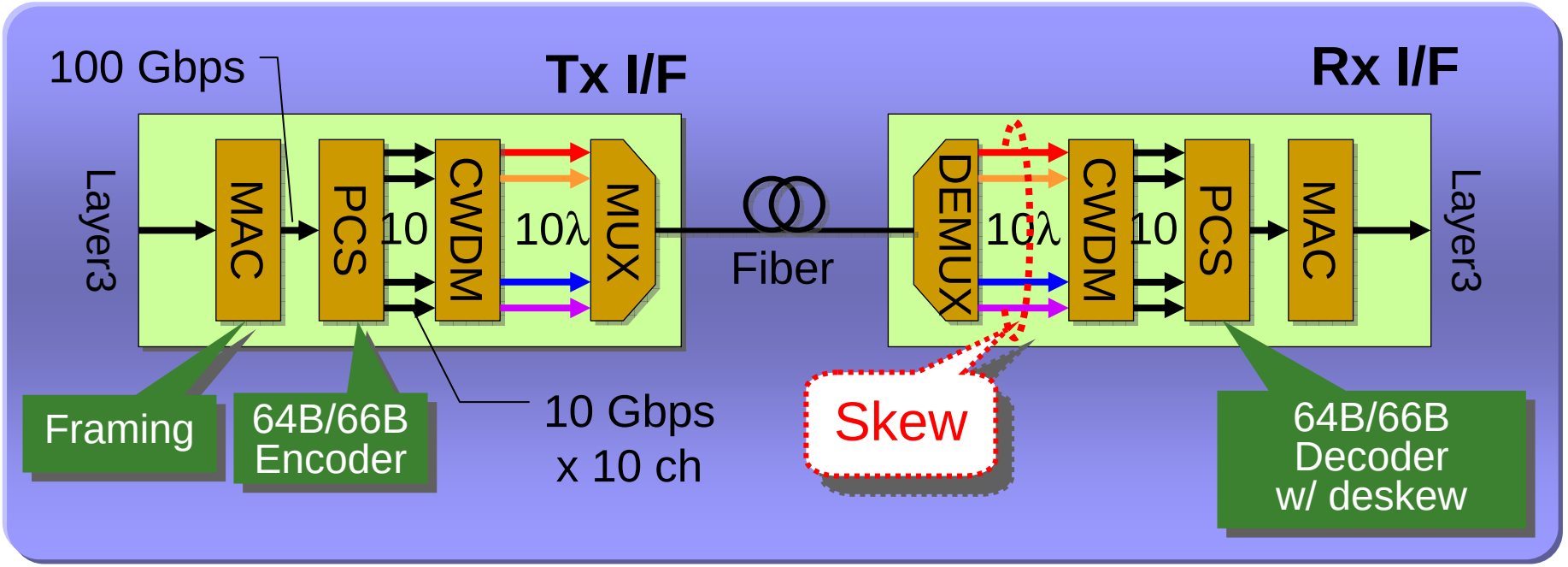


Future Challenges

- Skew Compensation in PCS
  - Between parallel links
- Electrical Interface
  - 25 Gbps x 4 ch (XENPAK) (or 12.5 Gbps x 8 ch ?)
- Error Correction
  - TBD
- EDC
  - TEB

Skew compensation

- Max. Skew
  - CWDM (4 wavelengths: 13xx nm): +/- 2 ns(10 km), +/+ 8 ns(40 km)
  - DWDM (10 wavelengths: 15xx nm): +/- 7 ns(40km), +/+ 14 ns(80 km):
  - Short reach: 10 ribbon fiber- +/- 10 ns(100 m) ~ +/- 30 ns(300 m)



Example: 10 Gbps x 10 channels

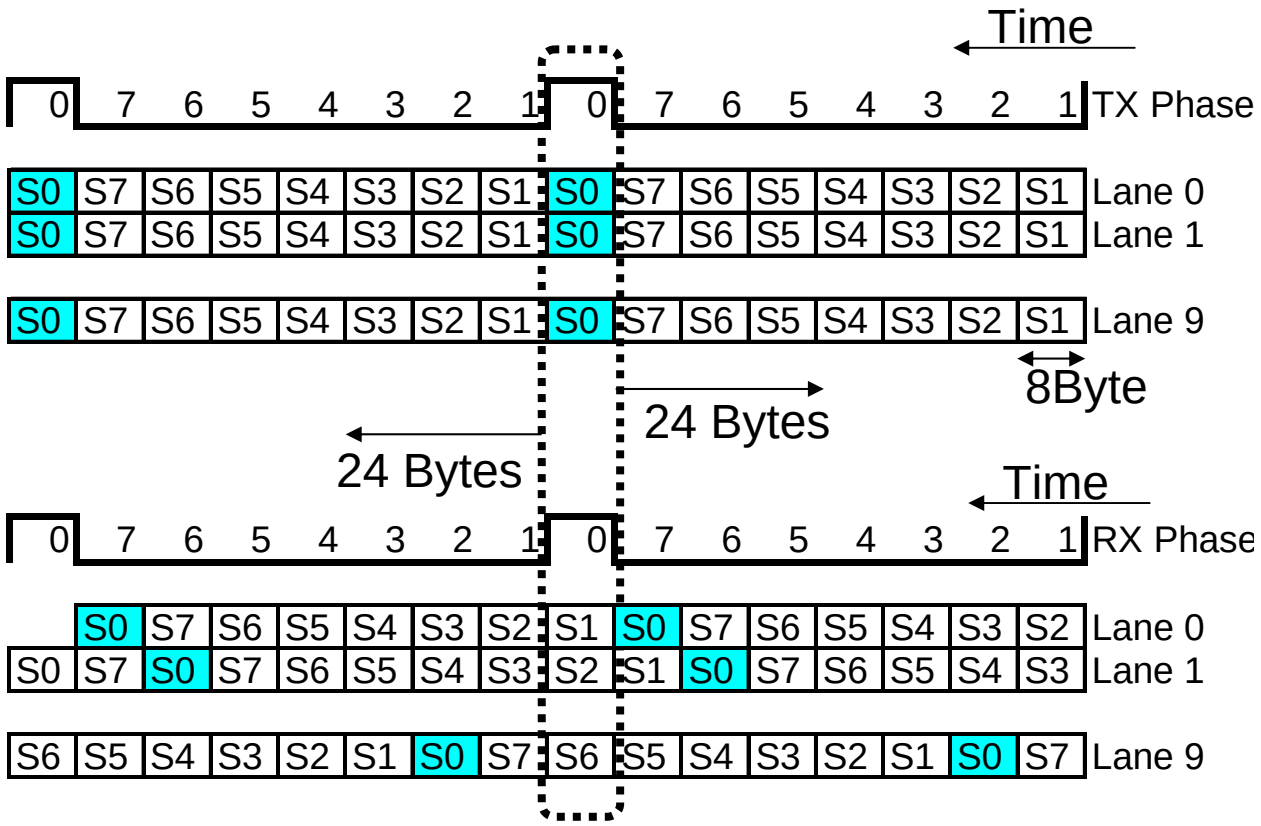
How to detect skew

- TX side

  64B66B based special data pattern into IFG is sequentially output in all lanes at the same time.

- RX side

  Skew between the lanes is detected based on the difference in timing of received signal.



In this example: all signals are IDLE

Summary

- Parallel link
  - 25 Gbps x 4 ch_(CWDM, DWDM and Ribbon)
  - 10 Gbps x 10 ch (DWDM and Ribbon)
- Reach Target (EA-DFB/DFB, PIN/APD)
  - 100 m, 300 m, 10 km, 40 km, 80 km
- Technical Challenges
  - Skew compensation
  - Electrical interface
  - Error correction
  - EDC